XN1049 Switch Power Supply PWM Controller

General Description

XN1049 which is optimized for high performance is a highly integrated current mode PWM control IC. It is applied for switch power of the small-sized and medium-sized for example the power adaptor. For lower the standby power and higher RoHS compliant, the IC has the Burst Mode function and very low startup current and working current. At the condition of no load or light load, the IC operates in extended 'burst mode' to minimize switching loss by lower the switching frequency. The low startup current and low operating current contribute to a reliable power on startup design with XN1049. A large value resistor could thus be used in the startup circuit to minimize the power consumption and improve the efficiency of the power convent.

The internal synchronous slope compensation circuit improves system large signal stability and reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. XN1049 offers complete protection coverage with automatic self-recovery feature including over current protection cycle by cycle (OCP), over load protection (OLP), under voltage lockout (UVLO). The gate-driven output is clamped to maximum 18V to protect the external MOSFET. Excellent EMI performance is achieved by using the frequency jitter and the soft-switching at the totem-pole-gate-drive output. The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation. The IC can be used as the best alternative products of the linear power supply or the RCC-mode power to improve the whole performance of the switch power system and lower the cost. XN1049 is offered in SOT23-6, SOP-8 and DIP-8 packages.

Features

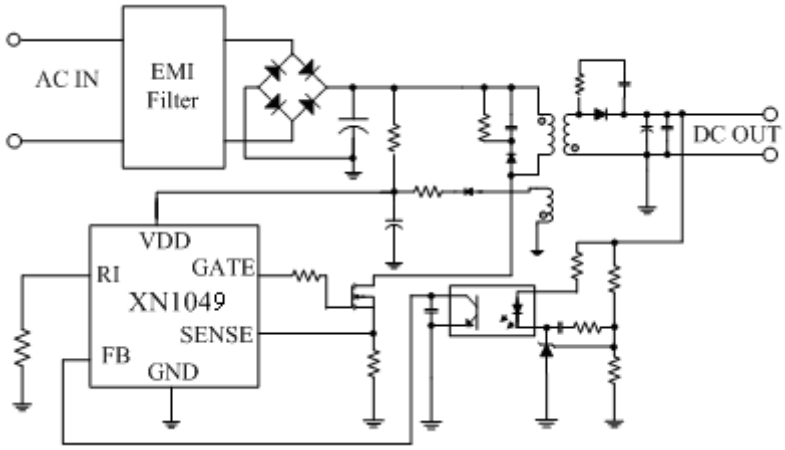
- Extended burst mode control for improving efficiency and minimum standby power
- Low startup current(4uA)
- Low operation current(1.4mA)
- Leading edge blanking was built in
- Synchronous slope compensation was built in
- Current mode operates
- External programmable PWM switching frequency
- Over current protection cycle by cycle(OCP)
- Good protection coverage with auto self-recovery
- VDD over voltage clamp and under voltage lockout with hysteresis (UVLO)
- Maximum gate-drive output clamped voltage (18V)
- Frequency jitter
- Constant limited output power
- Over load protection(OLP)
- Free audio noise operation

Applications

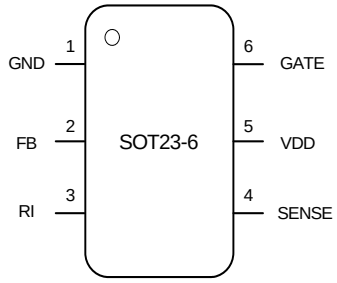
Universal switch power supply and offline AC/DC flyback converter:

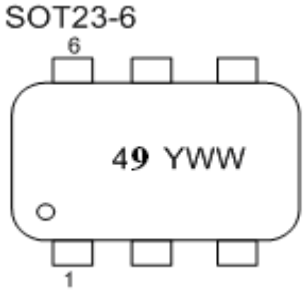
- Battery Charger
- Power Adaptor
- Set-Top Box Power Supplies
- Open-frame SMPS

Typical Application Circuit

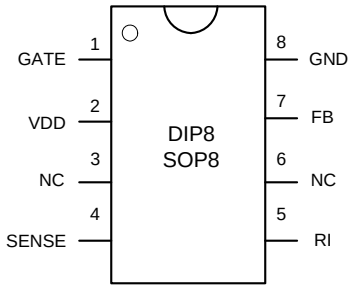


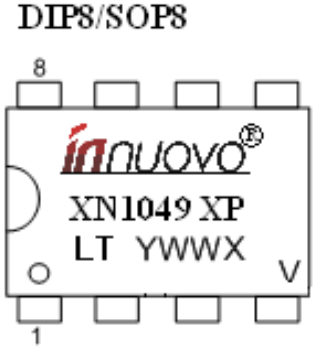
Pin Definition and Device Marking





49: XN1049
Y: Year Code
WW：Week Code





X: D = DIP8 ， S = SOP8
P: P = Pb-free package
Y: Year Code (0-9)
WW: Week Code (1-52)
X: Area Code
V: Internal Version Code (1-9)

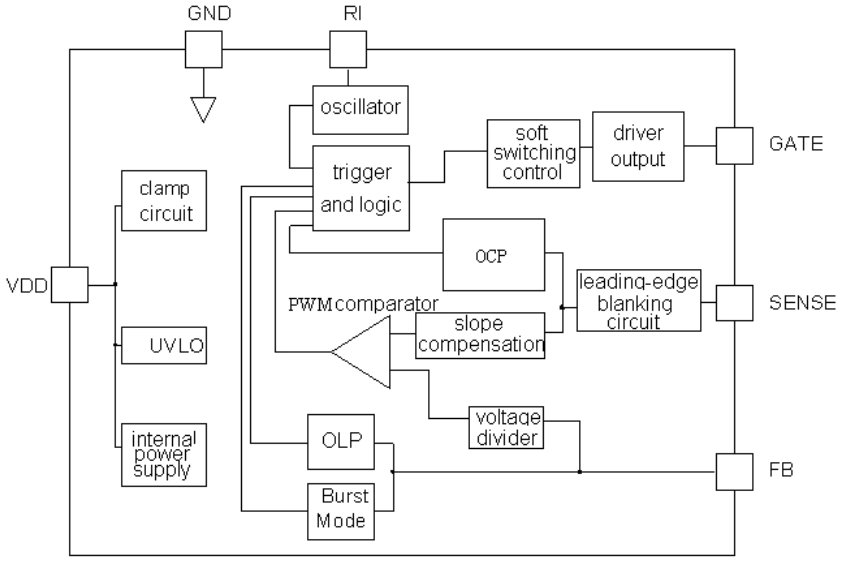
Ordering Information

Package	IC Marking Information	Purchasing Device Name
8-Pin DIP8, Pb-free	XN1049DP	XN1049DP
8-Pin SOP8, Pb-free	XN1049SP	XN1049SP
6-Pin SOT23-6, Pb-free	49 YWW	XN1049TP（SOT23-6）

Pin Function Description

Pin Name	Pin No. DIP8/SOP8	Pin Type	Function Description
GND	8 / 1	Ground	Ground
FB	7 / 2	Feedback Input	Feedback input pin. The PWM duty cycle is determined by voltage into this pin and the current-sense signal at Pin 4
RI	5 / 3	Frequency Setting	Internal oscillator frequency setting pin. A resistor which is connected between RI and GND sets the PWM frequency
NC	3	Floating	Floating
NC	6	Floating	Floating
SENSE	4 / 4	Current Monitoring	Current detection flyback input pin for estimating reaching the limit
VDD	2 / 5	Power	DC power supply pin
GATE	1 / 6	Output	Totem-pole gate drive output for the power MOSFET

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VDD	Input Voltage	30	V
V_{FB}	Input Voltage to FB	-0.3~7	V
V_{SENSE}	Input Voltage to Sense Pin	-0.3~7	V
V_{RI}	Input Voltage to RI Pin	-0.3~7	V
T_J	Work junction temperature	-20~150	℃
T_{STG}	Storage temperature	-55~160	℃
V_{CV}	VDD setting voltage	34	V
I_{CC}	VDD DC setting voltage	10	mA

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Condition

Symbol	Parameter	Value	Unit
VDD	VDD supply voltage	10 to 30	V
RI	RI resistor value	100	Kohm
T_A	Operating temperature	-20 to 85	℃

ESD Information

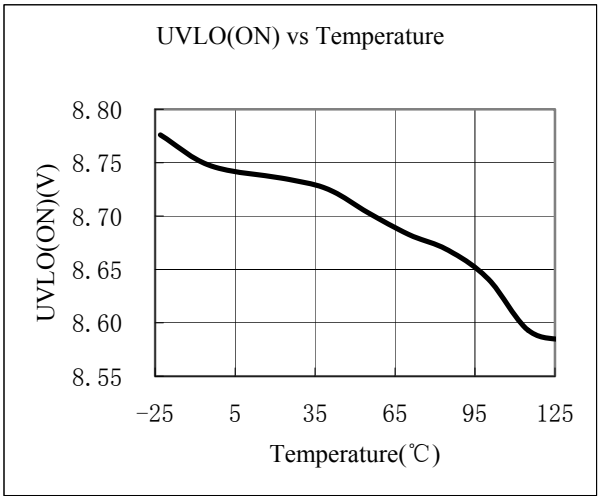
Symbol	Parameter	Value	Unit
$V_{ESD-HBM}$	Human body model on all pins except Vin and VDD	3	KV
V_{ESD-MM}	Machine model on all pins	150	V

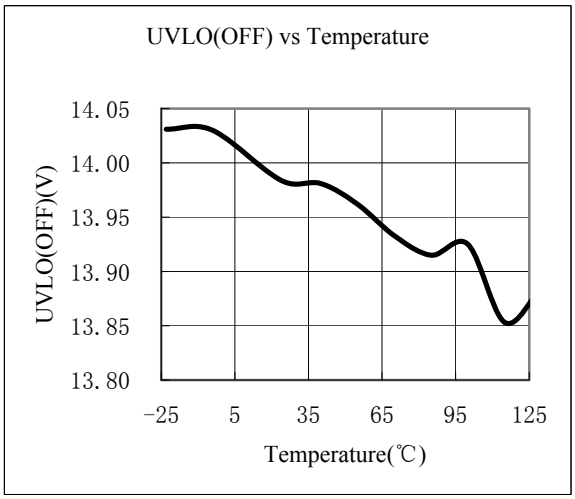
Electrical Characteristics

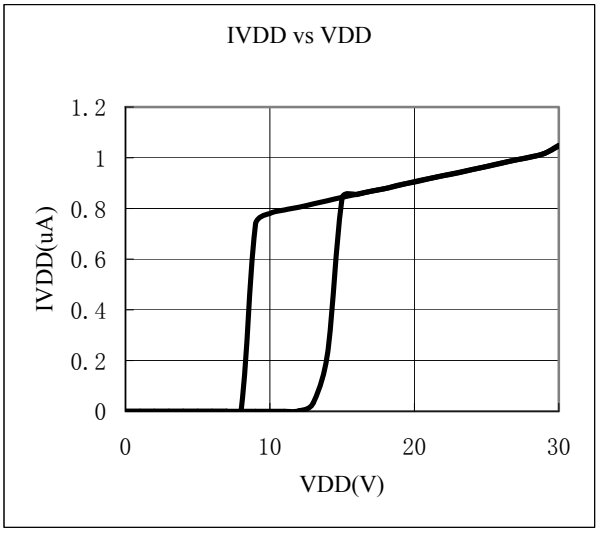
Supply Voltage (VDD)						
symbol	**parameter**	**Test condition**	**Min**	**Typ**	**Max**	**Unit**
VDD_OP	Operation voltage				30	V
UVLO_ON	Turn on threshold Voltage		7.5	8.5	9.5	V
UVLO_OFF	Turn-off threshold Voltage		13.5	14.3	15.5	V
I_VDD_ST	Start up current	VDD=13V,RI=100K		4	20	uA
I_VDD_OP	Operation Current	VDD=16V,RI=100K,V_{FB}=3V, GATE with 1nF to GND		1.4	2.4	mA
VDD_Clamp	VDD Zener Clamp Voltage	I_{VDD}=10mA		33		V
Feedback Input Section						
V_{FB}_Open	V_{FB} Open Loop Voltage		4.5	4.9	5.5	V
I_{FB}_Short	FB Pin Short Current	FB Shorted to GND		0.8		mA
V_{TH}_PL	Power limiting FB Threshold			3.65		V
T_D_PL	Power limiting Debounce			47		ms
Z_{FB}_IN	Input Impedance			6		kΩ
Max_Duty	Maximum duty cycle			75		%
Current Sense Section						
T_{LEB}	Leading edge Blanking Time			330		ns
Z_{sense}	Input impedance			40		kΩ
T_D_OC	OCP control delay	GATE with 1nF to GND		120		ns
T_{TH}_OC	OCP threshold	FB＝3V	0.70	0.75	0.80	V
Oscillator Section						
F_{osc}	Frequency	Oscillation @RI=100K,CS=0,FB=3V	60	65	70	KHz
F_{osc}_BM	Burst mode frequency	Oscillation @RI=100K,CS=0,FB=1.1V		22		KHz
Δf_temp	Frequency variation versus	TEMP = -20 to 85℃		5		%

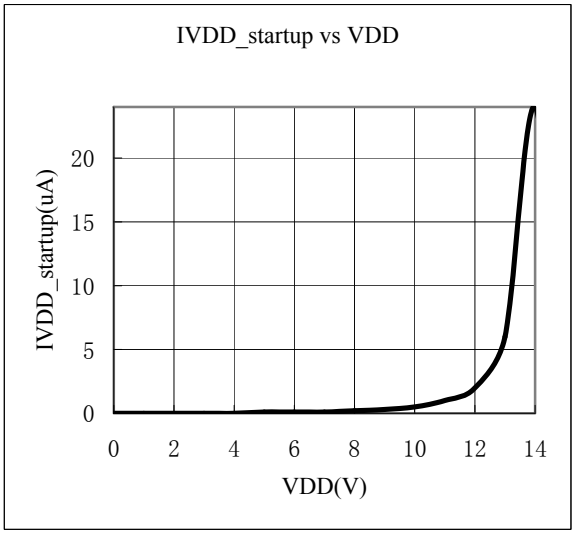
	temp. Deviation					
Δf_VDD	Frequency variation versus VDD	VDD = 12 to 25V		5		%
V_RI_Open	RI open Load Voltage			2		V
RI_range			50	100	150	kΩ
GATE Output Section						
V_{OL}	Output voltage low	VDD = 16V, Io = -20mA			0.8	V
V_{OH}	Output voltage high	VDD = 16V, Io = 20mA	10			V
V_{Clamp}	Output clamp voltage			18		V
T_r	Rising time	VDD = 16V, GATE with 1nF to GND		200		ns
T_f	Falling time	VDD = 16V, GATE with 1nF to GND		70		ns

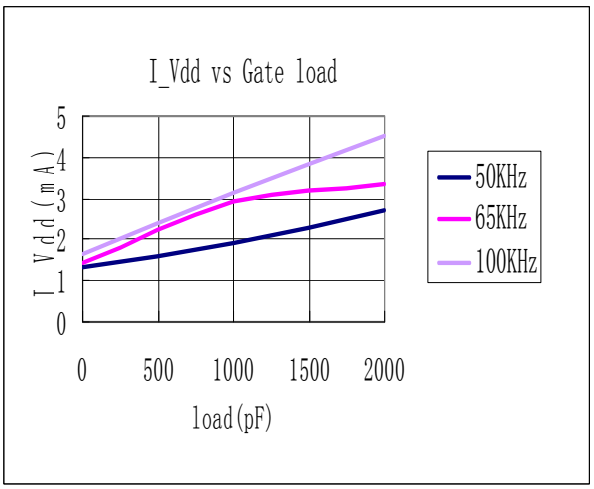
Typical Operating Characteristics

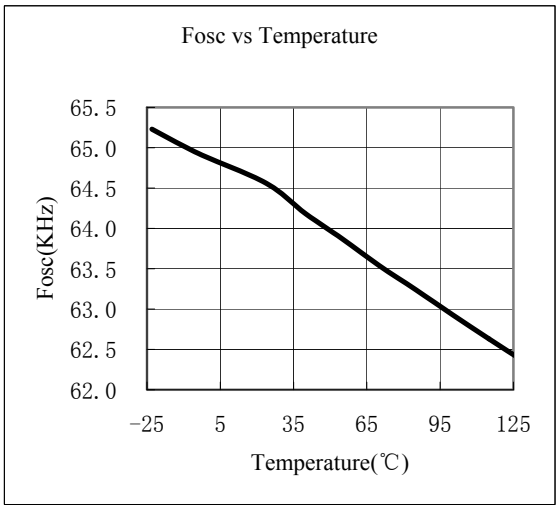





IVDD vs VDD
IVDD(uA)
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
VDD(V)


IVDD_startup vs VDD
IVDD_startup(uA)
20
15
10
5
0
0
2
4
6
8
10
12
14
VDD(V)


I_Vdd vs Gate load
I_Vdd(mA)
5
4
3
2
1
0
0
500
1000
1500
2000
load(pF)
50KHz
65KHz
100KHz


Fosc vs Temperature
Fosc(KHz)
65.5
65.0
64.5
64.0
63.5
63.0
62.5
62.0
-25
5
35
65
95
125
Temperature(℃)

Function Description

XN1049 is a highly integrated current mode PWM control IC which is optimized for high performance. It is applied for switch power of the small-sized and medium-sized for example the power adaptor. The knockdown startup current, operation current and burst mode function at the condition of no load and low load can decrease the standby cost of the power supply system effectively, and improve the power convert efficiency. The internal synchronous slope compensation, the leading edge blanking function of the flyback pin not only decrease the component number, but also improve the stability of the system and avoid the harmonics generation. XN1049 also have multiform general recovery protection mode. The main function is described as below.

Startup Current and Startup Control

Startup current of XN1049 is designed to be very low at 4μA so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss, predigest the design of startup circuit and provides reliable startup in application. For the design of AC/DC adaptor with universal input range, a startup resistor of 2 MΩ, 1/8 W could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The operating current of XN1049 is low at 1.4mA. Good efficiency is achieved with low operating current together and extended burst mode control circuit which can decrease the requirement of the VDD hold capacitor.

Extended Burst Mode Operation

At the condition of zero load or light load, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. XN1049 self adjusts the switching mode according to the loading condition. At the condition of no load or light/medium load, the FB input drops below burst mode threshold level. Device enters Burst Mode control on the basis of the judgment. The gate drive output switches only when VDD voltage drops below a preset level and FB input is active. Otherwise the gate drive remains at off-state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the charge/discharge time of the constant current source to the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation
within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = \frac{6500}{RI(Kohm)}(Khz)$$

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in XN1049 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds slope voltage onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

The GATE of XN1049 is connected to the gate of an external MOSFET for power switch control. The gate drive strength which is too weak results in over switch loss of MOSFET while too strong gate drive output compromises the over EMI. A good tradeoff which is in output strength and dead time control is achieved through the design of the built-in totem pole gate. The low standby loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO). The built-in OCP protection circuit can detect the average of the PWM signal effectively. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

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