SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	32.0" WXGA TFT LCD

BUYER	KONKA
MODEL	

SUPPLIER	LG.Display Co., Ltd.
*MODEL	LC320DXJ
SUFFIX	SFE1 (RoHS Verified)

APPROVED BY		SIGNATURE DATE
/		
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/		

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
S.J. Lee / Team Leader	6/5/08
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TV Products Development Dept.
LG. Display LCD Co., Ltd

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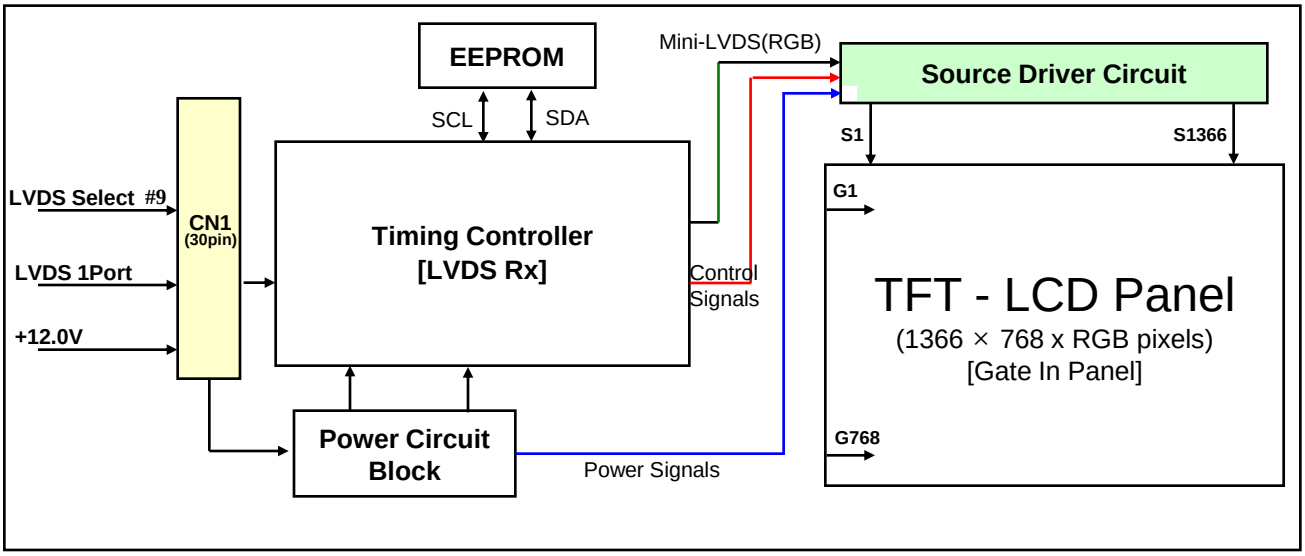
RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	Sep, 19, 2012	-	Preliminary Specification(First Draft)
0.2	Oct, 11, 2012	-	Kit. Biz New CAS Up-dated
0.3	Jan, 07, 2013	4	Up-dated General Features
		15	Up-dated Table 6. OPTICAL CHARACTERISTICS
		25, 28, 29	Up-dated 9-1. Packing Form, APPENDIX-I, APPENDIX-I-2
1.0	Jan, 08, 2013	-	CAS Version 1.0 Release
		-	Final Specification

1. General Description

The LC320DDXJ is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 31.51 inch diagonally measured active display area with WXGA resolution (768 vertical by 1366 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(6bit + FRC) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	31.51 inches(800.4mm) diagonal
Outline Dimension	715.0(H) x 411.0 (V) x 1.3 mm(D) (Typ.)
Pixel Pitch	170.25㎛ x 510.75㎛ x RGB
Pixel Format	1366 horiz. by 768 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit (D), 16.7 M colors
Drive IC Data Interface	Source D-IC : 6-bit mini-LVDS, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Transmittance (With POL)	6.15 % (Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Weight	0.86 Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment (Top)	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze < 1%)

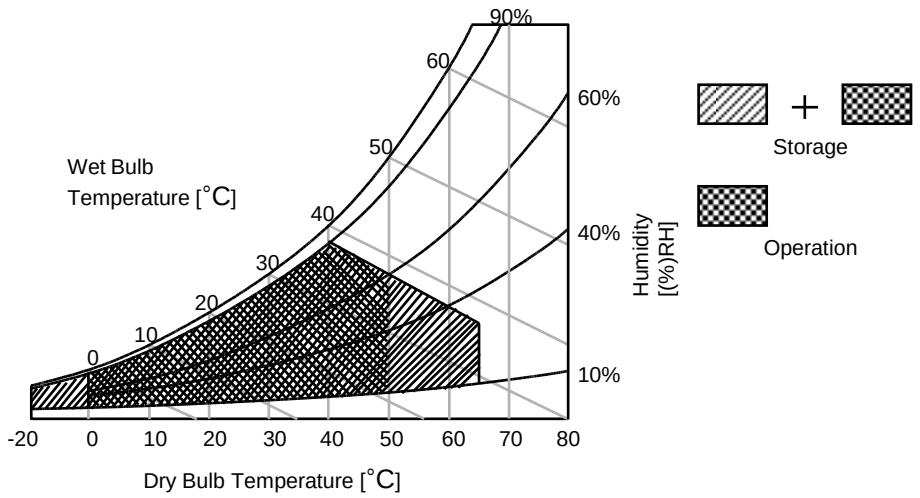
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	LCD Circuit	VLCD	-0.3	+14.0	VDC	1
T-Con Option Selection Voltage		VLOGIC	-0.3	+4.0	VDC	
Operating Temperature		TOP	0	+50	˚C	2,3
Storage Temperature		TST	-20	+60	˚C	
Panel Front Temperature		TSUR	-	+68	˚C	4
Operating Ambient Humidity		HOP	10	90	%RH	2,3
Storage Humidity		HST	10	90	%RH	

Notes: 1. Ambient temperature condition (Ta = 25 ± 2 ˚C)
2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 ˚C and no condensation of water.
3. Gravity mura can be guaranteed below 40℃ condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 ℃ with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 ℃. The range of operating temperature may degrade in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

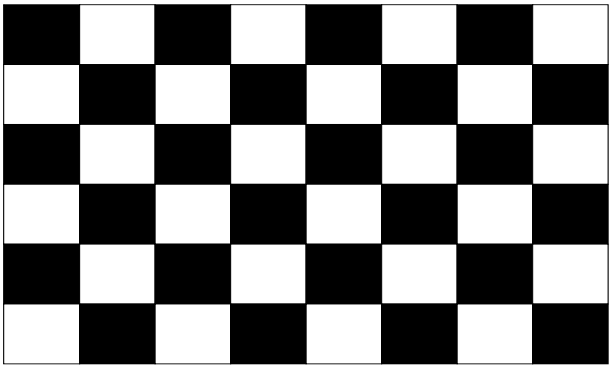
It requires two power inputs. One is employed to power for the LCD circuit. The other Is used for the LED backlight

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	notes
		Min	Typ	Max		
Circuit :						
Power Input Voltage	V_{LCD}	10.8	12.0	13.2	V_{DC}	
Power Input Current	I_{LCD}	-	255	332	mA	1
		-	320	416	mA	2
Power Consumption	P_{LCD}		3.1	4.0	Watt	1
Rush current	I_{RUSH}	-	-	4.0	A	3

Notes :
1. The specified current and power consumption are under the V_{LCD}=12.0V, Ta=25 ± 2°C, f_V=60Hz condition, and mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The duration of rush current is about 2ms and rising time of power input is 0.5ms (min.).
4. Ripple voltage level is recommended under ±5% of typical voltage

White : 255 Gray
Black : 0 Gray



Mosaic Pattern(8 x 6)

3-2. Interface Connections

3-2-1. LCD Module

- LCD Connector(CN1) : FI-X30SSL-HF (Manufactured by JAE) or Compatible.
- Mating Connector : FI-X30C2L (Manufactured by JAE) or Equivalent

Table 3. MODULE CONNECTOR(CN1) PIN CONFIGURATION

Pin No.	Symbol	Description	Note
1	VLCD	Power Supply +12.0V	
2	VLCD	Power Supply +12.0V	
3	VLCD	Power Supply +12.0V	
4	VLCD	Power Supply +12.0V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	LVDS Select	'H' =JEIDA , 'L' or NC = VESA	Appendix IV
10	NC	No Connection	4
11	GND	Ground	
12	RA-	LVDS Receiver Signal(-)	
13	RA+	LVDS Receiver Signal(+)	
14	GND	Ground	
15	RB-	LVDS Receiver Signal(-)	
16	RB+	LVDS Receiver Signal(+)	
17	GND	Ground	
18	RC-	LVDS Receiver Signal(-)	
19	RC+	LVDS Receiver Signal(+)	
20	GND	Ground	
21	RCLK-	LVDS Receiver Clock Signal(-)	
22	RCLK+	LVDS Receiver Clock Signal(+)	
23	GND	Ground	
24	RD-	LVDS Receiver Signal(-)	
25	RD+	LVDS Receiver Signal(+)	
26	GND	Ground	
27	NC	No Connection (Note 4)	4
28	NC	No Connection (Note 4)	4
29	NC	No Connection (Note 4)	4
30	GND	Ground	

Notes :

1. All GND (Ground) pins should be connected together to the LCD module's metal frame.
2. All VLCD (power input) pins should be connected together.
3. All Input levels of LVDS signals are based on the EIA 644 Standard.
4. These pins are used only for LGD (Do not connect)
5. Specific pin No. #30 is used for "No signal detection" of system signal interface.
   It should be GND for NSB (No Signal Black) while the system interface signal is not.
   If this pin is "H", LCD Module displays AGP (Auto Generation Pattern).

3-3. Signal Timing Specifications

Table 6 shows the signal timing required at the input of the LVDS transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 4. TIMING TABLE (DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	-	1366	-	tclk	
	Blank	t_{HB}	90	162	410	tclk	
	Total	t_{HP}	1456	1528	1776	tclk	
Vertical	Display Period	t_{VV}	-	768	-	t_{HP}	
	Blank	t_{VB}	20 (126)	22 (180)	240 (295)	t_{HP}	1
	Total	t_{VP}	**788** (894)	790 (948)	1008 (1063)	t_{HP}	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	63.0	72.4	80.0	MHz	
	Horizontal	f_H	45	47.4	55	KHz	2
	Vertical	f_V	57 (47)	60 (50)	63 (53)	Hz	2 NTSC : 57~63Hz (PAL : 47~53Hz)

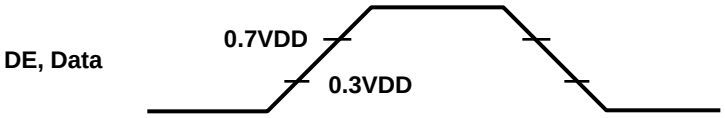
Note: 1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.

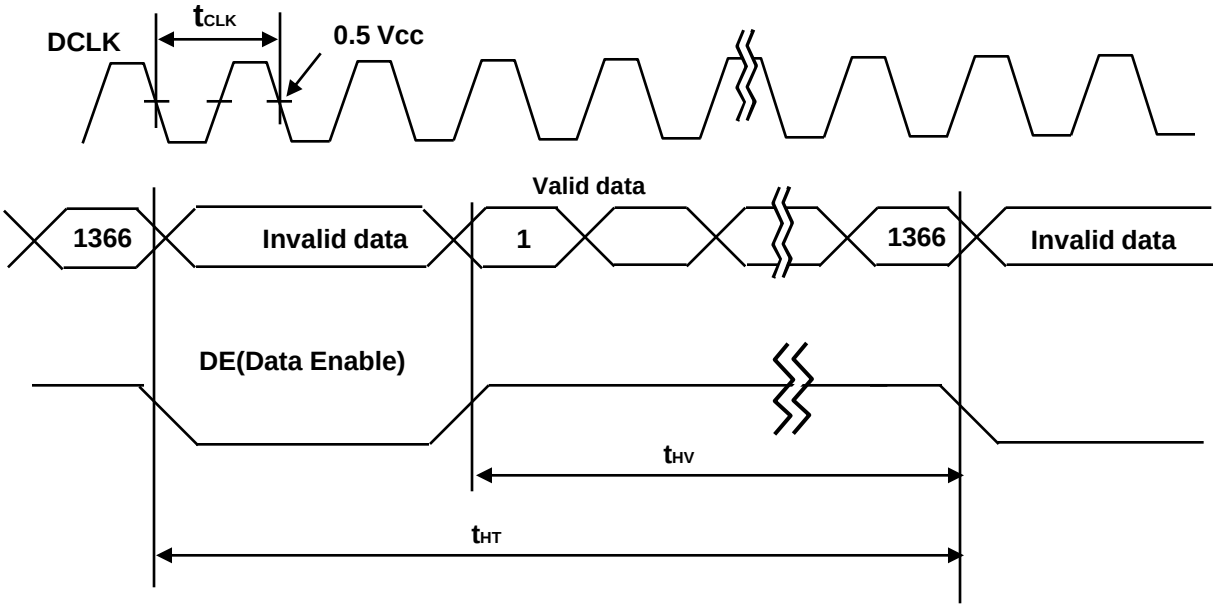
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency

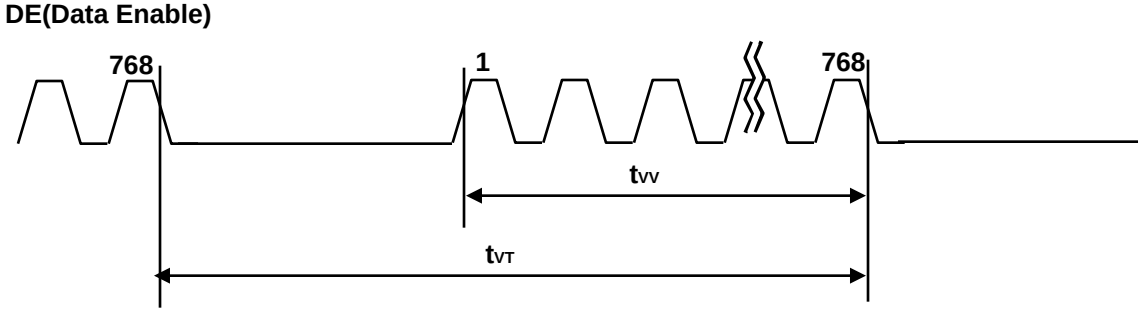
※ Timing should be set based on clock frequency.

3-4. LVDS Signal Specification

3-4-1. LVDS Input Signal Timing Diagram

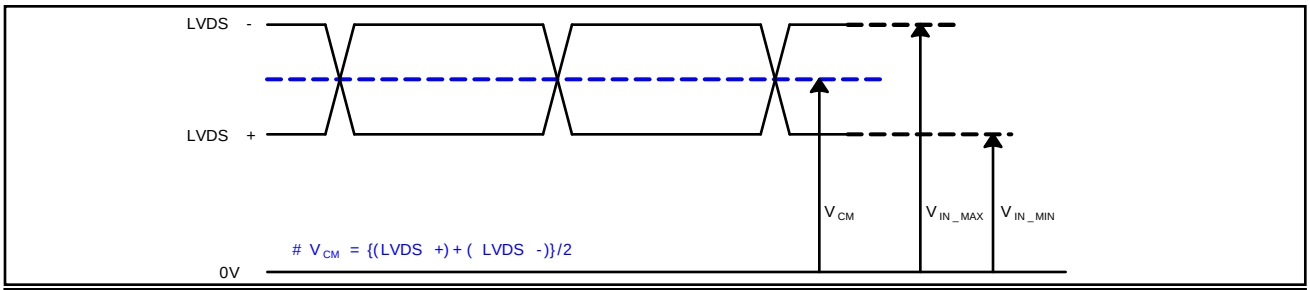






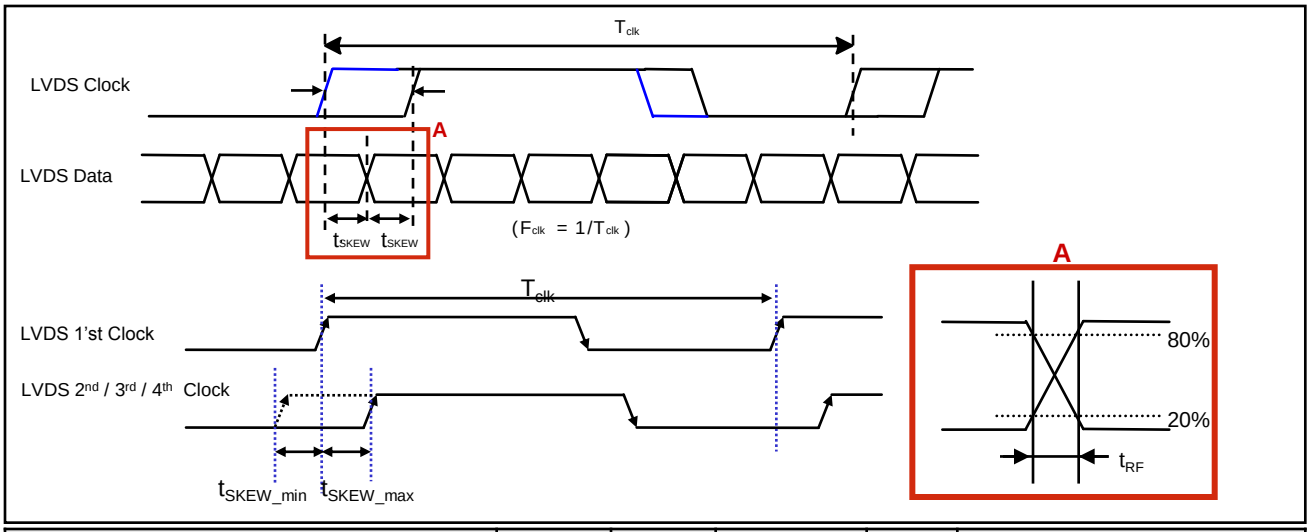
3-4-2. LVDS Input Signal Characteristics

1) DC Specification



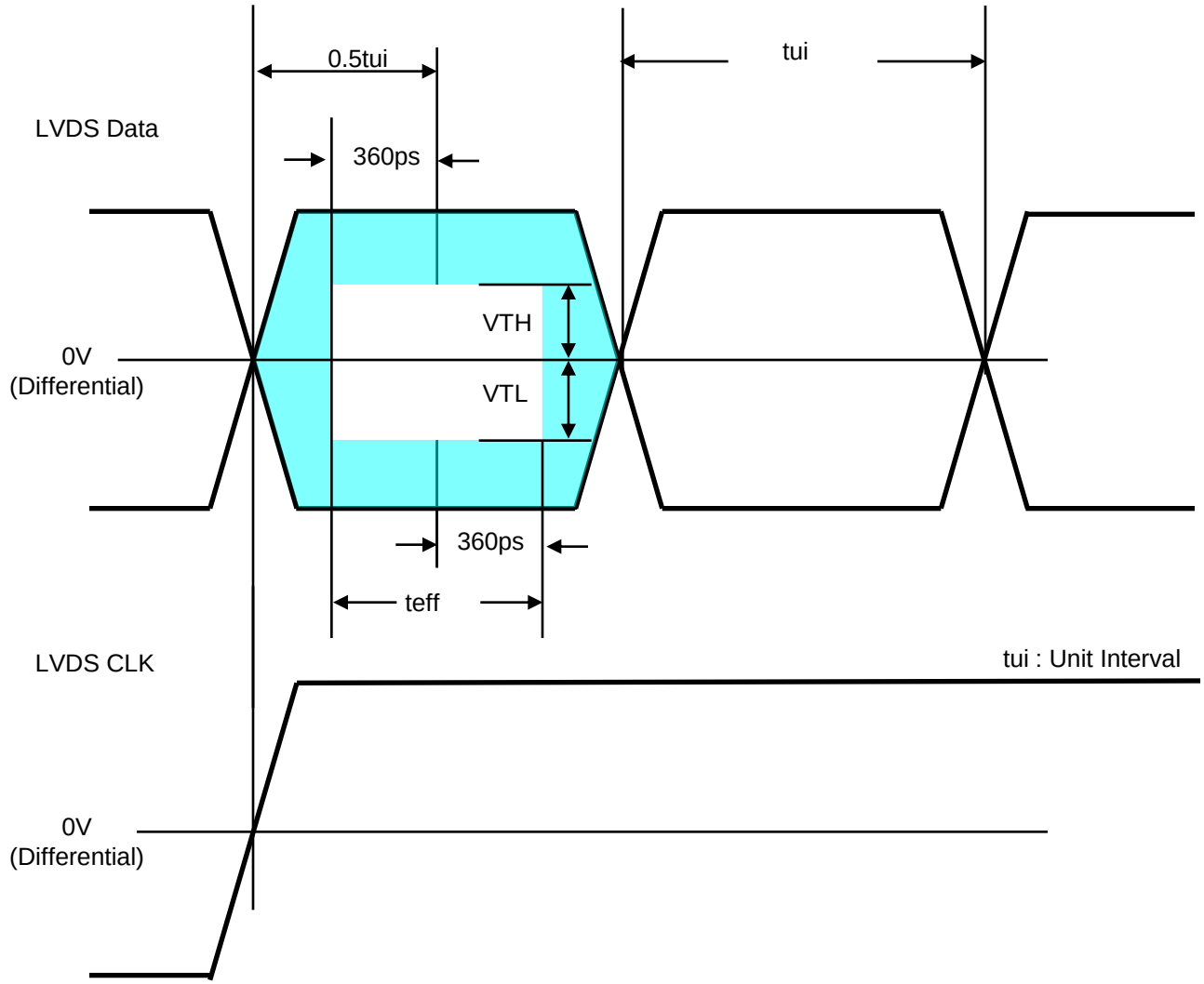
Description	Symbol	Min	Max	Unit	Note
LVDS Common mode Voltage	V_{CM}	1.0	1.5	V	-
LVDS Input Voltage Range	V_{IN}	0.7	1.8	V	-
Change in common mode Voltage	ΔVCM	-	250	mV	-

2) AC Specification



Description	Symbol	Min	Max	Unit	Note
LVDS Differential Voltage	V_{TH}	100	600	mV	Tested with Differential Probe 3
	V_{TL}	-600	-100	mV	
LVDS Clock to Data Skew	t_{SKEW}	-	$\|(0.20*T_{clk})/7\|$	ps	-
LVDS Clock/DATA Rising/Falling time	t_{RF}	260	$\|(0.3*T_{clk})/7\|$	ps	2
Effective time of LVDS	t_{eff}	$\|\pm 360\|$	-	ps	-
LVDS Clock to Clock Skew (Even to Odd)	t_{SKEW_EO}	-	$\|1/7* T_{clk}\|$	ps	-

notes 1. All Input levels of LVDS signals are based on the EIA 644 Standard.
2. If t_{RF} isn't enough, t_{eff} should be meet the range.
3. LVDS Differential Voltage is defined within t_{eff}



* This accumulated waveform is tested with differential probe

3-5. Intra interface Signal Specification

3-5-1. Mini-LVDS Signal Specification

Table 5. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	notes
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V		-	290	MHz	
mini-LVDS input Voltage (Center)	V_{IB}	Mini-LVDS Clock and Data	0.7 + (VID/2)	-	(VCC-1.2) − VID / 2	V	
mini-LVDS input Voltage Distortion (Center)	ΔV_{IB}		-	-	0.8	V	
mini-LVDS differential Voltage range	V_{ID}		200	-	800	mV	
mini-LVDS differential Voltage range Dip	ΔV_{ID}		25	-	800	mV	

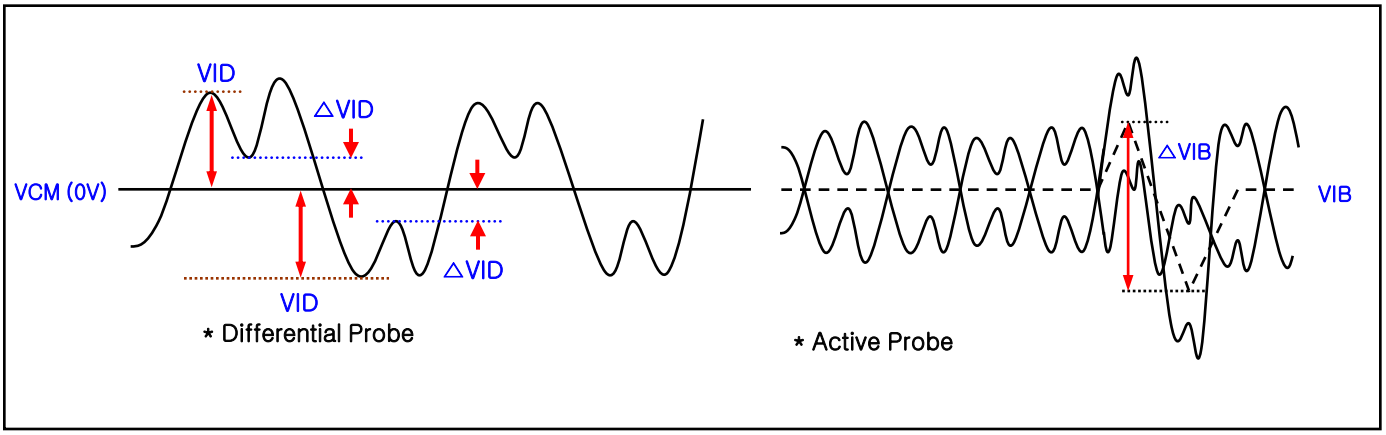


FIG. 1 Description of VID, ΔVIB, ΔVID

* Source PCB

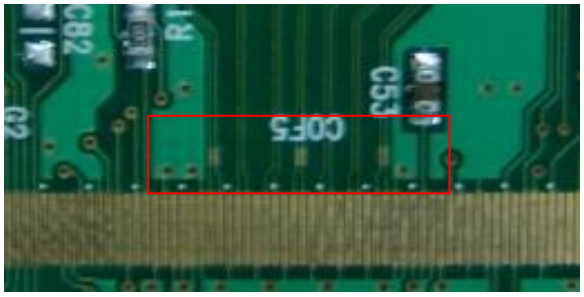


FIG. 2 Measure point

3-6. Color Data Reference

The brightness of each primary color(red,green,blue) is based on the 8bit gray scale data input for the color. The higher binary input, the brighter the color. Table 7 provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (000)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (001)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	...					**...**								...								...			
	RED (254)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (000)	0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	0	0	0	0	0	0	0
	GREEN (001)	0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	0	0	0	0	0	0	0	0
	...					...								**...**								...			
	GREEN (254)	0	0	0	0	0	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	0	0	0	0	0	0	0	0
BLUE	BLUE (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	BLUE (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	...					...								...								**...**			
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

3-7. Power Sequence

3-6-1. LCD Driving circuit

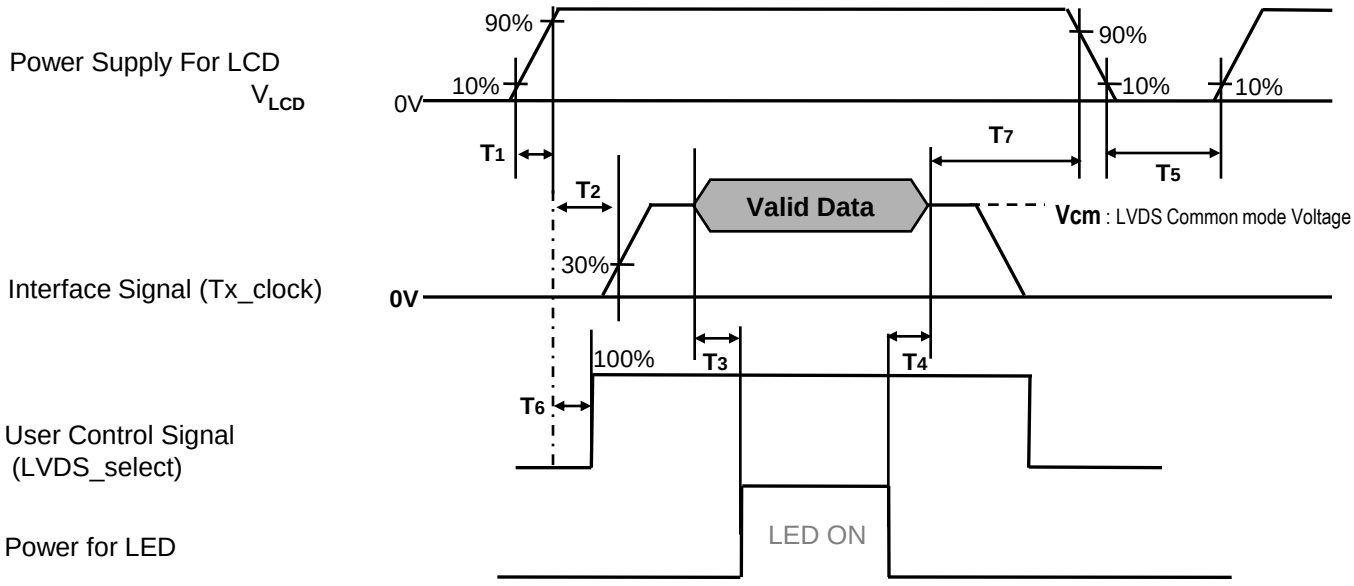


Table 8. POWER SEQUENCE

Parameter	Value			Unit	Note
	Min	Typ	Max		
T1	0.5	-	20	ms	1
T2	0	-	-	ms	2
T3	400	-	-	ms	3
T4	200	-	-	ms	3
T5	1.0	-	-	s	4
T6	0	-	T2	ms	5
T7	0	-	-	ms	6

Note :

1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.
2. If T2 is satisfied with specification after removing LVDS Cable, there is no problem.
3. The T3 / T4 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.
4. T5 should be measured after the Module has been fully discharged between power off and on period.
5. If the on time of signals (Interface signal and user control signals) precedes the on time of Power (V_{LCD}), it will be happened abnormal display. When T6 is NC status, T6 doesn't need to be measured.
6. It is recommendation specification that T7 has to be 0ms as a minimum value.

※ Please avoid floating state of interface signal at invalid period.
※ When the power supply for LCD (VLCD) is off, be sure to pull down the valid and invalid data to 0V.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °. FIG. 6 shows additional information concerning the measurement equipment and method.

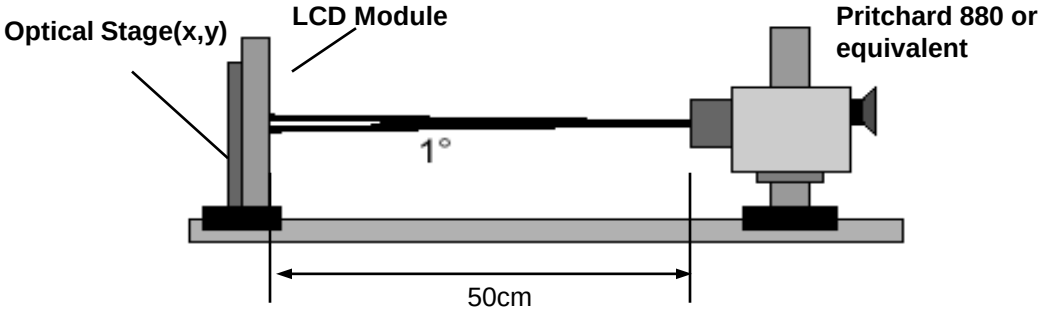


FIG. 3 Optical Characteristic Measurement Equipment and Method

Ta= 25±2°C, VDD,H_VDD,VGH,VGL=typ, fv=60Hz,
BW=0.693GBPS , **EXTV**BR-B =100% Back Light : LGD B/L

Table 6. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	notes
			Min	Typ	Max		
Contrast Ratio		CR	850	1200	-		1
Response Time	Rising	Tr	-	8	12	ms	2
	Falling	Tf	-	10	14		
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.647	Typ +0.03		
		Ry		0.331			
	GREEN	Gx		0.306			
		Gy		0.587			
	BLUE	Bx		0.151			
		By		0.063			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	3
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	-	-		4

notes : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance are determined after the unit has been 'ON' and 1 Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 3.
3. Response time is the time required for the display to transit from any gray to white (Rise Time, Tr_R) and from any gray to black (Decay time, Tr_D). For additional information see the FIG. 5.
※ G to G_{BW} Spec stands for average value of all measured points.
Photo Detector : RD-80S / Field : 2 °
4. G to G $_\sigma$ is Variation of Gray to Gray response time composing a picture

$$\text{G to G } (\sigma) = \sqrt{\frac{\Sigma(Xi - u)^2}{N}}$$

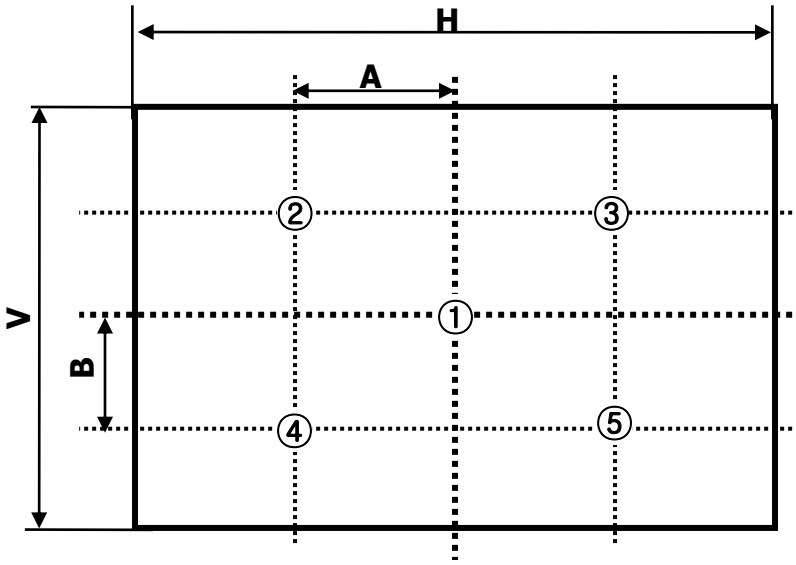
Xi = Individual Data
u = Data average
N : The number of Data

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 6.
6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 7.

Table 7. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.08
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

Measuring point for surface luminance & luminance variation



A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

FIG. 4 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Black" ~ "White" and "White" ~ "Black".

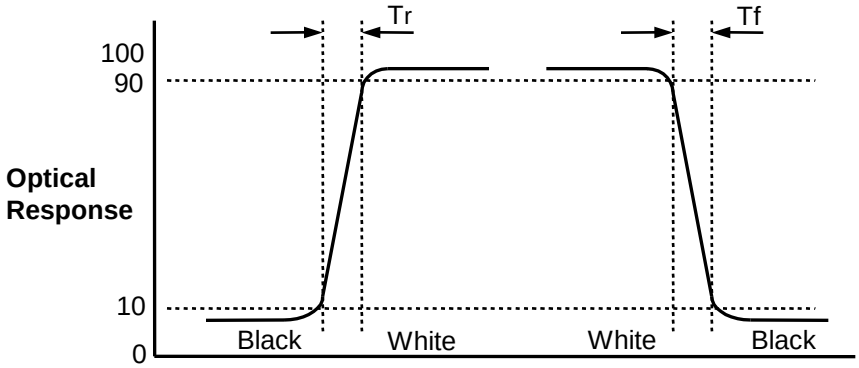


FIG. 5 Response Time

Dimension of viewing angle range

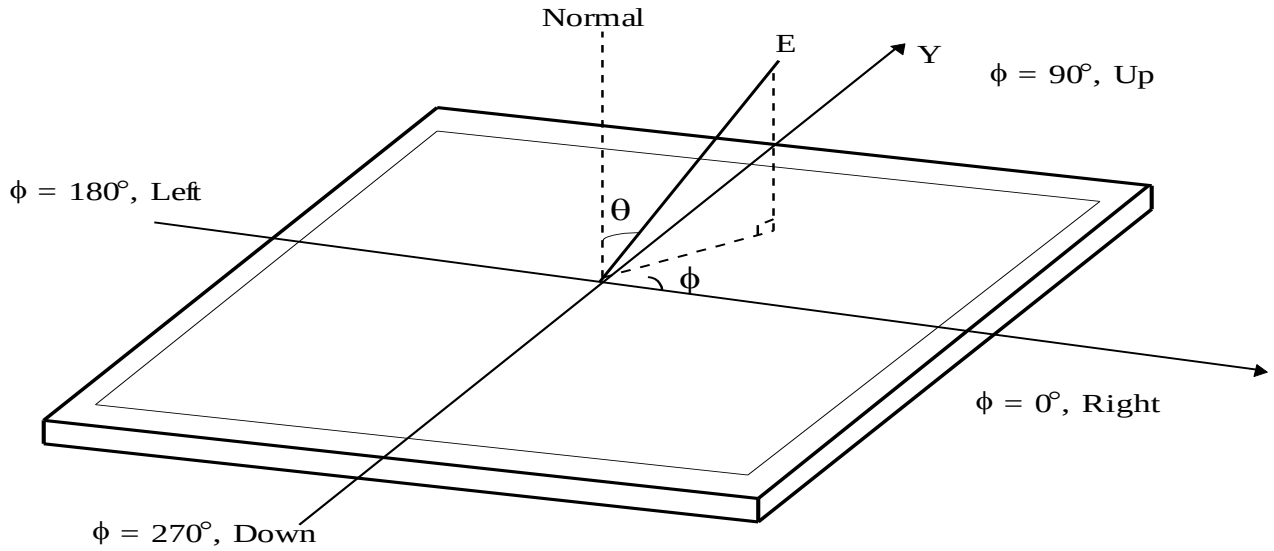


FIG.6 Viewing Angle

5. Mechanical Characteristics

Table 8 provides general mechanical characteristics.

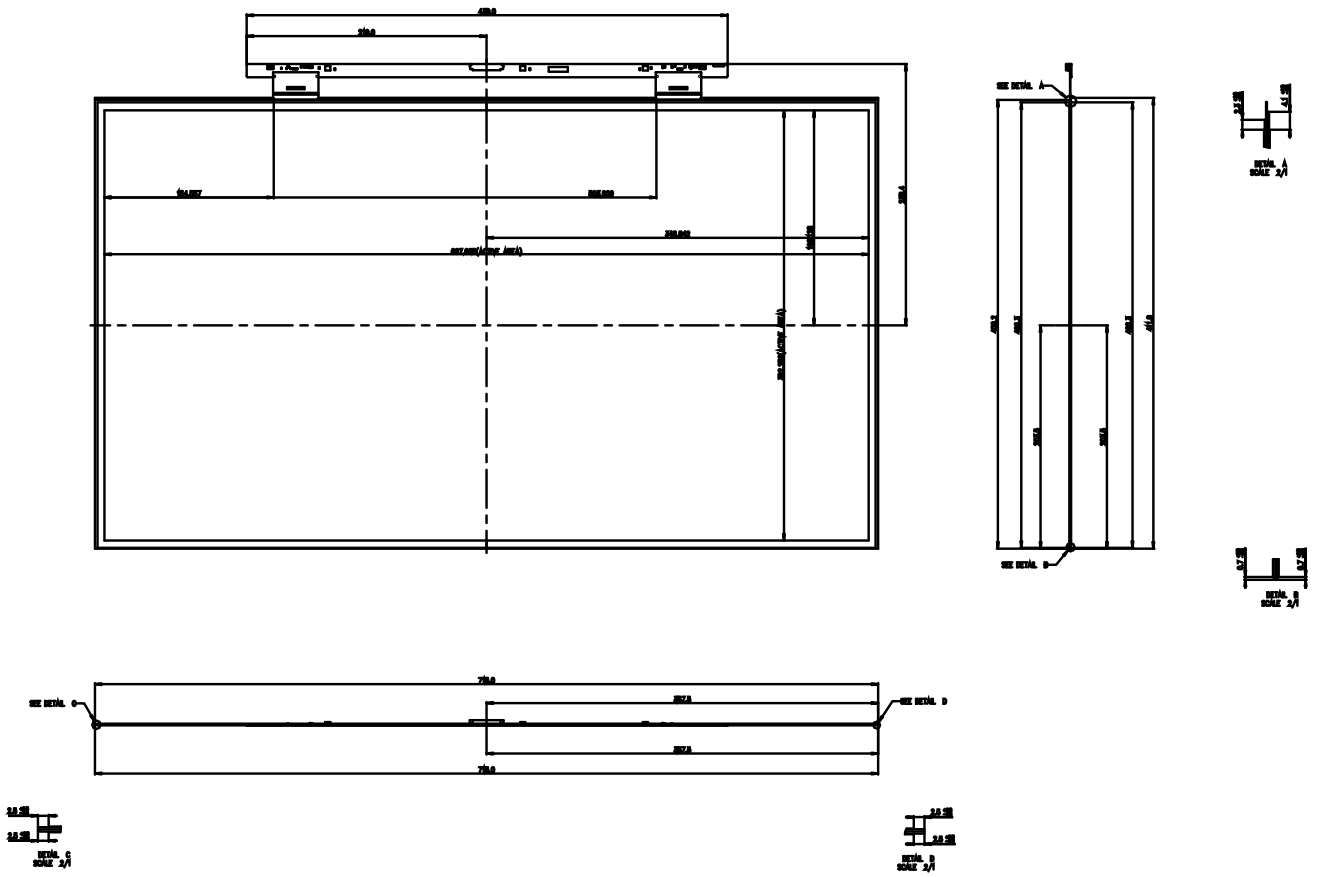
Table 8. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension (Only Glass)	Horizontal	715.0mm
	Vertical	411.0mm
	Thickness	1.3 mm
Active Display Area	Horizontal	697.9mm
	Vertical	392.3mm
Weight	0.86 (TBD) kg(typ)	
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze < 1%)	

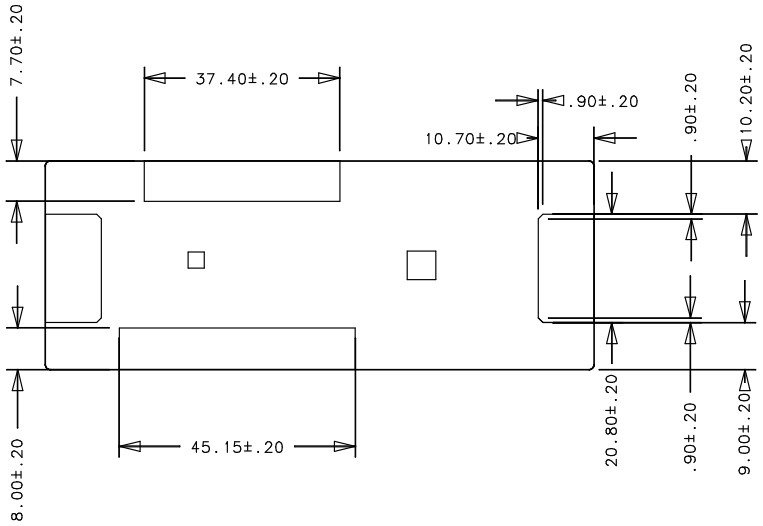
notes : Please refer to a mechanic drawing in terms of tolerance at the next page.

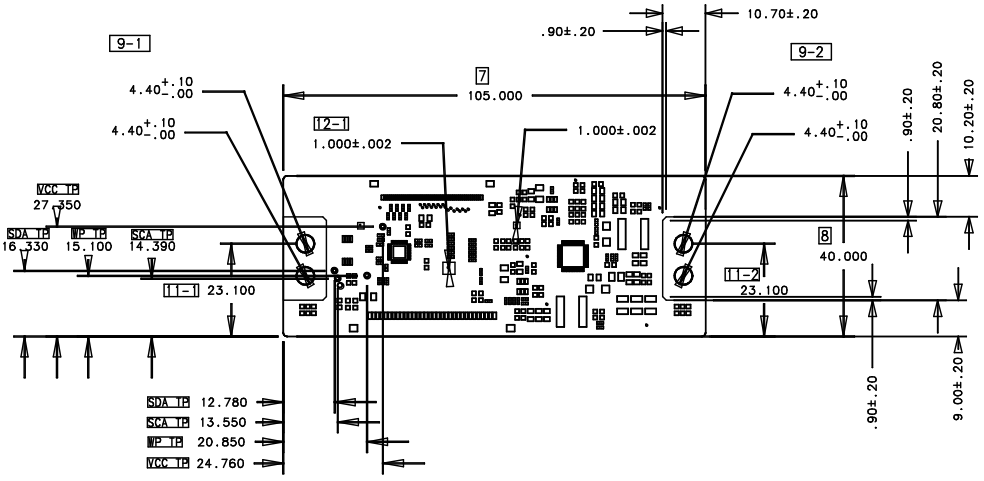
6. Mechanical Dimension

6-1. Board Assembly Dimension

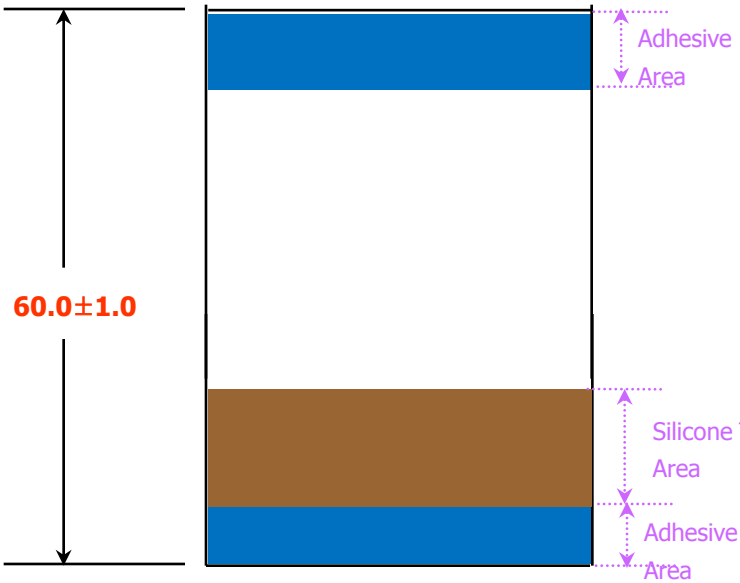


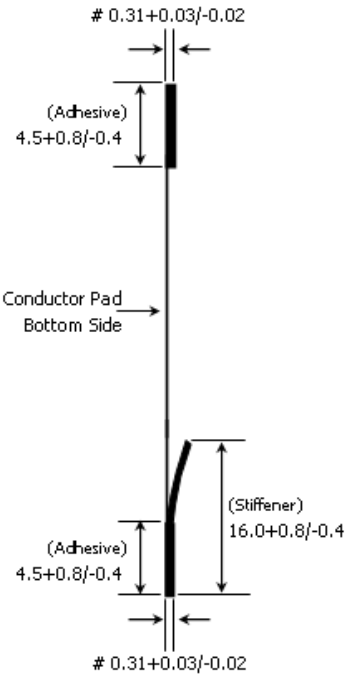
6-2. Control Board Assembly Dimension

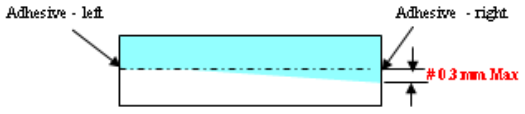




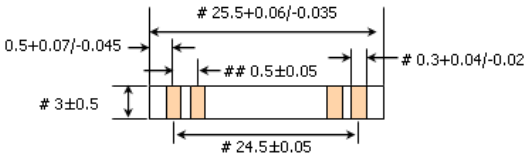
6-3. FFC Dimension







< Pad Detail– 50Pin >



◈ Note

- Layer : Single Side
- Pad : GOLD Plating
- #e dimension : Cpk 1.0 more
- ## dimension : Cpk 1.33 more
- Stiffener Color : Sky Blue
- H-F
- Dimension Unit : mm

- Material List

APPLICATION	STANDARD	MATERIAL	REFERENCE
1. CONDUCTOR	GOLD PLATED COPPER WIRE	1. 99.99% COPPER 2. GOLD PLATED	1. Tolerance - THICKNESS: ±0.01 - WIDTH: +0.04 -0.02 2. ELOGATION(%) : 10 MORE THAN 3. TENSION : (KGF) 0.2 MORE THAN 4. GOLD THICKNESS : 0.05 μm MIN *MAKER : DOSOL Processing : EunSung
2. INSULATION	POLYESTER FILM (PET/PET)	1. POLYESTER BASE FILM : 0.025 mm 2. POLYESTER HOTMELT ADHESIVE : 0.035 mm TOTAL THICKNESS : 0.060 mm	UL VW-1 FLAME Width : 120mm Length : 500M UNIT : ROLL * MAKER : COSMOAMT/ SHINCHANG HOTMELT
3. SUPPORTING TAPE	POLYESTER FILM	1. POLYESTER BASE FILM : 0.188 mm 2. POLYESTER HOTMELT ADHESIVE : 0.027 mm TOTAL THICKNESS : 0.215 mm	Width : 20.5mm Length : 250M Unit : ROLL *MAKER : SUNGSHIN Trading/ COSMOAMT
4. SILICON TAPE (BROWN)		TOTAL THICKNESS : 0.065 mm	*MAKER : DAEHYUN ST

7. Reliability

Table 9. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60˚C 240h
2	Low temperature storage test	Ta= -20˚C 240h
3	High temperature operation test	Ta= 50˚C 50%RH 240h
4	Low temperature operation test	Ta= 0˚C 240h
5	Humidity condition Operation	Ta= 40 ˚C ,90%RH
6	Altitude operating storage / shipment	0 - 16,400 ft 0 - 40,000 ft

notes : Before and after Reliability test, Board ass'y should be operated with normal function.

8. International Standards

8-1. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

9. Packing

9-1. Packing Form

a) Package quantity in one Pallet : 160 pcs

b) Pallet Size :1140 mm(L) X 910 mm(W) X 1085 mm(H)

10. Precautions

Please pay attention to the followings when you use this TFT LCD panel.

10-1. Assembly Precautions

(1) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(2) You should adopt radiation structure to satisfy the temperature specification.
(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Board ass'y should be put on the mold frame properly.
(8) FFC Cable should be connected between System board and Source PCB correctly.
(9) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.

10-2. Operating Precautions

(1) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(2) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(3) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or electrical impact to board assy. Otherwise, it can't be operated its full characteristics perfectly.

10-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.

10-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

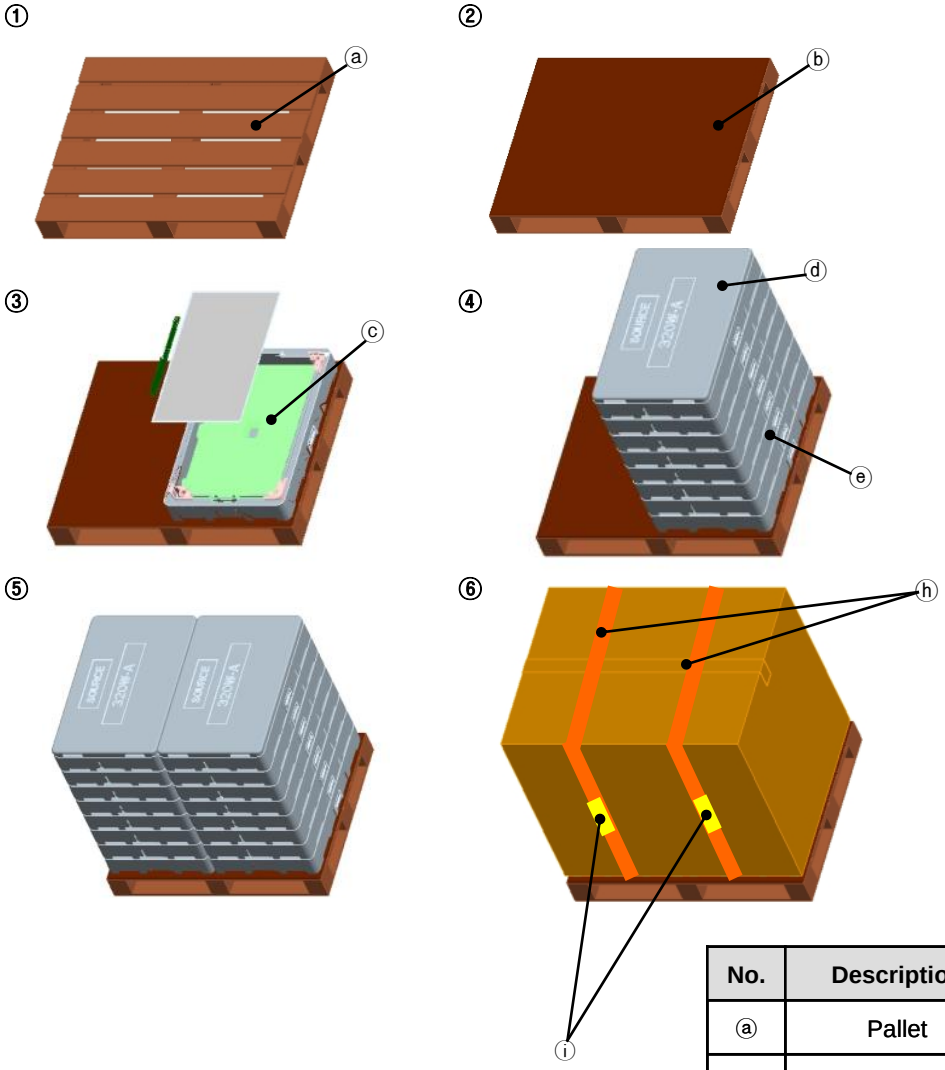
10-5. Storage

When storing the board ass'y as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the board ass'y to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

APPENDIX-I

■ Pallet Ass'y



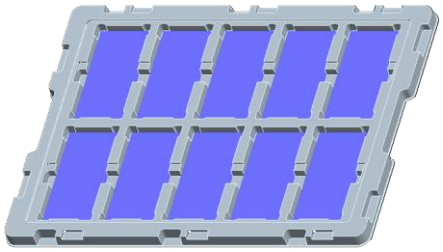
No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	Carton Plate	Single Wall
ⓒ	PE Sheet	Carbon
ⓓ	Top Packing	EPS
ⓔ	Bottom Packing	EPS
ⓕ	Angle Packing	Single Wall
ⓖ	Tape	OPP
ⓗ	Band	PP
ⓘ	Clip	PP

APPENDIX-I-2

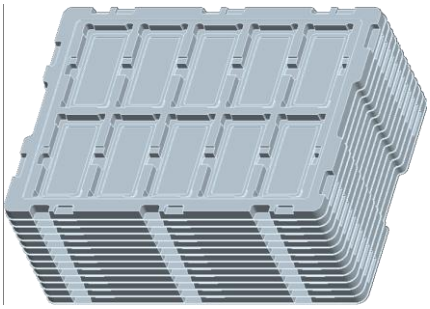
■ Control PCB Packing Ass'y

a) Control PCB Qty / Box : 160 pcs
b) Tray Qty / Box : 18Tray(Upperst Tray Is empty)
c) Tray Size : 466 X 353 X 16
d) Box size : 468 X 355 X 197

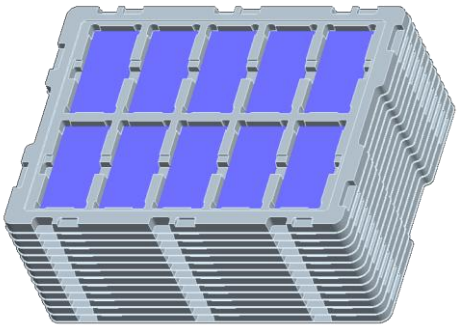
[10pcs/Tray]



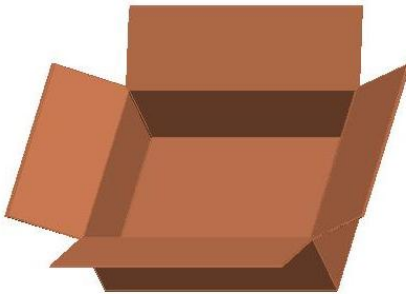
[18Tray+Empty Tray]



[17Tray]



[Inserting into Box



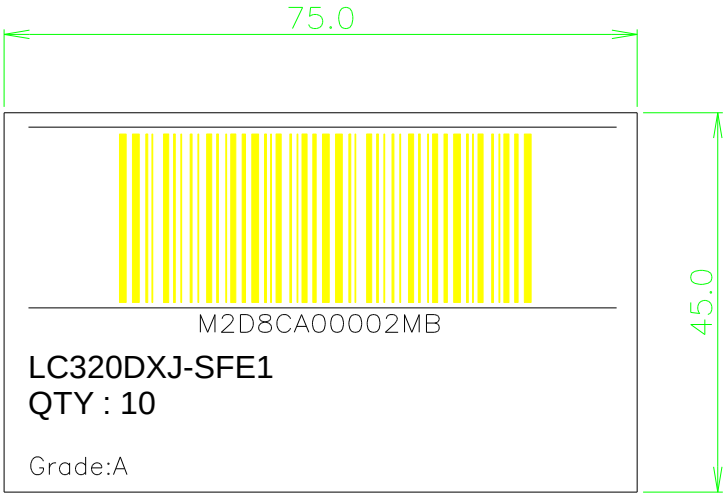
NO.	DESCRIPTION	MATERIAL
1	PCB Packing A,ssy	-
2	Tray	PET
3	Box	SWR4

 # APPENDIX- II-1

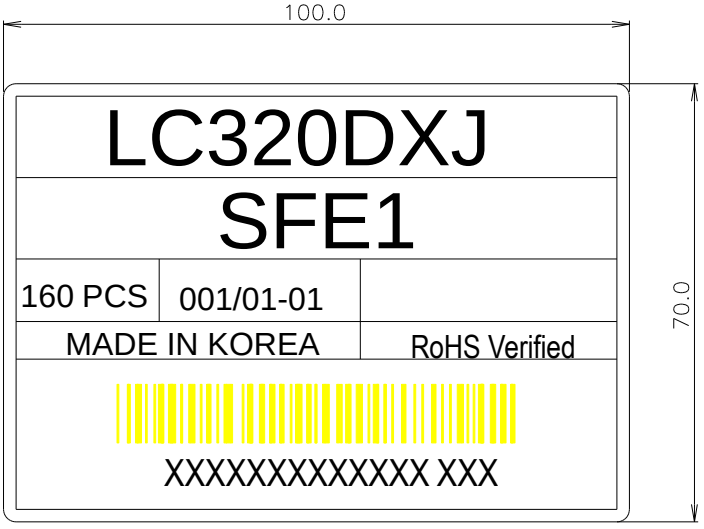
■ Board Ass'y ID Label

 # APPENDIX- II-2

■ BOX Label

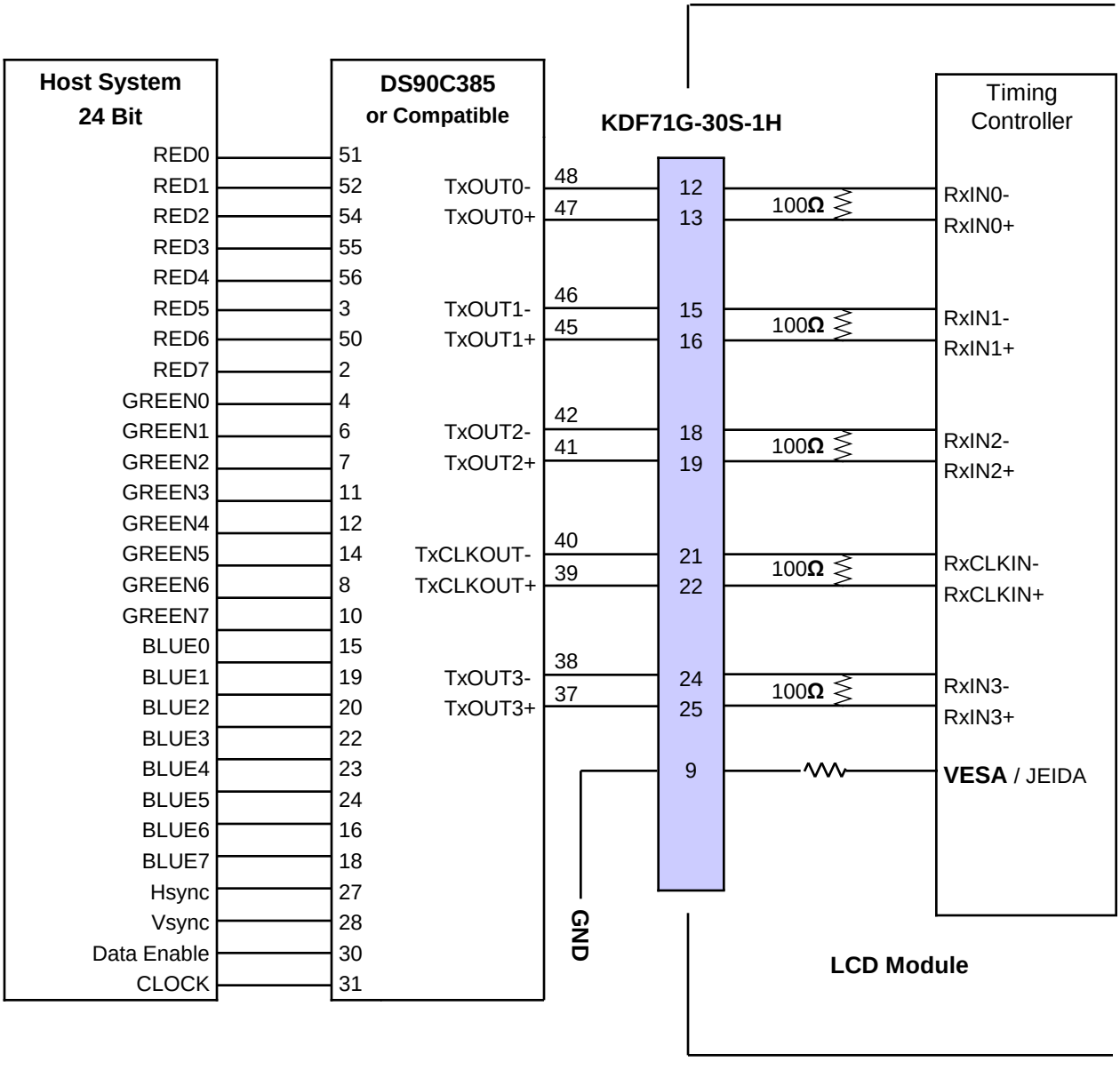


■ Pallet Label



APPENDIX- III-1

■ Required signal assignment for Flat Link (Thine : THC63LVD103) Transmitter(Pin7= **"L" or "NC"**)



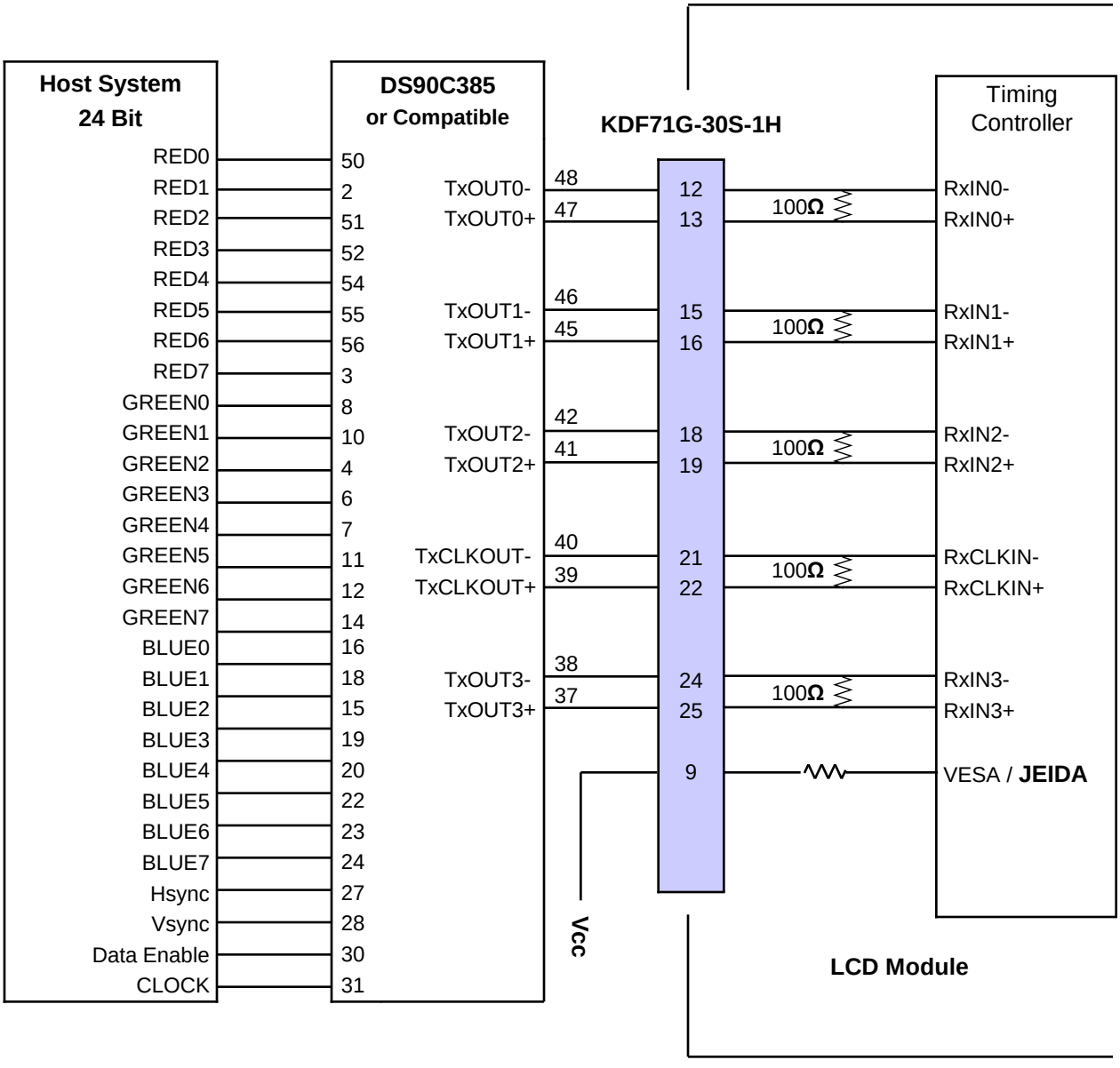
Note: 1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.

2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (THC63LVD103 or Compatible)

3. '7' means MSB and '0' means LSB at R,G,B pixel data.

APPENDIX- III-2

■ Required signal assignment for Flat Link (Thine : THC63LVD103) Transmitter(Pin7= **"H"**)



Note :1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.

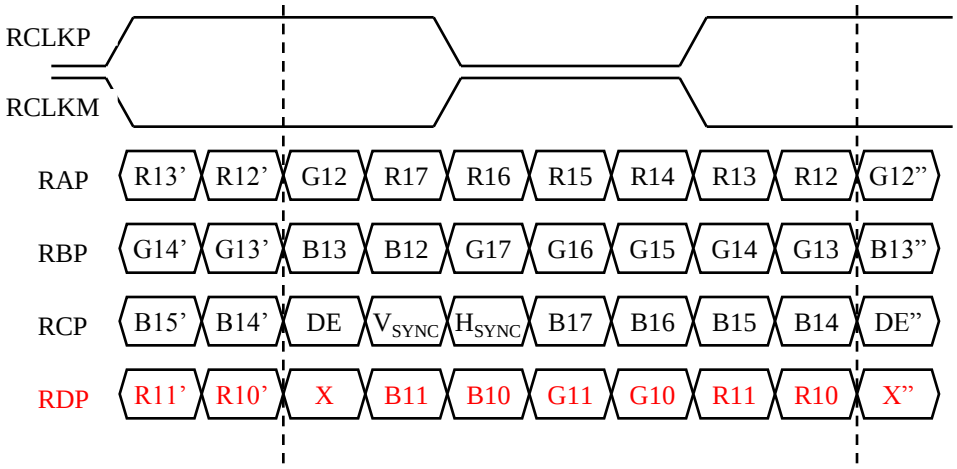
2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (THC63LVD103 or Compatible)

3. '7' means MSB and '0' means LSB at R,G,B pixel data.

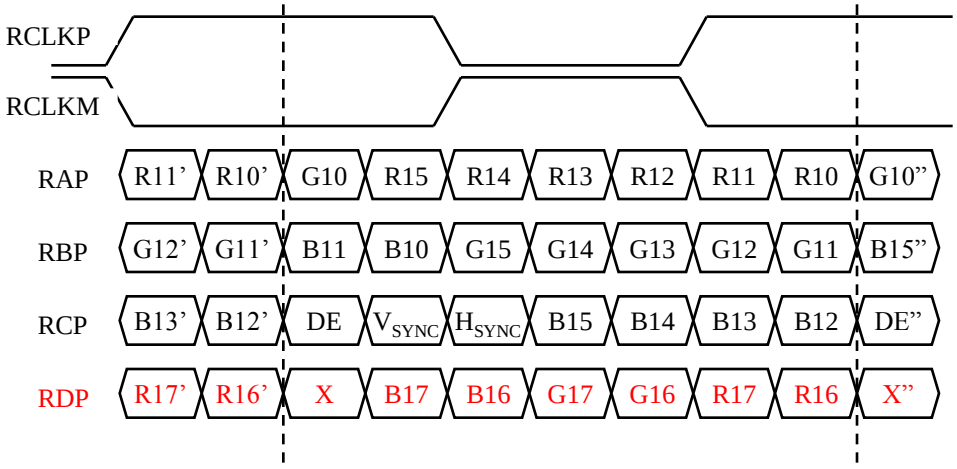
APPENDIX- IV

■ LVDS Data-Mapping Information (**8 Bit**)

1) LVDS Select : "**H**" Data-Mapping (**JEIDA format**)



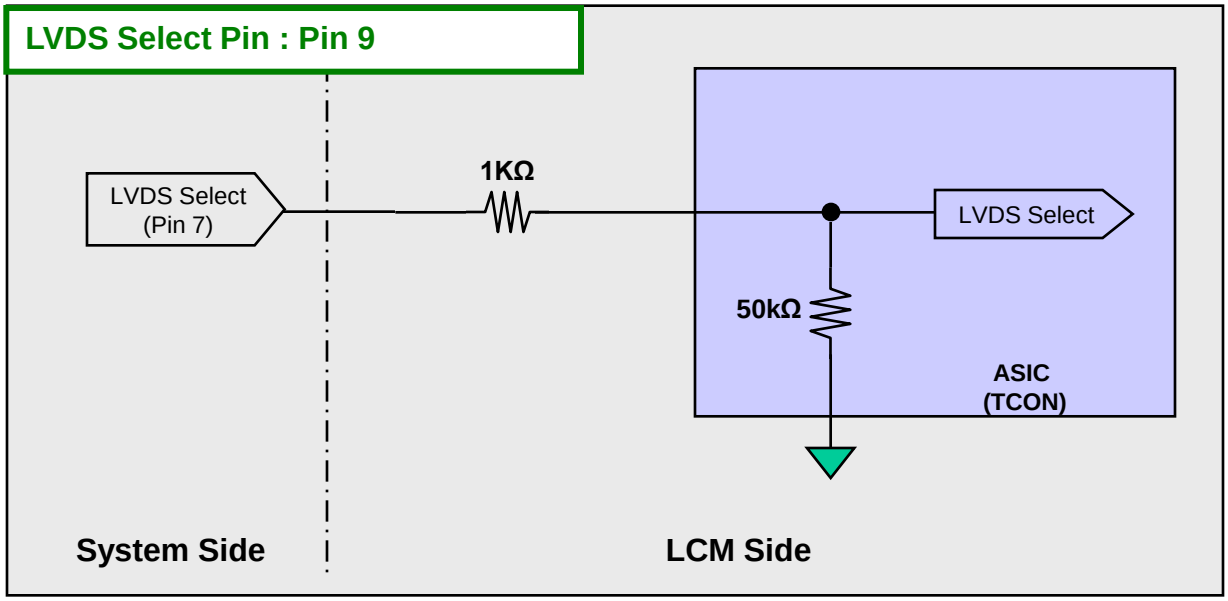
2) LVDS Select : "**L**" Data-Mapping (**VESA format**)



APPENDIX- V

■ **Option Pin** Circuit Block Diagram

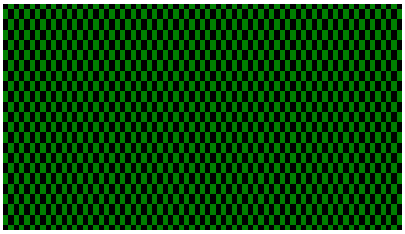
1) Circuit Block Diagram of **LVDS Format** Selection pin

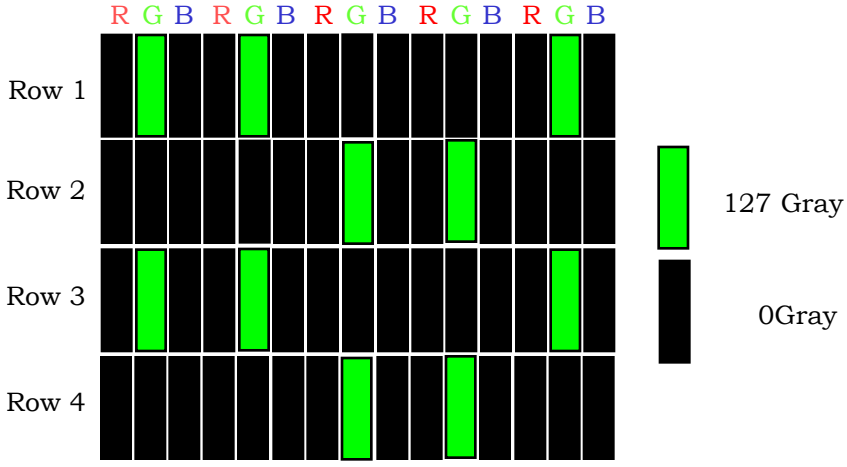


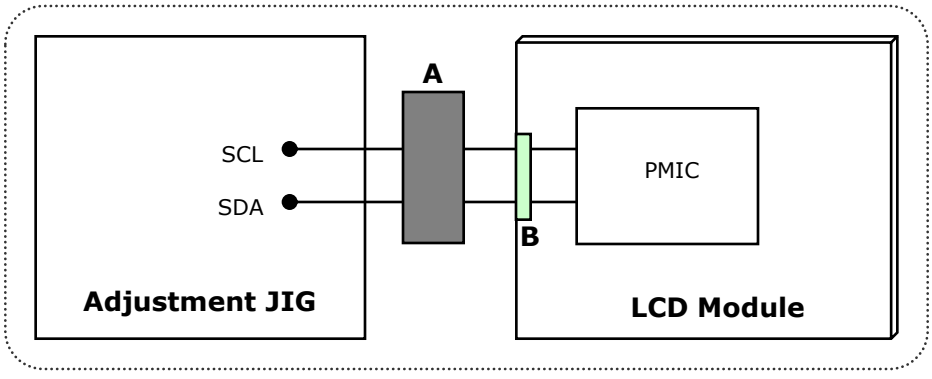
APPENDIX- VI

■ Flicker Adjustment

Parameter	Unit	Min	Typ	Max	Note
Inversion Method	-	H2-Dot Inversion			
Adjust Pattern / Gray Level	-	G H2-Dot Full Flicker, 127 Gray, 60Hz			60Hz
Position	-	Center			
Voltage range	V	5.4	6.4	7.4	







A : Pull-up Resistors (If it is necessary)

B : I2C Connector (Refer to Appendix IX)

FIG.7 VCOM Adjustment Pattern & Block Diagram

APPENDIX-Ⅶ

■ The reference method of BL burst dimming

It is recommended to use synchronous V-sync frequency to prevent waterfall
(Vsync * 2 =Burst Frequency)