SSC9522S

Data Sheet

Description

The SSC9522S is a controller IC (SMZ* method) for half-bridge resonant type power supply, incorporating a floating drive circuit for the high-side power MOSFET drive.

The product achieves high efficiency, low noise and high cost-performance power supply systems with few external components.

*SMZ; Soft-switched Multi-resonant Zero Current switch (All switching periods work with soft switching operation.)

Features

- Built-in floating drive circuit for high-side power MOSFET
- Soft Start Function
- Capacitive Mode Operation Detection Function (Pulse-by-pulse)
- Automatic Dead Time Adjustment Function
- Brown-in and Brown-out Function
- Protections
  High-side Driver UVLO Protection
  External Latched Shutdown Function
  Overcurrent Protection (OCP): Three steps protection corresponding to overcurrent levels
  Overload Protection (OLP): Latched shutdown
  Overvoltage Protection (OVP): Latched shutdown
  Thermal Shutdown (TSD): Latched shutdown

Package

SOP18

Not to Scale

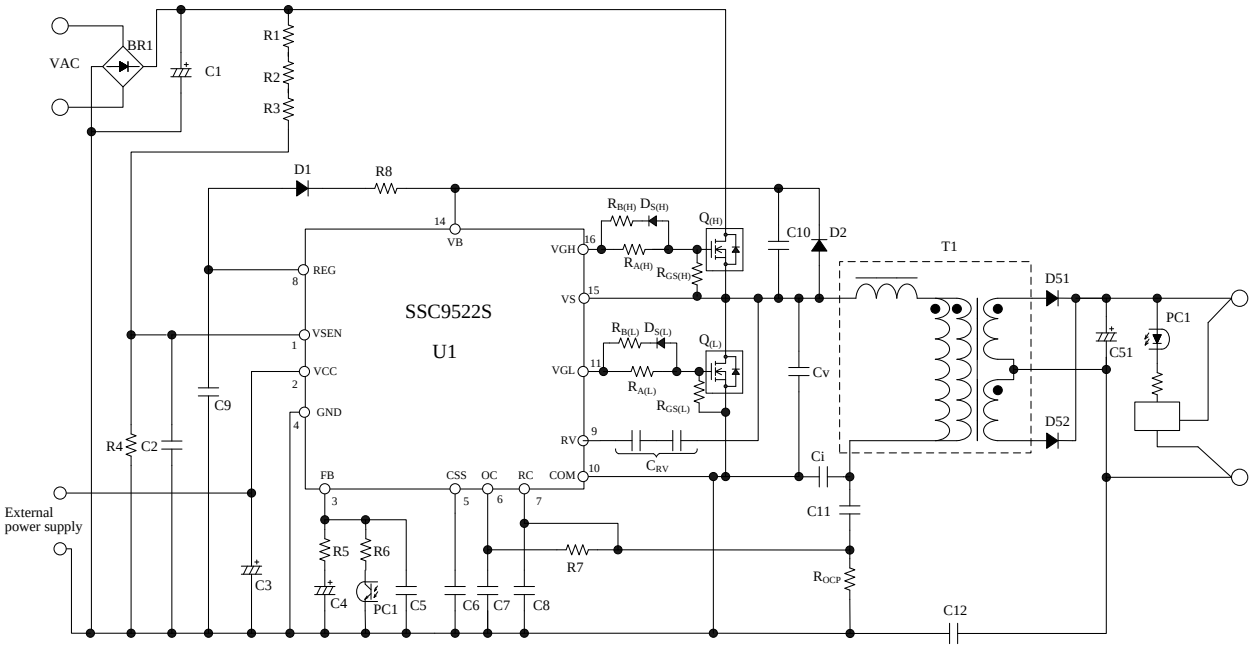
Electrical Characteristics

- Absolute maximum rating of VCC pin is 35 V
- Minimum oscillation frequency is 28.3 kHz (typ.)
- Maximum oscillation frequency is 300 kHz (typ.)

Application

- Digital appliance
- Office automation equipment
- Industrial equipment
- Communication equipment, etc

Typical Application



CONTENTS

1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified T_A = 25 °C

Characteristic	Symbol	Conditions	Pin	Rating	Units
VSEN Pin Voltage	V_{SEN}		1 − 4	− 0.3 to V_{REG}	V
VCC Pin Voltage	V_{CC}		2 − 4	− 0.3 to 35	V
FB Pin Voltage	V_{FB}		3 − 4	− 0.3 to 10	V
CSS Pin Voltage	V_{CSS}		5 − 4	− 0.3 to 12	V
OC Pin Voltage	V_{OC}		6 − 4	− 6 to 6	V
RC Pin Voltage	V_{RC}		7 − 4	− 6 to 6	V
REG Pin Source Current	I_{REG}		8 − 4	− 20.0	mA
RV Pin Current	I_{RV}	DC	9 − 4	− 2 to 2	mA
		Pulse 40 ns	9 − 4	− 100 to 100	mA
VGL Pin Voltage	V_{GL}		11 − 4	− 0.3 to V_{REG} + 0.3	V
Voltage between VB Pin and VS Pin	V_B−V_S		14 − 15	− 0.3 to 15.0	V
VS Pin Voltage	V_S		15 − 4	− 1 to 600	V
VGH Pin Voltage	V_{GH}		16 − 4	V_S − 0.3 to V_B + 0.3	V
Operating Ambient Temperature	T_{OP}		−	− 20 to 85	°C
Storage Temperature	T_{stg}		−	− 40 to 125	°C
Junction Temperature	T_j		−	150	°C

*The pin 14, pin 15 and pin 16, are guaranteed 1000 V of ESD withstand voltage (Human body model).
Other pins are guaranteed 2000V of ESD withstand voltage.

2. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC
- Unless otherwise specified, T_A = 25 °C, V_{CC} = 15 V

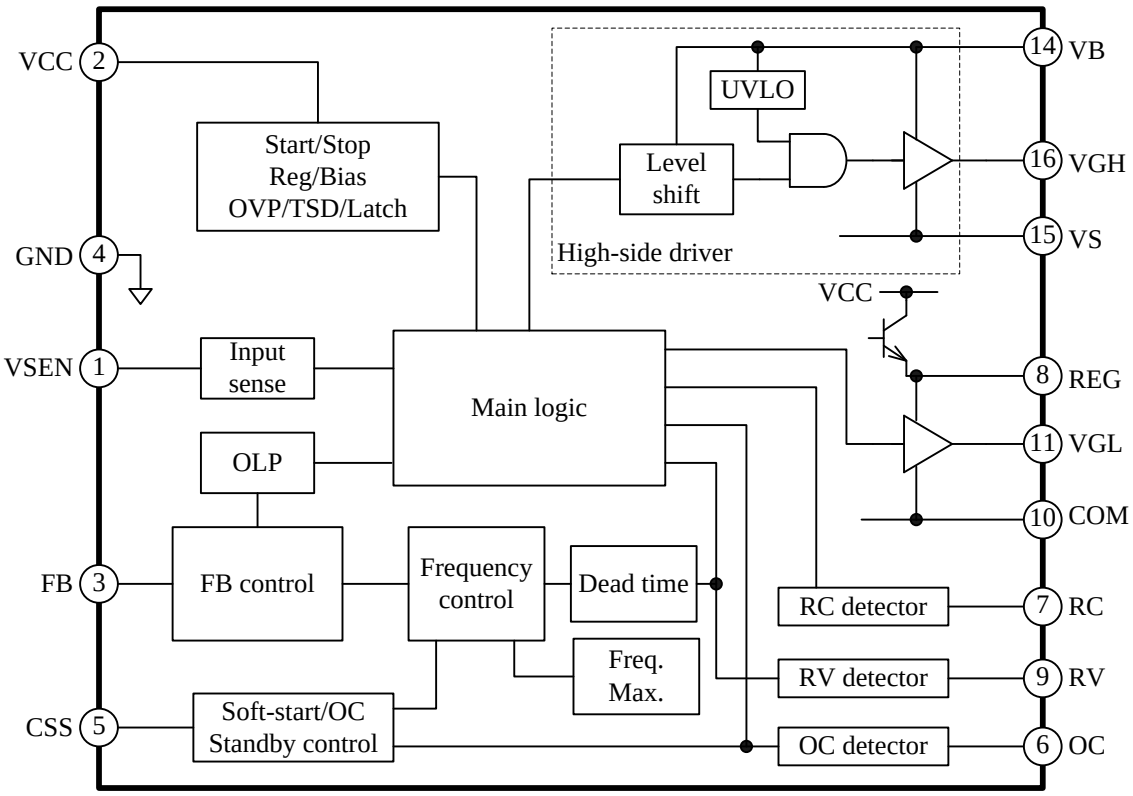
Characteristic	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
Startup Circuit and Circuit Current							
Operation Start Voltage	$V_{CC(ON)}$		2 − 4	10.2	11.8	13.0	V
Operation Stop Voltage [1]	$V_{CC(OFF)}$		2 − 4	8.8	9.8	10.9	V
Circuit Current in Operation	$I_{CC(ON)}$		2 − 4	−	−	20.0	mA
Circuit Current in Non-operation	$I_{CC(OFF)}$	V_{CC} = 9 V	2 − 4	−	−	1.2	mA
Circuit Current in Latched Shutdown Operation	$I_{CC(L)}$	V_{CC} = 11 V	2 − 4	−	−	1.2	mA
Soft Start							
CSS Pin Charge Current	$I_{CSS(C)}$		5 − 4	− 0.21	− 0.18	− 0.15	mA
CSS Pin Reset Current	$I_{CSS(R)}$	V_{CC} = 9 V	5 − 4	1.0	1.8	2.4	mA
ON / OFF							
CSS Pin Threshold Voltage (2)	$V_{CSS(2)}$	V_{SEN} = 3 V V_{OC} = 0 V	5 − 4	0.50	0.59	0.68	V
Oscillator							
Minimum Oscillation Frequency	$f_{(MIN)}$	V_{CC} = 9 V	11 − 10 16 − 15	26.2	28.3	31.2	kHz
Maximum Oscillation Frequency	$f_{(MAX)}$	I_{FB} = − 2 mA	11 − 10 16 − 15	265	300	335	kHz
Maximum Dead Time	$t_{d(MAX)}$	V_{SEN} = 3 V	11 − 10 16 − 15	1.90	2.45	3.00	µs
Minimum Dead Time	$t_{d(MIN)}$	I_{FB} = − 2 mA	11 − 10 16 − 15	0.25	0.50	0.75	µs
Standby Operation							
Burst Oscillation frequency	f_{CSS}	I_{FB} = − 3.5 mA	5 − 4	70	105	130	Hz
Feedback control							
FB Pin Source Current at Burst Mode Start	$I_{CONT(1)}$		3 − 4	− 2.9	− 2.5	− 2.1	mA
FB Pin Source Current at Oscillation stop	$I_{CONT(2)}$		3 − 4	− 3.7	− 3.1	− 2.5	mA
Supply of Driver Circuit							
REF Pin Output Voltage	V_{REG}	I_{FB} = − 2 mA	8 − 4	9.9	10.5	11.1	V
High-side Drive Circuit							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		14 − 15	6.3	7.3	8.3	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		14 − 15	5.5	6.4	7.2	V
Drive Circuit							
Source Current 1 of VGL Pin and VGH Pin	$IGL_{SOURCE1}$ $IGH_{SOURCE1}$	V_{REG} = 10.5V V_B = 10.5 V V_{GL} = 0 V V_{GH} = 0 V	11 − 10 16 − 15	−	− 515	−	mA

[1] $V_{CC(OFF)} < V_{CC(ON)}$

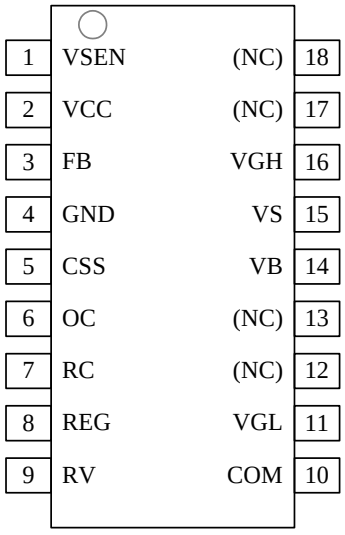
Characteristic	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
Sink Current 1 of VGL Pin and VGH Pin	IGL_{SINK1} IGH_{SINK1}	V_{REG} = 10.5V V_B = 10.5 V V_{GL} = 10.5 V V_{GH} = 10.5 V	11 − 10 16 − 15	–	685	–	mA
Source Current 2 of VGL Pin and VGH Pin	$IGL_{SOURCE2}$ $IGH_{SOURCE2}$	V_{REG} = 12 V V_B = 12 V V_{GL} = 10.5 V V_{GH} = 10.5 V	11 − 10 16 − 15	– 120	– 85	– 50	mA
Sink Current 2 of VGL Pin and VGH Pin	IGL_{SINK2} IGH_{SINK2}	V_{REG} = 12 V V_B = 12 V V_{GL} = 1.5 V V_{GH} = 1.5 V	11 − 10 16 − 15	70	113	160	mA
Brown-in / Brown-out Function							
VSEN Pin Threshold Voltage (ON)	$V_{SEN(ON)}$		1 − 4	1.32	1.42	1.52	V
VSEN Pin Threshold Voltage (OFF)	$V_{SEN(OFF)}$		1 − 4	1.08	1.16	1.24	V
Detection of Voltage Resonant							
Voltage Resonant Detection Voltage (1)	$V_{RV(1)}$		9 − 4	3.8	4.9	5.4	V
Voltage Resonant Detection Voltage (2)	$V_{RV(2)}$		9 − 4	1.20	1.77	2.30	V
Detection of Current Resonant and OCP							
Capacitive Mode Operation Detection Voltage	V_{RC}		7 − 4	0.055	0.155	0.255	V
				– 0.255	– 0.155	– 0.055	V
RC Pin Threshold Voltage (High Speed)	$V_{RC(S)}$		7 − 4	2.15	2.35	2.55	V
				– 2.55	– 2.35	– 2.15	V
OC Pin Threshold Voltage (Low)	$V_{OC(L)}$	V_{CSS} = 3 V	6 − 4	1.42	1.52	1.62	V
OC Pin Threshold Voltage (High)	$V_{OC(H)}$	V_{CSS} = 3 V	6 − 4	1.69	1.83	1.97	V
OC Pin Threshold Voltage (High Speed)	$V_{OC(S)}$	V_{CSS} = 5 V	6 − 4	2.15	2.35	2.55	V
C_{SS} Pin Sink Current (Low)	$I_{CSS(L)}$	V_{CSS} = 3 V V_{OC} = 1.65 V	5 − 4	1.0	1.8	2.4	mA
C_{SS} Pin Sink Current (High)	$I_{CSS(H)}$	V_{CSS} = 3 V V_{OC} = 2 V	5 − 4	12.0	20.0	28.0	mA
C_{SS} Pin Sink Current (High Speed)	$I_{CSS(S)}$	V_{RC} = 2.8 V	5 − 4	11.0	18.3	25.0	mA
OLP Latch and External Latch							
FB Pin Source Current	I_{FB}	V_{FB} = 5 V	3 − 4	− 30.5	− 25.5	− 20.5	µA
FB Pin Threshold Voltage	V_{FB}		3 − 4	6.55	7.05	7.55	V
CSS Pin Threshold Voltage (1)	$V_{CSS(1)}$		5 − 4	7.0	7.8	8.6	V
Latched Circuit Release VCC Voltage [(2)]	$V_{CC(LA\_OFF)}$		2 − 4	6.7	8.2	9.5	V
OVP and TSD							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$	V_{SEN} = 3 V	2 − 4	28.0	31.0	34.0	V
Thermal Shutdown Temperature	$T_{j\,(TSD)}$		–	150	–	–	°C
Thermal Resistance							
Thermal Resistance Junction to Ambient	θ_{j-A}		–	–	–	95	°C/W

(2) $V_{CC(LA\_OFF)} < V_{CC(OFF)}$

3. Block Diagram

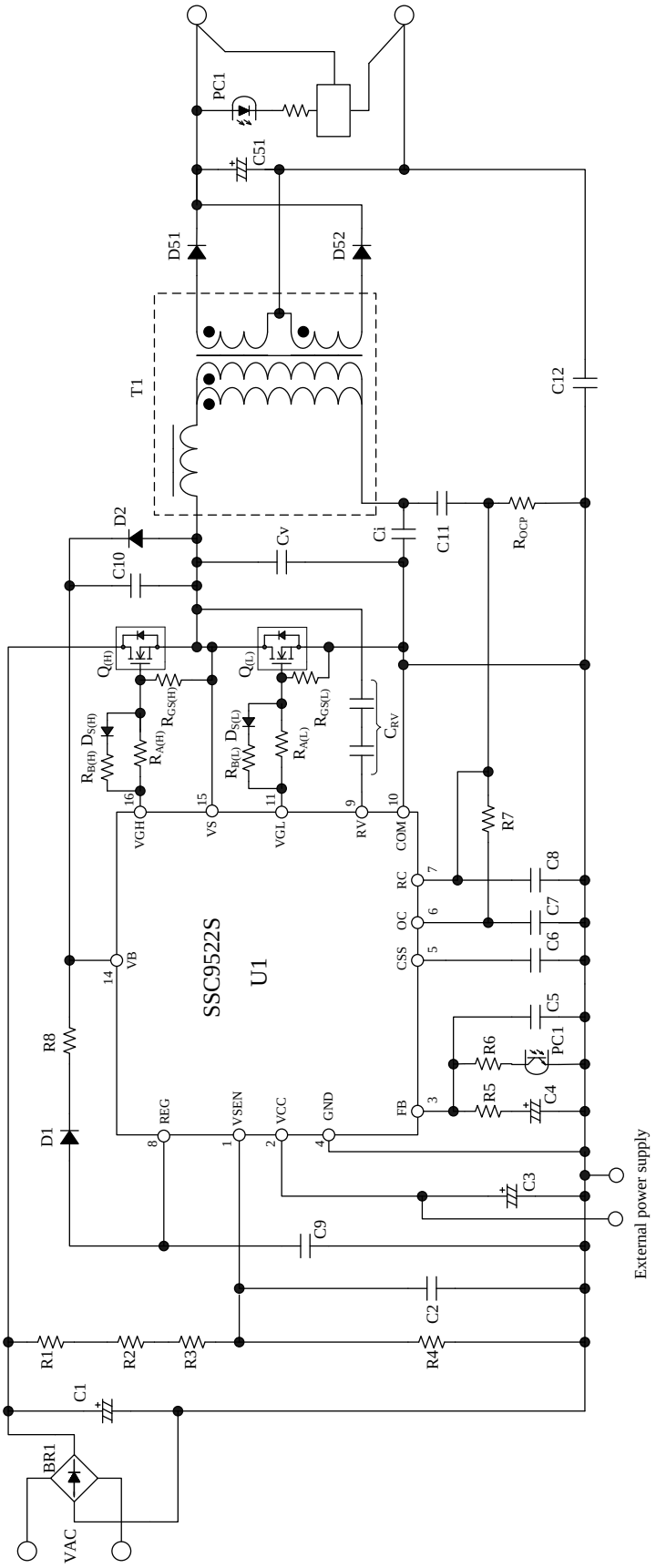


4. Pin Configuration Definitions



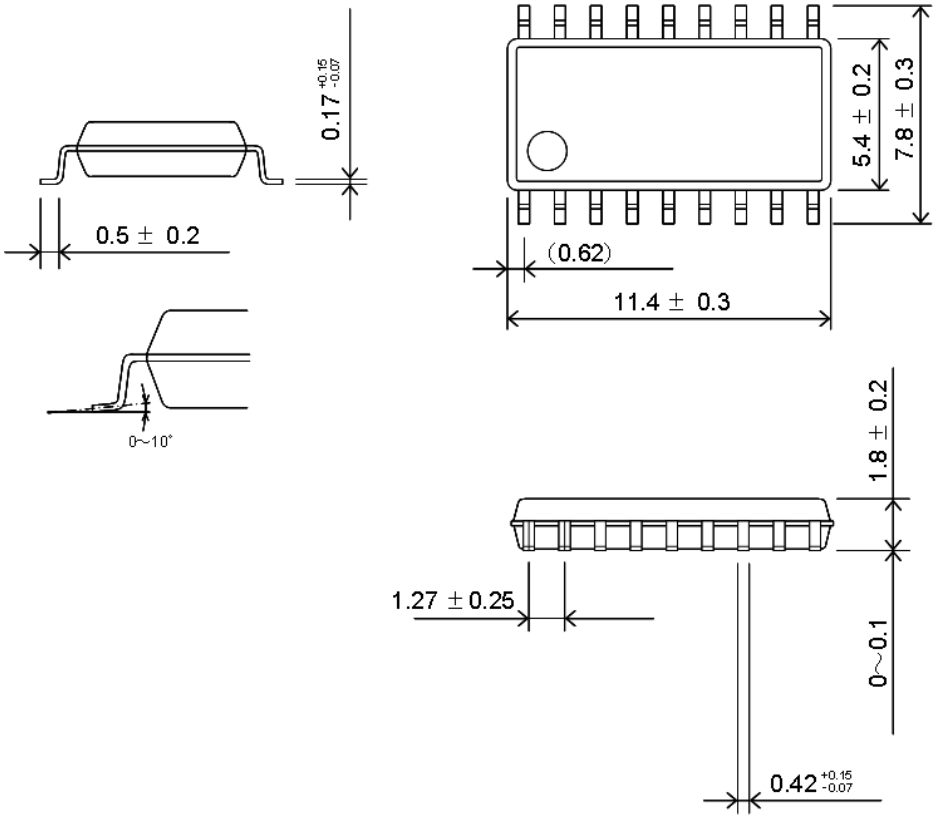
Number	Name	Function
1	VSEN	AC input voltage detection signal input
2	VCC	Power supply voltage input for the IC, and Overvoltage Protection (OVP) signal input
3	FB	Feedback signal input for constant voltage control signal, and Overload Protection (OLP) signal input
4	GND	Ground for control part
5	CSS	Soft start capacitor connection
6	OC	Overcurrent Protection (OCP) signal input
7	RC	Resonant current detection signal input
8	REG	Power supply output for high-side gate drive
9	RV	Resonant voltage detection signal input
10	COM	Ground for power part
11	VGL	Low-side gate drive output
12, 13	(NC)	−
14	VB	Power supply input for high-side gate drive
15	VS	Floating ground for high-side driver
16	VGH	High-side gate drive output
17, 18	(NC)	−

5. Typical Application



6. External Dimensions

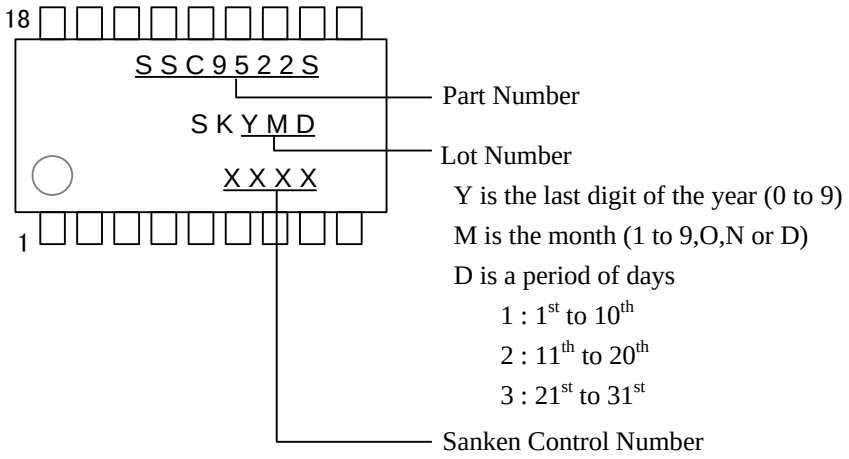
● SOP18



NOTES:

● Dimension is in millimeters
● Pb-free. Device composition compliant with the RoHS directive

7. Marking Diagram



8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

$Q_{(H)}$ and $Q_{(L)}$ indicate a high-side power MOSFET and a low-side power MOSFET respectively. Ci, and C_V indicate a current resonant capacitor and a voltage resonant capacitor respectively.

8.1 Resonant Circuit Operation

Figure 8-1 shows a basic RLC series resonant circuit.

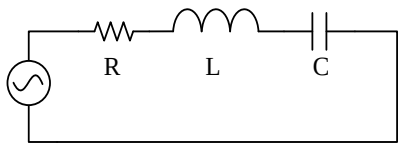


Figure 8-1 RLC series resonant circuit

The impedance of the circuit, Ż, is as the following Equation.

$$\dot{Z} = R + j\left(\omega L - \frac{1}{\omega C}\right) \quad (1)$$

where, ω is angular frequency and ω = 2πf.

$$\dot{Z} = R + j\left(2\pi fL - \frac{1}{2\pi fC}\right) \quad (2)$$

When the frequency, f, changes, the impedance of resonant circuit will change as shown in Figure 8-2

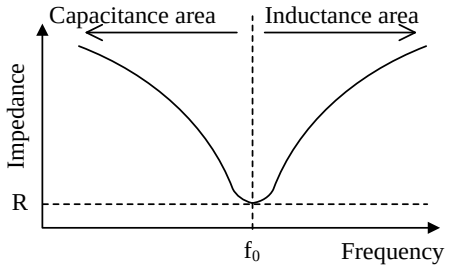


Figure 8-2 Impedance of resonant circuit

In Equation (2), Ż becomes minimum value (= R) at 2πfL = 1/2πfC, and then ω is calculated by Equation (3) .

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \quad (3)$$

The frequency in which Ż becomes minimum value is the resonant frequency, f_0. The higher frequency area than f_0 is the inductance area, and the lower frequency area than f_0 is the capacitance area.

From Equation (3), f_0 is as follows;

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (4)$$

Figure 8-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching device $Q_{(H)}$ and $Q_{(L)}$ are connected in series with V_{IN}. The series resonant circuit and the voltage resonant capacitor C_V are connected in parallel with $Q_{(L)}$. The series resonant circuit is comprised of a resonant inductor L_R, a primary winding P of a transformer T1 and a current resonant capacitor C_i.

In the resonant transformer T1, the coupling between primary winding and secondary winding is designed to be poor so that the leakage inductance increases. By using it as LR, the series resonant circuit can be down sized. The dotted mark in T1 shows the winding polarity, the secondary windings S1 and S2 are connected so that the polarities are set to the same position shown in Figure 8-3, and the winding numbers of each other are equal.

From Equation (1), the impedance of current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, f_0, is calculated by Equation (6).

$$\dot{Z} = R + j\left\{\omega(L_R + L_P) - \frac{1}{\omega Ci}\right\} \quad (5)$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times Ci}} \quad (6)$$

where,
R: the equivalent resistance of load
L_R: the inductance of the resonant inductor
L_P: the inductance of the primary winding P
Ci: the capacitance of current resonant capacitor

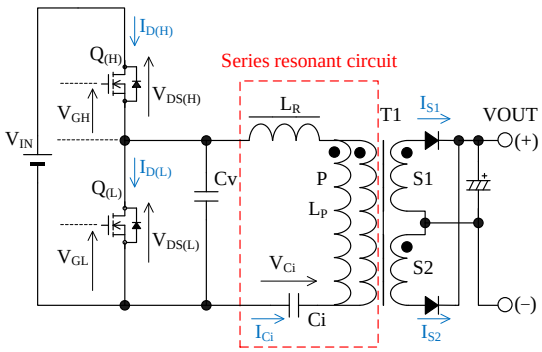


Figure 8-3 Current resonant power supply circuit

In the current resonant power supply, $Q_{(H)}$ and $Q_{(L)}$ are alternatively turned on and off. The on time and off time of them are equal. There is a dead time between $Q_{(H)}$ on period and $Q_{(L)}$ on period. During the dead time, both $Q_{(H)}$ and $Q_{(L)}$ are in off status.

The current resonant power supply is controlled by the frequency control. When the output voltage decreases, the IC makes the switching frequency low so that the output power is increased and the output voltage is kept constant. This control must operate in the inductance area ($f_{SW} > f_0$). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operation is ZCS (Zero Current Switching) and the turn-off operation is ZVS (Zero Voltage Switching). Thus, the switching loss of $Q_{(H)}$ and $Q_{(L)}$ is nearly zero,

In the capacitance area ($f_{SW} < f_0$), the current resonant power supply operates as follows. When the output voltage decreases, the switching frequency is decreased, and then the output power is more decreased. Thus, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, the operation with hard switching occurs in $Q_{(H)}$ and $Q_{(L)}$. Thus, the power loss increases.

This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (refer to Section 8.7 about details of it).

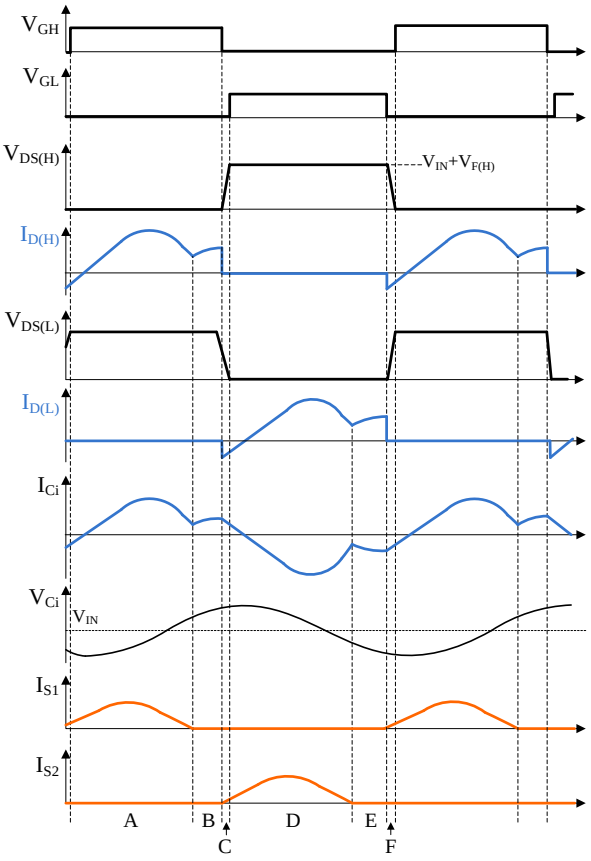


Figure 8-4 The basic operation waveforms of current resonant power supply

Figure 8-4 shows the basic operation waveform of current resonant power supply (see Figure 8-3 about the symbol in Figure 8-4). The current resonant waveforms in normal operation are divided a period A to a period F. The current resonant power supply operates in the each period as follows.

In following description,
$I_{D(H)}$ is the current of $Q_{(H)}$,
$I_{D(L)}$ is the current of $Q_{(L)}$,
$V_{F(H)}$ is the forwerd voltage of $Q_{(H)}$,
$V_{F(L)}$ is the forwerd voltage of $Q_{(L)}$,
I_L is the current of L_R,
V_{IN} is an input voltage,
V_{Ci} is Ci voltage, and
V_{CV} is C_V voltage.

1) Period A

When $Q_{(H)}$ is ON, energy is stored into the series resonant circuit by $I_{D(H)}$ flowing through the resonant circuit and the transformer as shown in Figure 8-5. At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the secondary rectifier ON, the energy to the secondary circuit is stopped.

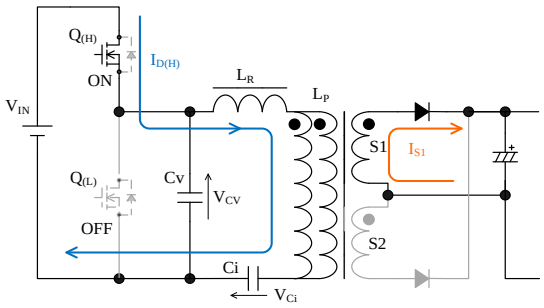


Figure 8-5 Operation in period A

2) Period B

After the secondary side current becomes zero, the resonant current flows to the primary side only as shown in Figure 8-6 and Ci is charged by it.

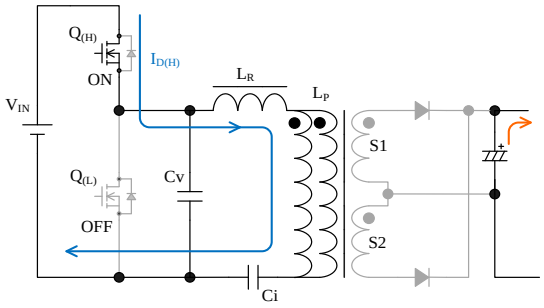


Figure 8-6 Operation in period B

3) Period C

Pireod C is the dead-time. Both $Q_{(H)}$ and $Q_{(L)}$ are in off-state.

When $Q_{(H)}$ turns off, I_L is flowed by the energy stored in the series resonant circuit as shown in Figure 8-7, and C_V is discharged. When V_{CV} decreases to $V_{F(L)}$, $-I_{D(L)}$ flows through the body diode of $Q_{(L)}$ and V_{CV} is clamped to $V_{F(L)}$.

After that, $Q_{(L)}$ turns on. Since $V_{DS(L)}$ is nearly zero at the point, $Q_{(L)}$ operates in ZVS and ZCS. Thus, switching loss is nearly zero.

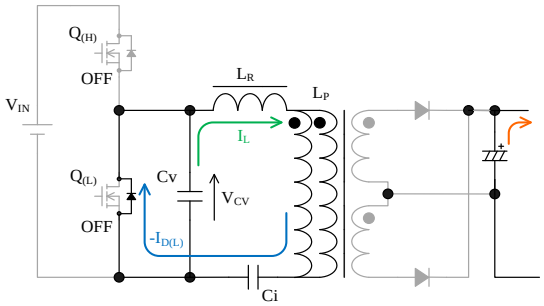


Figure 8-7 Operation in period C

4) Period D

When $Q_{(L)}$ turns on, $I_{D(L)}$ flows as shown in Figure 8-8 and the primary winding voltage of the transformer adds V_{Ci}. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the secondary rectifier ON, the energy to the secondary circuit is stopped.

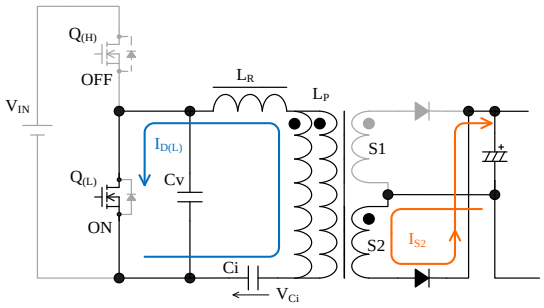


Figure 8-8 Operation in period D

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only as shown in Figure 8-9 and Ci is charged by it.

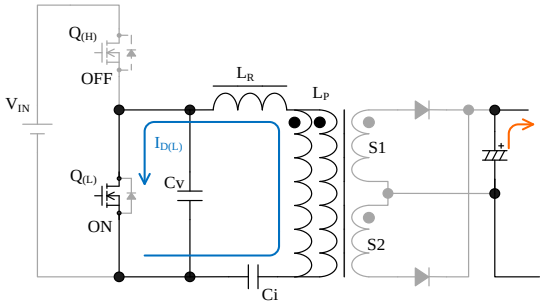


Figure 8-9 Operation in period E

6) Period F

This pireod is the dead-time. Both $Q_{(H)}$ and $Q_{(L)}$ are in off-state.

When $Q_{(L)}$ turns off, $-I_L$ is flowed by the energy stored in the series resonant circuit as shown in Figure 8-10. C_V is discharged. When V_{CV} decreases to $V_{IN} + V_{F(H)}$, $-I_{D(H)}$ flows through body diode of $Q_{(H)}$ and V_{CV} is clamped to $V_{IN} + V_{F(H)}$.

After that, $Q_{(H)}$ turns on. Since $V_{DS(H)}$ is nearly zero at the point, $Q_{(H)}$ operates in ZVS and ZCS. Thus, the switching loss is nearly zero.

7) After the Period F

Then, $I_{D(H)}$ flows and the operation returns to the period A.

The above operation is repeated, the energy is transferred to the secondary side from the resonant circuit.

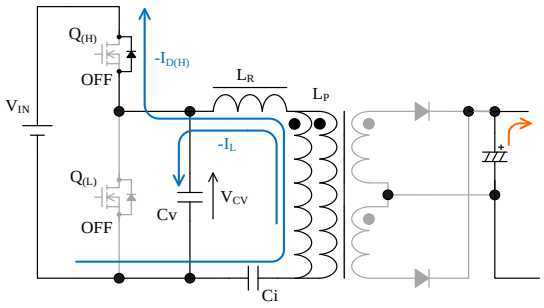


Figure 8-10 Operation in period F

8.2 Startup Operation

Figure 8-11 shows the VCC pin peripheral circuit with Brown-in and Brown-out Function, Figure 8-12 shows the VCC pin peripheral circuit without Brown-in and Brown-out Function (see Section 8.8 about Brown-in and Brown-out Function).

The VCC pin is a power supply input pin for a control circuit and is supplied from an external power supply. In Figure 8-13, when the VCC pin increases to the Operation Start Voltage, $V_{CC(ON)}$ = 11.8 V, the control circuit starts operation. When the VCC pin decreases to the Operation Stop Voltage, $V_{CC(OFF)}$ = 9.8 V, the control circuit is stopped by Undervoltage Lockout (UVLO) circuit, and returns to the state before startup.

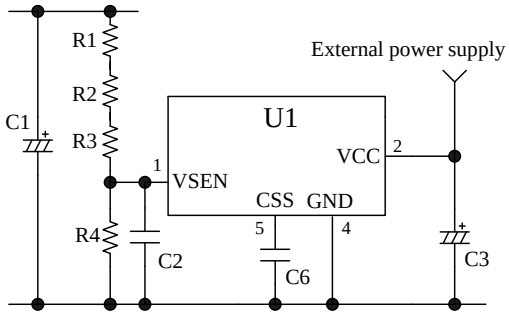


Figure 8-11 VCC pin peripheral circuit with Brown-in and Brown-out Function

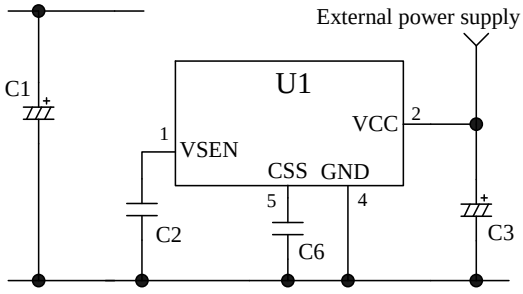


Figure 8-12 VCC pin peripheral circuit without Brown-in and Brown-out Function

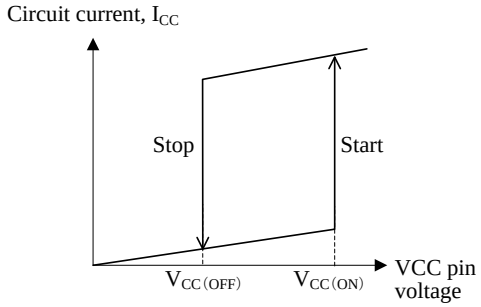


Figure 8-13 Relationship between VCC pin voltage and I_{CC}

In startup operation, the IC starts a switching operation when the IC satisfies all conditions below as shown in Figure 8-14.

VCC pin voltage ≥ $V_{CC(ON)}$ = 11.8 V
VSEN pin voltage ≥ $V_{SEN(ON)}$ = 1.42 V
CSS pin voltage ≥ $V_{CSS(2)}$ = 0.59 V

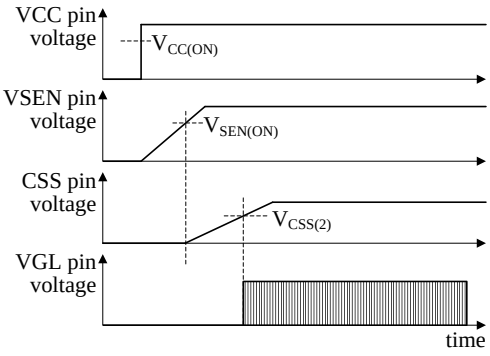


Figure 8-14 Startup waveforms

When the IC is supplied by the external power supply, t_{ST} is calculated by Equation (7).

t_{ST} is the total startup time until the IC starts a switching operation after VCC pin voltage reaches $V_{CC(ON)}$.

- With Brown-in and Brown-out Function

$$t_{ST} = t_{ST1} = \frac{C6 \times V_{CSS(2)}}{|I_{CSS(C)}|} \quad (7)$$

where, $V_{CSS(2)}$ is 0.59 V and $I_{CSS(C)}$ is − 0.18 mA.
If C6 is 1 µF, t_{ST} becomes about 3.3 ms.

- Without Brown-in and Brown-out Function
  In this case, t_{ST} is a value of adding t_{ST1} calculated by Equation (7) to t_{ST2} calculated by Equation (8). The period that until the VSEN pin voltage reaches to $V_{SEN(ON)}$ = 1.42 V after the VCC pin voltage reaches $V_{CC(ON)}$ is defined as t_{ST2}.

$$t_{ST2} = C2 \times 380k \quad (8)$$

If C6 is 1 µF and C2 is 0.01 µF, t_{ST1} becomes 3.3ms and t_{ST2} becomes about 3.8 ms.
Thus, t_{ST} is t_{ST1} + t_{ST2} = 7.1 ms.

8.3 Soft Start Function

Figure 8-15 shows the waveform of the CSS pin in the startup operation.

The IC has Soft Start Function to reduce stress of peripheral component and prevent the capacitive mode operation. During the soft start operation, C6 connected to the CSS pin is charged by the CSS Pin Charge Current, $I_{CSS(C)} = -0.18$ mA. The oscillation frequency is varied by the CSS pin voltage. The oscillation frequency becomes gradually low with the increasing CSS pin voltage. At same time, output power increases. When the output voltage increases, the IC is operated with an oscillation frequency controlled by feedback.

If the overcurrent protection activates as soon as the IC starts and the CSS pin voltage is under the CSS Pin Threshold Voltage (2), $V_{CSS(2)} = 0.59$ V, the IC stops switching operation. Since the period of the high peak current of primary windings becomes short, the stress of peripheral components is reduced.

When the IC becomes any of the following conditions, C6 is discharged by the CSS Pin Reset Current, $I_{CSS(R)} = 1.8$ mA.

- VCC pin voltage ≤ $V_{CC(OFF)}$= 9.8 V
- VSEN pin voltage ≤ $V_{SEN(OFF)}$= 1.16 V
- When the latched shutdown is operated by External Latched Shutdown Function or some protection (OVP, OLP and TSD)

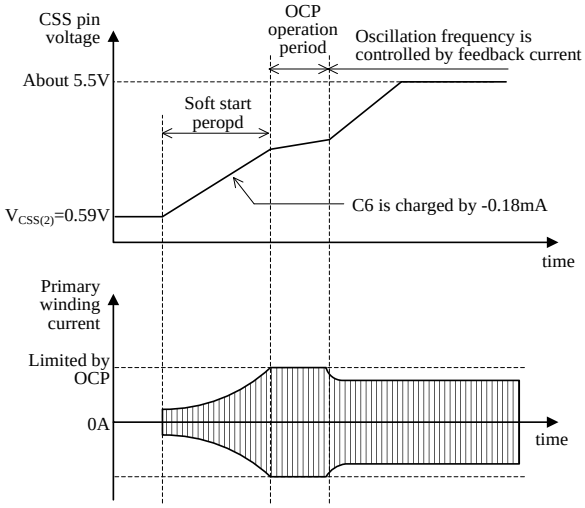


Figure 8-15 Soft start operation waveforms

8.4 High-side Driver

Figure 8-16 shows a bootstrap circuit. The bootstrap circuit is for driving to $Q_{(H)}$ and is made by D1, R8 and C10 between the REG pin and the VS pin.

When $Q_{(H)}$ is OFF state and $Q_{(L)}$ is ON state, the VS pin voltage becomes about ground level and C10 is charged from the REG pin.

When the voltage of between the VB pin and the VS pin, V_{B-S}, increases to $V_{BUV(ON)}$ = 7.3 V or more, an internal high-side drive circuit starts operation. When V_{B-S} decreases to $V_{BUV(OFF)}$ = 6.4 V or less, its drive circuit stops operation.

In case the both ends of C10 are short, the IC is protected by $V_{BUV(OFF)}$.

D1 should use a fast recovery diode that is short recovery time and low leakage current. AG01A (Vrm = 600 V, Sanken product) is recommended when the maximum input voltage is 265V AC.

C10 should use film or ceramic capacitor that is the low ESR and the low leakage current.

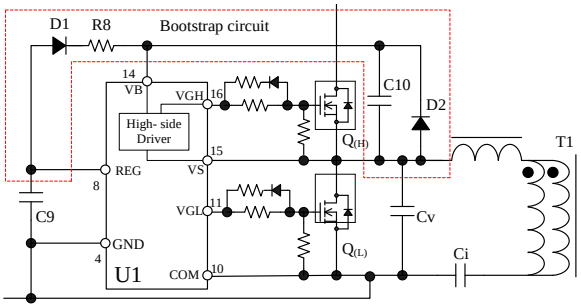


Figure 8-16 Bootstrap circuit

8.5 Constant Output Voltage Control

Figure 8-17 shows the FB pin peripheral circuit. The FB pin is sunk the feedback current by the photo-coupler, PC1, connected to FB pin. As a result, since the oscillation frequency is controlled by the FB pin, the output voltage is controlled to constant voltage (in inductance area).

When the FB pin current decreases to the FB Pin Source current at Burst Mode Start, $I_{CONT(1)} = -2.5$ mA or less at light load, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage. The photo-coupler of the secondary side should be considered about the secular change of CTR and its current ability for control should be set $I_{CONT(2)} = -3.7$ mA (min.) or less. The recommend value of R6 is 560 Ω.

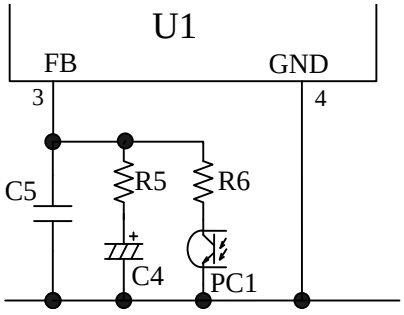


Figure 8-17 FB pin peripheral circuit

8.6 Automatic Dead Time Adjustment Function

As shown in Figure 8-18, if the dead time is shorter than the voltage resonant period, the power MOSFET is turned on and off during the voltage resonant operation. In this case, the power MOSFET turned on and off in hard switching operation, and the switching loss increases. The Automatic Dead Time Adjustment Function is the function that the ZVS (Zero Voltage Switching) operation of $Q_{(H)}$ and $Q_{(L)}$ is controlled automatically by the voltage resonant period detection of IC. The voltage resonant period is varied by the power supply specifications (input voltage and output power, etc.). However, the power supply with this function is unnecessary to adjust the dead time for each power supply specification.

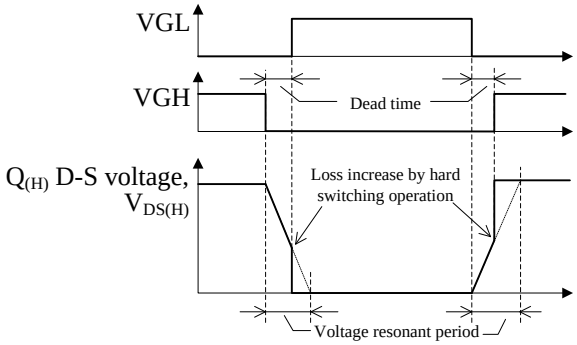


Figure 8-18 ZVS failure operation waveform

Figure 8-19 shows the RV pin peripheral circuit and the internal dead time detection circuit. The external components for this function is only high-voltage ceramic capacitor, C_{RV}, connected between the VS pin and the RV pin. The value of C_{RV} is about 5 pF.

The RV pin voltage is the divided voltage by resistors between the internal reference voltage, Reg, and the GND pin. When the drain to source voltage of $Q_{(L)}$, $V_{DS(L)}$, increases, the differential current, Δi, flows through C_{RV} (refer to Figure 8-20). The dv/dt when $V_{DS(L)}$ increases is detected by Δi input to the RV pin. Since SW1 and SW2 turn on necessary period, the IC circuit current reduction and the differential circuit response improvement are achieved.

Δi is calculated by Equation (9). The C_{RV} should be adjusted in all condition including transient state so that Δi satisfies Equation (10).

If Δi is large, the capacitance of C_{RV} is adjusted small. When dt is under 40 ns, Δi is ± 100 mA.

$$\Delta i = C_{RV} \times \left(\frac{dv}{dt} \right) \tag{9}$$

$$|\Delta i| \leq \frac{100\,(mA) \times 40\,(ns)}{dt} \tag{10}$$

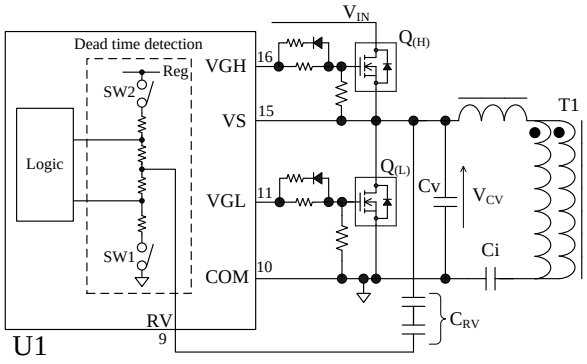


Figure 8-19 RV pin peripheral circuit and dead time detection circuit

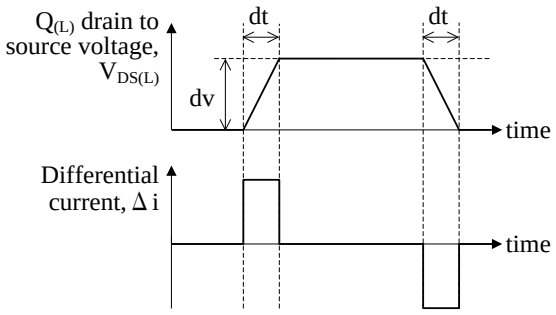


Figure 8-20 Differential current waveforms

Figure 8-21 shows the operating waveform of the Automatic Dead Time Adjustment Function. When $Q_{(L)}$ and $Q_{(H)}$ turn off, this function operates as follows:

- **$Q_{(L)}$ turns off**

  After $Q_{(L)}$ turns off, SW2 is turned on while SW1 is kept on state. The resonant current flows through C_V, Ci and T1 (refer to Figure 8-19) and the C_V voltage, V_{CV}, increases from 0 V. When V_{CV} becomes Equation (11), the resonant current flows through the body diode of $Q_{(H)}$ and V_{CV} is clamped $V_{IN} + V_{F(H)}$. The period that until V_{CV} is clamped after V_{CV} starts to increase is defined as the voltage resonant period.

$$V_{CV} \geq V_{IN} + V_{F(H)} \tag{11}$$

  Where, V_{IN} is input voltage and $V_{F(H)}$ is the forward voltage of the body diode of $Q_{(H)}$

  In this time, the differential current, Δi, flows through C_{RV}. The RV pin voltage increases from the voltage divided by internal resistors and becomes internal clamped voltage. When the voltage resonant period finishes and flowing Δi finishes, the RV pin voltage starts to decrease. When the RV pin voltage becomes the Voltage Resonant Detection Voltage (1), $V_{RV(1)}$ = 4.9 V, $Q_{(H)}$ is turned on and SW1 is turned off.

The period that until SW1 is turned off after SW2 is turned on is defined as the automatically adjusted dead time.

- **$Q_{(H)}$ turns off**

After $Q_{(H)}$ turns off, SW1 is turned on while SW2 is kept on state. The resonant current flows through C_V, Ci and T1 (refer to Figure 8-19) and the C_V voltage, V_{CV}, decrease from the input voltage, V_{IN}.
When V_{CV} becomes Equation (12), the resonant current flows through the body diode of $Q_{(L)}$ and V_{CV} is clamped $-V_{F(L)}$. The period that until V_{CV} is clamped after V_{CV} starts to decrease is defined as the voltage resonant period.

$$V_{CV} \leq -V_{F(L)} \quad (12)$$

Where, $V_{F(L)}$ is the forward voltage of the body diode of $Q_{(L)}$.

In this time, the differential current, Δi, flows through C_{RV}. The RV pin voltage decreases from the voltage divided by internal resistors and becomes about the ground voltage. When the voltage resonant period finishes and flowing Δi finishes, the RV pin voltage starts to increase. When the RV pin voltage becomes the Voltage Resonant Detection Voltage (2), $V_{RV(2)}$ = 1.77 V, $Q_{(L)}$ is turned on and SW2 is turned off. The period until SW2 is turned off after SW1 is turned on is defined as the automatically adjusted dead time.

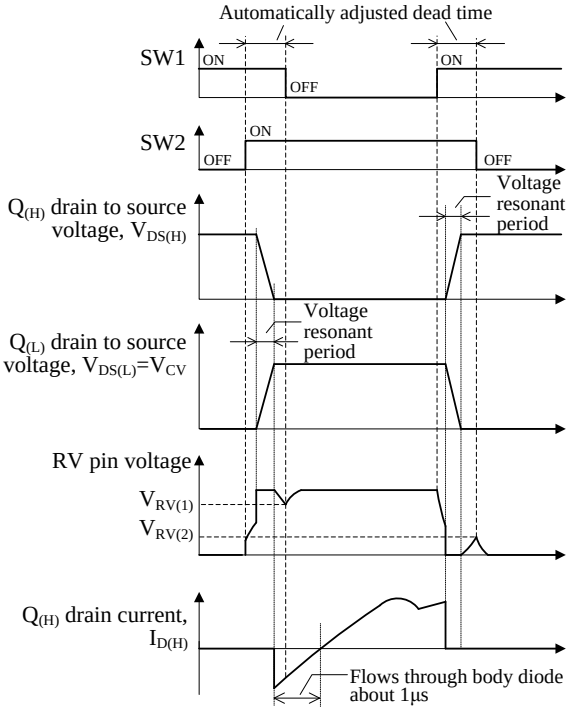


Figure 8-21 Automatic Dead Time Adjustment Function operating waveforms

When the RV pin is inputted the signal of $V_{RV(1)}$ and $V_{RV(2)}$, the IC is controlled ZVS (Zero Voltage Switching) always by the Automatic Dead Time Adjustment Function.

In minimum output power at maximum input voltage and maximum output power at minimum input voltage, the ZCS (Zero Current Switching) operation of IC (the drain current flows through the body diode is about 1 µs as shown in Figure 8-21), should be checked based on actual operation in the application.

8.7 Capacitive Mode Operation Detection Function

The resonant power supply is operated in the inductance area shown in Figure 8-22. In the capacitance area, the power supply becomes the capacitive mode operation (refer to Section 8.1). In order to prevent the operation, the minimum oscillation frequency is needed to be set higher than f_0 on each power supply specification.

However, the IC has the capacitive mode operation Detection Function kept the frequency higher than f_0. Thus, the minimum oscillation frequency setting is unnecessary and the power supply design is easier. In addition, the ability of transformer is improved because the operating frequency can operate close to the resonant frequency, f_0.

The RC pin detects the resonant current, and the capacitive mode operation is prevented. The Capacitive Mode Operation Detection Function operations as follows:

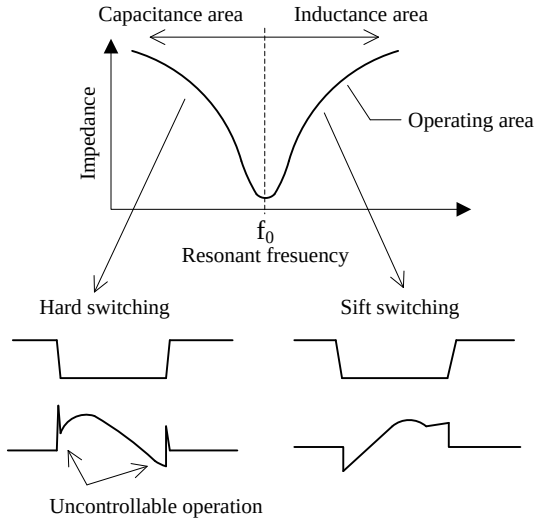


Figure 8-22 Operating area of resonant power supply

- **Period in which the $Q_{(H)}$ is ON**

Figure 8-23 shows the RC pin waveform in the inductance area, and Figure 8-24 shows the RC pin

waveform in the capacitance area.
In the inductance area, the RC pin voltage doesn't cross V_{RC} = + 0.155 V in the downward direction during the on period of $Q_{(H)}$ as shown in Figure 8-23.
On the contrary, in the capacitance area, the RC pin voltage crosses V_{RC} = + 0.155 V in the downward direction. At this point, the capacitive mode operation is detected. Thus, $Q_{(H)}$ is turned off, and $Q_{(L)}$ is turned on, as shown in Figure 8-24.

- **Period in which the $Q_{(L)}$ is on**
  Contrary to the above of $Q_{(H)}$, in the capacitance area, the RC pin voltage crosses V_{RC} = – 0.155 V in the upward directiont during the on period of Q(L). At this point, the capacitive mode operation is detected. Thus, $Q_{(L)}$ is turned off and $Q_{(H)}$ is turned on.

As above, since the capacitive mode operation is detected by pulse-by-pulse and the operating frequency is synchronized with the frequency of the capacitive mode operation, and the capacitive mode operation is prevented.

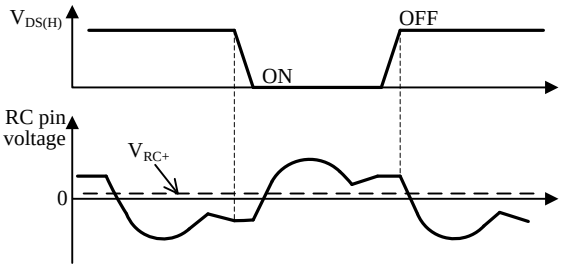


Figure 8-23 RC pin voltage in inductance area

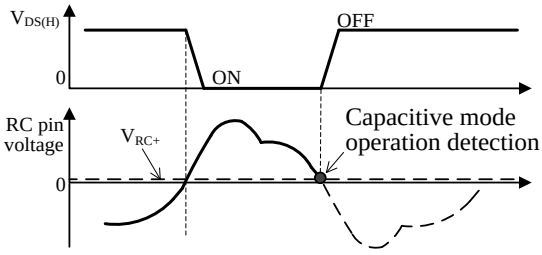


Figure 8-24 RC pin voltage in capacitance area

In order to quicken detection speed of the capacitive mode operation, the RC pin is connected before the filter circuit of the OC pin as shown in Figure 8-25. C8 is for preventing malfunction caused by noise. The value of C8 is about 100 pF.

The value of R_{OCP} and C11 should be adjusted so that the RC pin voltage reaches to V_{RC} = ± 0.155 V in the condition that the IC operation becomes the capacitive mode operation easily (startup operation, input voltage off, output short and dynamically output power changing). In addition, the RC pin voltage should be within the absolute maximum voltage ± 6 V.

Since R_{OCP} and C11 are used by Overcurrent Protection (OCP), these values should take account of OCP. If the RC pin voltage becomes more than the RC pin threshold voltage (High speed), $V_{RC(S)}$ = 2.35 V, or less than $V_{RC(S)}$ = – 2.35 V, OCP becomes active (refer to Section 8.9).

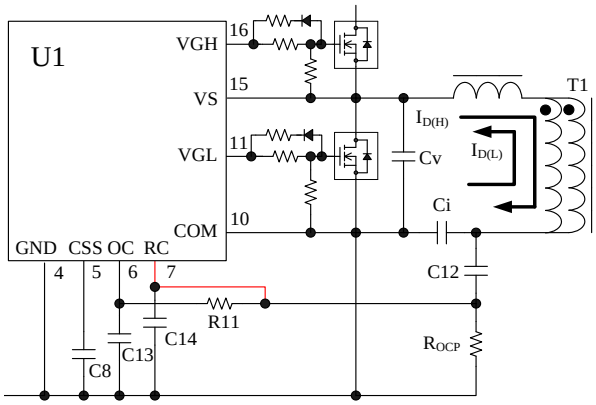


Figure 8-25 RC pin peripheral circuit

8.8 Brown-in and Brown-out Function

When the input voltage decreases, the switching operation of the IC is stopped by Brown-in and Brown-out Function. This function prevents excessive input current and overheats.

The detection voltage of Brown-in and Brown-out Function is set by R1 to R4 shown in Figure 8-26. When the VCC pin voltage is higher than $V_{CC(ON)}$, this function operates depending on the VSEN pin voltage as follows:

- When the VSEN pin voltage is more than $V_{SEN(ON)}$ = 1.42 V, the IC starts.
- When the VSEN pin voltage is less than $V_{SEN(OFF)}$ = 1.16 V, the IC stops switching operation.

Given, the DC input voltage when the IC starts as $V_{IN(ON)}$, the DC input voltage when the switching operation of the IC stops as $V_{IN(OFF)}$. $V_{IN(ON)}$ is calculated by Equation (13). $V_{IN(OFF)}$ is calculated by Equation (14). Thus, the relationship between $V_{IN(ON)}$ and $V_{IN(OFF)}$ is Equation (15).

$$V_{IN(ON)} \fallingdotseq V_{SEN(ON)} \times \frac{(R1+R2+R3+R4)}{R4} \quad (13)$$

$$V_{IN(OFF)} \fallingdotseq V_{SEN(OFF)} \times \frac{(R1+R2+R3+R4)}{R4} \quad (14)$$

$$V_{IN(OFF)} \fallingdotseq \frac{V_{SEN(OFF)}}{V_{SEN(ON)}} \times V_{IN(ON)} \quad (15)$$

The detection resistance is calculated from Equation (13) as follows:

$$R1+R2+R3 \fallingdotseq \frac{V_{IN(ON)} - V_{SEN(ON)}}{V_{SEN(ON)}} \times R4 \quad (16)$$

Because R1, R2, and R3 are applied high DC voltage and are high resistance, the following should be considered:

- Select a resistor designed against electromigration according to the requirement of the application, or
- Use a combination of resistors in series for that to reduce each applied voltage

C2 shown in Figure 8-26 is for reducing ripple voltage of detection voltage and making delay time. The value of C2 is about 0.1 μF.

The value of R1 to R4 and C2 should be selected based on actual operation in the application.

When the Brown-in and Brown-out Function does not be used, the detection resistance (R1, R2, R3, and R4) is removed. C2 is for preventing malfunction caused by noise. The value of C2 is about 0.01 μF.

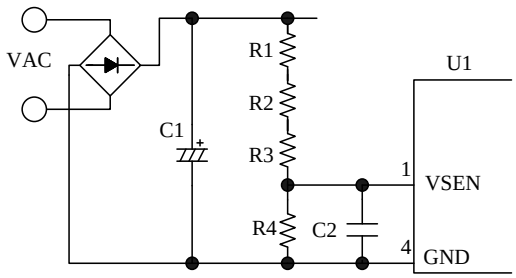


Figure 8-26 VSEN pin peripheral circuit

8.9 External Latched Shutdown Function

Figure 8-27 shows the CSS pin peripheral circuit example. When the voltage is inputted to the CSS pin from an external power supply, External Latched Shutdown Function is activated, the IC stops switching operation in the latch mode. When the VCC pin voltage is decreased to $V_{CC(LA\_OFF)}$ = 8.2 V or less, the latch mode is released.

This function can be used as the protection of abnormal operations.

The CSS pin input voltage should be set $V_{CSS(1)}$ = 8.6 V (max.) or more and less than the absolute maximum ratings 12 V.

Since the sink current flows from the CSS pin in the overcurrent operation (refer to Section 8.10), the current supply ability of the external circuit should be set more than the CSS pin sink current (about 100 mA).

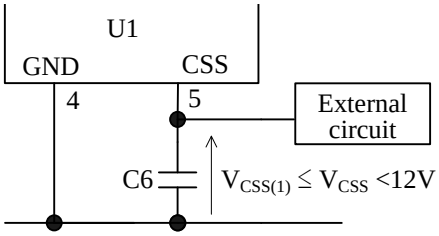


Figure 8-27 CSS pin peripheral circuit example

8.10 Overcurrent Protection (OCP)

When Overcurrent Protection (OCP) is activated, the output power is limited by detecting the drain current of the power MOSFET at pulse-by-pulse.

The overcurrent is detected by the OC pin or the RC pin. Figure 8-28 shows the peripheral circuit of the OC pin and the RC pin.

C11 is the bypass capacitor. Since C11 is smaller than Ci, the detection current of R_{OCP} becomes low. Thus, the R_{OCP} can reduce loss and be small resistor.

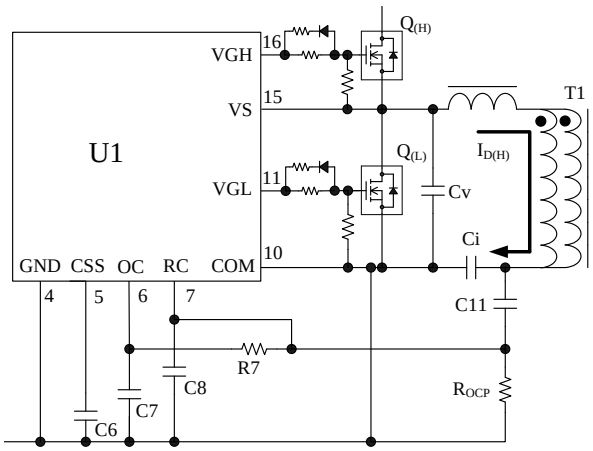


Figure 8-28 the peripheral circuit of OC pin and RC pin

Since the accurate value of the resonant current cannot be calculated easy from the condition of the resonant power supply including input voltage and output voltage, the value of R_{OCP}, C11, R7 and C7 should be adjusted based on actual operation in the application. R7 and C7 are the filter of the OC pin.

The value of R_{OCP}, C11, R7 and C7 are set as follows:

- C11 and R_{OCP}
  C11 is 100pF to 330pF (around 1 % of Ci value).
  R_{OCP} is around 100 Ω.
  Given the current of the high side power MOSFET at ON state as $I_{D(H)}$. R_{OCP} is calculated Equation (17).
  The detection voltage of R_{OCP} is used the detection of the capacitive mode operation (refer to Section 8.7). Therefore, setting of R_{OCP} and C11 should be taken account of both OCP and the capacitive mode

operation.

$$R_{OCP} \fallingdotseq \frac{V_{OC(L)}}{I_{D(H)} \times \left(\frac{C11}{C11 + Ci} \right)} \quad (17)$$

- R7 and C7 are for high frequency noise reduction. R7 is 100 Ω to 470 Ω. C7 is 100 pF to 1000 pF.

Table 8-1 shows the overcurrent detection voltage of the OC pin and the RC pin, and the sink current of CSS pin. There are three OCP operations as follows:

1) Low Level OCP Detection
When the OC pin voltage becomes $V_{OC(L)}$ or more, C6 connected to the CSS pin is discharged by the sink current $I_{CSS(L)}$. As a result, the oscillation frequency increases, the output power is limited.
If the OC pin voltage decreases less than $V_{OC(L)}$ during discharge of C6, the IC stops discharge of C6.

2) High Level OCP Detection
When the OC pin voltage becomes $V_{OC(H)}$ or more, C6 is discharged by the sink current $I_{CSS(H)}$. Since $I_{CSS(H)}$ is eleven times of $I_{CSS(L)}$, the oscillation frequency increases at high speed, the output power is limited quickly. If the OC pin voltage decreases less than $V_{OC(H)}$ during discharge of C6, the IC becomes the Low Level OCP Detection.

3) High Speed OCP Detection
In case the large current flows as output is shorted, this protection is activated. When the OC pin voltage or the RC pin voltage becomes as follows, the switching states of the power MOSFET is inverted.
OC pin voltage is more than $V_{OC(S)}$ or
RC pin voltage is more than $|V_{RC(S)}|$.
At same time, C6 is discharged by the sink current $I_{CSS(S)}$. As a result, the oscillation frequency increases at high speed, the output power is limited quickly. If the OC pin voltage decreases less than $V_{OC(S)}$ or the RC pin voltage becomes within $|V_{RC(S)}|$ due to reducing the output power, the IC becomes the High Speed OCP Detection and the Low Level OCP Detection.

Table 8-1 Overcurrent detection voltage and sink current of CSS pin

OCP	Pins	Detection voltage	CSS pin sink current
Low	OC	$V_{OC(L)}$ = 1.52 V	$I_{CSS(L)}$ = 1.8 mA
High	OC	$V_{OC(H)}$ = 1.83 V	$I_{CSS(H)}$ = 20.0 mA
High speed	OC	$V_{OC(S)}$ = 2.35 V	$I_{CSS(S)}$ = 18.3 mA
	RC	$V_{RC(S)}$ = 2.35 V, − 2.35 V	

8.11 Overload Protection (OLP)

Figure 8-29 shows the FB pin peripheral circuit, Figure 8-30 shows the FB pin waveform at Overload Protection (OLP) operation.

When the output power becomes overload state that the drain current is limited by Overcurrent Protection (OCP) operation, the oscillation frequency increases. When the oscillation frequency increases, the output voltage decreases and the current of the secondary photo-coupler becomes zero. Thus, the feedback current flowing through the photo-coupler connected the FB pin becomes zero. As a result, C4 is charged by the FB Pin Source Current I_{FB} = − 25.5 μA, and the FB pin voltage increases. If the FB pin voltage increases to the FB Pin Threshold Voltage V_{FB} = 7.05 V, the IC stops switching operation in the latch mode. When the VCC pin voltage is decreased to $V_{CC(LA\_OFF)}$ = 8.2 V or less or the VSEN pin voltage is decreased to $V_{SEN(OFF)}$ = 1.16 V or less, the latch mode is released.

The stresses of the power MOSFET and the secondary side rectifier diode are reduced by OLP.

Given the time that until the FB pin voltage reaches to V_{FB} as the OLP delay time, t_{DLY} (refer to Figure 8-30). t_{DLY} is calculated Equation (18).

If R5 is 47 kΩ and C4 is 4.7 μF, t_{DLY} becomes about 0.5 s.

$$t_{DLY} \fallingdotseq \frac{\left(4.05V - R5 \times |I_{FB}|\right) \times C4}{|I_{FB}|} \quad (18)$$

Where, I_{FB} is the FB Pin Source Current − 25.5 μA.

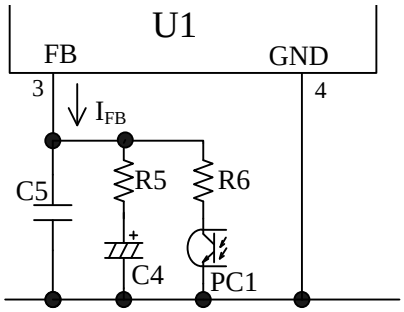


Figure 8-29 FB pin peripheral circuit

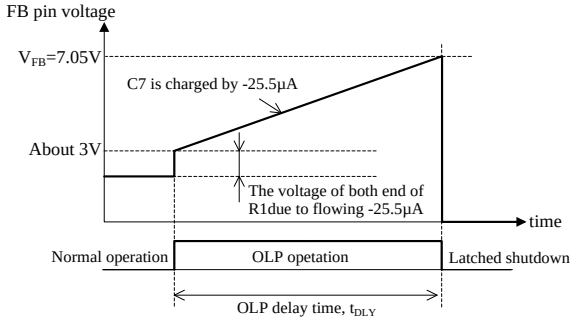


Figure 8-30 OLP operation

8.12 Overvoltage Protection (OVP)

When the VCC pin voltage increases to the VCC Pin OVP Threshold Voltage $V_{CC(OVP)}$ = 31.0 V, Overvoltage Protection (OVP) is activated and the IC stops switching operation in the latch mode. When the VCC pin voltage is decreased to $V_{CC(LA\_OFF)}$ = 8.2 V or less or the VSEN pin voltage is decreased to $V_{SEN(OFF)}$ = 1.16 V or less, the latch mode is released.

The VCC pin input voltage should be set absolute maximum ratings 35 V or less.

8.13 Thermal Shutdown (TSD)

When the junction temperature of the IC reach to the Thermal Shutdown Temperature $T_{j(TSD)}$ = 150 °C (min.), Thermal Shutdown (TSD) is activated and the IC stops switching operation in the latch mode. When the VCC pin voltage is decreased to $V_{CC(LA\_OFF)}$ = 8.2 V or less or the VSEN pin voltage is decreased to $V_{SEN(OFF)}$ = 1.16 V or less, the latch mode is released.

9. Design Notes

9.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

- **Input and Output Electrolytic Capacitor**
  Apply proper derating to ripple current, voltage, and temperature rise. The electrolytic capacitor of high ripple current and low impedance types, designed for switch mode power supplies, is recommended to use.

- **Resonant Transformer**
  The resonant power supply uses the leakage inductance of transformer. Therefore, in order to reduce the effect of the eddy current and the skin effect, the wire of transformer should be used a bundle of fine litz wires.

- **Current Detection Resistor, R_{OCP}**
  Choose a type of low internal inductance because a high frequency switching current flows to R_{OCP}, and of properly allowable dissipation.

- **Current Resonant Capacitor, Ci**
  Large resonant current flows through Ci. Ci should use the polypropylene film capacitor with low loss and high current capability. In addition, Ci must be considered its frequency characteristic since high frequency current flows.

- **Gate Pin Peripheral Circuit**
  The VGH pin and the VGL pin are for the gate dive of an external power MOSFET. The source peak current of the VGH pin and the VGL pin are – 515 mA, the sink peak current of these pins are 685 mA.
  In Figure 9-1, R_A, R_B and D_S should be adjusted by the loss of the power MOSFET and the gate waveform (reduction of ringing caused by pattern layout, and others) and EMI noise.
  R_{GS} is for preventing malfunction caused by precipitous dv/dt when the power MOSFET turns off. The value of R_{GS} is about 10 kΩ to 100 kΩ. R_{GS} is connected to near the Gate pin and the Source pin.
  When the gate resistances are adjusted, the gate waveforms should be checked that the dead time is ensured as shown in Figure 9-2.

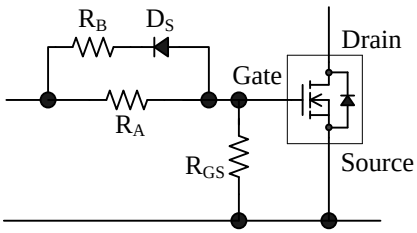


Figure 9-1 Peripheral circuit of power MOSFET gate

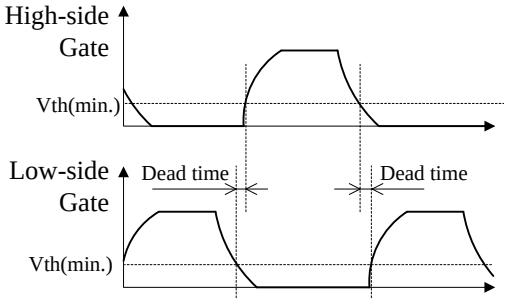


Figure 9-2 Dead time confirmation

9.2 PCB Trace Layout and Component Placement

Since the PCB circuit design and the component layout significantly affect the power supply operation, EMI noise, and power dissipation, the high frequency trace of PCB shown in Figure 9-3 should be designed low impedance by small loop and wide trace.

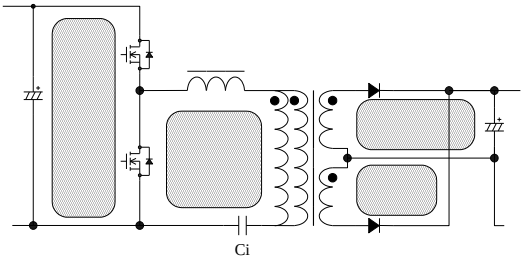


Figure 9-3 High frequency current loops (hatched areas)

In addition, the PCB circuit design should be taken account as follows:

Figure 9-4 shows the circuit design example.

1) Main Circuit Trace Layout
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

2) Control Ground Trace Layout
When large current flows into the control ground trace, the operation of IC might be affected by it. The control ground trace should be separate from the main circuit trace, and should be connected at a single point grounding as close to the GND pin as possible.

3) VCC Trace Layout
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C3 and the IC are distant from each other, placing a film capacitor C_f (about 0.1 µF to 1.0 µF) close to the VCC pin and the GND pin is recommended.

4) Peripheral Components for the IC Control
These components should be placed close to the IC, and be connected to the IC pin as short as possible.

5) Bootstrap Circuit Components
These components should be connected to the IC pin as short as possible, and the loop for these should be as small as possible.

6) Secondary side Rectifier Smoothing Circuit Trace Layout
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible.

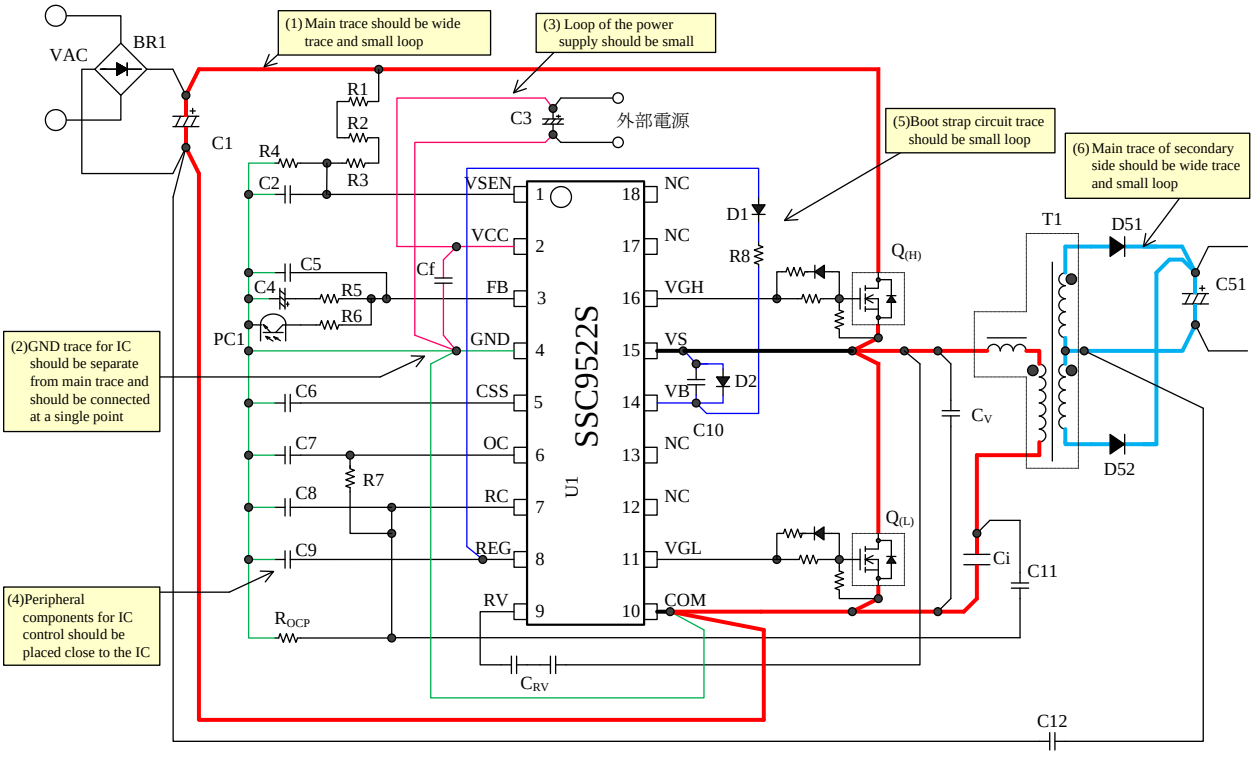


Figure 9-4 Peripheral circuit example around the IC

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