32V, 4A, Synchronous, Step-Down Converter

LA1314D

Overview


UDFN2x3-8

The LA1314D is an easy to use synchronous step-down Buck. Which integrated low on resistance high-side and low-side power MOSFETs. The LA1314D can deliver 4A of output current efficiently with constant on time (COT) control for fast loop response.

The LA1314D achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

The LA1314D has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The LA1314D is available in a space-saving UDFN2x3-8 package.

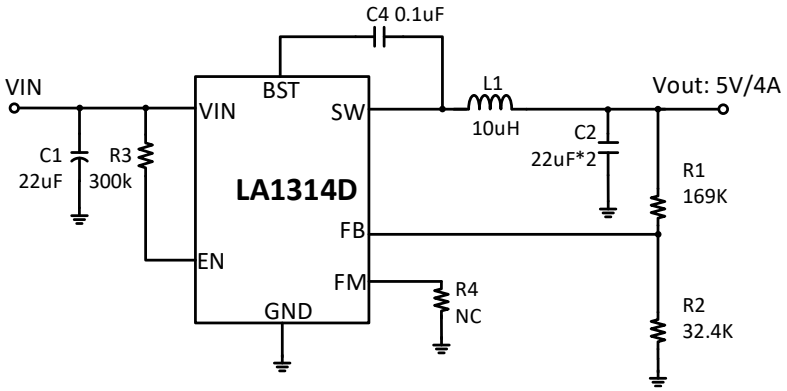
Features

- 4.5V to 32V Wide Input Range
- 4A Peak Output Current
- 85mΩ/55mΩ Internal Power MOSFETs
- 185uA Low Quiescent Current
- Constant On Time Control for Fast Loop Response
- 180/340kHz Switching Frequency Selectable and PFM and FPWM Operation Mode Selectable
- Support Up to 98% Large Duty Cycle
- Internal Soft Start
- Output Voltage adjustable from 0.798V
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection
- Available in an UDFN2x3-8 Package

Applications

- Surveillance Camera
- Home Appliance and Whitegoods
- Multi-functional Printer
- Automotive
- Industrial Control

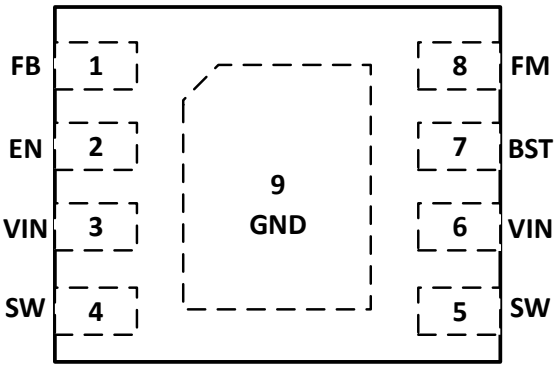
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1314D	UDFN2x3-8	-40 to 125℃	T/R 4000pcs/roll	sales@latticeart.com

Pin Diagram (Top view)

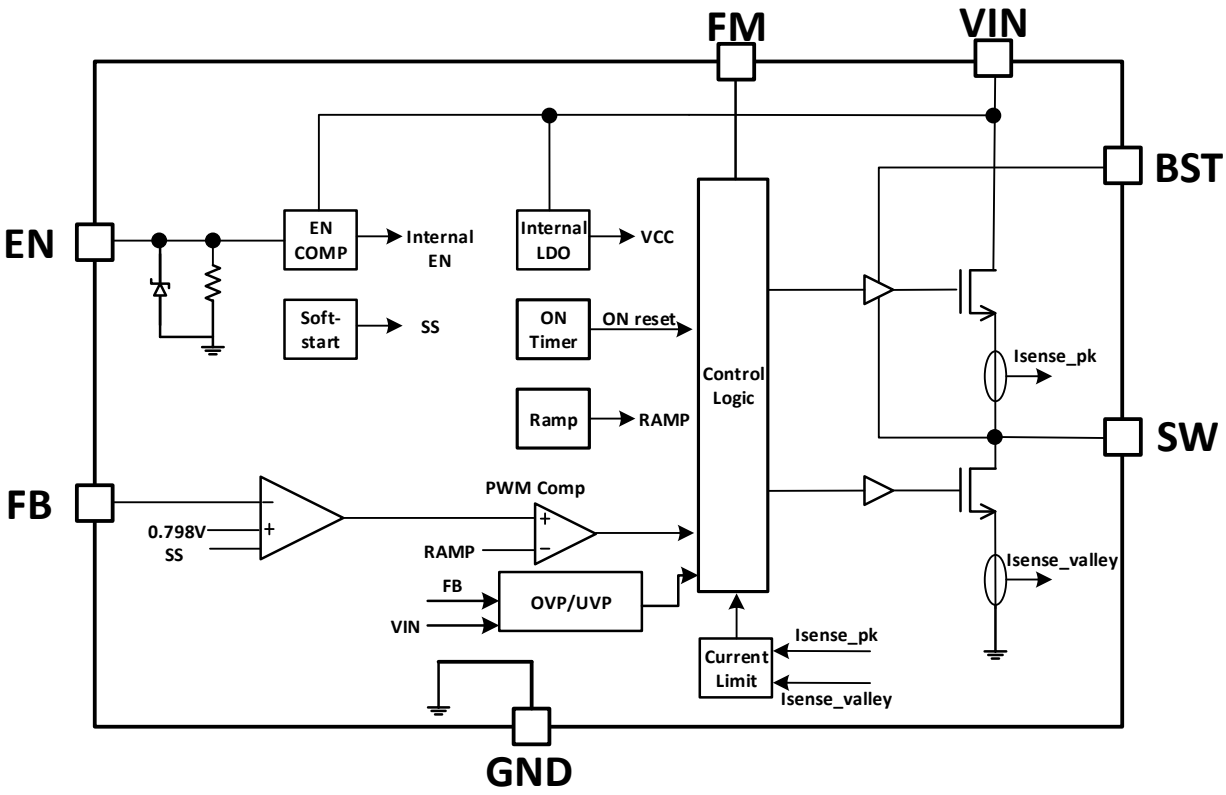


LLLLLLL: Lot number
1314D: Product code
WWY: Date Code

Pin Description

Pin No.	Symbol	Pin Description
1	FB	**Feedback input to the convertor**. Connect a resistor divider to set the output voltage.
2	EN	**Enable Pin**. Drive EN Pin High to enable IC, otherwise float or pull down EN to disable IC. EN pin Can be tied to VIN by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
3,6	VIN	**Supply input Pin**. VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
4,5	SW	**Switching output of the convertor**. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
7	BST	**Bootstrap**. Connect a capacitor between SW and BST pins to form a floating supply across the High-side switch driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
8	FM	**Operation mode and frequency selection**. Program FM to select CCM, pulse skip mode, and the operating switching frequency. Connect a resistor between FM pin and GND can configure the frequency. See the table 1 for frequency and mode configuration.
9	GND(EP)	**System ground**. GND is the reference ground of the regulated output voltage. Requires extra care during PCB layout. Connect to GND with wide copper traces and vias.

Block Diagram



Absolute Maximum Ratings (Note 1/2)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
V_{IN}	VIN to GND	-0.3~33	V
SW	SW to GND	-0.7 (-5V in 10ns)~VIN + 0.7	V
EN	Max Input current to EN pin	100(2)	uA
BST	BST to SW	-0.3~6	V
All Other Pins		-0.3~6	V
T_{STG}	Storage temperature	-65 to150	^{o}C
T_j	Junction temperature	-40 to150	^{o}C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Note 2: For details on ENs ABS max rating, please refer to the Enable Control section.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
BST	BST to SW	4~5	V
FB	FB to GND	0~1	V
V_{IN}	VIN to GND	4.5~32	V
EN	EN to GND	0~5	V
V_{OUT}	V_{OUT} to GND	0.8~0.98xVIN or VOUT<18	V
I_{OUT}	Max Continuous Output Current	4	A

Thermal Resistance (Note 3)

Symbol	Definition	Ratings	Unit
$R_{\theta JC}$	Junction to case (top) thermal resistance	10	^{o}C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	40	^{o}C/W

Note 3: Measured on Latticeart DEMO DEM1314D-00A, 4-Layer PCB, 63mm x 48mm board.

ESD

Symbol	Definition	Ratings	Unit
HBM	Human Body Mode	±2000	V
CDM	Charged Device Mode	±1500	V

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input UVLO and Quiescent Current						
VIN_{UVR}	VIN UVLO rising threshold		4.2	4.28	4.35	V
VIN_{UVF}	VIN UVLO falling threshold		3.8	3.9	4	V
VIN_{UV_hys}	VIN UVLO hysteresis			0.38		V
I_{QS}	Shutdown supply current	V_{EN} < 0.3V, V_{IN}=12V		1	3	μA
I_Q	Quiescent supply current	V_{IN}=12V, No load, VFB = 0.83V, no switching	170	185	200	μA
High Side and Low Side MOSFETs						
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 32V			1	μA
R_{ON_HS}	High-Side Switch on resistance	V_{BST-SW} = 5V		85		mΩ
R_{ON_LS}	Low-Side Switch on resistance	V_{IN} = 12V		55		mΩ
Feedback Voltage and SS						
V_{FB}	Feedback voltage	Ta = 25°C	790	798	806	mV
		Ta = -40°C to +125°C	782	798	814	mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
Tss	Soft-Start time	V_{FB} from 0% to 100%	1.8	2.4	3.2	ms
Current Limit						
I_{Valley}	Low-Side Current limit	V_{OUT}=0V	4	4.5	5	A
ZCD				160		mA
Enable						
V_{EN_R}	EN Rising Threshold	Low to High	1.1	1.2	1.3	V
V_{EN_F}	Enable falling threshold	High to Low	0.94	0.98	1.02	V
V_{EN_Hys}	Enable Threshold Hysteresis			0.22		V

Electrical Characteristics

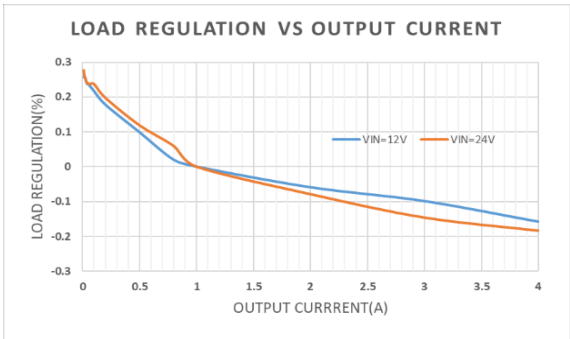
V_{IN}=12V, V_{EN}=2V, T_A=25ºC, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{EN}	Enable input resistor.			1500		kΩ
Switching Frequency and Duty Cycle						
F_{sw} Oscillator frequency		FM=GND, FPWM		340		KHz
		FM=39k, FPWM		180		KHz
		FM=200k, PFM		180		KHz
		FM=Float, PFM		340		KHz
T_{ONMIN}	Minimum on time(4)			60		ns
D_{MAX}	Max duty cycle			98		%
V_{OUT} OVP/UVP threshold hold						
FB_{OVP}			107	110	115	%
FB_{OV_Hys}				5		%
FB_{UVP}				30		%
T_{OTP_R}	Thermal shutdown(4)			150		°C
T_{OTP_Hys}(3)	OTP hysteresis(4)			20		°C
T_{OFFMIN}	Minimum off time(4)			150		ns

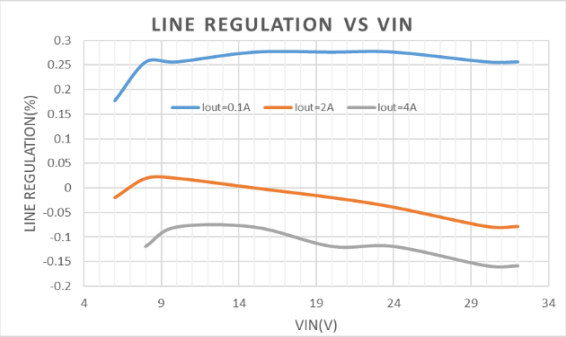
Typical Performance Characteristic

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = +25°C, unless otherwise noted.

Load Regulation

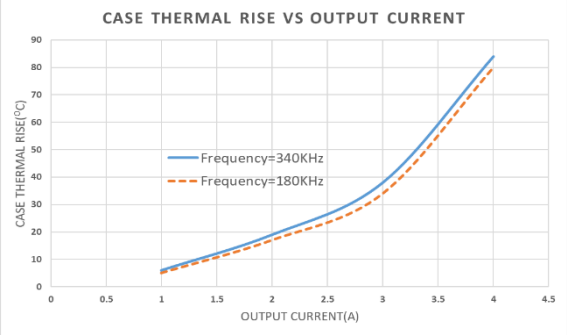


Line Regulation



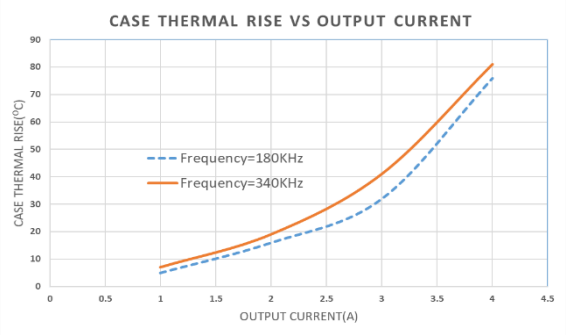
Case Temperature Rise

V_{OUT}=5V



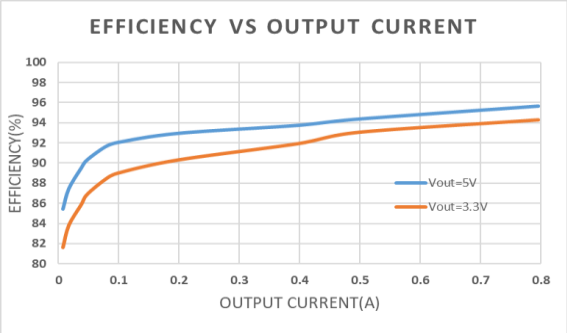
Case Temperature Rise

V_{OUT}=3.3V



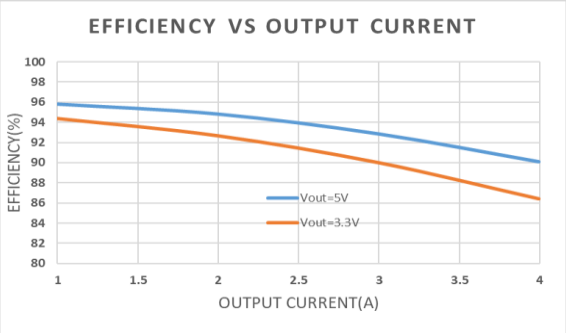
Efficiency at light load

Frequency=340kHz, PFM mode, DCR=26mohm



Efficiency at heavy load

Frequency=340kHz, DCR=26mohm, FPWM Mode

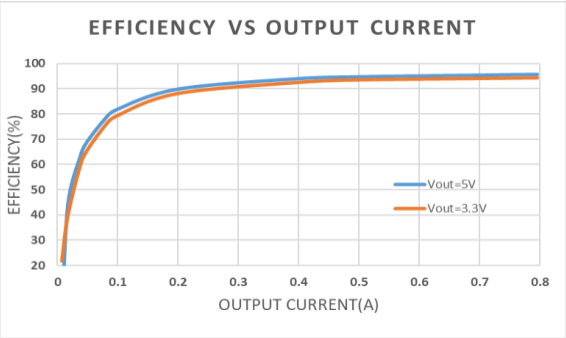


Typical Performance Characteristic

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = +25°C, unless otherwise noted.

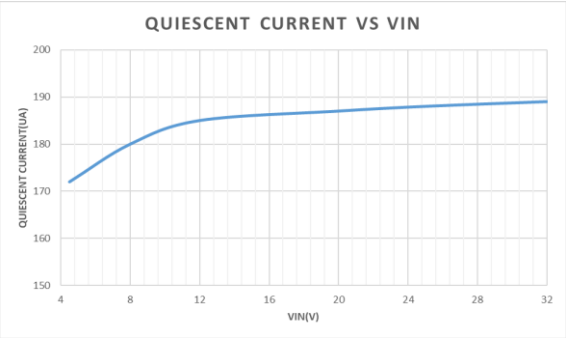
Efficiency at light load

Frequency=340kHz, FPWM mode, DCR=26mohm

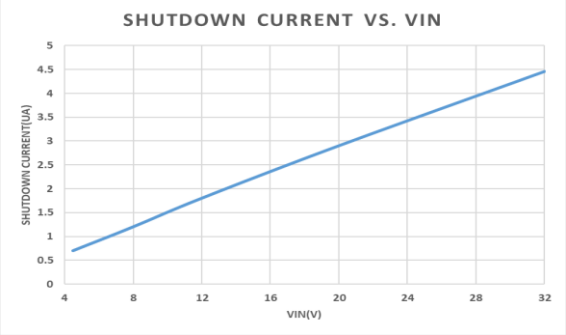


Quiescent Current Vs VIN

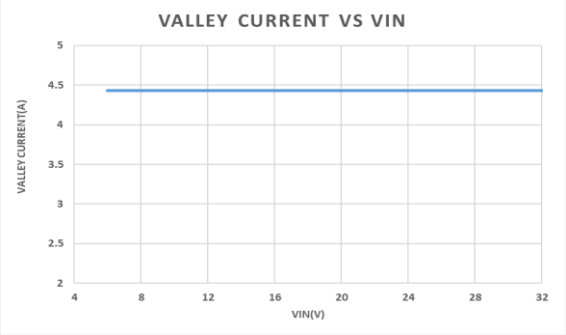
PFM Mode



Shutdown Current Vs VIN



Valley Current limit Vs VIN

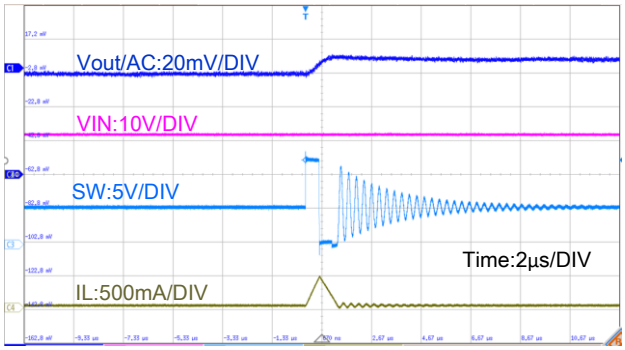


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = +25°C, Frequency = 340kHz, unless otherwise noted.

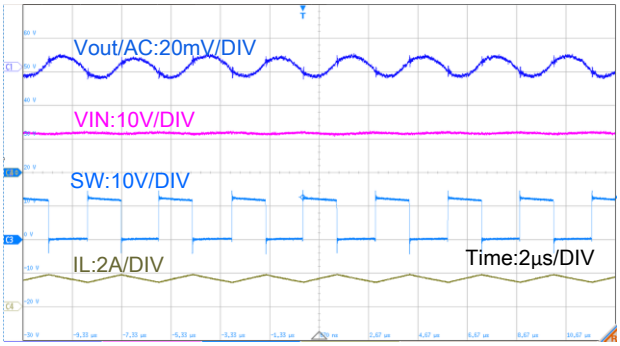
Output Voltage Ripple

IOUT = 0A, PFM Mode



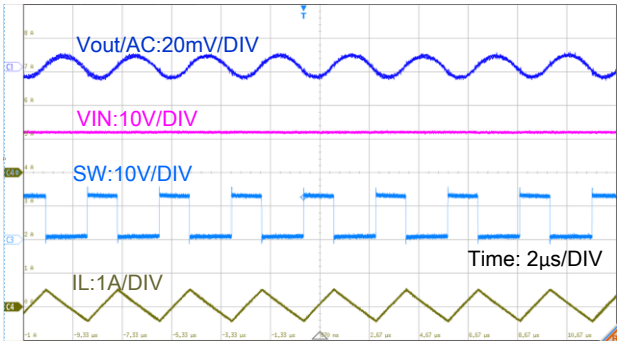
Output Voltage Ripple

IOUT = 4A



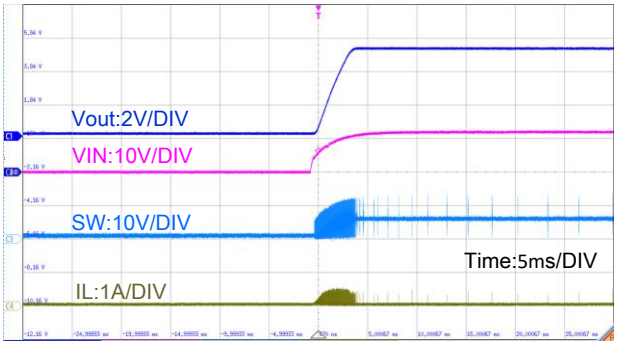
Output Voltage Ripple

IOUT = 0A, FPWM Mode



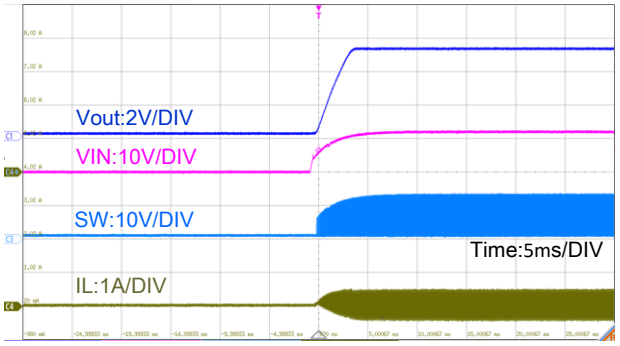
Start-Up through V_{IN}

IOUT = 0A, PFM Mode



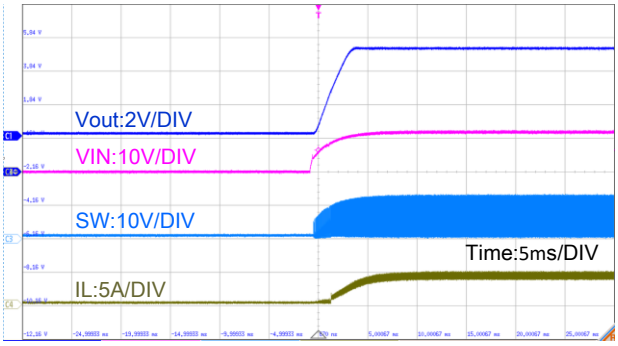
Start-Up through V_{IN}

IOUT = 0A, FPWM Mode



Start-Up through V_{IN}

IOUT = 4A, FPWM Mode

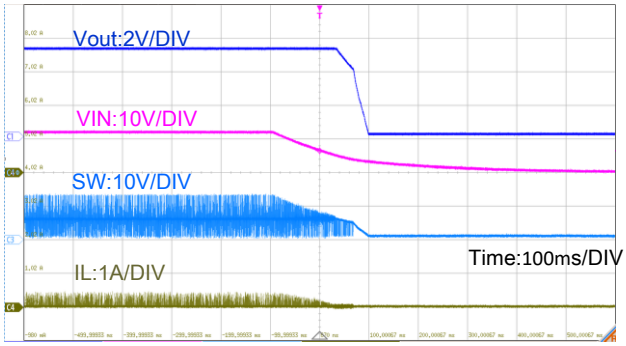


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = +25°C, Frequency = 340kHz, unless otherwise noted.

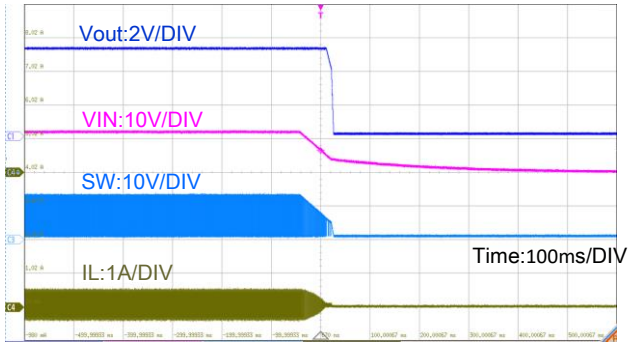
Shutdown through V_{IN}

IOUT = 0A, PFM Mode



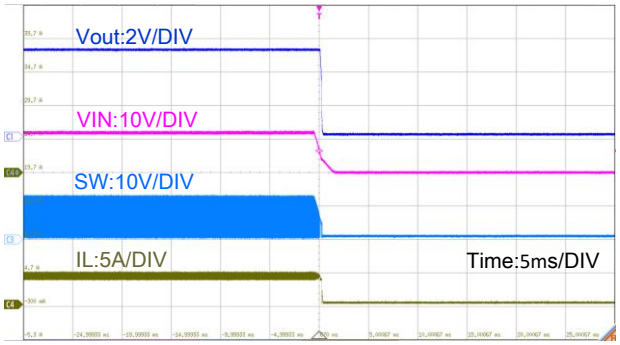
Shutdown through V_{IN}

IOUT = 0A, FWM Mode



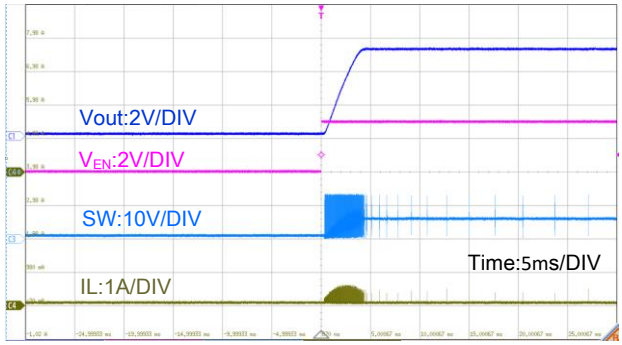
Shutdown through V_{IN}

IOUT = 4A



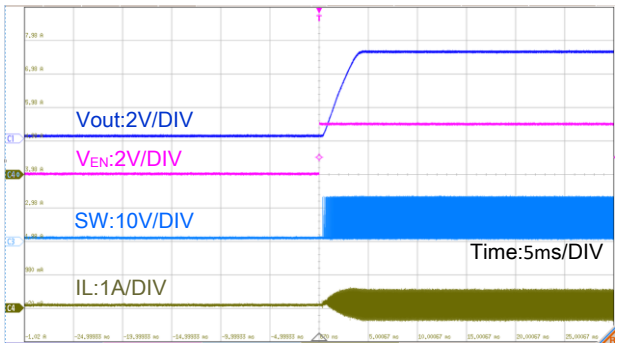
Start-Up through EN

IOUT = 0A, PFM Mode



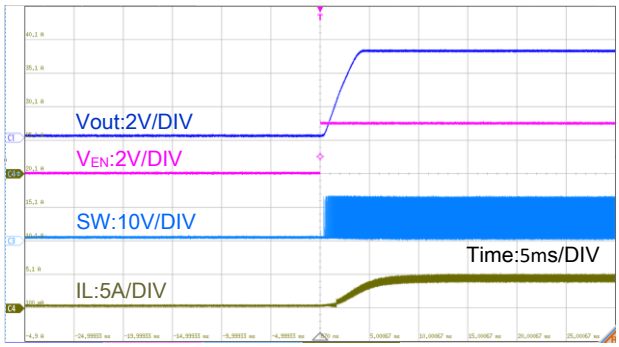
Start-Up through EN

IOUT = 0A, FPWM Mode



Start-Up through EN

IOUT = 4A

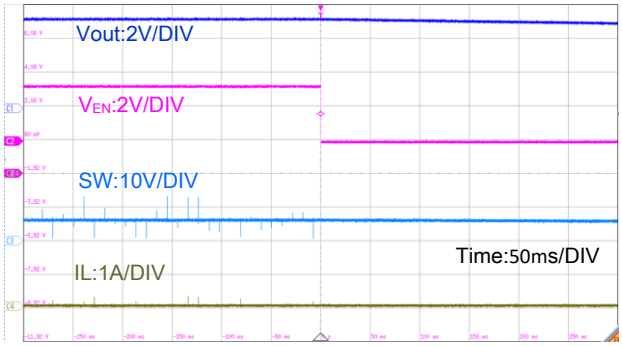


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = +25°C, Frequency = 340kHz, unless otherwise noted.

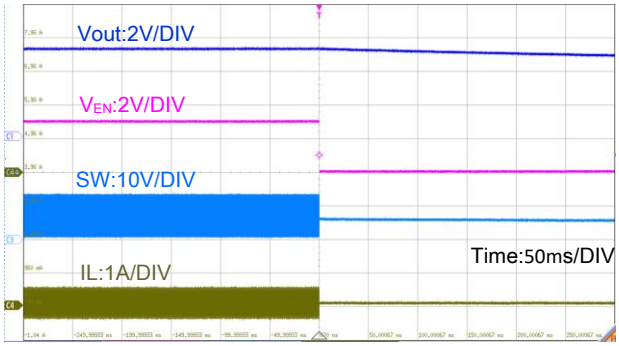
Shutdown through EN

IOUT = 0A, PFM Mode



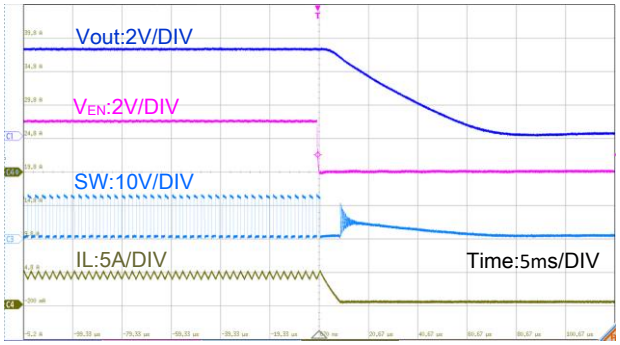
Shutdown through EN

IOUT = 0A, FPWM Mode



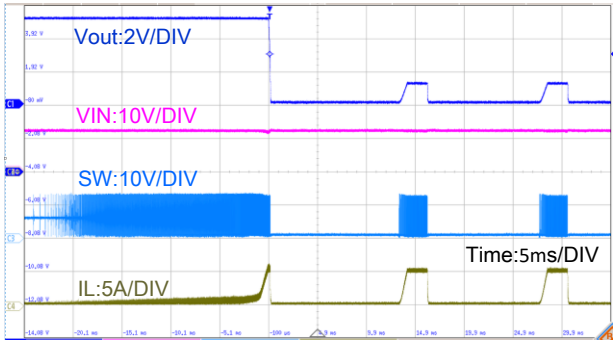
Shutdown through EN

IOUT = 4A



Short Entry

IOUT = 0A, PFM Mode



Short Entry

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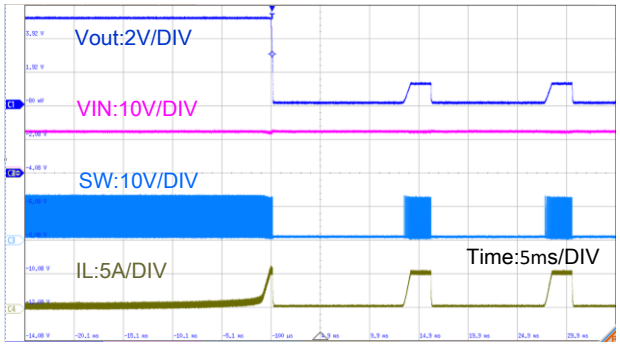
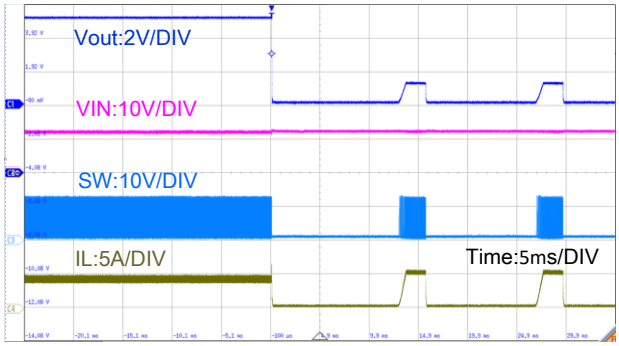


Short Entry

IOUT = 4A

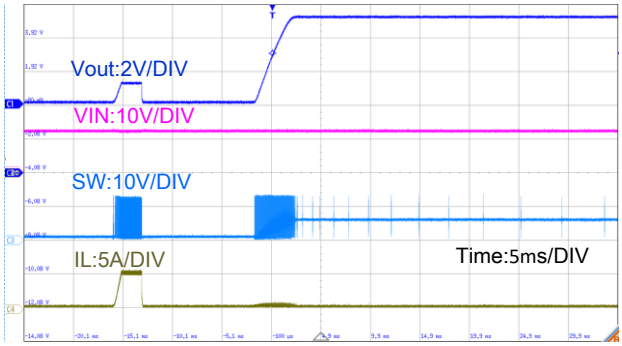


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = +25°C, Frequency = 340kHz, unless otherwise noted.

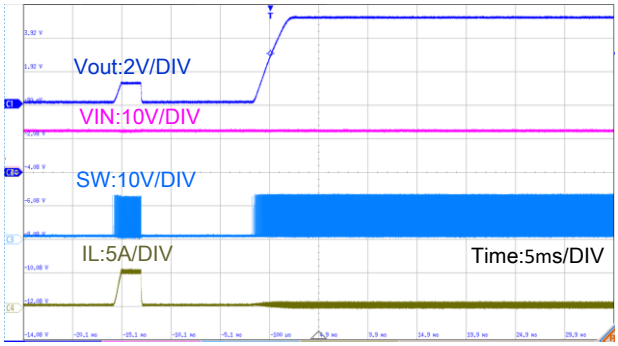
Short Recovery

IOUT = 0A, PFM Mode



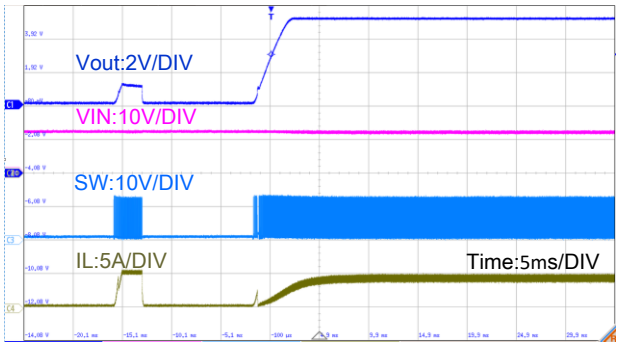
Short Recovery

IOUT = 0A, FPWM Mode

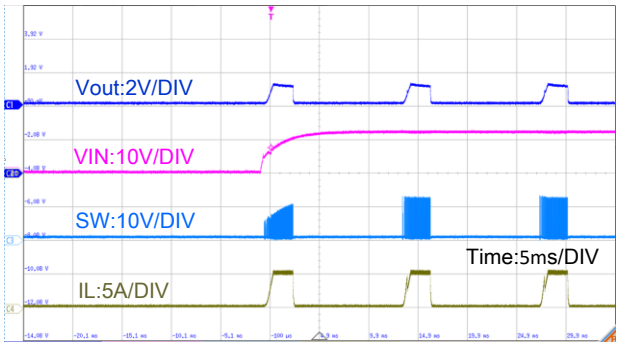


Short Recovery

IOUT = 4A

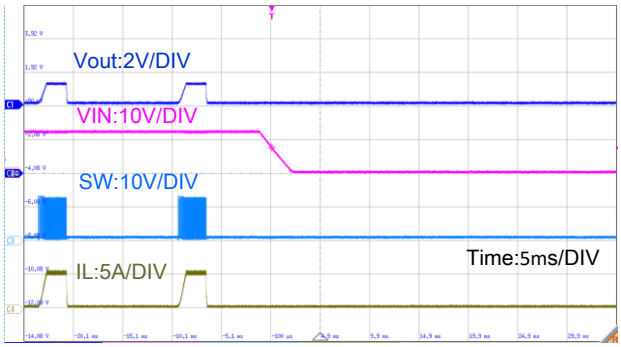


Short Start-Up through VIN

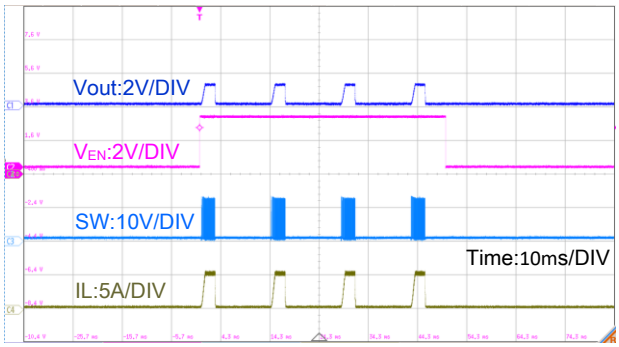


Short Shutdown through VIN

IOUT = 0A, FPWM Mode



Short EN ON/OFF



Function Descriptions

Pulse-Width Modulation (PWM) Control

The LA1314D is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low- side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. To avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

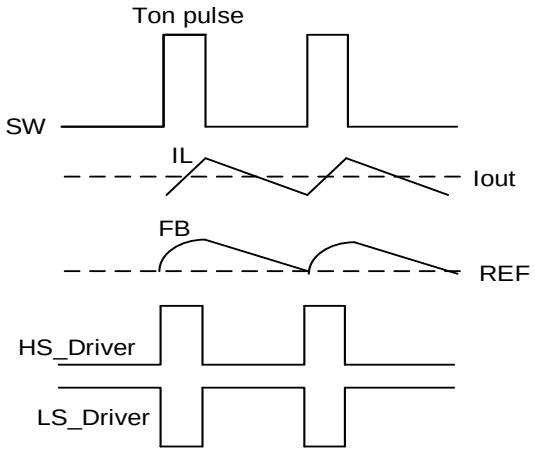


Figure 1. FPWM Operation

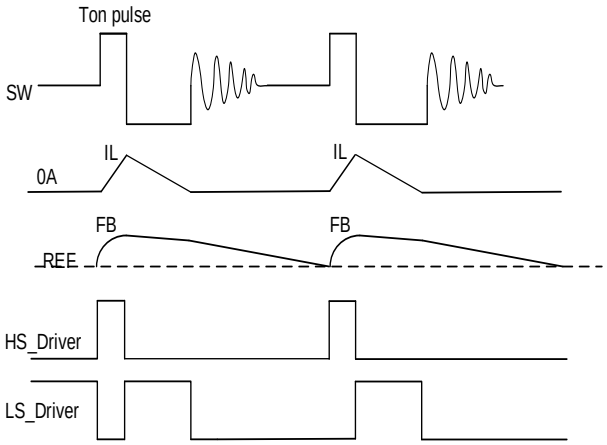


Figure 2. PFM Operation

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous- conduction-mode (DCM).

When the LA1314D works in pulse-frequency modulation (PFM) mode during light-load operation, the LA1314D reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side will be off the LA1314D enters Hi-zi state. The output capacitors discharge slowly to GND through R1 and R2. When VFB drops below the reference voltage, the HS-FET is turned on again. This operation improves device efficiency greatly when the output current is low.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.5MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 6V Zener diode. EN can connected to VIN directly by a resistor.

The EN Pin can connect to VIN by a pull-up resistor, but EN input current need below 100uA. For example, if VIN=24V, the IZener=(24-6)/RPULL-UP<100uA, So, RPULL-UP>180KΩ.

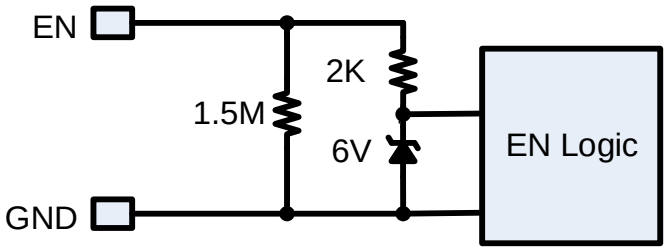


Figure 3. Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The LA1314D UVLO comparator monitors the input voltage. The UVLO rising threshold is 4.28V(typically), while its falling threshold is consistently 3.9V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (VSS) that ramps up linearly. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 2.4ms(typically) internally.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The LA1314D has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the LS limit compactor active. The device enters over current protection mode. High side will not be turned on until the valley current limit disappear. Meanwhile, the output voltage drops until VFB is below the under voltage (UV) threshold (typically 30% of the reference). Once UV is triggered, the LA1314D enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

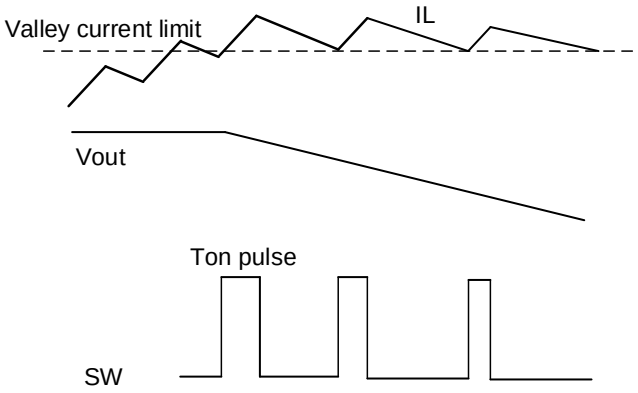


Figure 4. Valley Current limit control

Pre-Bias Start-Up

The LA1314D is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Output OVP and UVP

The LA1314D monitors a resistor-divided VFB to detect over- and under-voltage. When VFB becomes higher than 110%(typically) of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turned off until the negative current (-1.1A typically) limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed. When VFB drops below 30%(typically) of VREF, the UVP-2 comparator output goes high, and the LA1314D enters the hiccup protection.

Large Duty Cycle Operation

When LA1314D will automatically extend the On time to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The LA1314D can support up to 98% maximum duty cycle.

Frequency/Mode Programmable

The LA1314D can setup the operation mode and PWM frequency by connecting FM pin to GND with a resistor(R6). Below table shows the configuration.

Table 1. Frequency and Mode configuration

R6(kΩ)	Operation Mode	Frequency(KHz)
0	FPWM	340
39	FPWM	180
200	PFM	180
Float	PFM	340

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Application Information

Setting the Output Voltage

The LA1314D output voltage can be set by the external resistor dividers. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It I recommended to choose a value within 2k to 100k for R2. The reference voltage is fixed at 0.8V. The feedback network is shown below Figure.

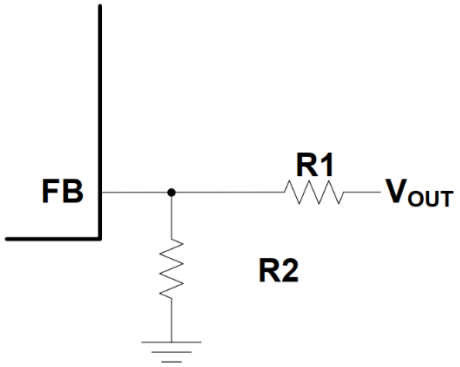


Figure 5. Feedback Network

Choose R1 and R2 using Equation:

$$\mathbf{V_{OUT} = V_{FB}(R_1 + R_2)/R_2}$$

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to_peak ripple current in the inductor to be in the range of 30% to 60% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$\mathbf{L = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * \Delta I_L * F_{OSC}}}$$

Where ΔIL is the inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$\mathbf{I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}}$$

Selecting Input capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the stepdown converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$\mathbf{C_{IN}} = \mathbf{I_{OUT}} \times \sqrt{\frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}} \times \left(1 - \frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}}\right)}$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\mathbf{I_{CIN}} = \frac{\mathbf{I_{OUT}}}{\mathbf{2}}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta \boldsymbol{V_{IN}} = \frac{\mathbf{I_{OUT}}}{\mathbf{F_{OSC}} \times \boldsymbol{C_{IN}}} \times \frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}} \times \left(\mathbf{1} - \frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}}\right)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta \boldsymbol{V_{IN}} = \frac{\mathbf{1}}{\mathbf{4}} \times \frac{\mathbf{I_{OUT}}}{\mathbf{F_{OSC}} \times \boldsymbol{C_{IN}}}$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\mathbf{\Delta V_{OUT}} = \frac{\mathbf{V_{OUT}}}{\mathbf{F_{OSC}} * \mathbf{L}} * \left(\mathbf{1} - \frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}}\right) * \left(\mathbf{R_{ESR}} + \frac{\mathbf{1}}{\mathbf{8} * \mathbf{F_{OSC}} * \mathbf{C_{OUT}}}\right)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor, F_{OSC} is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * (\frac{1}{8 * F_{OSC} * C_{OUT}})$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The LA1314D can be optimized for a wide range of capacitance and ESR values.

Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{OUT_max} can be limited approximately by:

$$C_{OUT\_MAX} = (I_{limit_{ave}} - I_{OUT}) * T_{ss}/V_{OUT}$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period, Tss is the soft-start time(2.4ms typically).

The recommended parameters for typical output application as table 2(5) shown.

Table 2: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT}(uF)
5	169	32.4	10	44
3.3	102	32.4	6.8	44
2.5	119	56	4.7	44
1.8	150	120	3.3	44
1.2	100	200	2.2	44
1	30	120	2.2	44
0.8	0	Float	2.2	44

Note 5: Table 2 based on frequency=340KHz, for 180KHz application, should increase the inductor and output capacitor for improving stability performance.

PCB layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below and take figures as the reference.

- The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

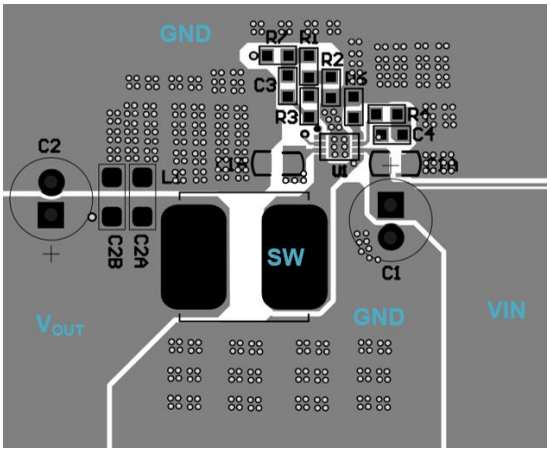


Figure 6. Top Layer

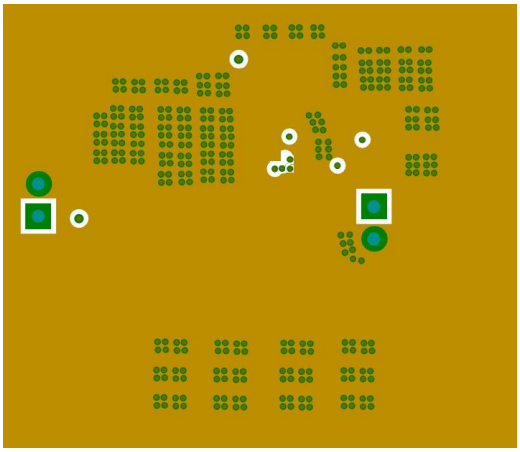


Figure 7. Inner 1 Layer

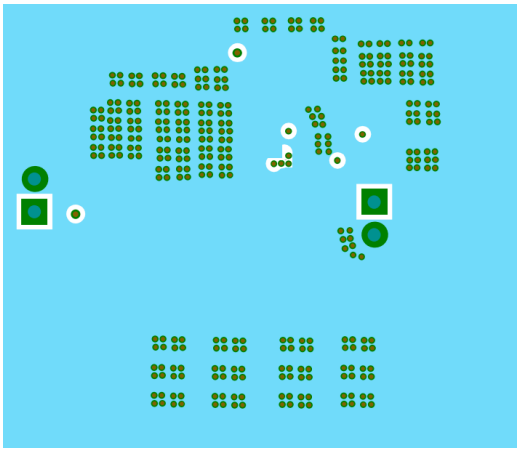


Figure 8. Inner 2 Layer

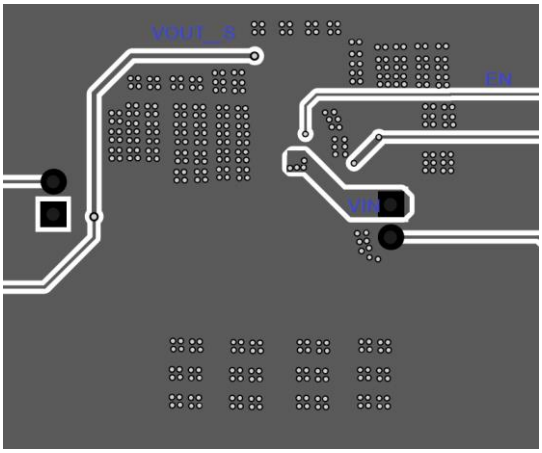
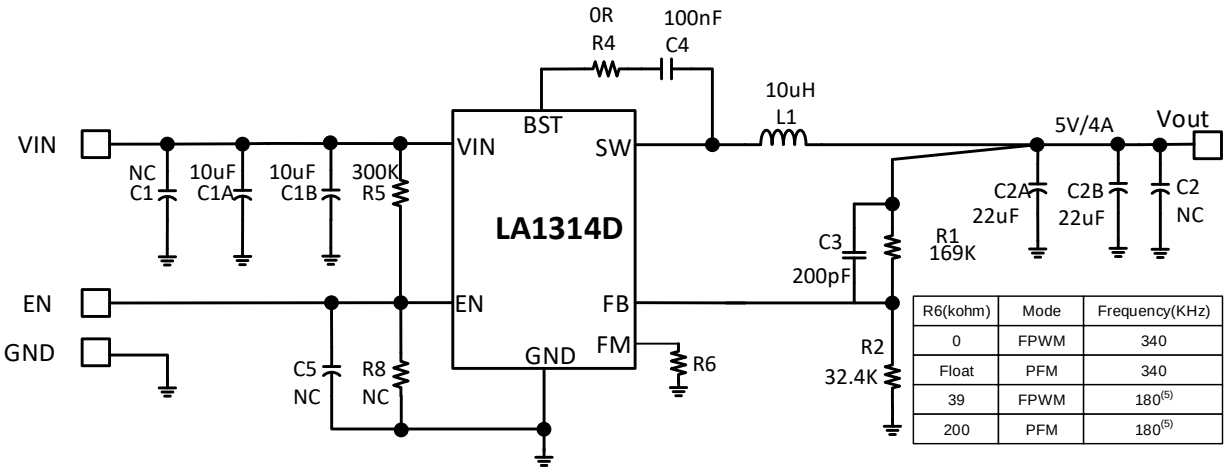


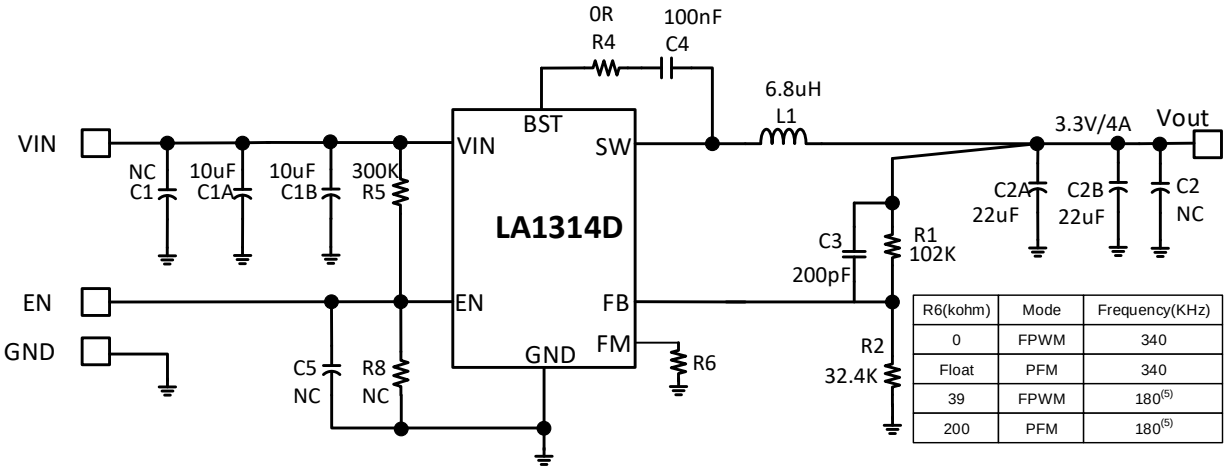
Figure 9. Bottom Layer

Typical Application Circuits



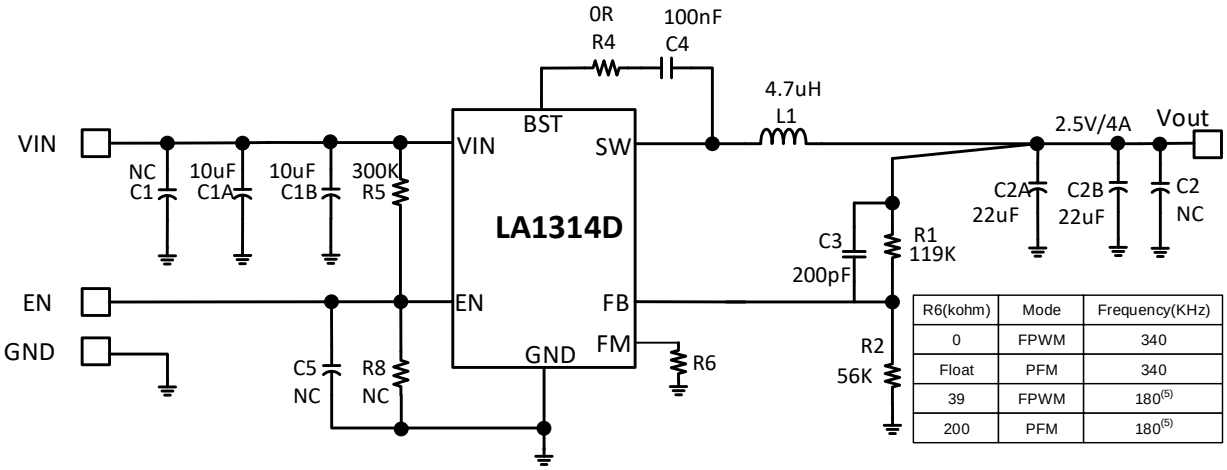
R6(kohm)	Mode	Frequency(KHz)
0	FPWM	340
Float	PFM	340
39	FPWM	180(5)
200	PFM	180(5)

Figure 10. Typical VOUT=5V/4A application



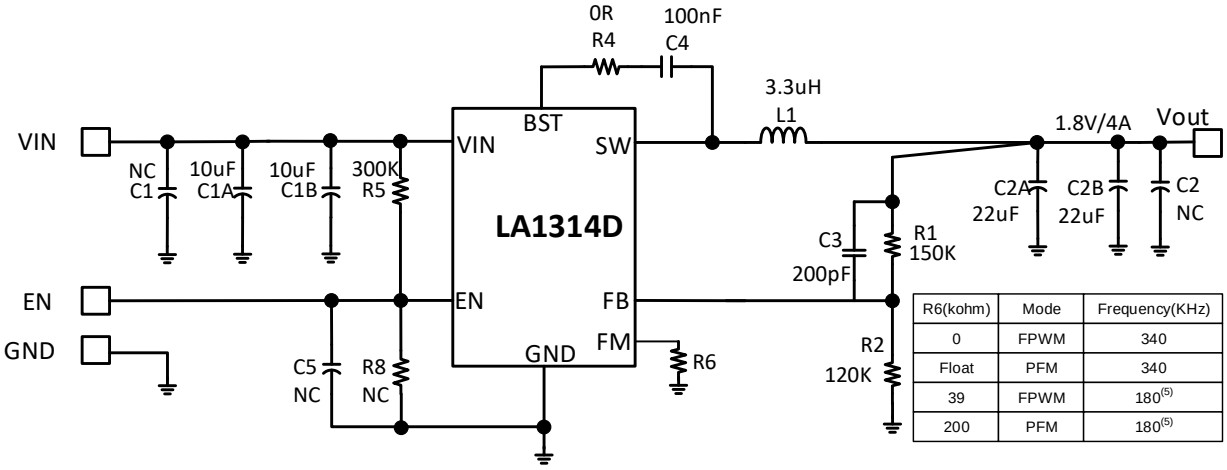
R6(kohm)	Mode	Frequency(KHz)
0	FPWM	340
Float	PFM	340
39	FPWM	180(5)
200	PFM	180(5)

Figure 11. Typical VOUT=3.3V/4A application



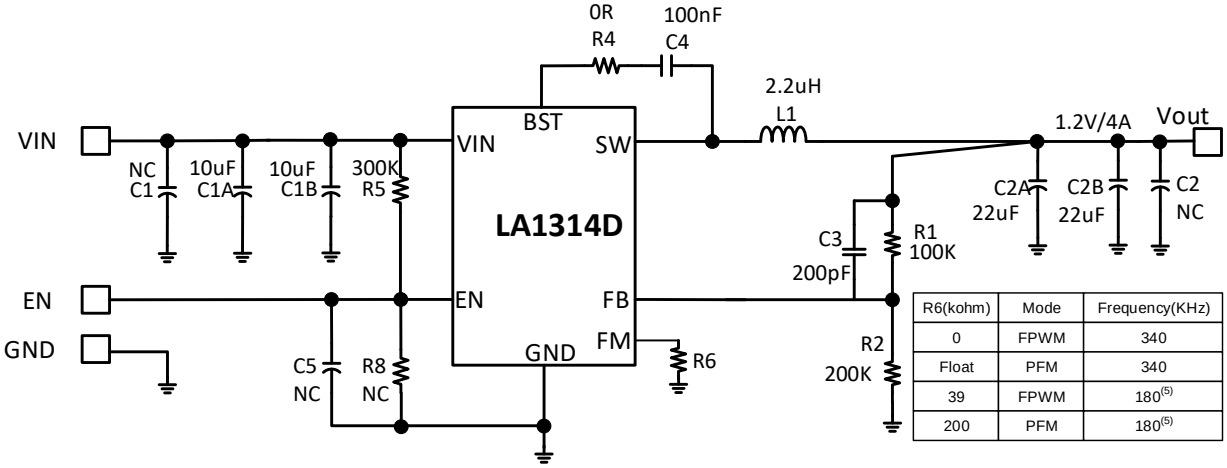
R6(kohm)	Mode	Frequency(KHz)
0	FPWM	340
Float	PFM	340
39	FPWM	180(5)
200	PFM	180(5)

Figure 12. Typical VOUT=2.5V/4A application



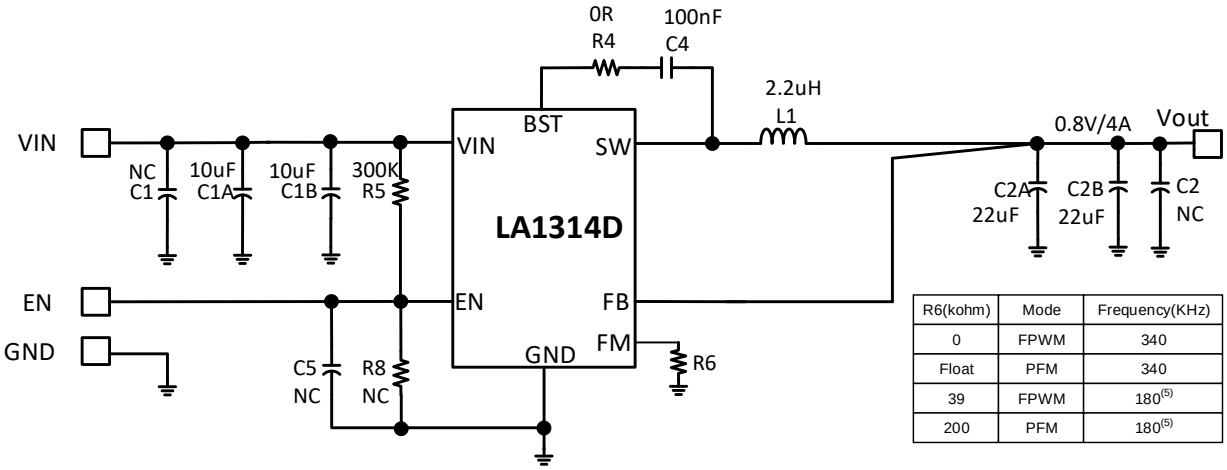
R6(kohm)	Mode	Frequency(KHz)
0	FPWM	340
Float	PFM	340
39	FPWM	180(5)
200	PFM	180(5)

Figure 13. Typical VOUT=1.8V/4A application



R6(kohm)	Mode	Frequency(KHz)
0	FPWM	340
Float	PFM	340
39	FPWM	180(5)
200	PFM	180(5)

Figure 14. Typical VOUT=1.2V/4A application

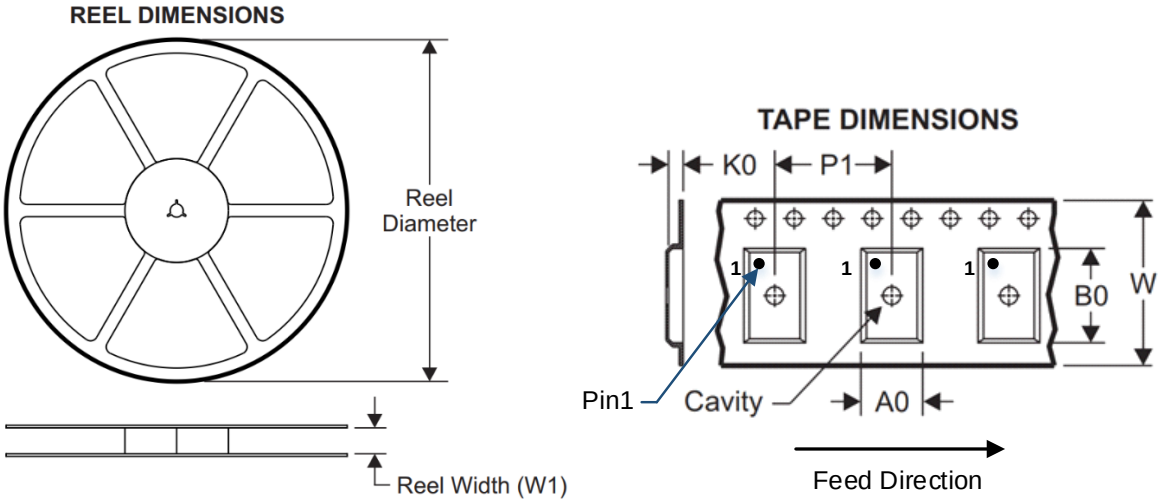


R6(kohm)	Mode	Frequency(KHz)
0	FPWM	340
Float	PFM	340
39	FPWM	180(5)
200	PFM	180(5)

Figure 15. Typical VOUT=0.8V/4A application

Note 5: For 180KHz application, should increase inductor and output capacitor for improving stability performance.

Tape and Reel Information

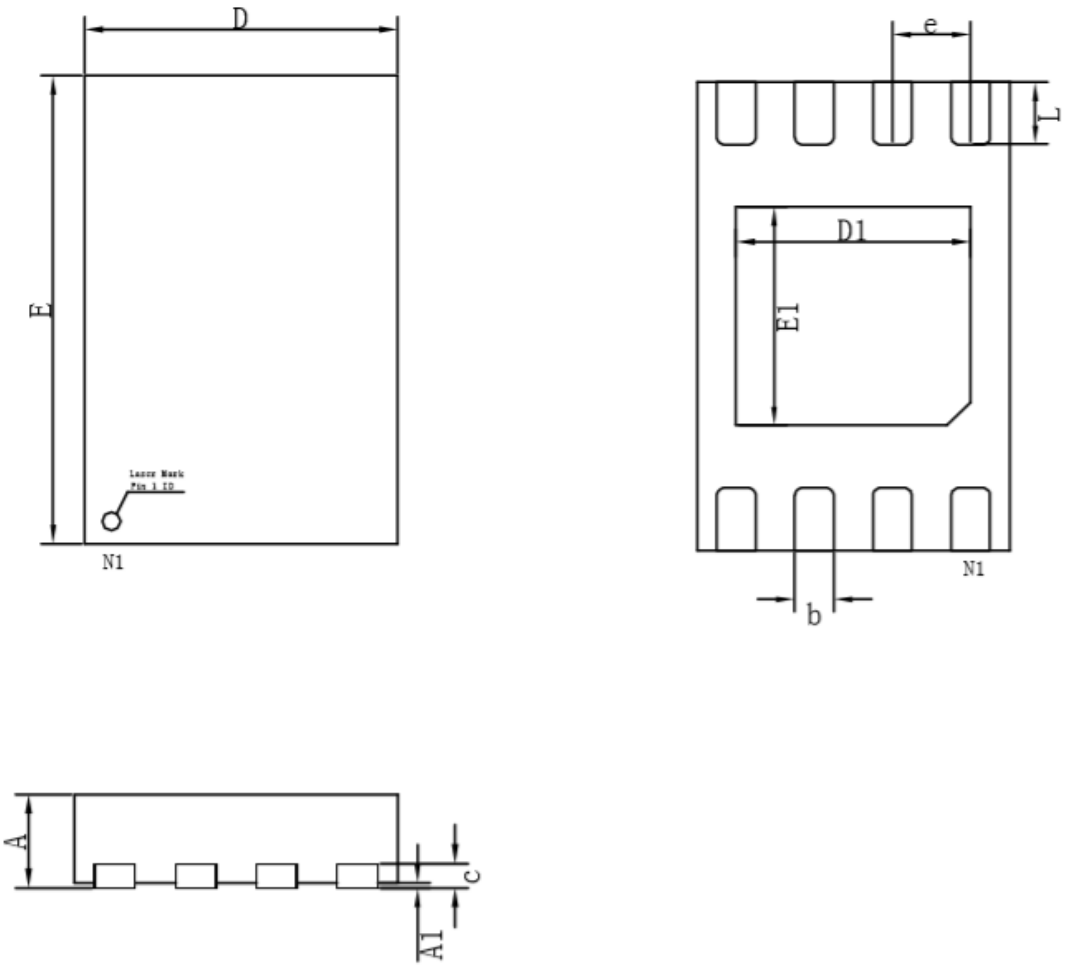


Information

Device	Package Type	Pins	SPQ	Real Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LA1314D	UDFN 2x3-8	8	4000	178	9	2.25	3.25	0.95	4	8

Detail Package Outline Drawing

Package type: UDFN2*3-8



尺寸 / 标注	最小(mm)	标准(mm)	最大(mm)	尺寸 / 标注	最小(mm)	标准(mm)	最大(mm)
A	0.50	0.55	0.60	e		0.50TYP	
A1	0.00	0.03	0.05	E	2.90	3.00	3.05
b	0.20	0.25	0.30	E1	1.30	1.40	1.50
c		0.152REF		D1	1.40	1.50	1.60
D	1.90	2.00	2.05	L	0.30	0.40	0.50