High Efficiency, Fast Response, 2.0A, 18V Input Synchronous Step Down Regulator

General Description

The SY8121B1 is a high efficiency, synchronous step-down DC/DC converter capable of delivering 2A load current. The SY8121B1 operates over a wide input voltage range from 4.5V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8121B1 adopts the instant PWM architecture to achieve fast transient responses for high step down applications. In addition, it operates at pseudo-constant frequency of 1.4MHz to minimize the size of inductor and capacitor.

Ordering Information

SY8121 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8121B1ABC	SOT23-6	----

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 130mΩ/105mΩ
- 4.5~18V Input Voltage Range
- 2A Output Current Capability
- 1.4MHz Switching Frequency Minimize the External Components
- Stable with 10μF C_{OUT} and 1.0μH Inductor
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Forced PWM Operation
- Cycle-by-cycle Peak/Valley Current Limitation
- Hic-cup Mode Output Short Circuit Protection
- Thermal Shutdown with Auto Recovery
- Compact Package SOT23-6

Applications

- Set Top Box
- Portable TV
- DSL Modem
- LCD TV
- IP CAM
- Networking

Typical Application

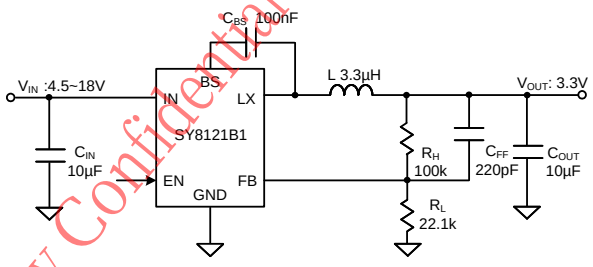


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [μH]	C_{OUT} [μF] 4.7	10	22
1.2	1.0		√	√
	1.5		☆	√
1.8	1.5		☆	√
3.3	2.2		√	√
	3.3		☆	√
5	3.3		√	√
	4.7		☆	√

Note: '☆' means recommended for most applications.

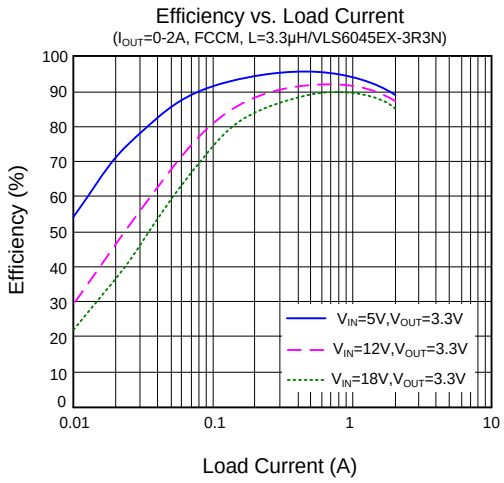
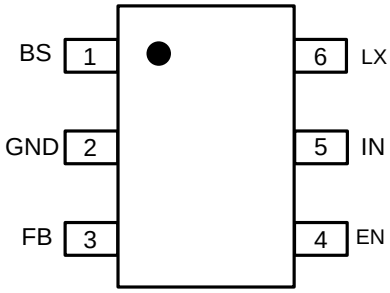


Figure2. Efficiency vs. Load Current

Pin-out (top view)

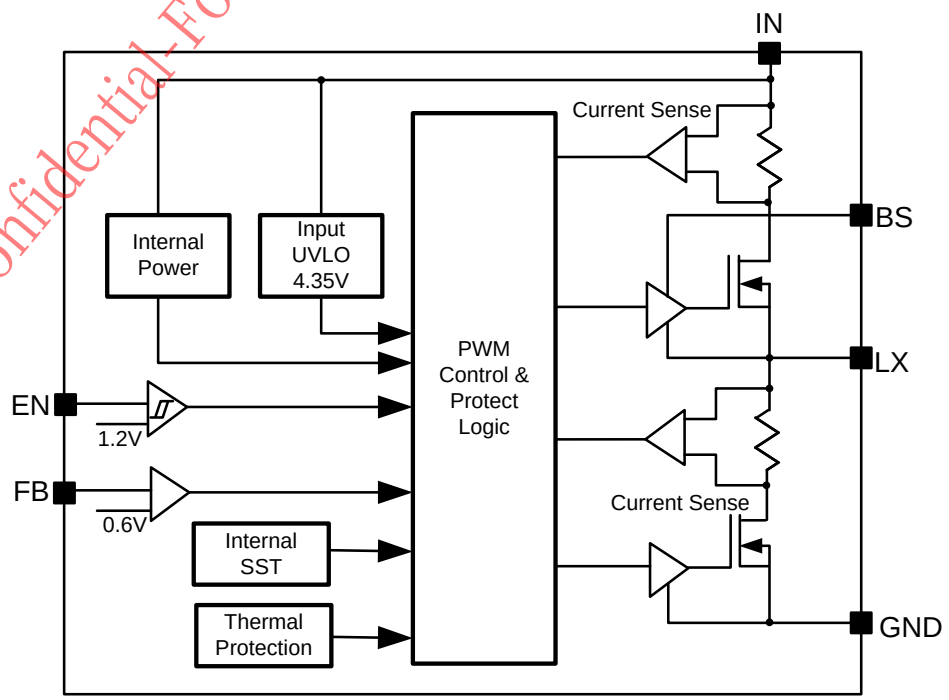


(SOT23-6)

Top mark: **K9*xyz*** (Device code: **K9**, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
GND	2	Power ground pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
EN	4	Enable control. Pull high to turn on. Do not leave this pin floating.
IN	5	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of the inductor.

Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 19V
LX, EN Voltage---------- -0.3V to V_{IN} + 0.3V
FB, BS-LX Voltage---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25℃ SOT23-6, ---------- 1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 100℃/W
θ_{JC} ---------- 25℃/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
Dynamic LX voltage in 10ns duration (Note3) ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 18V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3μH, C_{OUT} = 10μF, T_A = 25℃, I_{OUT} = 1A unless otherwise specified)

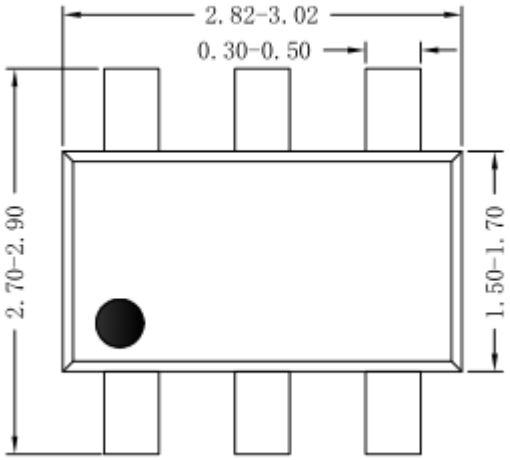
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		18	V
Input UVLO Threshold	V_{UVLO}				4.35	V
Input UVLO Hysteresis	V_{HYS}			0.6		V
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		591	600	609	mV
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET R_{ON}	$R_{DS(ON)1}$			130		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			105		mΩ
EN Rising Threshold	$V_{EN, R}$		1.08	1.2	1.32	V
EN Falling Threshold	$V_{EN, F}$		0.9	1.0	1.1	V
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			150		ns
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		300		μs
Soft-start Time	t_{SS}	V_{OUT} from 0 to 100%		1		ms
Switching Frequency	f_{SW}	I_{OUT}=1A		1.4		MHz
Top FET Current Limit	$I_{LMT,TOP}$		3			A
Bottom FET Current Limit	$I_{LMT,BOT}$		2			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$		1			A
Output Under Voltage Protection Threshold	V_{UVP}			0.33		V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			200		μs
UVP Hiccup On Time	$t_{UVP,ON}$			1.4		ms
UVP Hiccup Off Time	$t_{UVP,OFF}$			5.2		ms
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

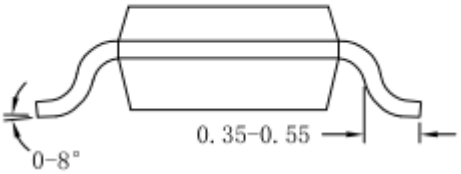
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a 2-oz two-layer Silergy evaluation board. Paddle of SOT23-6 package is the case position for SY8121B1 θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

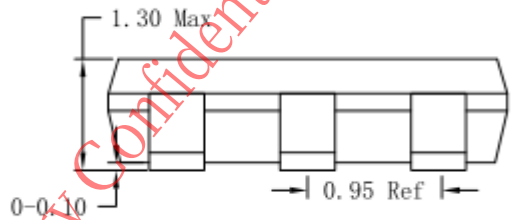
SOT23-6 Package Outline & PCB Layout Design



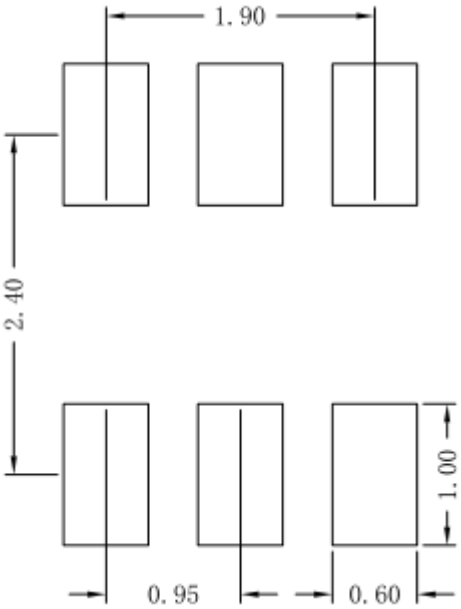
Top View



Side View



Side View

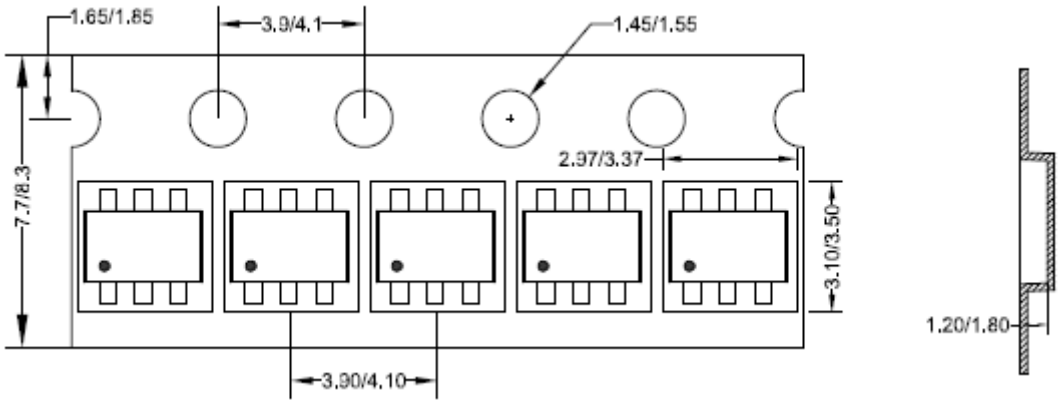


Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

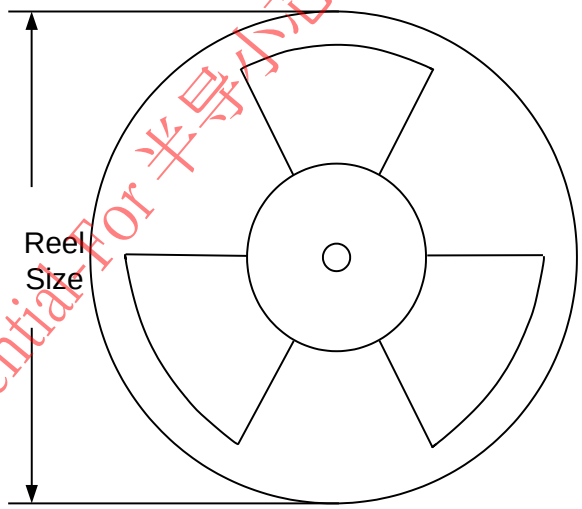
Taping & Reel Specification

1. Taping orientation for package



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA