# JW3312

**Battery Protection IC For 3-5 Cells Battery Pack With Automatic Balance**

*Parameters Subject to Change Without Notice*

## DESCRIPTION

JW®3312 is a battery protection IC for the3~5cellsrechargeable lithium-ion battery pack.By using cascadeconnection, it is also possible to protect 6 or more cells battery pack.

JW3312integrates high-accuracy voltage detection circuits, which realizes multiple protection functions including overcharge, overdischarge, overcurrent, over-temperature and VC5~VC0 pins open-wire.

## FEATURES

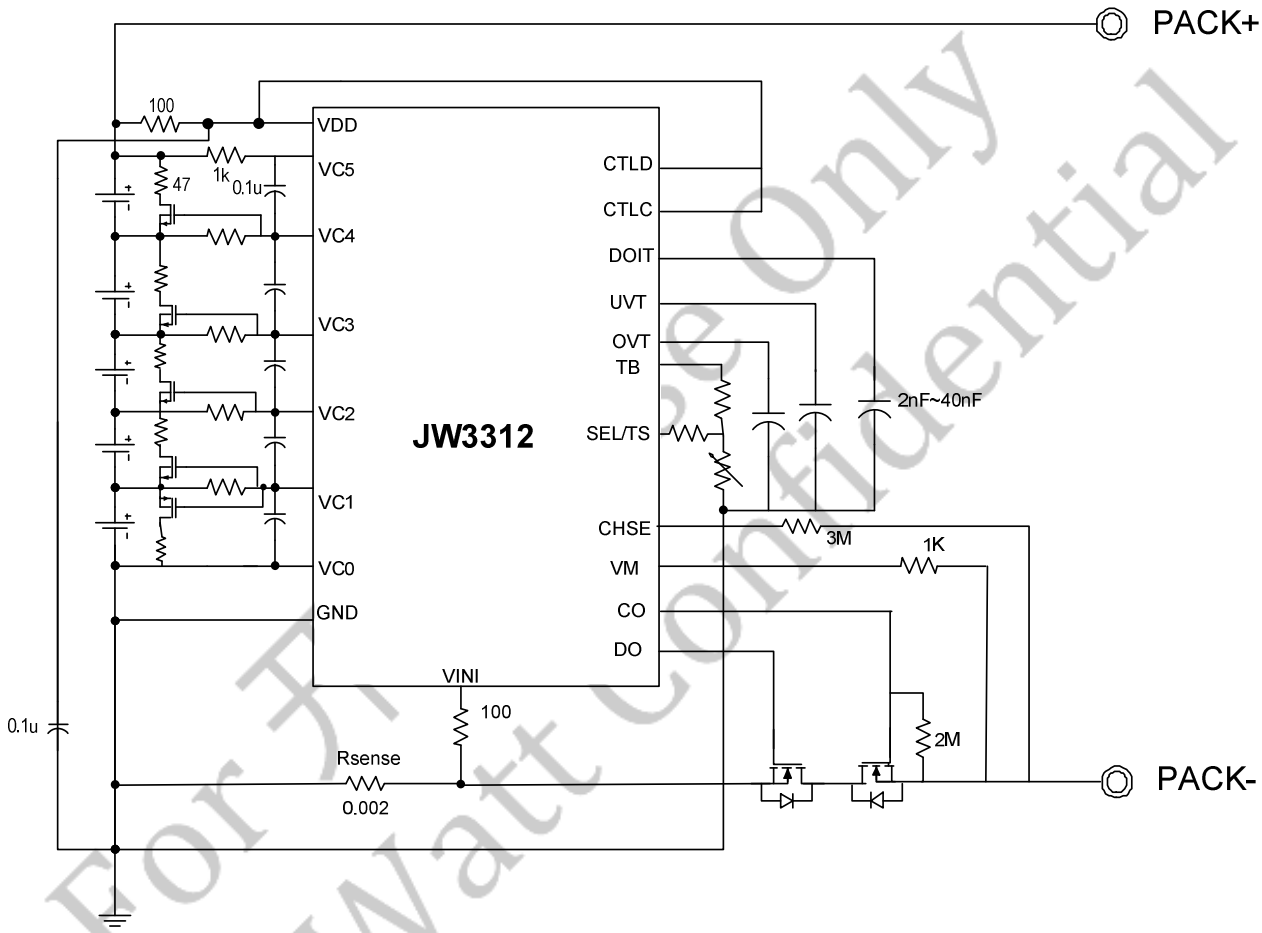
- Input voltage is high to 40V
- Monitor 3~5 series battery pack
- High-accuracy voltage detection for each cell
  Overcharge detection voltage:
  3.55~4.6V (50mV step) Accuracy ±20 mV
  (-40℃~85℃) Accuracy ±30 mV
  Overcharge release hysteresis:
  0V/0.1~0.4V (20mV step)
  Overdischarge detection voltage:
  2.0~3.2V (50mV step) Accuracy ±80 mV
  Overdischarge release hysteresis:
  0V/0.1~1V (60mV step)
- Discharge overcurrent detection in 3-step
  1st Discharge overcurrent detection voltage:
  0.025~0.25V (15mV step) Accuracy ±10mV
  2nd Discharge overcurrent detection voltage:
  0.05~0.5V (15mV step) Accuracy ±10mV
  Short circuit detection voltage:
  0.1~1.6V (100mV step) Accuracy ±40mV
- Charge overcurrent detection voltage
  -0.015~-0.160V (10mV step) Accuracy ±10mV
- Fixed internally:
  Load short circuit detection delay time
  100us, 200us, 300us,400us optional
  Charge overcurrent detection delay time
  0.1s, 1s optional
- Programmable by external capacitor:
  Discharge overcurrent detection delay time,
  1st: 0.1s~2s 2nd: (0.1~2s)×0.1
  Overdischarge detectiondelay time,
  0.1s~3s
  Overcharge detection delay time
  0.1s~5s
- High-accuracy battery temperature detection
- Provide passive balance
- Provide VC5~VC0 open-wire detection
- Wide range of operation voltage4.5V to 35V
- Wide range of operation temperature
  -40°C to +85°C
- Low current consumption (T=25°C)
  During full power 15μA. (From chip GND)
  During sleep mode 2μA.
  During shutdown 350nA.
- 20-Pin TSSOP

## APPLICATIONS

- Rechargeable lithium-ion battery pack
- Power tool
- UPS backup battery

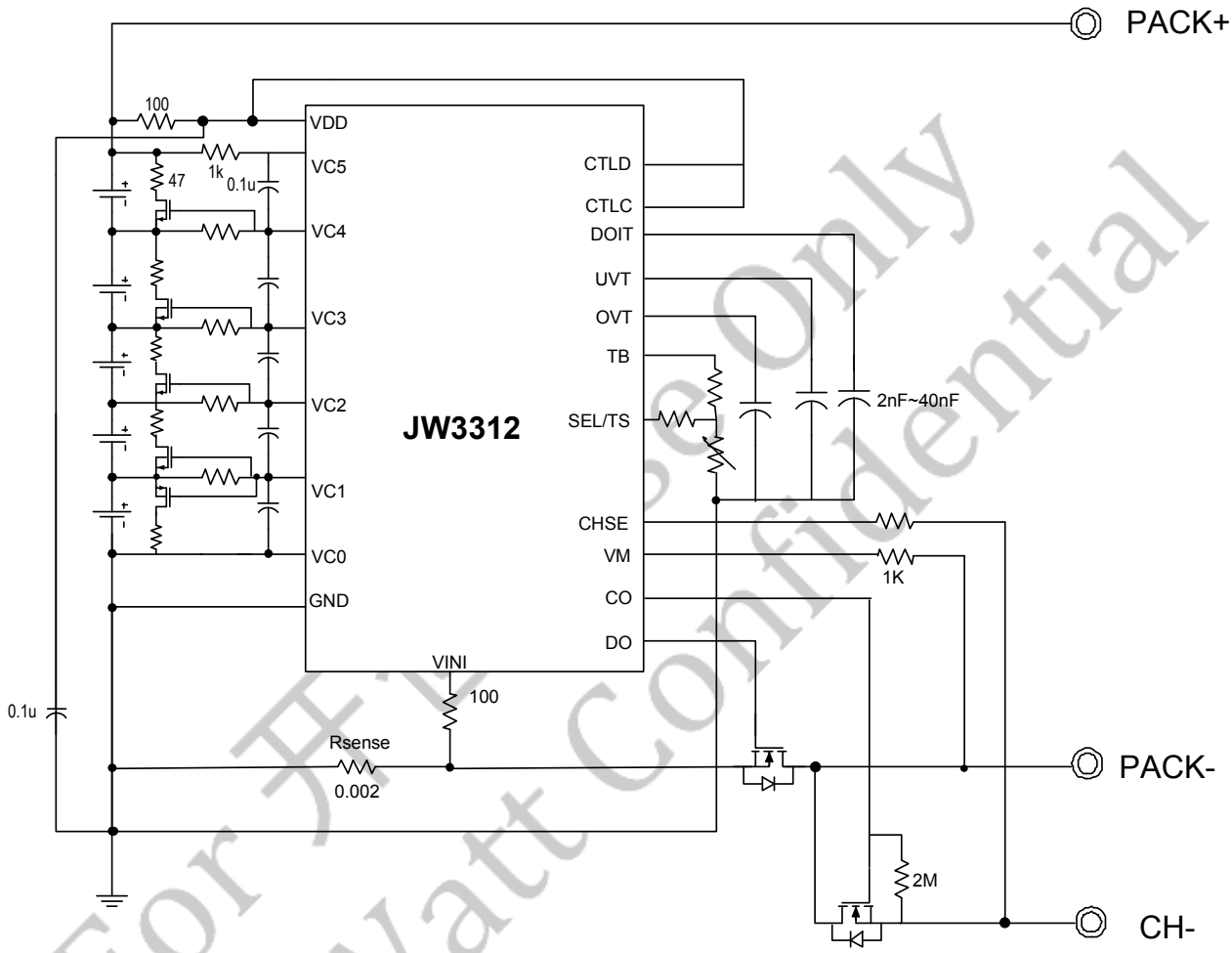
## TYPICAL APPLICATION

One PACK- PORT



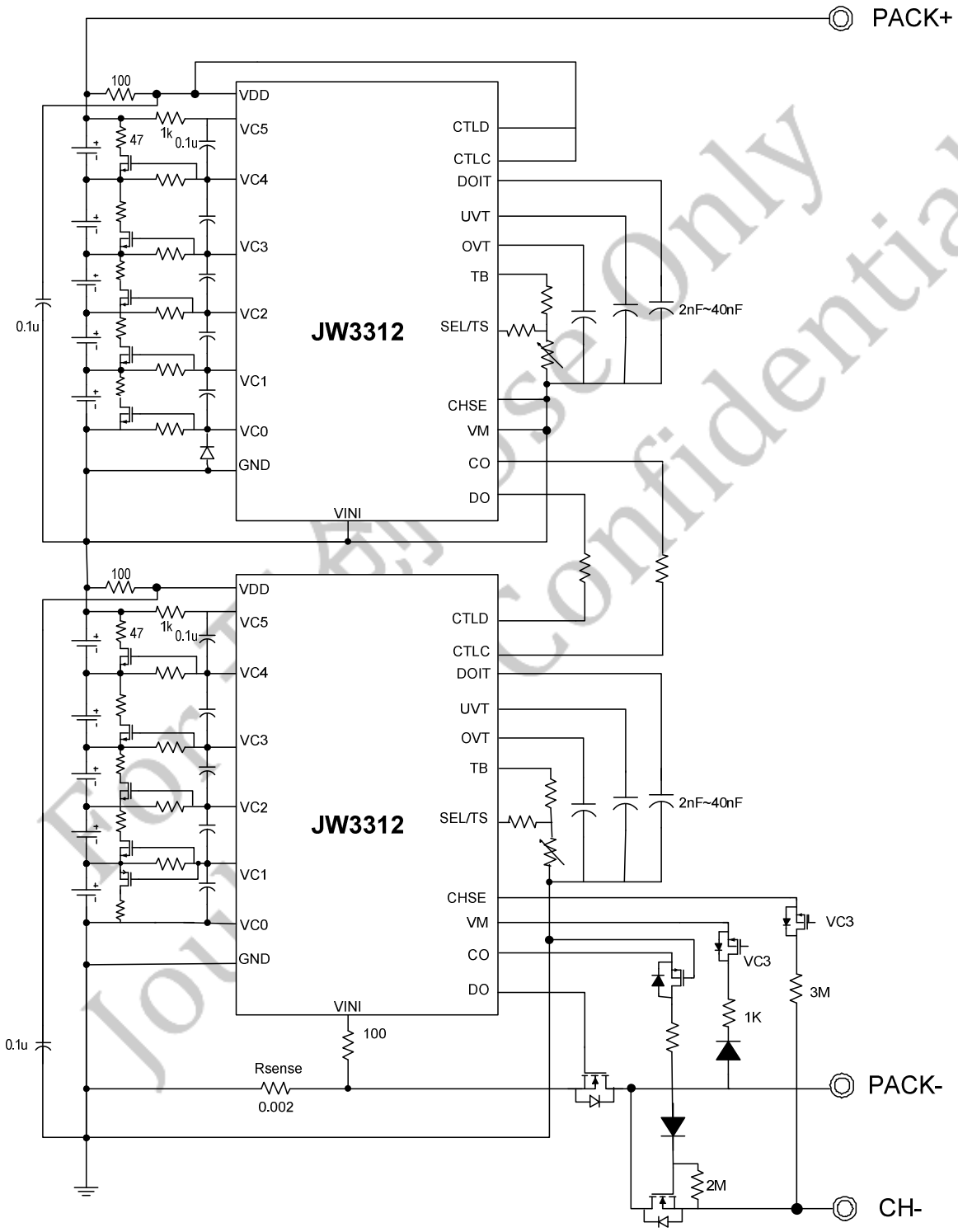
## TYPICAL APPLICATION

PACK- CHG- separated



## TYPICAL APPLICATION

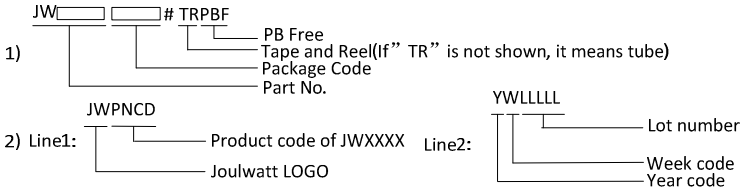
Cascade application



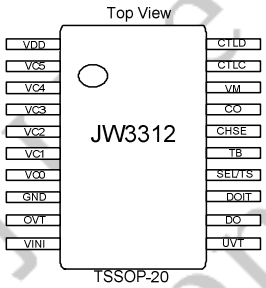
## ORDER INFORMATION

| DEVICE[1)] | PACKAGE | TOP MARKING[2)] |
|---|---|---|
| JW3312TSSOPE#TRPBF | TSSOP20 | JW3312<br>YWLLLLL |

**Notes:**




## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATING[1)]

VDD,VC5,VC4,VC3,VC2,CHSE,.....-0.3V to +40V
VC1.....-0.3V to +20V
VC0.....-0.3V to +6V
CTLD,CTLC.....-0.3Vto VDD+0.7V
DO.....-0.3V to +12V
CO, VM.....Max(-18,VDD-40) to VDD
UVT, SEL/TS,DOIT,VINI, OVT, TB..... -0.3V to +6V
Battery cell voltage.....-0.3V to 24V
Junction Temperature[2)3)]..... 150ºC
Lead Temperature ..... 260ºC
Storage Temperature .....-65ºC to +150ºC

## RECOMMENDED OPERATING CONDITIONS

Junction Temperature ($T_J$)..... -40ºC to 125ºC

## THERMAL PERFORMANCE[4)]

| | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| TSSOP20 | 98.4 | 37ºC/W |

**Note：**

**1)** Exceeding these ratings may damage the device.

**2)** The JW3312guarantees robust performance from -40°Cto 150°C junction temperature.The junction temperature range specification is assured by design,characterization and correlation with statistical process controls.

**3)** Continuous operation over the specified absolutemaximum operating junction temperature may damagethe device.

**4)** Measured on JESD51-7, 4-layer PCB

## ELECTRICAL CHARACTERISTICS

*TA = 25ºC, unless otherwise stated.*

| Item | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ***Power supply*** | | | | | | |
| Operation voltage betweenVDD pin and GND pin | $V_{DSOP}$ | | 4.5 | | 35 | V |
| Power-on reset threshold | $V_{PON}$ | | | $V_{PDOWN}$ +0.3 | | V |
| Shutdown threshold | $V_{PDOWN}$ | $V_{PDOWN}$ = 4.5 | $V_{PDOWN}$-6% | $V_{PDOWN}$ | $V_{PDOWN}$+6% | V |
| Current consumption during full power | $I_{FP}$ | | | 15 | | μA |
| Current consumption during sleep | $I_{SLEEP}$ | | | 2 | | μA |
| Current consumption during shutdown | $I_{SHUTDOWN}$ | | | 350 | | nA |
| ***Voltage/Current Protections Threshold Voltage*** | | | | | | |
| Overcharge detection voltage | $V_{OC}$ | | $V_{OC}$ -0.02 | $V_{OC}$ | $V_{OC}$ +0.02 | V |
| Overcharge release voltage | $V_{OCL}$ | | | $V_{OCL}$ | | V |
| Overdischarge detection voltage | $V_{OD}$ | | $V_{OD}$ -0.08 | $V_{OD}$ | $V_{OD}$ +0.08 | V |
| Overdischarge release voltage[5] | $V_{ODH}$ | | | $V_{ODH}$ | | V |
| 1st Discharge overcurrent detection voltage | $V_{DOI1}$ | | $V_{DOI1}$-10 | $V_{DOI1}$ | $V_{DOI1}$+10 | mV |
| 2nd Discharge overcurrent detection voltage | $V_{DOI2}$ | | $V_{DOI2}$-10 | $V_{DOI2}$ | $V_{DOI2}$+10 | mV |
| Load short circuit detection voltage | $V_{SHT}$ | | $V_{SHT}$ -40 | $V_{SHT}$ | $V_{SHT}$ +40 | mV |
| Charge overcurrent detection voltage | $V_{COI}$ | T=-40ºC to 85 ºC | $V_{COI}$-10 | $V_{COI}$ | $V_{COI}$+10 | |
| Discharge detection threshold | $V_{TH\_DSG}$ | | 2.5 | 4 | 7.5 | mV |
| ***Temperature Protection Threshold Voltage*** | | | | | | |
| Discharging detection threshold | $V_{TH\_DSG}$ | | 2.5 | 4 | 7.5 | mV |
| Charging over temperature protection threshold | $V_{COT}$ | | 28.58% | 29.58% | 30.58% | $V_{TB}$ |
| Charging over temperature protection hysteresis[5] | $V_{COTH}$ | | | 3.33% | | $V_{TB}$ |
| Discharging over temperature protection threshold | $V_{DOT}$ | | 17.33% | 18.33% | 19.33% | $V_{TB}$ |

| | | | | | | |
|---|---|---|---|---|---|---|
| Discharging over temperature protection hysteresis[5] | $V_{DOTH}$ | | | 5% | | $V_{TB}$ |
| Charging under temperature protection threshold | $V_{CUT}$ | | 72.33% | 73.33% | 74.33% | $V_{TB}$ |
| Charging under temperature protection hysteresis[5] | $V_{CUTH}$ | | | 4.58% | | $V_{TB}$ |
| Discharging under temperature protection threshold | $V_{DUT}$ | | 86.08% | 87.08% | 88.08% | $V_{TB}$ |
| Discharging under temperature protection hysteresis[5] | $V_{DUTH}$ | | | 6.25% | | $V_{TB}$ |
| Chip over temperature protection threshold[5] | $T_{CHIP}$ | | | 150 | | ºC |
| Chip over temperature protection release threshold[5] | $T_{CHIPR}$ | | | 125 | | ºC |
| ***Voltage/Current Protections Delay Time*** | | | | | | |
| Detection period time for OV, UV | $t_{DETV}$ | | | 0.5 | | S |
| Overcharge detection delay time | $t_{OC}$ | | $t_{OC}$ -25% | $t_{OC}$ | $t_{OC}$+25% | S |
| Overdischarge detection delay time | $t_{OD}$ | | $t_{OD}$ -25% | $t_{OD}$ | $t_{OD}$ +25% | S |
| Load short circuit detection delay time | $t_{SHT}$ | | $t_{SHT}$ -150 | $t_{SHT}$ | $t_{SHT}$ +150 | μS |
| DOIT/UVT pin current | $I_{DOIT}$ | | 7.7 | 8 | 8.3 | μA |
| 1st Discharge overcurrrentdetection delay time | $t_{DOI1}$ | $C_{DOIT}$ =2nF | 0.07 | 0.1 | 0.13 | S |
| DOIT pin short detected 1st discharge overcurrent detection delay time | $t_{DOI1S}$ | | 1.4 | 2 | 2.6 | S |
| DOIT pin open detected 1st discharge overcurrent detection delay time | $t_{DOI1O}$ | | 0.07 | 0.1 | 0.13 | S |
| Charge overcurrent detection delay time | $t_{COI}$ | | | 1 | | s |
| UVT pin short detected over dischargedetection delay time | $t_{UVS}$ | | 2.4 | 3 | 3.6 | s |
| UVT pin open detected over discharge detection delay time | $t_{UVO}$ | | 0.07 | 0.1 | 0.13 | S |
| OVT pin short detected over | $t_{OVS}$ | | 4.4 | 5 | 5.6 | S |

| | | | | | | |
|---|---|---|---|---|---|---|
| dischargedetection delay time | | | | | | |
| OVT pin open detected over discharge detection delay time | $t_{OVO}$ | | 0.07 | 0.1 | 0.13 | S |
| ***Temperature Protection Delay Time*** | | | | | | |
| Temperature detection period time | $t_{DETT}$ | | | 2 | | S |
| Charge over temperature detection delay time | $t_{COT\_DELAY}$ | | 3.4 | 4 | 4.6 | S |
| Charge under temperature detection delay time | $t_{CUT\_DELAY}$ | | 3.4 | 4 | 4.6 | S |
| Dischargeover temperature detection delay time | $t_{DOT\_DELAY}$ | | 3.4 | 4 | 4.6 | S |
| Dischargeunder temperature detection delay time | $t_{DUT\_DELAY}$ | | 3.4 | 4 | 4.6 | S |
| Temperature protection release delay time | $t_{TREL\_DELAY}$ | | 3.4 | 4 | 4.6 | S |
| ***Balance Function*** | | | | | | |
| Level-1 Bleeding threshold voltage | $V_{BAL1}$ | | $V_{BAL1}$-0.025 | $V_{BAL1}$ | $V_{BAL1}$+0.025 | V |
| Level-2 bleeding threshold voltage | $V_{BAL2}$ | | $V_{BAL2}$-0.025 | $V_{BAL2}$ | $V_{BAL2}$+0.025 | V |
| Level-1 allowance bleeding deviation voltage between high voltage battery and low voltage battery | $\triangle V_{B\_ALLOW}$ | | 15 | 40 | 65 | mV |
| Bleeding current[5] | $I_{BAL}$ | | | 50 | | Ω |
| Balance period time | $t_B$ | | | 0.6 | | S |
| Bleeding delay time[5] | $t_{BAL\_DELAY}$ | | | 100 | | mS |
| Odd cells bleeding time[5] | $t_{B\_ODD}$ | | | 200 | | mS |
| Even cells bleeding time[5] | $t_{B\_EVEN}$ | | | 200 | | mS |
| Cell balancing relaxation time before cell voltage measured[5] | $t_{B\_RELAX}$ | | | 100 | | mS |
| ***VCN Open-Wire Detection*** | | | | | | |
| VCN open-wire detection cycle | $t_{OPEN}$ | | | 2 | | S |
| ***3/4/5 Cells Application Configuration*** | | | | | | |
| SEL/TS pin source current | $I_{SEL}$ | | | 5 | | μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 Cells configuration comparator threshold voltage | $V_{SEL1}$ | | | 250 | | mV |
| 5 Cells configuration comparator threshold voltage | $V_{SEL2}$ | | | 750 | | mV |
| ***CTLx Control*** | | | | | | |
| CTLD/CTLC sink current | $I_{CTL}$ | | | 1 | | μA |
| CTLD/CTLCchange voltage | $V_{CTL}$ | | | $V_{DD}$-1 | | V |
| CTLC/CTLD response time | $t_{CTL}$ | | | 100 | | ms |
| ***Output Voltage*** | | | | | | |
| CO output voltage L | $V_{COL}$ | | 0 | High_Z | 0.5 | V |
| CO output voltage H | $V_{COH}$ | | | 12(max) | | V |
| DO output voltage L | $V_{DOL}$ | | 0 | 0 | 0.5 | V |
| DO output voltage H | $V_{DOH}$ | | | 12(max) | | V |
| ***Input Current*** | | | | | | |
| VC5 pin current | $I_{VC4}$ | | | | 2.5 | μA |
| VC4~VC1 pin current | $I_{VC9\sim1}$ | | -1.0 | 0 | 1.0 | μA |
| VC0 pin current | $I_{VC0}$ | | | | 2.5 | μA |
| ***Output Current*** | | | | | | |
| CO pin maximum source current[5)] | $I_{COH}$ | | | 1 | | mA |
| DO pin maximum source current[5)] | $I_{DOH}$ | | | 1 | | mA |
| DO pin maximum sink current[5)] | $I_{DOL}$ | | | 100 | | mA |
| ***0V battery charge function*** | | | | | | |
| 0V battery charge starting threshold voltage | $V_{0CHA}$ | | 2.5 | | | V |
| 0V battery charge CO pin source current | $I_{0CHA}$ | | | 3 | | μA |

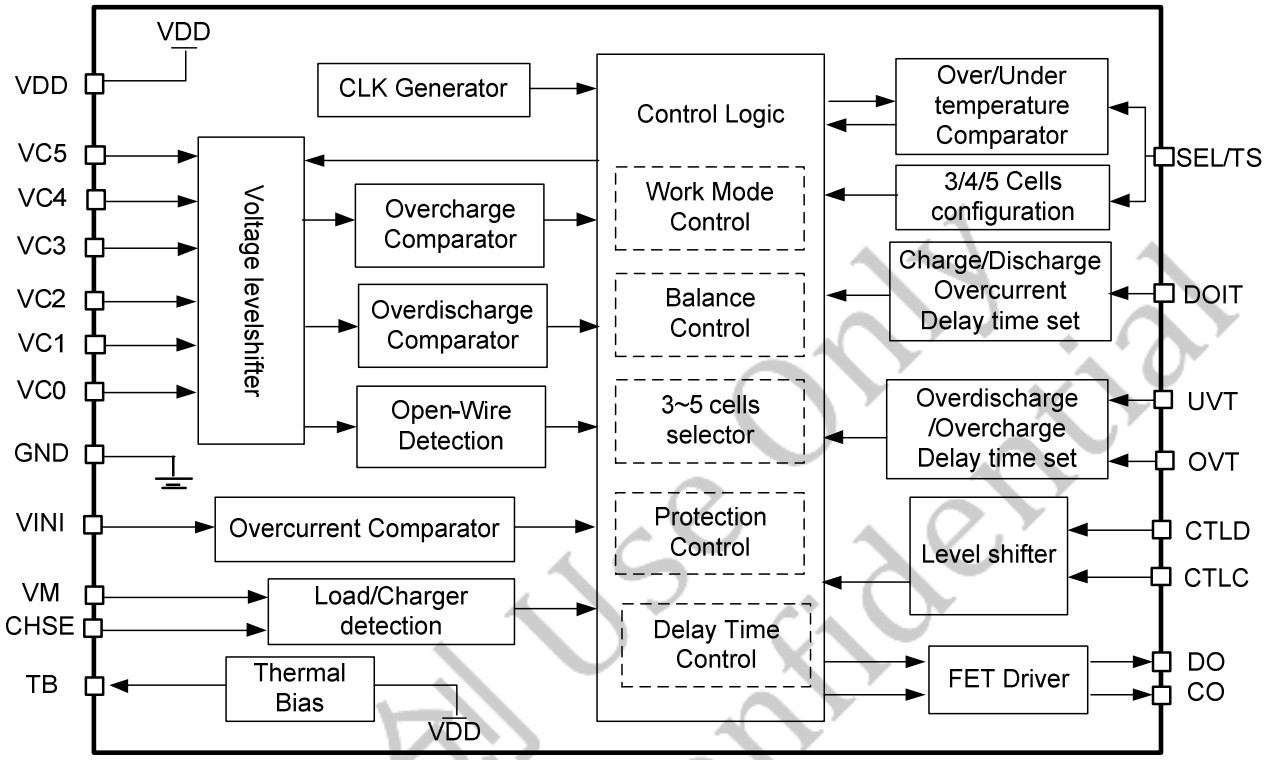
***Notes:***

5) Guaranteed by design.

## PIN DESCRIPTION

| Pin No. | Name | Description |
|---|---|---|
| 1 | VDD | Input pin for positive power supply,<br>Connection pin for battery5's positive voltage |
| 2 | VC5 | Connection pin for battery5's positive voltage |
| 3 | VC4 | Connection pin for battery 5's negative voltage,<br>Connection pin for battery 4's positive voltage |
| 4 | VC3 | Connection pin for battery 4's negative voltage,<br>Connection pin for battery 3's positive voltage |
| 5 | VC2 | Connection pin for battery 3's negative voltage,<br>Connection pin for battery 2's positive voltage |
| 6 | VC1 | Connection pin for battery 2's negative voltage,<br>Connection pin for battery 1's positive voltage |
| 7 | VC0 | Connection pin for battery 1's negative voltage, |
| 8 | GND | Connection pin for battery 1's negative voltage,<br>Input pin for negative power supply |
| 9 | OVT | Capacitor connection pin for delay for overcharge detection |
| 10 | VINI | Pin for voltage detection between VINI pinand GND pin |
| 11 | UVT | Capacitor connection pin for delay for over discharge detection |
| 12 | DO | Gate connection pin for discharge control MOSFET |
| 13 | DOIT | Capacitor connection pin for delay for charge and discharge overcurrent detection |
| 14 | SEL/TS | Thermal sense input<br>This is a dual-purposePin. Also asSelect terminal for 3/4/5 cells application |
| 15 | TB | Thermal bias output |
| 16 | CHSE | Pin for charger detection |
| 17 | CO | Gate connection pin for charge control MOSFET |
| 18 | VM | Pin for voltage detection between VM pinand GND pin |
| 19 | CTLC | CO pin control input from the unit above for cascaded operation; |
| 20 | CTLD | DO pin control input from the unit above for cascaded operation; |

## BLOCK DIAGRAM



# FUNCTIONAL DESCRIPTION

## Normal Status

In the JW3312, both of CO pin and DO pin output “H” level voltage when all battery voltages are between overdischarge detection voltage ($V_{OD}$) and overcharge detection voltage ($V_{OC}$), and the VINI pin's voltage is lower than 1$^{st}$discharge overcurrent detection voltage ($V_{DOI1}$). This is the normal status. At this time, the charge and discharge MOSFETs are on.

## Overcharge Status

JW3312 checks for cell over voltage once per detection time period ($T_{DETV}$). When any battery voltageincreases to $V_{OC}$ or more for longer than the overcharge detection delay time ($t_{OC}$), the CO pin outputs “High_Z”. Since the CO pin pulled down to the CHA- voltage by an external resistor, the charge MOSFET is turned off to stop charging. This is the overcharge status.

The overcharge status is released if one of the conditions mentioned below is satisfied:

(1) All batteryvoltagedrops to overcharge release voltage ($V_{OCL}$) or less.

(2) The VINI pin voltage is higher than $V_{TH\_DSG}$ during discharging and all batteryvoltagedrops to overcharge voltage ($V_{OC}$) or less.

## Overdischarge Status

JW3312 checks for cell under voltage once per detection time period ($T_{DETV}$). When any voltage of the batteries decreases to the level of $V_{OD}$ or less for longer than the overdischarge detection delay time ($t_{OD}$), the DO pin outputs “L” voltage. The discharge MOSFET is turned off and it stops discharging. This is the overdischarge status.

The VM pin is pulled down to the GND level via $R_{VMS}$ internally.

The overdischarge status is released if either condition mentioned below is satisfied:

(1) The VM pin voltage is 1V or less, and all battery voltages increase to overdischarge release voltage ($V_{ODH}$) or more.

(2) Any battery voltage gets to be higher than $V_{OC}$ or more for longer than $t_{OC}$.

## Discharge Overcurrent Status

In the JW3312, if the VINI pin voltage increases to the level of $V_{DOI}$ or morefor longer than the discharge overcurrent detection delay time ($t_{DOI}$), the DO pin outputs “L” voltage. The discharge MOSFET is turned off and it stops discharging.This is the discharge overcurrent status.

The VM pin is pulled down to the GND level via $R_{VMS}$ internally.

JW3312 has three levels for discharge overcurrent detection ($V_{DOI1}$, $V_{DOI2}$, $V_{SHT}$). The JW3312 actions against load short circuit detection voltage ($V_{SHT}$) are as well in $V_{DOI}$.

The discharge overcurrent status is released if the following condition is satisfied.

(1) The VM pin voltage gets 1V or less.

## Charge Overcurrent Status

In the JW3312, if the VINI pin voltage decreases to the level of $V_{COI}$ or lower for longer than the charge overcurrent detection delay time ($t_{COI}$), the CO pin outputs “Hi-z”. The charge MOSFET is turned off and it stops charging.This is the charge overcurrent status.

The CHSE pin is pulled up to the 5V regulatorvia resistor internally.

Charge overcurrent protection will be released when we disconnect the charger.

## Delay Time Setting

In the discharge over current and over discharge detection, users are able to set the delay time by a current in JW3312 and an external capacitor.

Take the discharge overcurrentdetectionfor example, when the VINI pin voltage gets $V_{DOI1}$ or more, JW3312 starts charging to the DOIT pin's capacitor ($C_{DOIT}$) via the DOIT pin's output current ($I_{DOIT}$). After a certain period, the DO pin outputs “L” voltage. This period is the 1$^{st}$dischageovercurrent detection delay time ($t_{DOI1}$), which is calculated using the following equation.

$t_{DOI1}$[s]= n × ΔV× $C_{DOIT}$[nF] / $I_{DOIT}$ [uA]

= 400(typ.) × $C_{DOIT}$[nF] /8[uA] (typ.)

= 50[MΩ](typ.) × $C_{DOIT}$[nF]

In case $C_{DOIT}$=2nF, $t_{DOI1}$ is calculated as follows.

$t_{DOI1}$ [s] = 50[MΩ](typ.)× 2[nF] = 0.1 [s] (typ.)

The 2$^{nd}$ discharge overcurrent detection delay time ($t_{DOI2}$) is calculated as below.

$t_{DOI2}$=$t_{DOI1}$×0.1

The function of overdischarge detection delay time is same to the discharge overcurrent detection delay time.

The function of overcharge detection delay time is same to the discharge overcurrent detection delay time.

The loadshort circuit detection delay time are fixed internally.

## Fault Detection on DOIT& UVT

To set the dischargeovercurrent detection delay time and theoverdischarge detection delay time, a capacitor is connected between DOIT/UVT pin and GND pin.

Take the discharge overcurrent for example. If the discharge overcurrent is detected and the DOIT pin is shorted to ground, $t_{DOI1}$ is automatically changed to the DOIT pin short detected 1$^{st}$ discharge overcurrent detection delay time ($t_{DOI1S}$).

In the same manner, if the discharge overcurrent is detected and the DOIT pin is floating, $t_{DOI1}$ is automatically changed to the DOIT pin open detected 1$^{st}$ discharge overcurrent detection delay time ($t_{DOI1O}$).

The fault detection function of pin UVT is similar to the pin DOIT.

## Temperature Protection

When the VINI pin voltage is bigger than $V_{TH\_DSG}$, the battery pack is regarded as in discharging status. Otherwise, the battery pack is regarded as in charging status.

The JW3312do the temperature detection every $t_{DETT}$, see figure 1 for temperature detection timing chart. In normal status, the JW3312 continuously turns on TB output for $t_{EFF\_DETT}$ every $t_{DETT}$. When the TB output turns on, the external temperature is monitored.

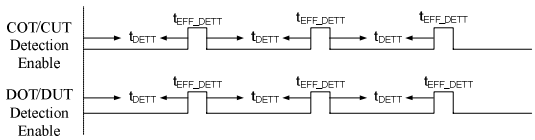



Figure 1 temperature detection timing

When the temperature of battery pack increases, the voltage of the TS pin decreases. Once the battery temperature is over the Charging/Discharging OverTemperature Threshold and the state continues for $t_{COT\_DELAY}$, JW3312 shuts down both the charge and discharge MOSFETs. This status is released only when the battery temperature goes down.

When the battery pack temperature becomes lower than $T_{CUT}$ in charging status and the state continues for $t_{CUT\_DELAY}$, the charging and discharging FETs is turned off to stop charging and discharging. The charging under-temperature status is released only when the battery pack temperature becomes higher.

When the battery pack temperature becomes lower than $T_{DUT}$ in discharging status and the state continues for $t_{DUT\_DELAY}$, the charging and discharging FETs is turned off to stop charging and discharging. The discharging under-temperature status is released only when the battery pack temperature becomes higher.

he CTLC/CTLD pin is used for cascaded operation. When any error is detected such as over-charge, over-discharge,open-wire in the upper unit, the CO/DO pin signal are passed down to the CTLC/CTLD pinof the lower unit to control charging/discharging.

When the CTLC/CTLD pin of the top cell isdirectly connected to VDD pin, JW3312 works normally. If the CTLC/CTLD pin of the top cell is connected to VDD pin via external 2M resistor, the CO/DO pin voltage is forced to be “L”. As a result, JW3312 enters the charge/discharge disable mode and the charge/discharge MOSFET is forced off.

External FET’s state by CTLx pins

| CTLC pin | External FET for CO pin |
|---|---|
| GND | High Z |
| No connection | High Z |
| VDD | ON (normal operation) |

| CTLD pin | External FET for DO pin |
|---|---|
| GND | Forced OFF |
| No connection | Forced OFF |
| VDD | ON (normal operation) |

## Operation Modes

JW3312 has twooperation modes: Full power mode, and Sleep mode.

For Full power mode, JW3312 checks for over-voltage, overdischarge-voltage events and over-temperature every detection period. Besides, over-current events are checked continuously. These safety events decide the status of the charge and discharge MOSFETs. The typical current consumption is 15uA.

JW3312 enters Sleep mode after entering over-discharge status, over-temperature status, under-temperature status or open wire status.The typical current consumption is lower down to be 2uA at sleep mode.

For the other case, JW3312 only waits for temperature events or open wire events releasing.

JW3312 enters Shutdown mode when VDD pin voltage becomes lower than $V_{PDOWN}$. During this mode, JW3312 does not check for any safety events. The charge and discharge MOSFET are both off. The typical current consumption is as low as 350nA.

## Balance Function

JW3312 provides cells’ balance function to balance the cells’ capacity in a battery pack. When any cell voltage is higher than Level-1 bleeding threshold voltage$V_{BAL1}$, and the cell voltage is higher than the lowest cell$\triangle V_{B_ALLOW}$, theoff-chip balance will be turn on and provide about 100mA bleeding current.
Odd-even balance strategy is adopted. The balance period time is 600mS. The first 100mS is used for over/under voltage detection. The second 200mS is used for the odd cells bleeding that satisfy the balance conditions. The

third 200mS is used for the even cellsbleeding that satisfy the balance conditions. The last 100mS is cell balancing relaxation time before cell voltage measured

When the JW3312 is used in extended condition, to avoid the unbalance between IC1 and IC2, the JW3312 provide level-2 balance function.If all the five cell voltage exceed the Level-2 bleeding threshold voltage $V_{BAL2}$, the external discharge MOS turn on.

The balance exitsif one of the conditions mentioned below is satisfied:

(1) When all voltages of VC1, (VC2-VC1), (VC3-VC2), (VC4-VC3) and (VC5-VC4) are lower $V_{BAL1}$, or higher than VBAL1 and Lower than $V_{BAL2}$, all the external balance discharge circuits will not work.

(2) When any battery voltage is higher than $V_{BAL1}$, but lower than the lowest$\triangle V_{B_ALLOW}$

(3) The system entries sleep mode

## Open-wire Detection

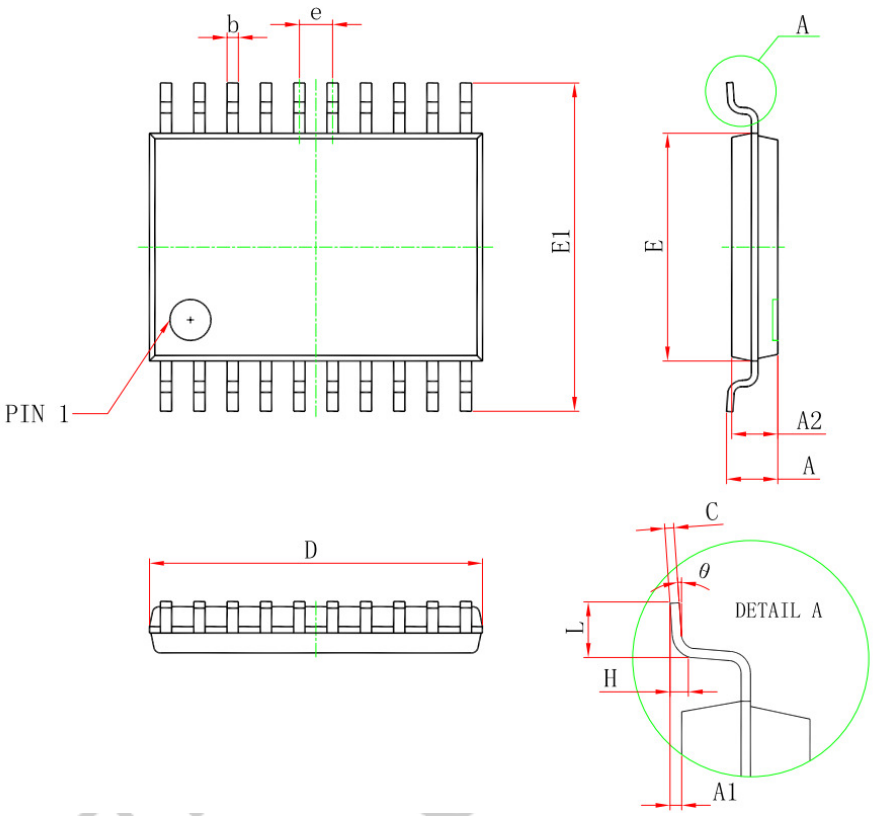
JW3312 checks for VC5-VC0open-wire once per detection time period $t_{OPEN}$.

When any of V5 to V0 pin open, it will detect open-wire and charge and discharge is prohibited

The release from open-wire protection is done by open-wire point being connected and VDD power on again.

## PACKAGE OUTLINE

TSSOP20 UNIT: mm




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| D | 6. 400 | 6. 600 | 0. 252 | 0. 259 |
| E | 4. 300 | 4. 500 | 0. 169 | 0. 177 |
| b | 0. 190 | 0. 300 | 0. 007 | 0. 012 |
| c | 0. 090 | 0. 200 | 0. 004 | 0. 008 |
| E1 | 6. 250 | 6. 550 | 0. 246 | 0. 258 |
| A | | 1. 200 | | 0. 047 |
| A2 | 0. 800 | 1. 000 | 0. 031 | 0. 039 |
| A1 | 0. 050 | 0. 150 | 0. 002 | 0. 006 |
| e | 0. 65 (BSC) | | 0. 026 (BSC) | |
| L | 0. 500 | 0. 700 | 0. 020 | 0. 028 |
| H | 0.25(TYP) | | 0.01(TYP) | |
| θ | 1° | 7° | 1° | 7° |

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