

SSW1N50B / SSI1N50B

520V N-Channel MOSFET

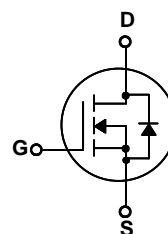
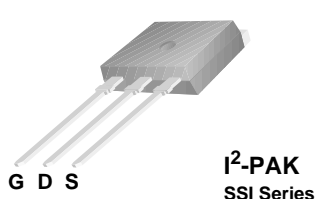
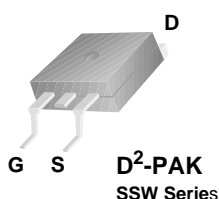
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

Features

- 1.5A, 520V, $R_{DS(on)} = 5.3\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 8.3 nC)
- Low C_{rss} (typical 5.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SSW1N50B / SSI1N50B	Units
V_{DSS}	Drain-Source Voltage	520	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	1.5	A
	- Continuous ($T_C = 100^\circ\text{C}$)	0.97	A
I_{DM}	Drain Current - Pulsed (Note 1)	5.0	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	100	mJ
I_{AR}	Avalanche Current (Note 1)	1.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	3.6	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	36	W
	- Derate above 25°C	0.29	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.44	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	520	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.54	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.75\text{ A}$	--	4.1	5.3	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 0.75\text{ A}$ (Note4)	--	1.8	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	260	340	pF
C_{oss}	Output Capacitance		--	25	33	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	7.2	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 1.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note4, 5)	--	14	40	ns
t_r	Turn-On Rise Time		--	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
t_f	Turn-Off Fall Time		--	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 1.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note4, 5)	--	8.3	11	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge		--	3.4	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	5.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.5 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 1.5 A, dI _F / dt = 100 A/μs (Note4)	--	230	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.94	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 80\text{ mH}, I_{AS} = 1.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 1.5\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

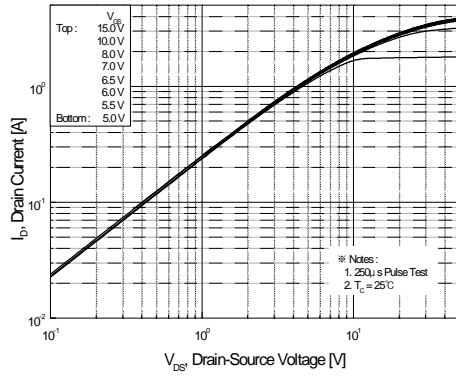


Figure 1. On-Region Characteristics

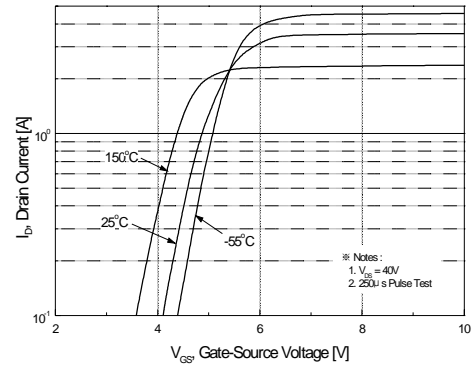


Figure 2. Transfer Characteristics

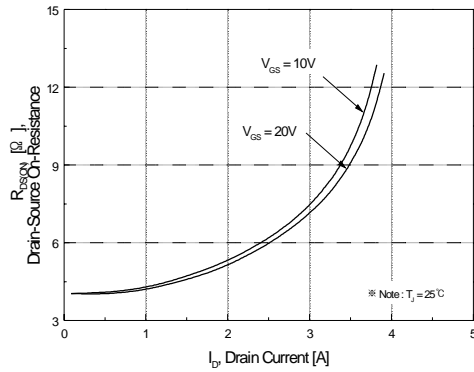


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

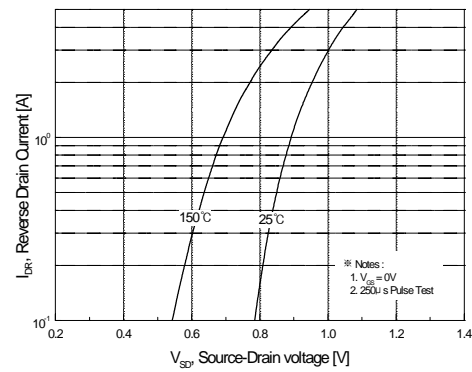


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

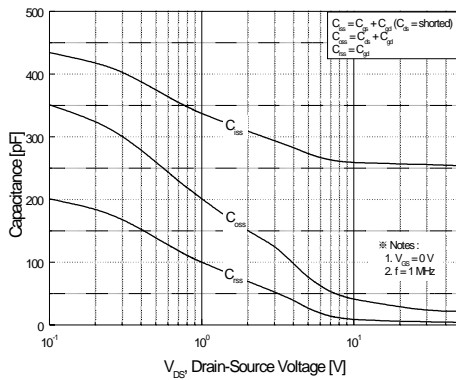


Figure 5. Capacitance Characteristics

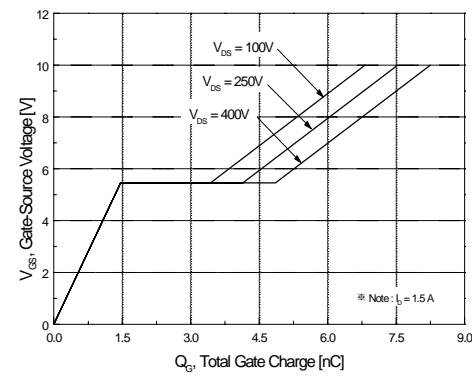


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

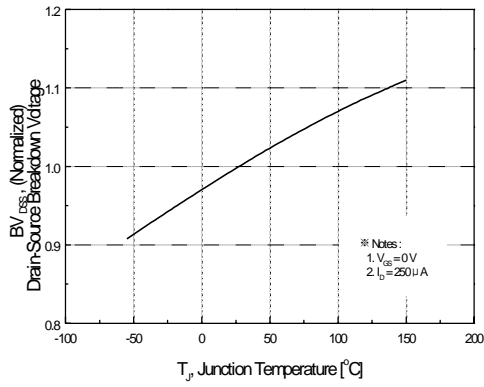


Figure 7. Breakdown Voltage Variation vs Temperature

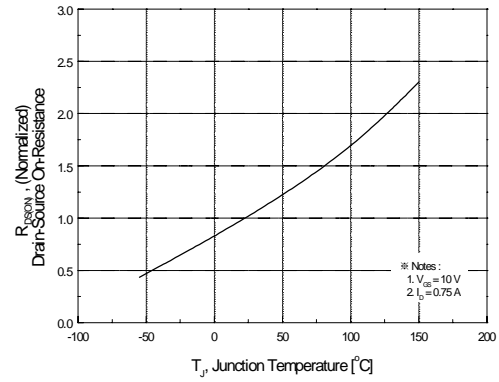


Figure 8. On-Resistance Variation vs Temperature

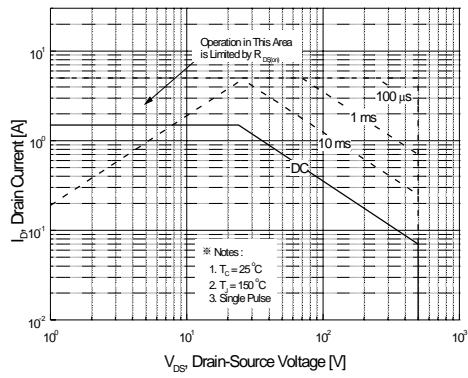


Figure 9. Maximum Safe Operating Area

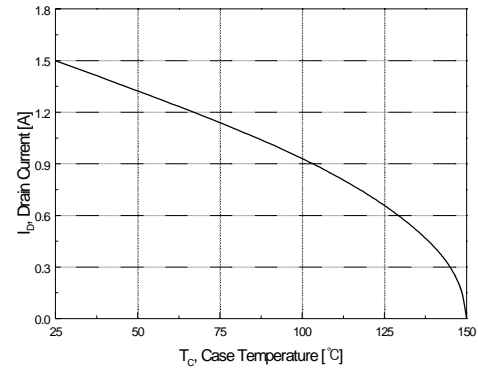


Figure 10. Maximum Drain Current vs Case Temperature

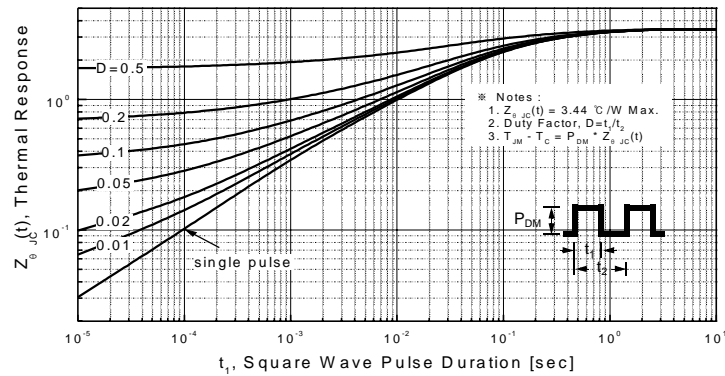
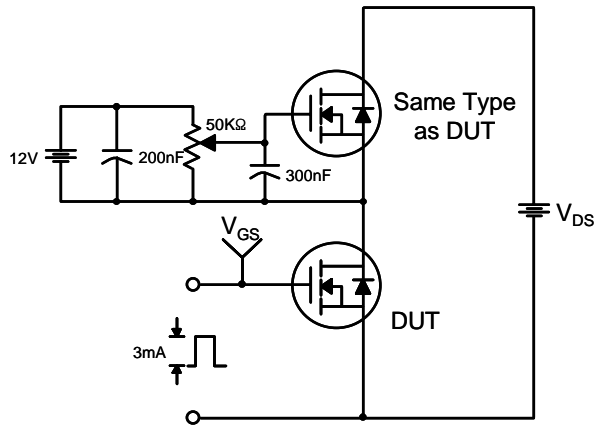
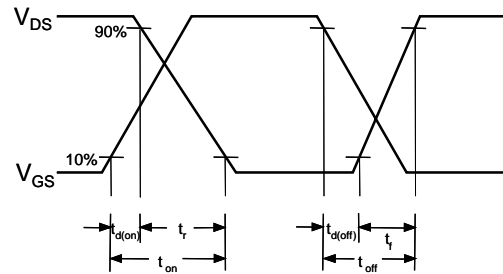
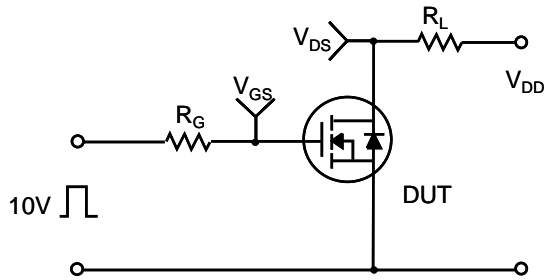


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



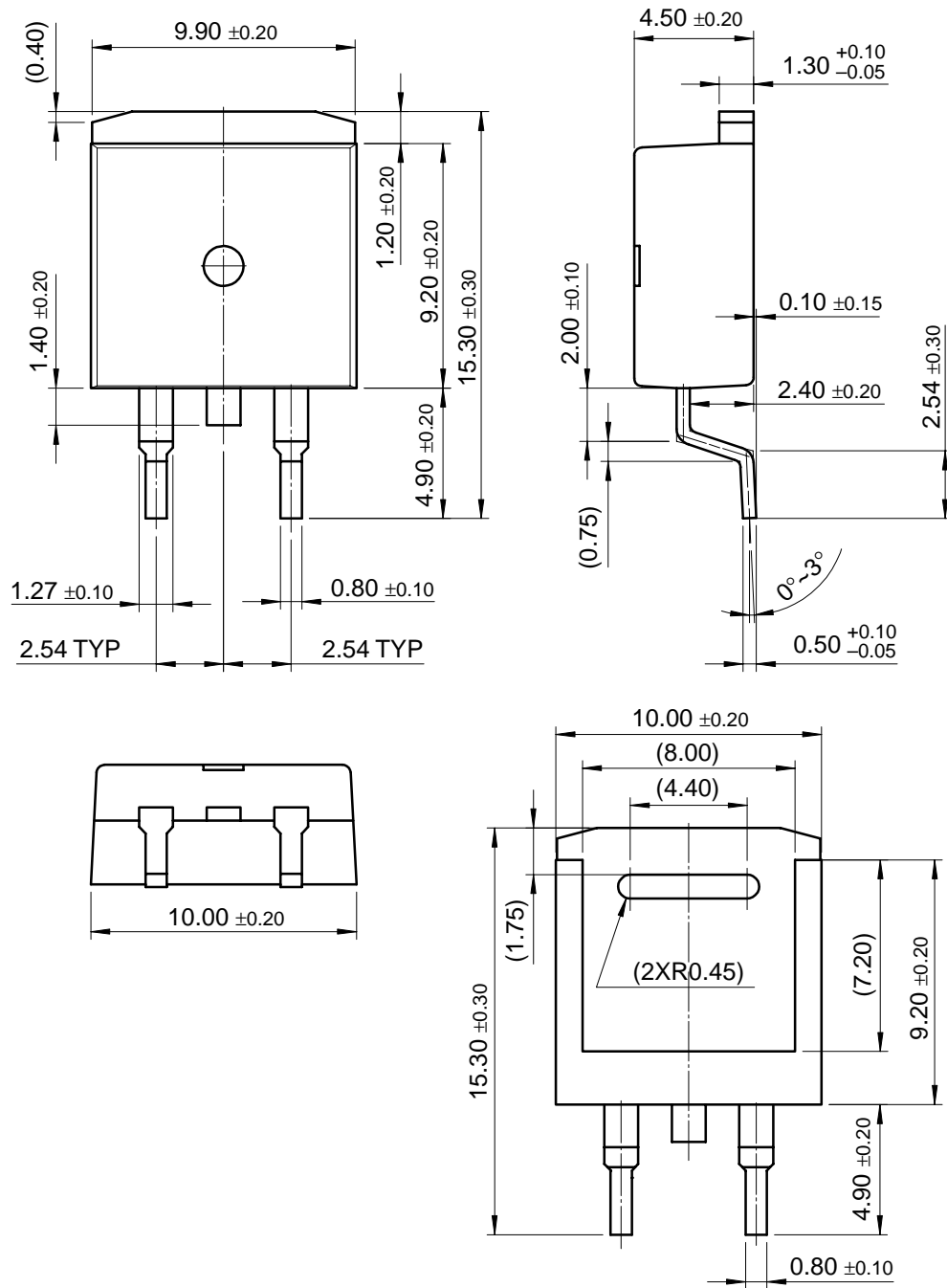
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



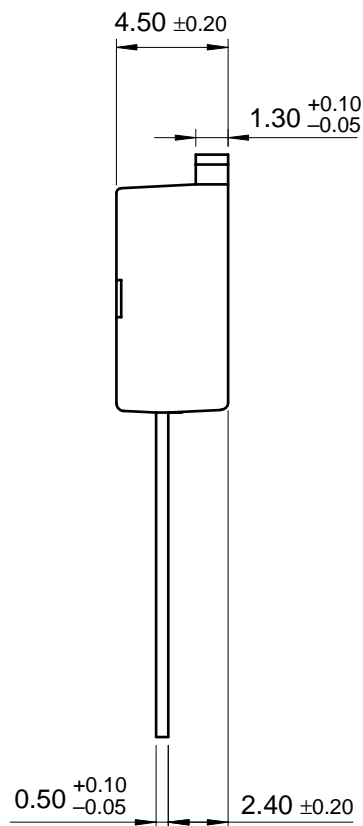
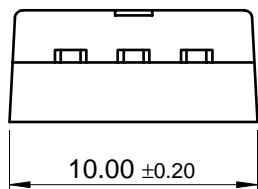
Package Dimensions

D²-PAK

Dimensions in Millimeters

SSW1N50B / SSI1N50B

Technical drawing of a 3-pin connector. The drawing shows a top view and a side view. The top view dimensions are: overall width 9.90 ± 0.20 mm, distance from top edge to the start of the pins (0.40) mm, distance from the start of the pins to the center of the pins (1.46) mm, distance from the center of the pins to the bottom edge 1.27 ± 0.10 mm, and the width of the pins 1.47 ± 0.10 mm. The side view dimensions are: overall height 13.08 ± 0.20 mm, distance from the top edge to the start of the pins (0.94) mm, distance from the start of the pins to the bottom edge 10.08 ± 0.20 mm, and the height of the pins 3.00 mm. The pins are spaced 2.54 TYP mm apart. The pins have a 45° chamfer. The overall width of the connector is 9.90 ± 0.20 mm. The overall height of the connector is 13.08 ± 0.20 mm. The distance from the top edge to the center of the pins is 1.20 ± 0.20 mm. The distance from the center of the pins to the bottom edge is 9.20 ± 0.20 mm. The maximum height of the pins is $\text{MAX } 13.40$ mm.



©2002 Fairchild Semiconductor Corporation

Rev. C, May 2002

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E ² CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I ² C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.