Data Sheet

# BIT3106

## High Efficiency Dual ZVS CCFL Controller

Version : 1.01

*Notice*

*All information contained in this document is subject to change without notice.*

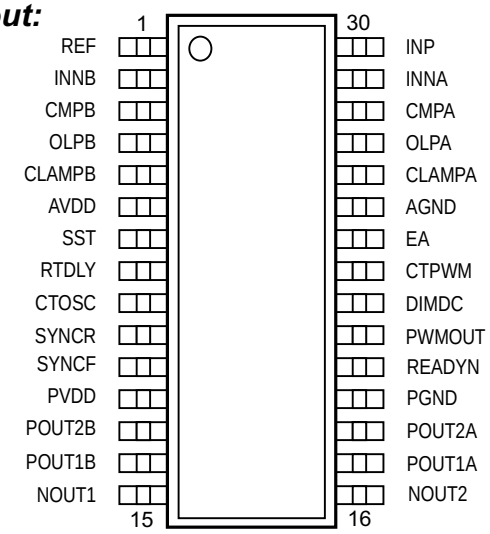
## Features:

- **4.5V ~ 13.2V Operation Voltage**
- **Dual Full Bridge Fixed Frequency ZVS Control**
- **High Accuracy Multi-Lamp Synchronous Operation**
- **Built-in PWM Dimming**
- **Programmable Soft Start**
- **Programmable Striking Voltage**
- **Dual Independent Latched Open Lamp Protection**
- **ON/OFF Control with almost zero Standby Current**
- **Rail-to-Rail Totem Pole Output**
- **Low Power CMOS Process**

## Applications:

- **Cold Cathode Fluorescent Lamps system**
- **LCD Monitor**
- **LCD PC**
- **LCD TV**
- **Video Phone/ Door Phone**
- **Navigation Devices (GPS Equipment)**
- **ATM/ Financial Terminal**
- **POS Terminal**

## Pin Layout:




## General Description:

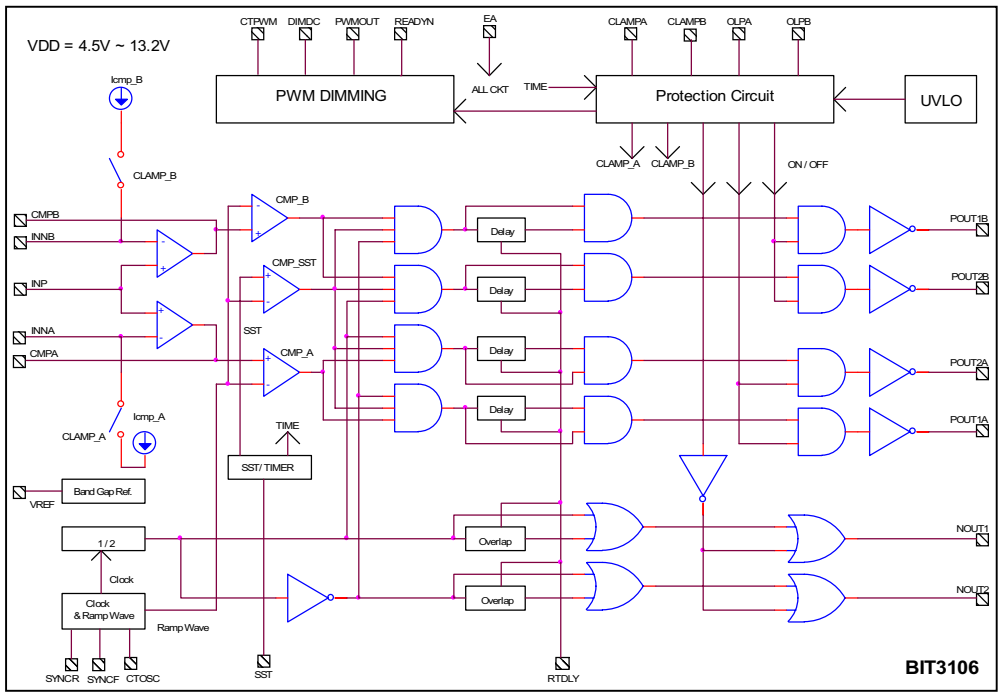
BIT3106 integrated dual fixed frequency controller and the essential features for controlling the CCFL in 30-pin package. New developed full bridge ZVS configuration provides a symmetry AC output and a more than 85% efficiency. The synchronization design synchronizes both of frequency and phase of the lamps. Such design makes BIT3106 especially suitable for high brightness, multi-lamp LCD backlight applications. BIT3106 senses the lamp current directly to enable the built-in PWM dimming. If no current flow into the lamp, BIT3106 provides a continuous AC output to ensure the successful ignition, PWM dimming is started immediately while both of the lamps are ignited. For more than two lamps applications, BIT3106 senses all of the lamps that are driven by different ICs and start the PWM dimming while all of the lamps are ignited. BIT3106 uses up to 13.2V high voltage CMOS process to design the output drivers to drive high side PMOS switches directly without any boost circuitry. BIT3106 provides dual clamped striking voltage control loops to protect transformer while ignition and the lamp current monitors provide the independent reliable latched open lamp protection.

**Patent pending.**

## Recommended Operating Condition:

Supply Voltage……4.5 ~ 13.2 V
Operating Ambient Temperature……..0 ~ 70 ℃
Operating Frequency……30K ~ 250K Hz

## Functional Block Diagram:



## Functional Description:

**UVLO:** The under-voltage-lookout circuit turns the output driver off when supply voltage drops too low. System is shut down with all outputs turned to logic high level.

**Band Gap Reference:** An internal trimmed band-gap reference provides a high accuracy and temperature insensitive voltage reference. By amplifying or dividing this voltage that can generate the other required reference voltages.

**Over Voltage Clamping:** While a > 2.0V is sensed by CLAMPA/B pin, an internal ~ 180uA current will flow into the pin INNA (INNB), the inverting input of the error amplifier, to clamp the output.

**On/Off Function:** The EA pin provides the function to turn on and off the output without shut down the supply voltage. An internal 80K ohm pulled low resistor is connected here. All of the outputs are forced to logic high will the chip is turned off.

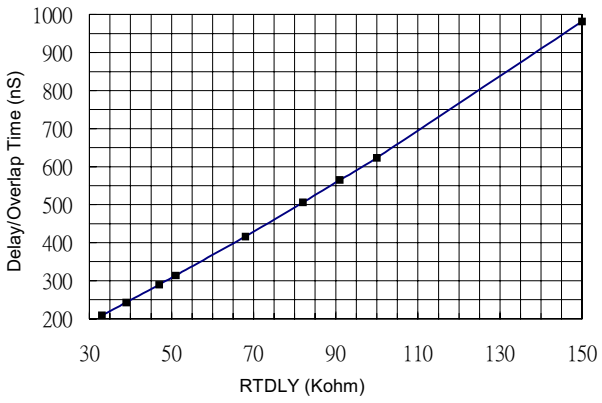
**Set the Delay/Overlap Time for ZVS Operation:** The period of the internal delay generation circuitry dependent on the resistance of $R_{RTDLY}$. The CCFL control requires timing circuitry, the required period of ignition, lamp operation frequency, PWM dimming PWM frequency and the delay/overlap for ZVS switching. The resistor $R_{RTDLY}$ connected to pin RTDLY and the internal 1.25V determines a reference current $I_{REF}$ with

The Delay/Overlap time $T_{Delay}$ and $T_{Overlap}$ in typical case;

$$I_{REF} = \frac{1.25V}{R_{RTDLY}} \quad \text{.....(1)}$$

12V, 25°C operation, can be found from bellow:

RTDLY vs. Delay/Overlap Time




**Set the Lamp Operation Frequency:** The lamp operation frequency can be calculated as equation (2)

$$F_{LAMP} = \frac{1.3}{R_{RTDLY} \times C_{TOSC}} \quad \text{.....(2)}$$

For a 45KHz operation CCFL if an 82K ohm resistor is used as the delay resistor. A 350pF capacitor can be connected to the pin CTOSC.

**The Soft Start and Open Lamp Protection:** A current mirror provides current with value ~ 0.02 x $I_{REF}$ to charge the SST pin. The slope of Soft Start $\Delta V/\Delta T$ can be determined by

$$\frac{\Delta V}{\Delta T} = \frac{0.025}{R_{RTDLY} \times C_{SST}} \quad \text{.....(3)}$$

The required time of ignition is set as equation (4)

$$T_{STRIKE} = 50 \times R_{RTDLY} \times C_{SST} \quad \text{.....(4)}$$

In the case of $R_{RTDLY}$= 82K ohm. A 0.47 uF capacitor connected on the pin SST can set a ~ 2 S period for striking the lamp. If the voltage of OLPA/B pin less than 300mV or the output of the error amplifier, after striking period, the latched protection function will latch the output drivers to VDD high level. The latched situation can be released while the system is re-started.

**PWM Dimming:** To compare the input of pin DIMDC and the 0.2V ~ 2.0V ramp wave makes the PWM pulses for PWM dimming. The internal ramp wave generator generates a ramp wave with peak=2V and valey=0.2V. Its frequency can be set as equation (5)

$$F_{PWM} = \frac{0.347}{R_{RTDLY} \times C_{CTDIM}} \quad \text{.....(5)}$$

The output of pin PWMOUT is pulled to VDD to make the dark portion of the CCFL output bursts and the floating state to make the bright portion. A less than 0.2V input on pin DIMDC will make the PWMOUT to be floating to obtain 100% brightness. BIT3106 provides the continuous high voltage to strike the lamp. It sends the PWM pulse while the voltage of READYN pin is a logic low level.

**Multi-Lamp Operation:** In the case of multi-lamp operation, several criteria must be considered:

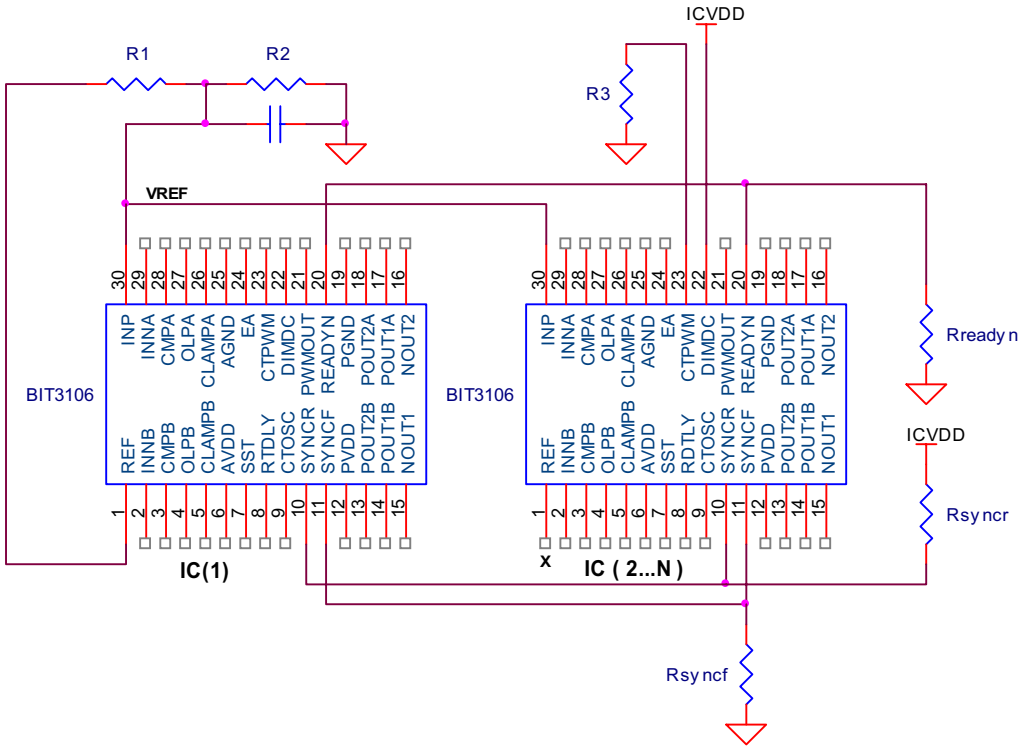
(1)To keep the lamp current to be balanced.

(2)To synchronize the lamp frequency to reduce the interference.

(3)To synchronize the phase of the lamps to minimize the leakage between the lamps.

(4)To determine when to start the PWM dimming.

The bellowing figure is an example to use more than one BIT3106 for multi-lamp operation.




In above figure each chip uses same reference that can keep the lamps balanced. BIT3106 uses two-pin SYNCR (10) and SYNCF (11) to synchronize both of lamp frequency and phase. With two ~ 50 K ohm resistors connected to VDD and ground as above figure shows, the chip with highest frequency will dominate the operation frequency and phase of the whole system. The timing of PWM dimming is dependent on operation situations. In normal case, all of the lamps have been ignited then the pin READYN is pulled to logic low level to start the bursts from pin PWMOUT. But if any one of the lamps is open, the burst will be sent while the user set striking period has been over.

## Pin Description:

| Pin | Names | I/O | Description |
|---|---|---|---|
| 1 | REF | O | Trimmed band gap reference voltage output. |
| 2 | INNB | I | The inverting input of the error amplifier of the channel B. |
| 3 | CMPB | I/O | The output of the error amplifier of the channel B. |
| 4 | OLPB | I | Lamp current detection pin of channel B, the open lamp situation is detected if a less than 300mV input is sensed. |
| 5 | CLAMPB | I/O | Over voltage clamping of channel B. If a > 2 V voltage is detected. A ~ 100uA current will flow into the INNB pin to reduce the output of the error amplifier CMPB to clamp the output voltage. |
| 6 | AVDD | I | The power supply of analog control circuitry. |
| 7 | SST | O | With the RTDLY pin made reference current and an external capacitor connected here can set the required period of ignition and the slop of soft start. The open lamp protection function will be enabled after this node is charged to > 2.5V. |
| 8 | RTDLY | I/O | An external resistor connected here makes a reference current which determines the delay and overlap timing of the output drivers. With this reference current and different capacitors can set the period of soft start, the frequency of PWM dimming and the operation frequency of the lamp. |
| 9 | CTOSC | I/O | With the RTDLY pin made reference current and an external capacitor connected here can set the lamp operation frequency. |
| 10 | SYNCR | I/O | SYNCR and SYNCF pins are used as the frequency and phase synchronization. It requires an ~ 51Kohm resistor connected here to AVDD to implement the synchronization. |
| 11 | SYNCF | O | SYNCR and SYNCF pins are used as the frequency and phase synchronization. It requires an ~ 51Kohm resistor connected here to AGND to implement the synchronization. |
| 12 | PVDD | I | The power supplies input output drivers. |
| 13 | POUT2B | O | The number 2 PMOSFET switch driver of channel B. |
| 14 | POUT1B | O | The number 1 PMOSFET switch driver of channel B. |
| 15 | NOUT1 | O | The number 1 NMOSFET switch driver of channel A, B. |
| 16 | NOUT2 | O | The number 2 NMOSFET switch driver of channel A, B. |
| 17 | POUT1A | O | The number 1 PMOSFET switch driver of channel A. |
| 18 | POUT2A | O | The number 2 PMOSFET switch driver of channel A. |
| 19 | PGND | I/O | The ground pin of the output drivers. |
| 20 | READYN | I | The ignition indicator of the system. An external ~ 50K ohm pulled low resistor must be used here. A logic low output will enable the output of PWM dimming. |
| 21 | PWMOUT | O | The output of PWM dimming. An ~ 200ohm pull to AVDD switch can be used to turn off the lamp with low frequency. |
| 22 | DIMDC | I | PWM dimming control input. A PWM output comes out by comparing this DC input and the triangle wave that is generated by CTPWM. |
| 23 | CTPWM | I/O | With the RTDLY pin made reference current and an external capacitor connected here can set the PWM dimming operation frequency and a 0.2V ~ 2V triangle wave output is generated for PWM input |
| 24 | EA | I | ON/OFF control pin, 1.4V threshold with an internal 50K ± 15% ohm pull low resistor. |
| 25 | AGND | I/O | The ground pin of the analog control circuitry. |
| 26 | CLAMPA | I/O | Over voltage clamping of channel A. If a > 2 V voltage is detected. A ~ 100uA current will flow into the INNA pin to reduce the output of the error amplifier CMPA to clamp the output voltage. |
| 27 | OLPA | I | Lamp current detection pin of channel A, the open lamp situation is detected if a less than 300mV input is sensed. |
| 28 | CMPA | I/O | The output of the error amplifier of the channel A. |
| 29 | INNA | I | The inverting input of the error amplifier of the channel A. |
| 30 | INP | I | The Non-inverting input of the error amplifier of both channel A, B. |

## Absolute Ratings: (if Ta=25℃)

| Parameter | Symbol | Ratings | Unit | Remarks |
|---|---|---|---|---|
| Control Supply Voltage | AVDD | -0.3~+ 15 | V | Ta=25°C |
| Analog Ground | AGND | ±0.3 | V | |
| Driver Supply Voltage | PVDD | -0.3~+ 15 | V | |
| Driver Ground | PGND | ±0.3 | V | |
| Input Voltage | | -0.3~ VDD+0.3 | V | |
| Power Dissipation | | 800 | mW | |
| Operating Ambient Temperature | Ta | 0~ +70 | ° C | |
| Operating Junction Temperature | | +150 | ° C | |
| Storage Temperature | | -55~+150 | ° C | |

## DC/AC Characteristics:

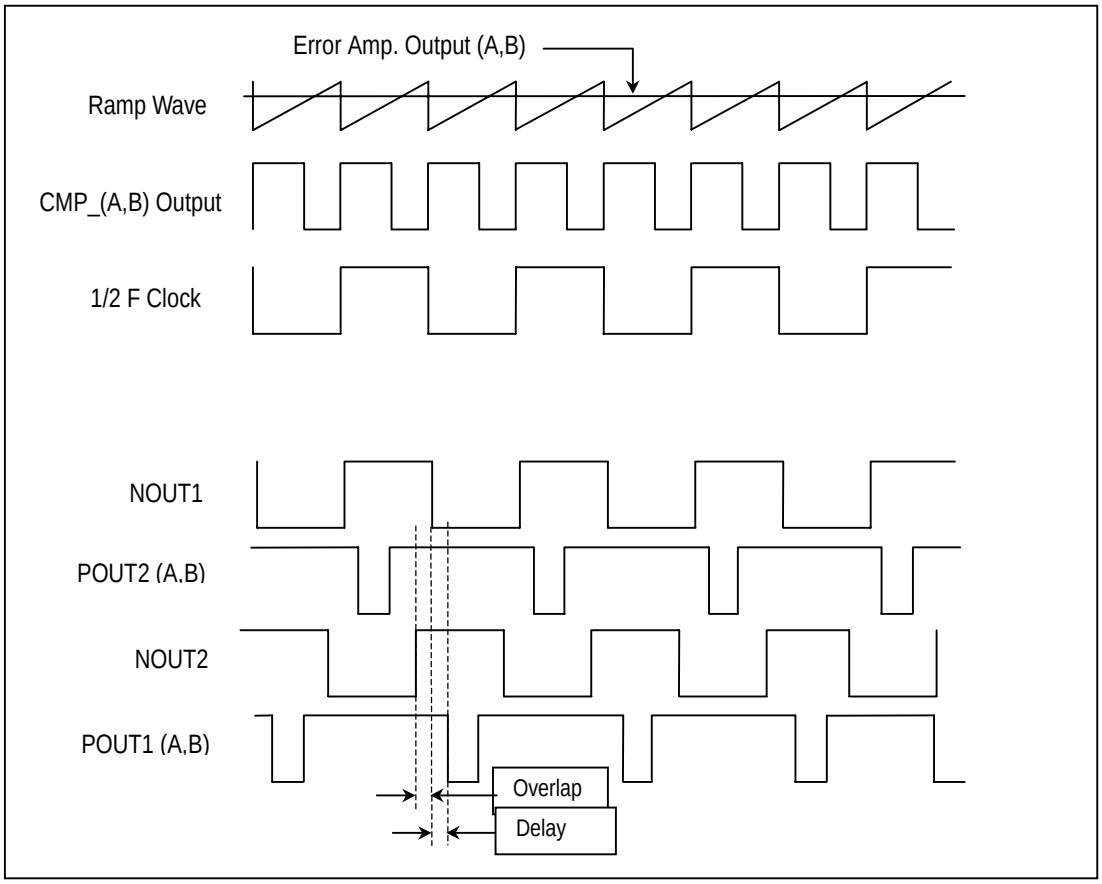
| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Supply Voltages** | | | | | |
| AVDD(Note1) | | 4.0 | | 13.2 | V |
| PVDD(Note1) | | 4.0 | | 13.2 | V |
| Chip Consumed Current | 12V AVDD, 12V PVDD Ta=25°C | | 3 | | mA |
| **Reference Voltage** | | | | | |
| Output voltage | 12V, Ta=25°C | | 2.5 | | V |
| Line regulation | VDD=4.5 ~13.2 V | | 2 | 20 | mV |
| **Under Voltage Look Out** | | | | | |
| Positive Going Threshold | Ta=25°C | 3.8 | 4 | 4.2 | V |
| Hysteresis | | 0.1 | 0.2 | 0.3 | V |
| **Ramp Wave Generator and Lamp Frequency** | | | | | |
| Operating Frequency | Note2 | 50 | | 250K | Hz |
| Output peak | | | 2.25 | | V |
| Output valley | | | 0.45 | | V |
| **Error Amplifier** | | | | | |
| Open loop gain | | 60 | 80 | | dB |
| Unit gain band width | | 1 | 1.5 | | MHz |
| **SST Soft Start and Open Lamp Enable** | | | | | |
| Output current | VDD=12V, Ta=25°C | | $25/R_{RTDLY}$ | | mA |
| Open Lamp Detection Enable | | | 2.5 | | V |
| **Open Lamp Protection** | | | | | |
| OLPA/B pin Open lamp detection lower threshold | VDD=12V, Ta=25°C | | 300 | | mV |
| CMP pin Open lamp detection lower threshold | | | 2.5 | | V |
| Hysterisis | | | 20 | | mV |
| **Over Voltage Clamping** | | | | | |
| CLAMPA/B pin detection lower threshold | VDD=12V, Ta=25°C | | 2.0 | | V |
| Hysterisis | | | 20 | | mV |
| INN pin driving current | | | 180 | | uA |
| **On/Off Function** | | | | | |
| The threshold of EA pin | VDD=12V, Ta=25°C | | 1.2 | | V |
| Internal pulled low resistance | | | 80K | | Ω |
| **PWM Dimming** | | | | | |
| Ramp Wave Peak | VDD=12V, Ta=25°C | | 2.0 | | V |
| Ramp Wave Valley | | | 0.2 | | V |
| PWM Frequency | | 10 | | 100K | Hz |
| 100 % Brightness Dimming Voltage on pin DIMDC | | | | 0.2 | V |
| 0 % Brightness Dimming Voltage on pin DIMDC | | 2 | | | V |
| Pulled high resistance of Pin PWMOUT output for making the dark burst | | | 200 | | Ω |
| Pin PWMOUT output for making the bright burst | | | Floating | | |
| **Output** | | | | | |
| CMOS output impedance | (Note2, Note3) | | 50 | | Ω |
| Rising Time | VDD=5V, 1000pF(Note3, Note4) | | 110 | | ns |
| Falling Time | | | 100 | | ns |

Note 1. AVDD and PVDD must be set to an equal supply voltage VDD in typical application.

Note 2. The lamp operation frequency is the half of the ramp wave frequency
Note 3. Only verified by simulation. Not 100% tested.
Note 4. The voltages of the output drivers are equal to PVDD in each off states.

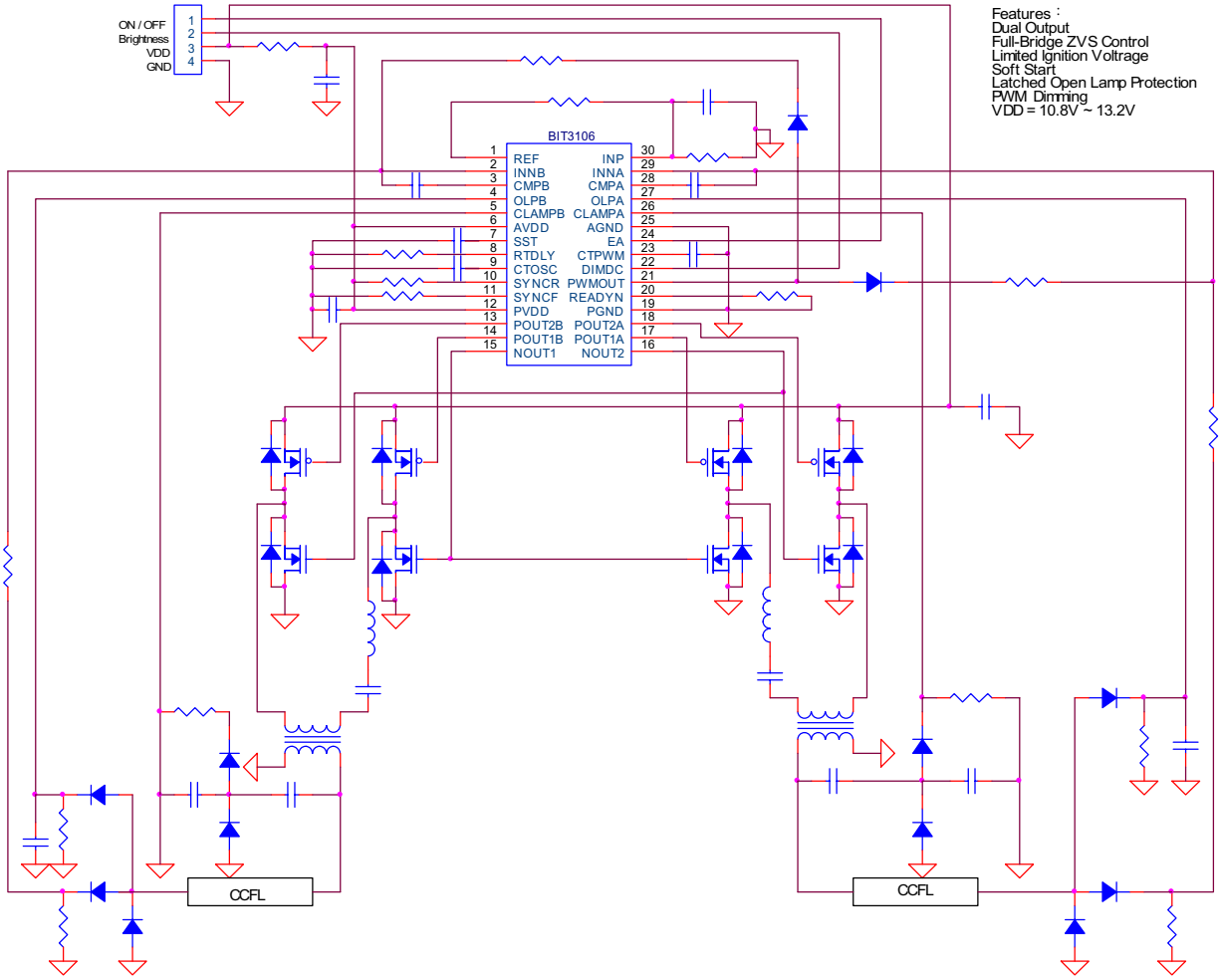
## Timing Diagram

BIT3106 uses new developed fixed frequency full bridge driving methodology to drive CCFL. The low side switches; NMOSFETs are driven by fixed frequency and fixed; > 50% duty cycle signals. The high side switches; PMOSFETs are driven by fixed frequency PWM controlled signals. The detail timing relationship is shown as bellow:



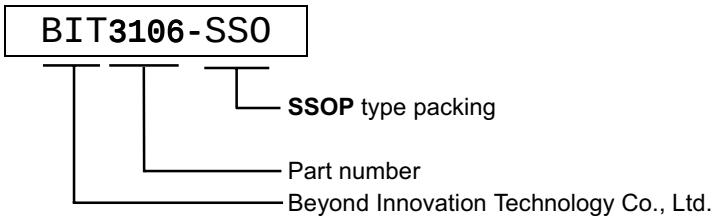

If the lamp operation frequency is set to higher than resonant frequency of the LC tank, symmetry ZVS switching operation can be performed. A well-controlled delay and overlap timing relationship play the key role of this control scheme. It can be set through using proper resistor connected on RTDLY pin. (Patent pending)

## Application Information:



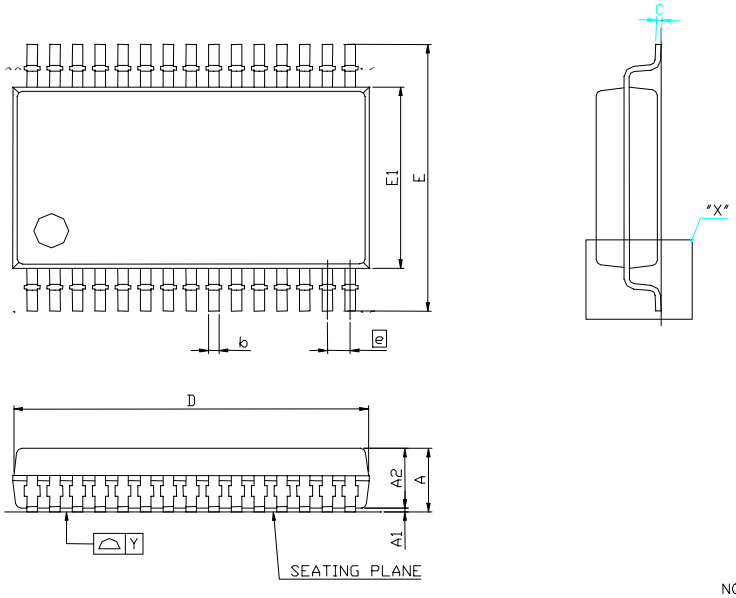

A Typical application of BIT3106

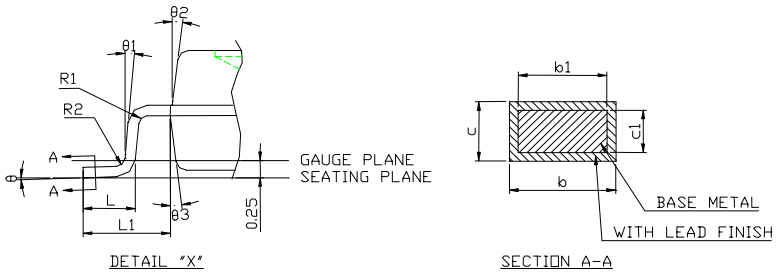
## Order Information:



## Package Information :

### SSOP type :




| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 2.0 | | | 79 |
| A1 | 0.05 | 0.13 | 0.21 | 2 | 5 | 8 |
| A2 | 1.65 | 1.75 | 1.85 | 65 | 69 | 73 |
| b | 0.22 | | 0.38 | 9 | | 15 |
| b1 | 0.22 | 0.30 | 0.33 | 9 | 12 | 13 |
| c | 0.09 | | 0.25 | 4 | | 10 |
| c1 | 0.09 | 0.15 | 0.21 | 4 | 6 | 8 |
| D | 9.90 | 10.20 | 10.50 | 390 | 402 | 413 |
| E | 7.40 | 7.80 | 8.20 | 291 | 307 | 323 |
| E1 | 5.00 | 5.30 | 5.60 | 197 | 209 | 220 |
| e | 0.65 BSC | | | 26 BSC | | |
| L | 0.55 | 0.75 | 0.95 | 22 | 30 | 37 |
| L1 | 1.25 REF | | | 49 REF | | |
| R1 | 0.15 | 0.20 | 0.25 | 6 | 8 | 10 |
| R2 | 0.15 | 0.20 | 0.25 | 6 | 8 | 10 |
| Y | | | 0.075 | | | 3 |
| θ | 0° | 4° | 8° | 0° | 4° | 8° |
| θ1 | 0° | | | 0° | | |
| θ2 | 7° TYP | | | 7° TYP | | |
| θ3 | 7° TYP | | | 7° TYP | | |

NOTE:
1. REFER TO JEDEC MO-150AH
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6mil) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUS SHALL NOT EXCEED 0.25mm (10 mil) PER SIDE.
4. CONTROLLING DIMENSION: MILLIMETER