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Super Economic Digital Audio

KHTEK DA1166

24Bit, 192KHz 6-Channel Digital Audio to Analog Converter

General Description

The DA1166 is a 6-channel digital audio to analog converter especially designed to work with MPEG2/AC-3 decoded data for applications such as, DVD player, home theater, set-top box, and digital TV, etc. The DA1166 integrates 6 DA channels, each supports 16 – 32 bit word lengths and 16KHz – 192 KHz sampling rate. The DA1166 also provides customers several selectable functions via hardware control pins.

Features

High Resolution:

- 16/18/20/24/32 Bit Selectable

High Performance:

- Sampling Rate: 16KHz ~ 192KHz
- THD+N: -90 dB
- Dynamic Range: 103dB
- S/N Ratio: 103dB
- Channel Separation: 108dB

28 Pin SSOP Package

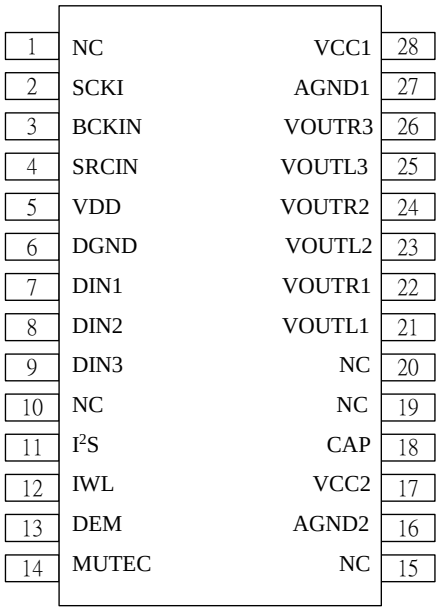
High Integration:

- 6 Audio Channels, Each Contains:
  - Over-sampling Digital Filter
  - High-Resolution Delta Sigma DAC
  - Analog Low Pass Filter
  - Output Amplifier

High Versatility

- Control via Hardware Pins
  - Right-justified or IIS Format Selectable
  - Bi-directional Mute Control Pin
  - De-emphasis for 44.1KHz Sampling Rate

Pin Configuration



Pin Assignments

Pin	Name	I/O	Description
1	NC	-	Not Connected (Don't Care)
2	SCKI	IN	External Master/System Clock Input
3	BCKIN	IN	Bit Clock Input for Audio Data
4	SRCIN	IN	Sample Rate Clock Input
5	VDD	PWR	Digital Power Supply
6	DGND	GND	Digital Ground
7	DIN1	IN	Audio Data Input to DAC1
8	DIN2	IN	Audio Data Input to DAC2
9	DIN3	IN	Audio Data Input to DAC3
10	NC	-	Not Connected (Don't Care)
11	I^2S	IN	Audio Input Format Selection
12	IWL	IN	Input Word Length Selection
13	DEM	IN	De-emphasis Control. Set this pin "High" to Enable De-emphasis Function.
14	MUTEC	IN	Mute Control, Active "High". To Mute, Pull this pin "High".
		OUT	Output Pin to Control External Mute Circuit.
15	NC	-	Not Connected (Don't Care)
16	AGND2	GND	Analog Ground
17	VCC2	PWR	Analog Power
18	CAP	-	Analog Common Mode Pin
19	NC	-	Not Connected (Don't Care)
20	NC	-	Not Connected (Don't Care)
21	VOUTL1	OUT	L-Channel Output from DAC1
22	VOUTR1	OUT	R-Channel Output from DAC1
23	VOUTL2	OUT	L-Channel Output from DAC2
23	VOUTR2	OUT	R-Channel Output from DAC2
25	VOUTL3	OUT	L-Channel Output from DAC3
26	VOUTR3	OUT	R-Channel Output from DAC3
27	AGND1	GND	Analog Ground
28	VCC1	PWR	Analog Power

Note:

1. All digital input pins have Schmitt triggers.
2. Logic high is denoted as either "H" or "1"; logic low is denoted as either "L" or "0" in this document.

Absolute Maximum Rating

Power Supply Voltage	+ 6.5V
Input Logic Voltage	-0.3V to (VDD + 0.3V)
Power Dissipation	600mW
Operating Temperature Range	-25 C to +85 C
Storage Temperature	-55 C to +125 C

ESD Sensitive Device

Although DA1166 is furnished with KHTEK's proprietary ESD protection circuitry, proper ESD precaution is still recommended to avoid performance degradation or permanent damage.

Ordering and Package Information

Part No.	Suffix	Package	Package Drawing No.
DA1166	None	28 pin SSOP	128 -SS
	F	28 pin SSOP, Pb Free	128 –SS
	G	28 pin SSOP, Green Package - Halogen and Pb free	128 -SS

Package drawing is at the end of this data sheet

Specifications

Electrical Characteristics:

VCC1=VCC2=VDD=5V/3.3V, @ 25 °C, fs=48kHz, 24Bit input data, System Clock = 384/256fs/128fs.

Parameter	Conditions	Min	Type	Max	Unit
Sampling Frequency		16	48	192	KHz
System Clock Frequency	128fs	1.024	6.144	24.5760	MHz
	192fs	1.536	9.216	36.8640	MHz
	256fs	2.048	12.288	49.1520	MHz
	384fs	3.072	18.432	-	MHz
	512fs	4.096	24.576	-	MHz
	768fs	6.144	36.864	-	MHz
Audio Data Format	Selectable		Right Justified		
			I^2S		
Data Bit Length	Right Justified	16	24	24	Bits
	I^2S	16	24	32	Bits
Digital Input/Output					
Input Logic Level	VCC1=VCC2=VDD				
V_{IH}	Pin2,3,4,7,8,9,11,12,13,14 ---Schmitt Trigger	52%			VDD
V_{IL}				16%	VDD
Output Logic Level	VCC1=VCC2=VDD				
V_{OH}		90%			VDD
V_{OL}				10%	VDD
DC Accuracy					
Gain Error			+/- 1	+/- 3	%FSR
Gain Mismatch Ch to Ch			+/- 1	+/- 2	%FSR

Electrical Characteristics (*Cont.*):

VCC1=VCC2=5V, VDD=3.3V/5V, @25 °C, 24Bit input data, System Clock = 384/256fs/128fs.

Parameter	Conditions	Min	Type	Max	Unit
Power Supply					
Voltage Range: VCC1, VCC2, VDD	VCC1=VCC2=VDD	4.5	5	5.5	V
Supply Current: ICC1+ICC2+IDD	@fs=44.1KHz VCC1=VCC2=VDD=5V		43		mA
Power Dissipation:			215		mW
Supply Current: ICC1+ICC2+IDD	@fs=96KHz VCC1=VCC2=VDD=5V		47		mA
Power Dissipation:			235		mW
Analog Output					
Voltage Range			1.06		Vrms
Center Voltage	Vout=0dB		2.5		V
Load Impedance		10			KOhm
Frequency Response	AC Load	0		20	KHz
Dynamic Performance (Measurement Bandwidth 20Hz to 20KHz)					
@fs=48KHz (Full –Scale Output Sine Wave, 997Hz)					
THD+N at FS(0dB)	Un-weighted		-90		dB
THD+N at –60dB	Un-weighted		-39		dB
Dynamic Range	EIAJ, A-weighted		103		dB
SNR	EIAJ, A-weighted		103		dB
Channel Separation		103	108		dB
@fs=96KHz (Full –Scale Output Sine Wave, 997Hz)					
THD+N at FS(0dB)	Un-weighted		-86		dB
THD+N at –60dB	Un-weighted		-40		dB
Dynamic Range	EIAJ, A-weighted		104		dB
SNR	EIAJ, A-weighted		104		dB
Channel Separation		101	106		dB
@fs=192KHz (Full –Scale Output Sine Wave, 997Hz)					
THD+N at FS(0dB)	Un-weighted		-86		dB
THD+N at –60dB	Un-weighted		-39.6		dB
Dynamic Range	EIAJ, A-weighted		103		dB
SNR	EIAJ, A-weighted		103		dB
Channel Separation		101	106		dB

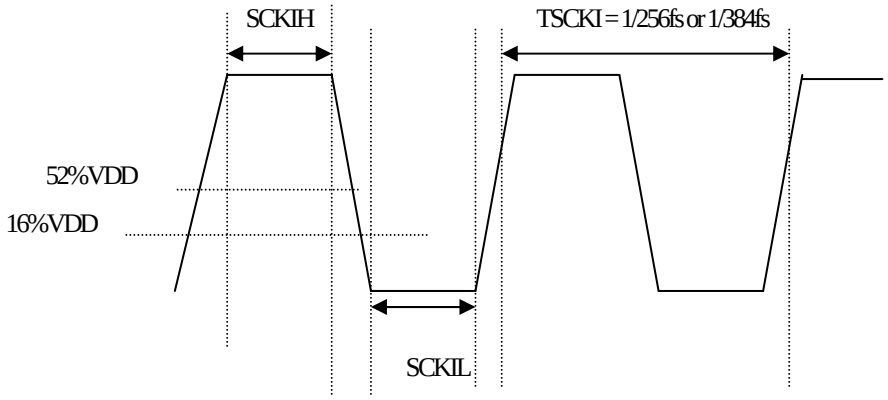
Timing Characteristics:

SCKI/Master Clock Input Timing:

Timing Parameter @25°C, fs=48kHz, 24Bit input data, System Clock = 384/256fs

Parameter	Symbol	Value	Unit
Master Clock Timing			
SCKI clock high level	SCKIH	>10	ns
SCKI clock low level	SCKIL	>10	ns

Timing Diagram

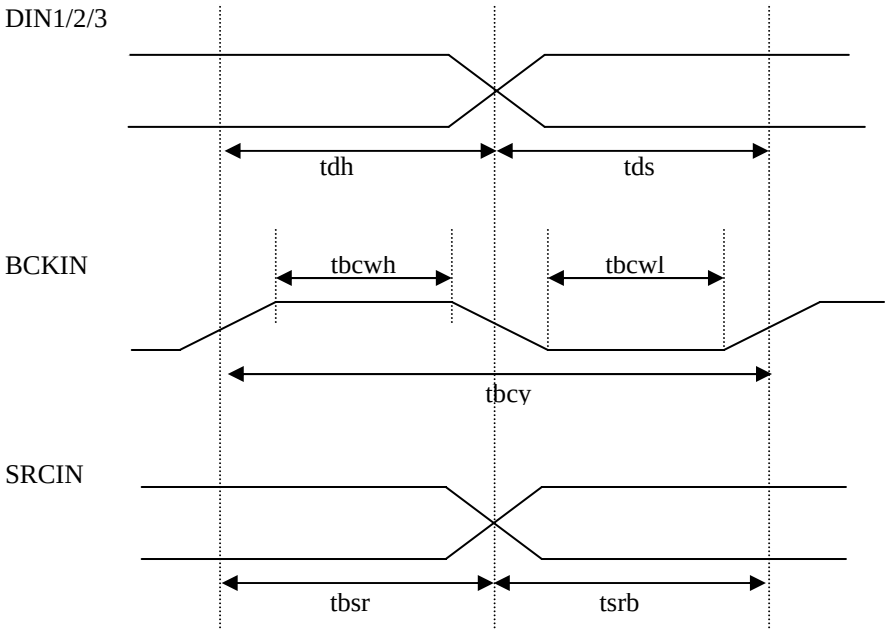


Data Input Timing:

Timing Parameter: @25°C, fs=48kHz, 24Bit input data, System Clock = 384/256fs

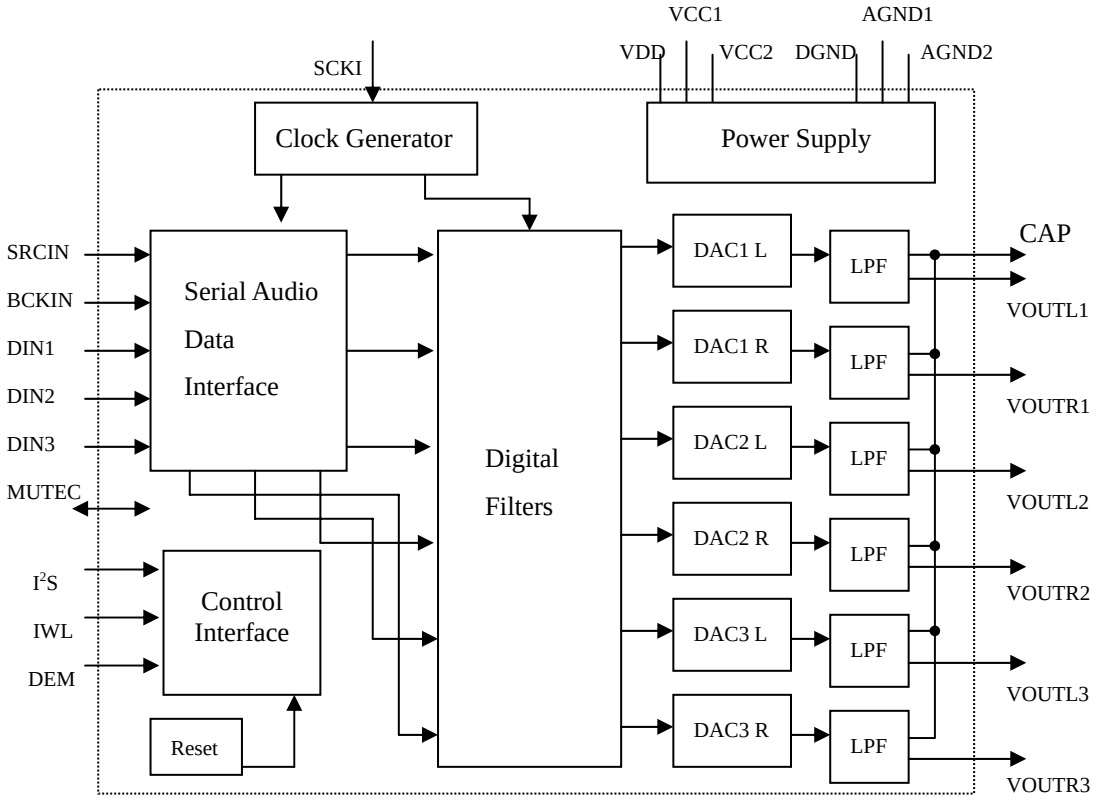
Parameter	Symbol	Value	Unit
Data Input Timing			
DIN setup time	tds	>30	ns
DIN hold time	tdh	>30	ns
BCKIN high-level, low-level	tbcwh, tbcwl	>50	ns
BCKIN pulse cycle time	tbcy	>100	ns
BCKIN rising edge to SRCIN	tbsr	>30	ns
SRCIN to BCKIN rising edge	tsrb	>30	ns

Timing Diagram



Functional Description

Functional Block Diagram



System Clock

The system clock must be 128fs, 192fs, 256fs, 384fs, 512fs, or 768fs, where fs is the standard audio frequency including 32KHz, 44.1KHz, 48KHz, 96KHz, or 192KHz. The system clock can be input via SCKI (pin2) from an external clock and is used to operate the digital filter and delta sigma modulator. The system clock should be synchronized with SRCIN (pin4) – sampling rate clock. If the phase difference between them becomes greater than 6 bits of BCKIN (pin3), the synchronization will be automatically performed and at this time the analog outputs are forced to VCC/2 by the chip.

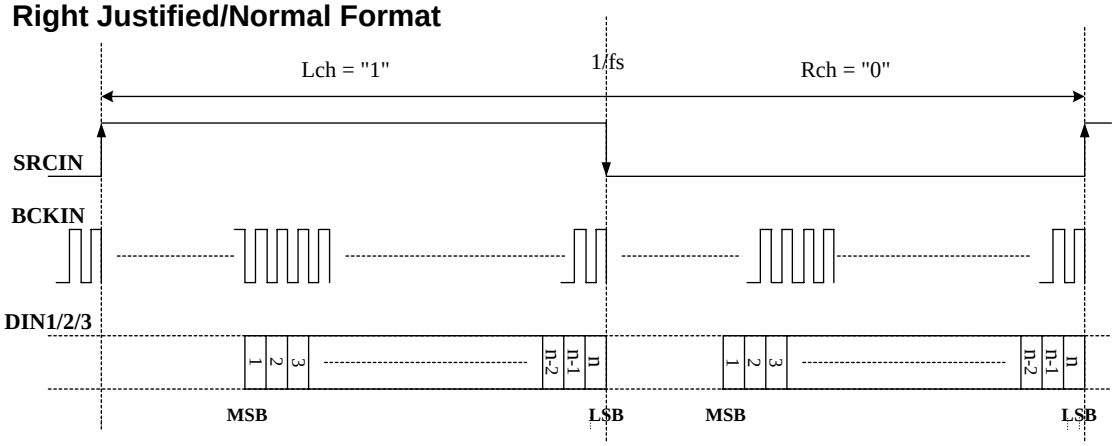
Table-1 System Clock and Sampling Rate

Sampling Rate fs	System Clock Frequency (MHz)					
	128 fs	**192 fs**	**256fs**	**384fs**	**512fs**	**768fs**
32KHz	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760
44.1KHz	5.6448	8.4670	11.2896	16.9340	22.5792	33.8688
48KHz	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640
96KHz	12.2880	18.4320	24.5760	36.8640	49.1520	-
192KHz	24.5760	36.8640	49.1520	-	-	-

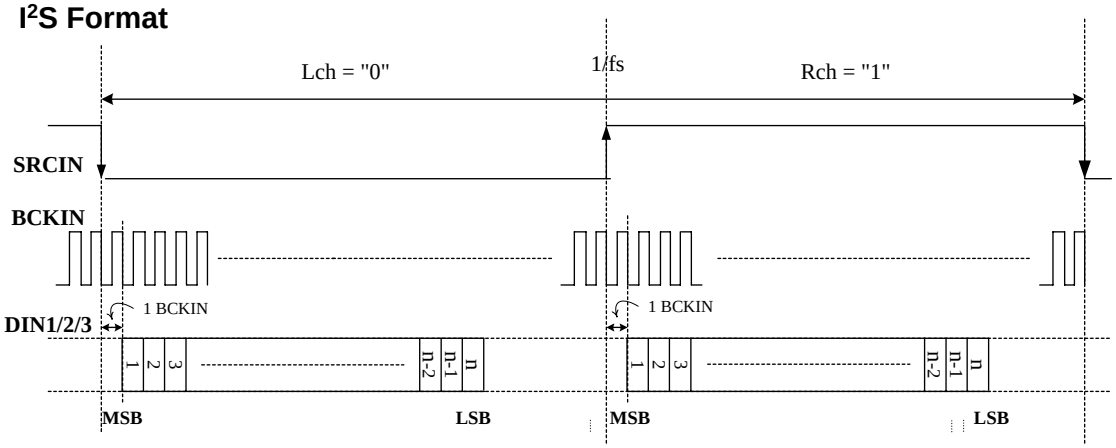
Serial Digital Audio Data Input Interface

The digital audio information is applied to DA1166 via DIN1/2/3 (pin 7, 8, 9) for audio data input, SRCIN (pin 4) for sampling rate clock, and via BCKIN (pin 3) for bit clock. The DA1166 supports right justified/normal data format and I^2S data format. All data formats are MSB first and two's complement. The I^2S format supports word length from 16 Bit to 32 Bit, but the right justified format supports word length only up to 24 Bit. The I^2S data format, which is compatible with Philips serial data protocol, is left justified and one bit clock delay between SRCIN and data MSB. The relationship of the three audio input signals, DIN, SRCIN, and BCKIN is illustrated in the following figures for three formats:

Right Justified/Normal Format



I^2S Format



Note: 1. Logic high is denoted as either "H" or "1"; logic low is denoted as either "L" or "0" in this document.

2. With I^2S format, the word length can go up to 32 Bit as long as the SRCIN period can accommodate.

Multi-Functions & Controls

The logic levels set on the hardware pins – I^2S (pin 11), IWL (pin 12), DEM (pin 13), and MUTEC (pin 14) control a few functions implemented in the DA1166.

Audio Data Format Selection

I^2S (pin11) and IWL (pin12) together can be used to obtain different input data format and word length. The proper settings are shown in the following table:

Table-2 Selectable Input Data Formats and Word Length

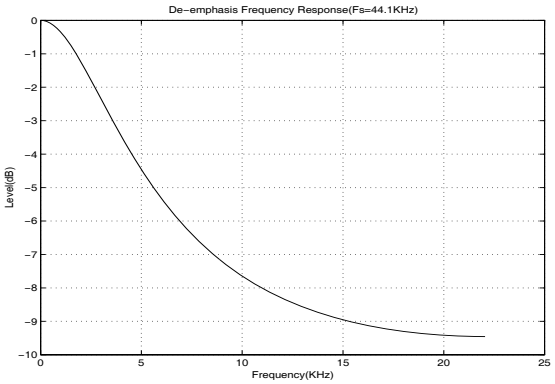
Input Data Format	I^2S (pin11)	IWL (pin12)
Normal Format -24Bit	0	0
Normal Format -20Bit	0	1
I^2S Format - 16Bit	1	0
I^2S Format - 24Bit to 32Bit	1	1

De-emphasis Function and Control

The De-emphasis function is controlled by the DEM (pin13) in hardware mode. A logic "0" on DEM pin (pin 13) allows for a normal operation; while a logic "1" on DEM pin (pin 13) would enable the de-emphasis function.

Table-5 De-emphasis Function

DEM (pin 13)	De-emphasis
0	OFF
1	ON



Soft Mute Function and Control

Soft mute function is implemented for all DAC channels in DA1166. It takes 256/fs seconds for DAC to soft mute its output; therefore the time needed to soft mute the DAC depends on the sampling rate used.

A bi-directional MUTEC (pin 14) controls this function. When MUTEC (pin 14) is used as a control input pin, a logic "0" on MUTEC pin (pin 14) allows for a normal operation; while a logic "1" on MUTEC pin (pin14) would force the outputs to be soft muted.

Table-3 Selectable Mute Function

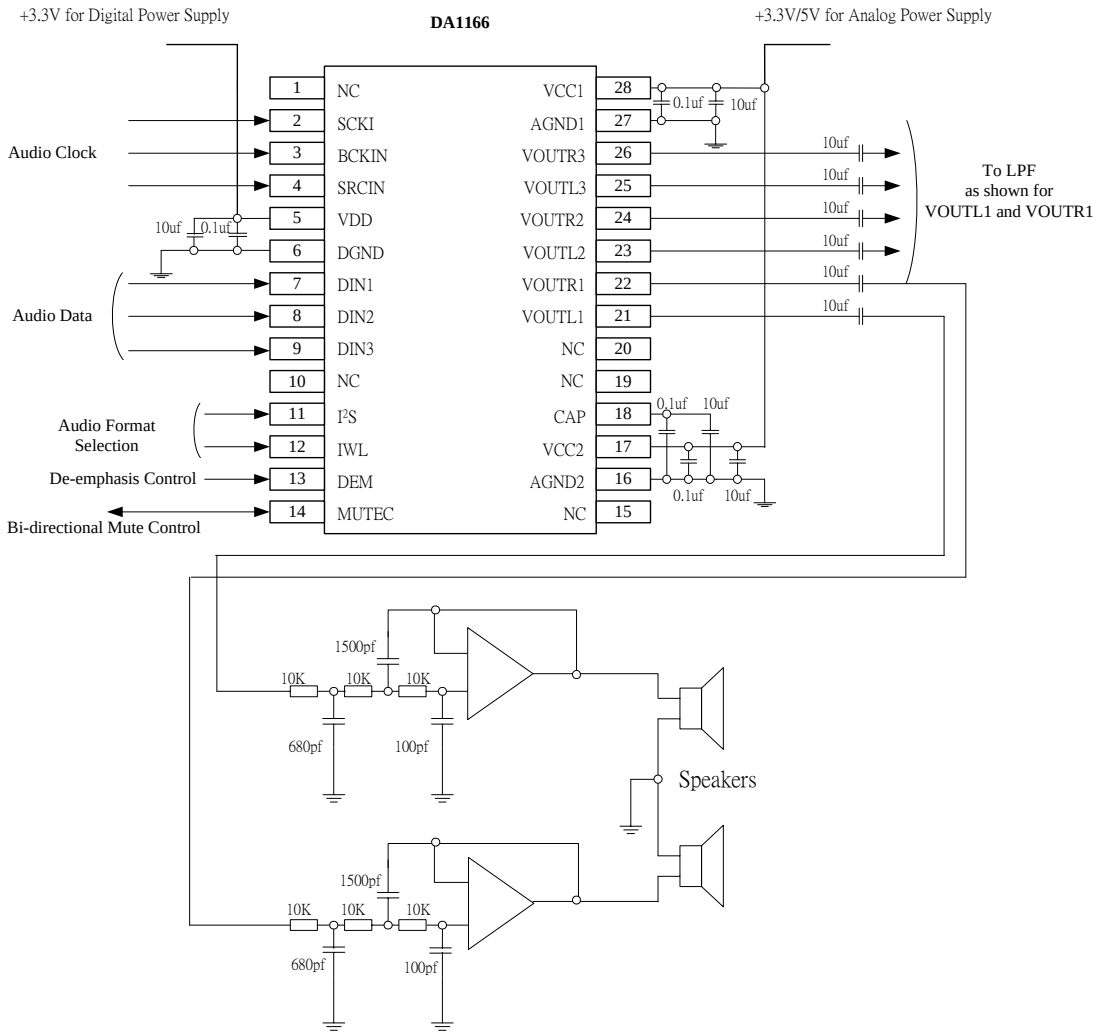
MUTEC (pin 14)	Mute Function
0	OFF
1	ON

The Mute Control pin MUTEC (pin 14) can be used as an output pin to control the external mute circuit to suppress the clicks and pops that often occur during power up stage; the irritating noises when clocks are not correct as specified; or the unpleasant DC tone when the input data on all six channels is consecutive zeros. The MUTEC pin (pin 14) goes high when any of the situations described above occurs to activate the external mute circuit. It will go back to low when power and clocks are stabilized or a non-zero input data occurs on either channel.

The use of the external mute circuit is not mandatory for special cares having been taken within the DA1166 to minimize the problems described above. However it is recommended for designs requiring extreme quietness in above situations.

Application Considerations

Application Circuit



Power Supply Connections

The power and grounding should be carefully arranged to achieve the highest performance possible. The power pins should be connected together before being connected to a clean supply and all the ground pins should be connected to the analog ground plane at locations near by the physical pins.

Power and Reference Decoupling

All switching signals, especially clocks, should be kept away from CAP (pin 18) to avoid unwanted coupling. The decoupling capacitors for CAP and power should be located on the same layer as the device and as close to the device as possible with the smaller capacitor, 0.1uf, being the closest.

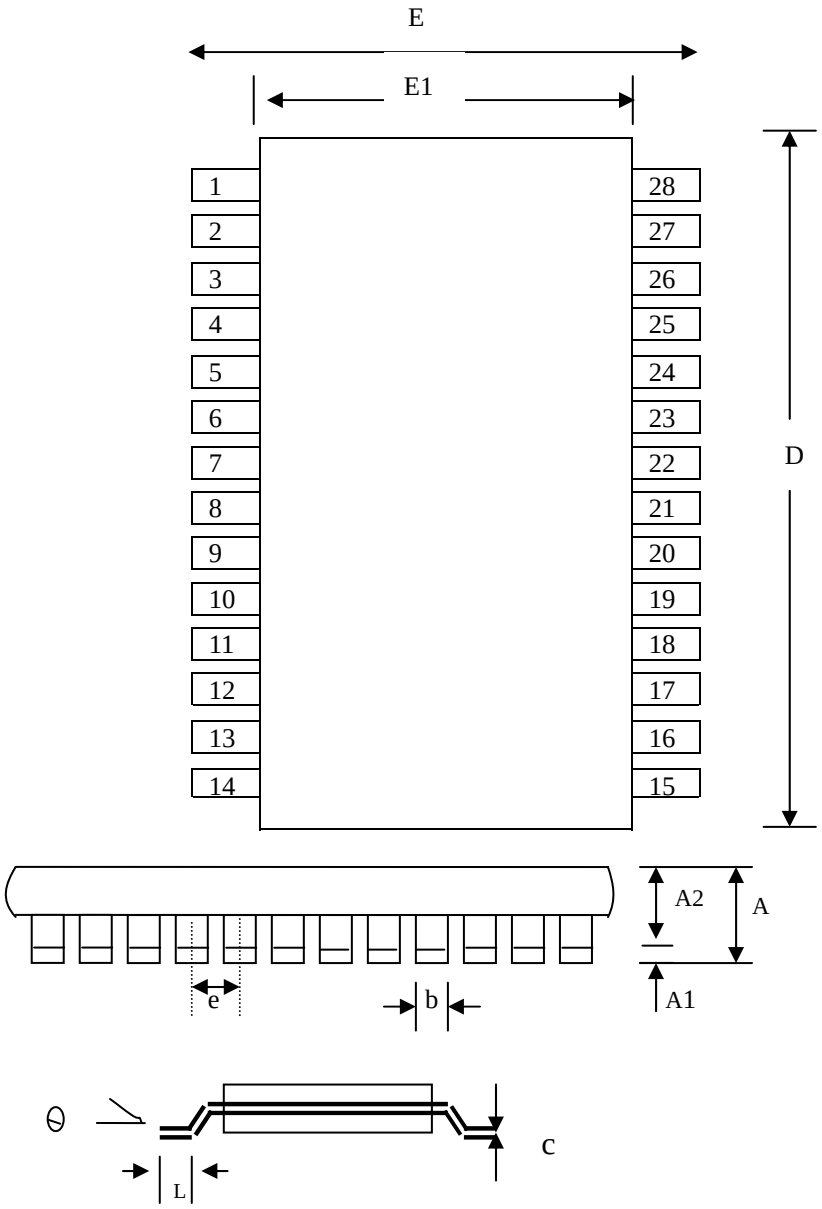
Output Filtering

The internal low pass filter has 3dB bandwidth at 100kHz. To limit out of band noise, an external 3rd order filter as shown in the application circuit diagram is recommended, especially when the chip is to drive a wide band amplifier.

Package Drawing No. 128-SS

Model	Package	Package Drawing No.
DA1166/F/G	28 pin SSOP	128-SS

Package outline drawing is shown as below:



Symbols	Dimensions in millimeters			Dimensions in inches		
	Min	Nom	Max	Min	Nom	Max
A	-----	-----	2.00	-----	-----	0.079
A1	0.05	----	-----	0.002	----	-----
A2	----	1.75	----	----	0.069	----
b	0.22	0.30	0.38	0.0086	0.012	0.015
c	0.13	0.15	0.20	0.0051	0.006	0.0079
D	10.08	10.20	10.34	0.397	0.402	0.407
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	----	0.65	----	----	0.0256	----
L	0.56	0.75	0.97	0.022	0.030	0.037
θ	-----	4^o	8^o	----	4^o	8^o