Techwell, Inc.

TW9903 – Multi-standard Video Decoder With High Quality Down Scaler

Preliminary Data Sheet

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TW9903 – NTSC/PAL/SECAM Analog to Digital Video Decoder with High Quality Scaler

Introduction and Features

Techwell' s TW9903 is a high quality NTSC, PAL, and SECAM video decoder plus high quality down scaler designed for multimedia applications.

TW9903 uses the mixed-signal 3.3V CMOS technology to provide a low-cost and low-power integrated solution. Minimum external components are required due to its integrated analog front-end containing AGC, clamping, and three 8-bit high speed ADCs. For composite inputs, an adaptive comb filter and luma/chroma processing produce exceptionally high quality pictures using proprietary techniques. A high quality internal scaling engine offers arbitrarily filtered down scaling of the output picture. A built-in Closed-Caption decoder and VBI data pass-through support data applications such Closed-Captioning and Intercast™.

Analog Video Decoder

- NTSC (M, 4.34) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection
- Advanced synchronization processing for VCR fast forward, backward, and pause mode
- Software selectable analog inputs allows any of the following combinations:
  - Up to four composite video inputs
  - Three composite and one S-video inputs
- Two 8-bit ADCs and analog clamping circuit.
- Fully programmable static gain or automatic gain control for the Y or CVBS channel
- Programmable white peak control for the Y or CVBS channel

Video processing

- Switchable Notch or 2H comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with programmable peaking.
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL and advanced synchronization processing for non-standard video signals
- Programmable hue, brightness, saturation, and contrast.
- Automatic color control and color killer
- High quality horizontal and vertical filtered scaling with arbitrary scale down ratio
- Detection of level of copy protection according to Macrovision standard

Video Output

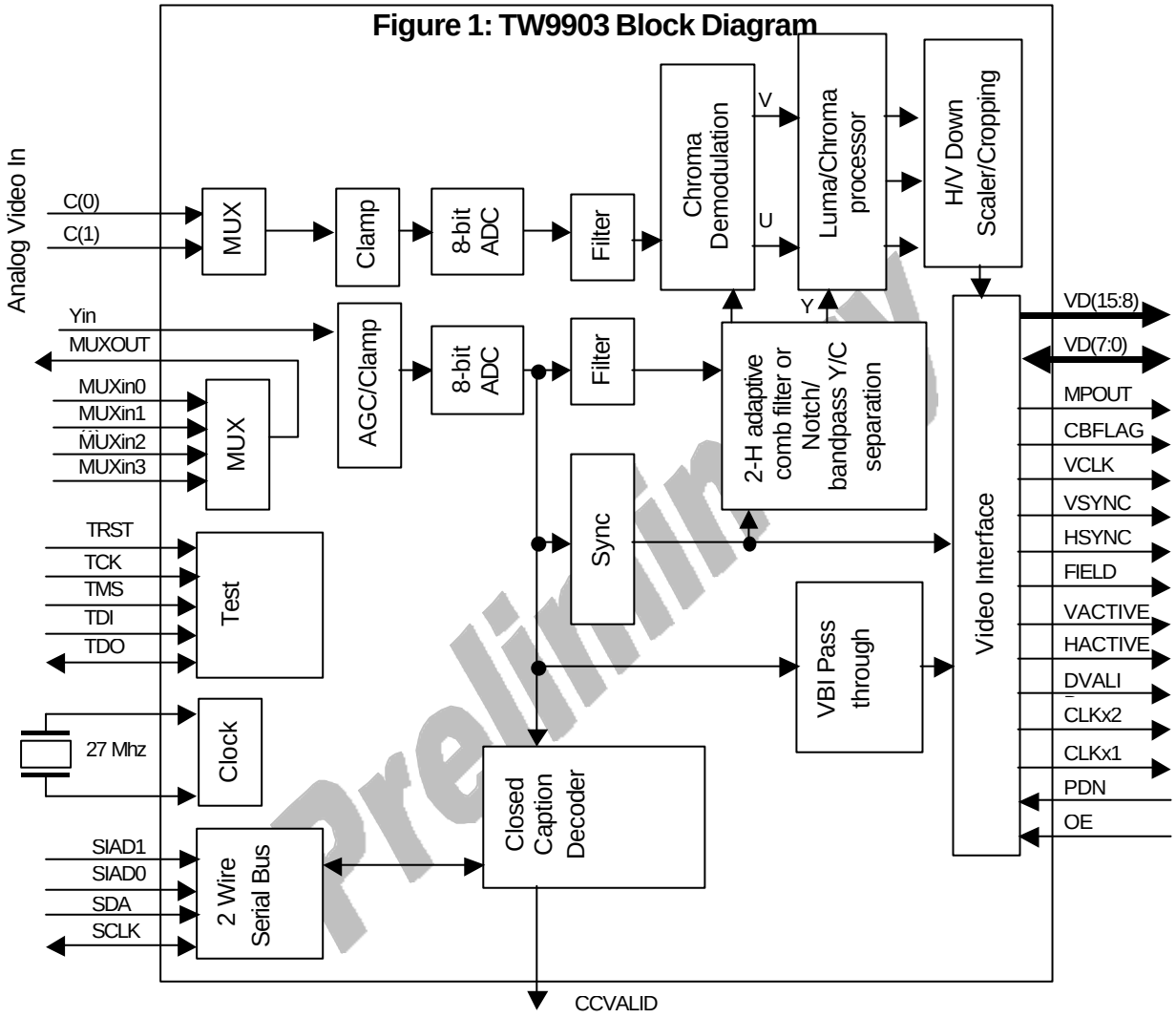
- Programmable output cropping
- VMI 1.4 compatible 8-bit or 16-bit pixel interface
- ITU-R 601 or ITU-R 656 compatible output YCbCr(4:2:2) output format
- Closed caption decoding
- VBI data pass through, raw ADC data for Intercast™

Miscellaneous

- Two wire MPU serial bus interface
- Power-down mode
- Typical power consumption 0.4W
- Single 27MHz crystal for all standards
- Supports 24.54MHz and 29.5MHz crystal for high resolution square pixel format
- 5V tolerant I/O
- 3.3 V power supply
- 100-pin PQFP package

Functional Description

Figure 1: TW9903 Block Diagram



Overview

Techwell's TW9903 is a high quality NTSC/PAL/SECAM video decoder that is designed for multimedia applications. It uses the mixed-signal 3.3V CMOS technology to provide a low-power integrated solution.

The TW9903 analog front-end is equipped with three separate analog channels that enable it to accept two possible analog video signal standards: composite or S-video. All channels include an analog multiplexer (MUX) for maximum flexibility in software controlled input selection. It is possible to connect up to four composite inputs at one time and allow the software to switch between them. Alternatively several combinations of composite inputs and S-Video component inputs may be switched under software control. (Four input channels of any format can be accommodated with but there is a maximum of 2 S-Video inputs and 2 component inputs.)

The front-end contains all the necessary circuits to simplify the system design. AGC and clamping circuits, and three 8-bit analog-to-digital converters (ADCs) convert inputs into digital signals for processing.

The TW9903 uses proprietary adaptive comb filter for chroma and luma separation to achieve high video quality. The image enhancement uses nonlinear methods to enhance picture sharpness with little overshoot.

The advanced synchronization processing can produce stable pictures for non-standard signal such as those produced by VCR during fast forward, rewind or pause.

The high quality scaler uses multi-tap poly-phase decimation filter to reduce aliasing effects. It can be programmed to scale-down the output picture to an arbitrary ratio with cropping.

The TW9903 supports flexible pixel interface. It outputs YCbCr (4:2:2) data stream over 8-bit or 16-bit data path. The output is VMI 1.4 compatible.

A 2-wire serial MPU interface is used to simplify system integration. All the functions can be controlled through this interface.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are three analog channels with clamping circuits and ADCs. The Y channel has 4-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). Its four inputs are identified as MUX0, MUX1, MUX2 and MUX3. The C_Pb channel has 2-input multiplexer. Its two inputs are identified as C_PbIn0 and C_PbIn1. The C_Pb channel is internally clamped to the zero level of the bipolar input source when enabled.

Video Source Selection

All analog signals should be AC-coupled to these inputs.

The Y channel analog multiplexer selects one of the four inputs MUX[0-3]. MUX[0-3] can be connected to composite video inputs or the Y signal of an S-Video or component input. When decoding a S-Video input, the Y signal should connect to one of the MUX inputs and the C signal to C_PbIn0 or C_PbIn1.

Software selectable analog inputs allow several possible input combinations:

1. Up to four composite video inputs. 2. Three composite, one S-video.

The input video signals in any certain channel maybe momentarily connected together through the equivalent of a 200 ohm resistor during multiplexer switching. Therefore, the multiplexer cannot be used for switching on a real-time pixel-by-pixel basis.

Clamping and Automatic Gain Control

All three analog channels have built-in clamping circuit that restore the signal DC level. The Y channel restores the back porch of the digitized video to a level of 64 or a programmable level. The C_Pb channel restores the back porch of the digitized video to a level of 128. This operation is automatic through internal feedback loop.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. A programmable white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Analog to Digital Converter

TW9903 contains three 8bit pipelined ADCs that consume less power than conventional flash ADC. The output of the Clamp and AGC connects to one ADC that digitizes the composite input or the Y signal of the S-Video input. The second ADC digitizes the C signal when decoding S-video signal.

Sync Processing

The sync processor of TW9903 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal sync detector detects the presence of a horizontal sync tip by examining low-pass filtered input samples whose level is lower than a threshold. After sufficient low levels are detected, a horizontal sync is recognized. Additional logic is also used to avoid false detection on glitches.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. The PLL has free running frequency that matches the standard raster frequency. It also has wide lock-in range for tracking any non-standard video signal.

In case the horizontal sync is missing, a "free-wheel" mechanism keeps generating horizontal sync signal until horizontal sync is detected again. This option can also be turned off for some applications that determine video loss by detecting the existence of horizontal sync.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. It achieves the functionality of a PLL without the complexity of a PLL. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field. The field logic can also be controlled to toggle automatically while tracking the input.

Color Decoding

Y/C separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter is shown in the filter curve section.

In the case of comb filter, the TW9903 separates luma (Y) and chroma (C) of a NTSC composite video signal using a proprietary 2H adaptive comb filter. The filter uses a two-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the 90-degree phase difference on adjacent lines of a PAL chroma signal, the 2H line memory are used optionally to provide an adequate PAL comb filter performance.

Due to the line buffer used in the comb filter, there is always one line processing delay in the output images in general except the PAL comb filter case, which has no line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Color demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. The mixing frequency is equal to the sub-carrier frequency for NTSC and PAL. After the mixing, a low-pass filter is used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the mixing frequency is 4.286Mhz. After the mixer and low-pass filter, it yields the FM modulated chroma. The SECAM demodulation process therefore consists of low-pass filter, FM demodulator and de-emphasis filter. The filter characteristics are shown in filter curve section. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

During S-video operation, the Y signal bypasses the comb filter. The C_Pb signal connects directly to the color demodulator. During component input operation, all the chroma processing and color demodulator blocks are bypassed.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then increased or decreased in amplitude accordingly. The range of ACC control is –6db to +24db.

This function is always enabled to provide consistent image quality under different signal conditions.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be "killed". The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer function. The color killer function can be disabled by programming a low threshold value.

Automatic standard detection

The TW9903 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

TW9903 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by the TW9903

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	625	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The TW9903 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW9903 video decoder also performs a coring function. It can force all values below a certain level, programmed in the Coring Control Register, to zero. This is useful because human eyes are sensitive to variations in nearly black images. Changing levels near black to true black, can make the image appears clearer.

Gamma

Y Gamma function is provided to compensate for different display types. Four pre-programmed Gamma levels can be selected through registers.

Sharpness

The TW9903 also provides a sharpness control function through control registers. It provides the control in 16 steps up to +12db. The center frequency of the enhancement curve is around 3.5Mhz. It also provides a high frequency coring function to minimize the amplification of high frequency noise. The coring level is adjustable through the Coring Control register. The same function can also be used to soften the images. This can be used to provide noise reduction on noisy signal.

To further enhance the image, a programmable vertical peaking function is provided for up to +6db of enhancement. A programmable coring level can be adjusted to minimize the noise enhancement.

The Hue and Saturation

When decoding NTSC signals, TW9903 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Closed Caption Decoding

TW9903 has a built-in Closed Caption (CC) and Extended Data Services (EDS) decoder that adheres to the EIA-608 standard. This decoder can be enabled or disabled independently on line 21 and line 284 for NTSC.

The decoded data is made available through CC_DATA and CC_STATUS registers that can be accessed through the 2-WIRE SERIAL MPU interface.

Power Management

The TW9903 can be put into power-down mode in which its clock is turned off for most of the circuits. The Y, C/Pr and Pb path can be separately powered down.

Control Interface

The TW9903 registers are accessed via 2-WIRE SERIAL MPU interface. It operates as a slave device. Serial clock and data lines, SCL and SDA, transfer data from the bus master at a rate of 400 Kbits/s. The TW9903 has two serial interface address select pins to program up to four unique serial addresses TW9903. This allows as many as four TW9903 to share the same serial bus. Reset signals are also available to reset the control registers to their default values.

Output Interface

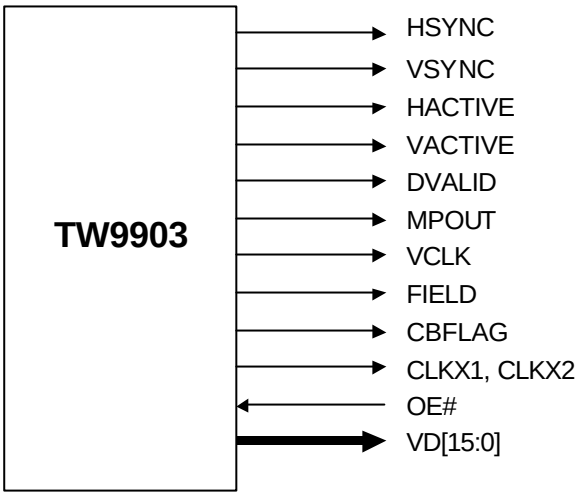


Figure 2. TW9903 Video Data Output Interface

The TW9903 supports a synchronous 8-bit or 16-bit YCbCr 4:2:2 data output stream. The interface consists of VD [15:0], HSYNC, VSYNC, HACTIVE, VACTIVE, DVALID, MPOUT, VCLK, FIELD, CBFLAG, and OE# as shown in Figure 2. In 8-bit output mode, Reg0x03[6] is "0".In 16-bit output mode,Reg0x03[6] is "1".

The TW9903 outputs all pixel data and control signals synchronous with CLKX2 rising edge for both the 8-bit format and the 16bit format.

The mapping of video data stream formats is shown in Table 2. When the output is configured for a 8-bit format, the data is output on pins VD[15:8] with 8 bits of chrominance data preceding 8 bits of luminance data for each pixel output. The data output is synchronous to the rising edge of CLKX2. When the output is configured for a 16-bit format, the luminance data is output on VD[15:8], and the chrominance data is output on VD[7:0]. In 16-bit mode, the data output is synchronous with the rising edge of CLKX2 and VD[15:0] data changes when CLKX1 goes high. Figure3a shows 8-bit video data output timing. Figure3b shows 16-bit video data output timing.

Pin Name		VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
CK1	2N	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0
	2N+1	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0
CK2	4N	Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0								
	4N+1	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
	4N+2	Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0								
	4N+3	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
ITU-R BT.656		SAV and EAV sequence, YCbCr data and blanking data are transferred on these pins															

Table 2. Output mapping between various data formats

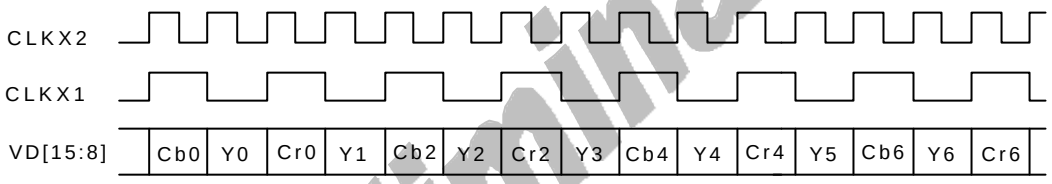


Figure 3a. 8-bit Video Data Output timing

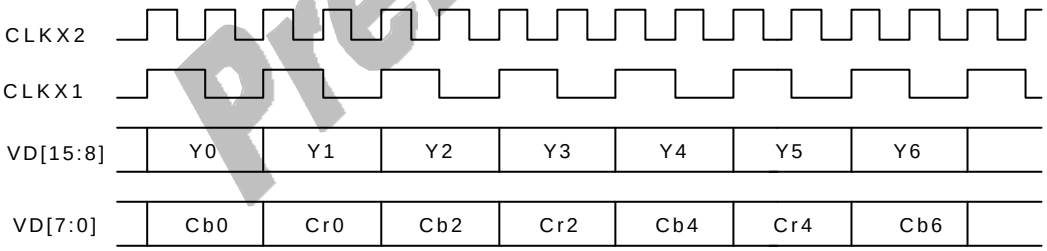


Figure 3b. 16-bit Video Data Output Timing

Clock and Control Signal Output

The default output format of TW9903 is a synchronous 8-bit YCbCr 4:2:2 data format with separate syncs and flags. Video data is compliant with ITU-601format. HSYNC, VSYNC, HACTIVE, VACTIVE, LVALID (MPOUT), FIELD have the same output timings in both 8-bit output mode and 16-bit output modes. All control signals are synchronous with the rising edge of CLKX2.and they are illustrated with default polarity register setting values bellow.

HSYNC, VSYNC and FIELD

The HSYNC and VSYNC output timing is VMI v1.4 compliant. The leading edge of HSYNC depends on the input video signal. The pulse width of HSYNC is programmable from 8-128 CLKX1 cycles. The leading edge of VSYNC also depends on the video input. It typically occurs on the low period of first serration pulse of the video signal. The trailing edge of VSYNC follows the HSYNC in order to be VMI compliant. For the start of the odd field, it occurs 64 CLKX2 cycles after the trailing edge of HSYNC that follows the last equalization pulse of the input. For the indication of the even field, the trailing edge of VSYNC occurs 64 CLKX2 cycles after the leading edge of HSYNC that follows the last equalization pulse of the input. In this latter case, the HSYNC width has to be set at least 64 CLKX1 cycles. The FIELD output indicates the input video source field state as determined by the decoder. It changes state at the leading edge of VSYNC to reflect the state of following field. If the field cannot be determined due to video source noise, it will toggle its state for each field until it can be corrected by the source. Figure4 shows HSYNC output timing. HSYNC changes when CLKX1 goes high. Figure 5a shows Odd field VSYNC and HSYNC Timing. Figure 5b shows Even field VSYNC and HSYNC timing. Figure 6 shows FIELD and VSYNC Timing. The leading edge of VSYNC changes with FIELD signal. The video timing of these outputs is also illustrated in Figure 7a and 4b.

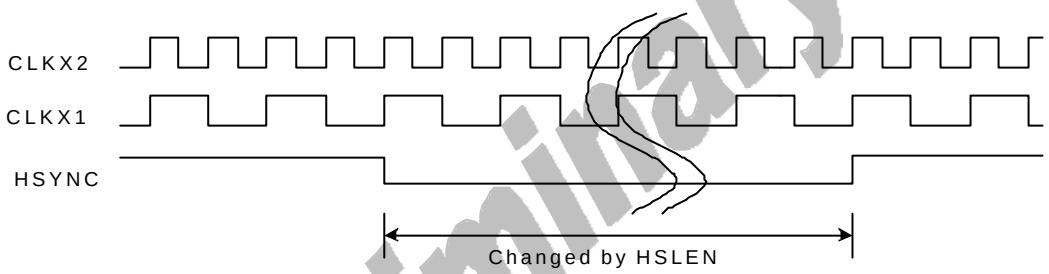
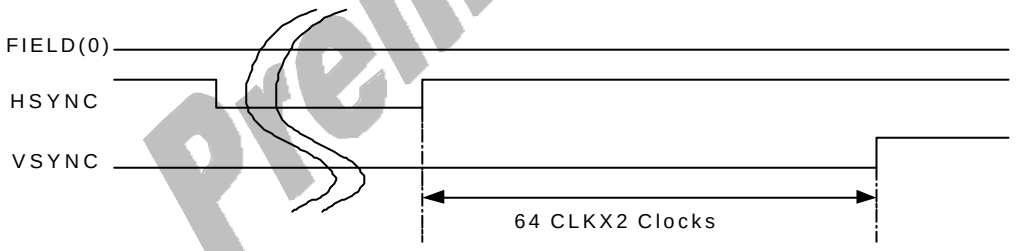


Figure 4 HSYNC output timing



Fgure 5a. Odd field VSYNC and HSYNC timing

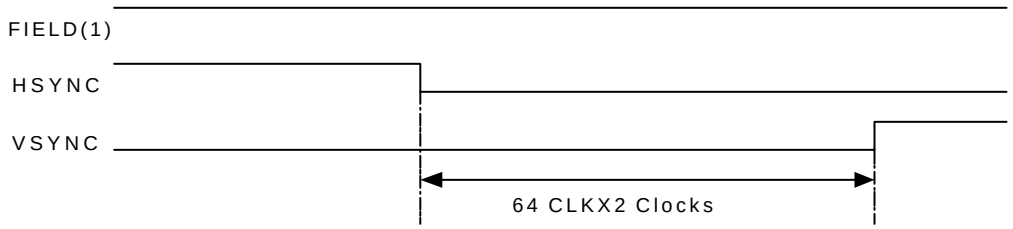


Figure 5b. Even field VSYNC and HSYNC timing

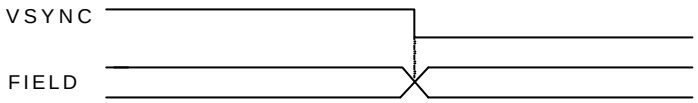


Figure 6. VSYNC and FIELD timing

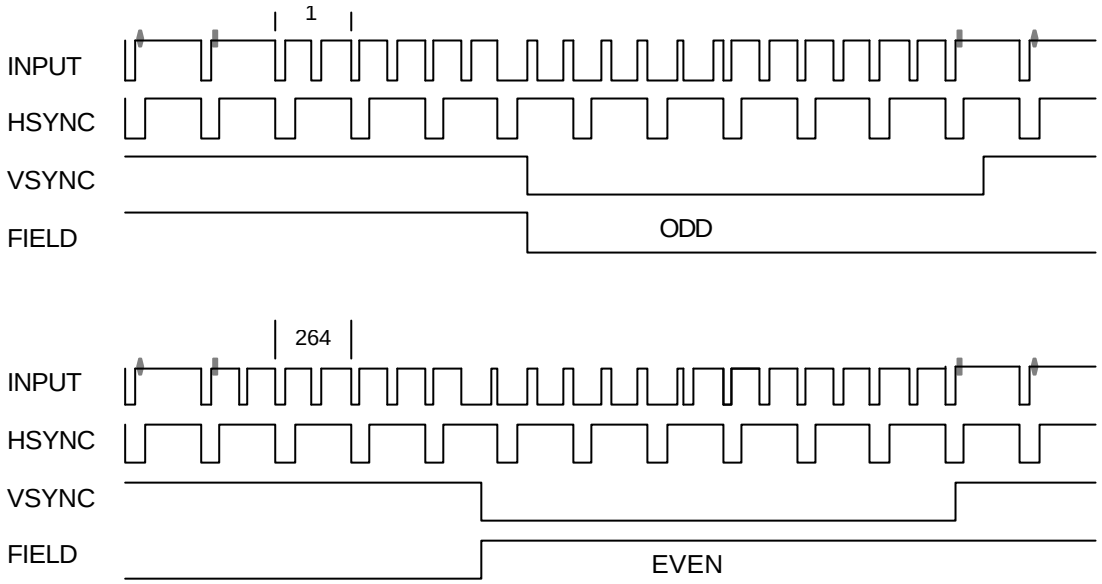


Figure 7a. HSYNC, VSYNC and FIELD timing for NTSC field transition

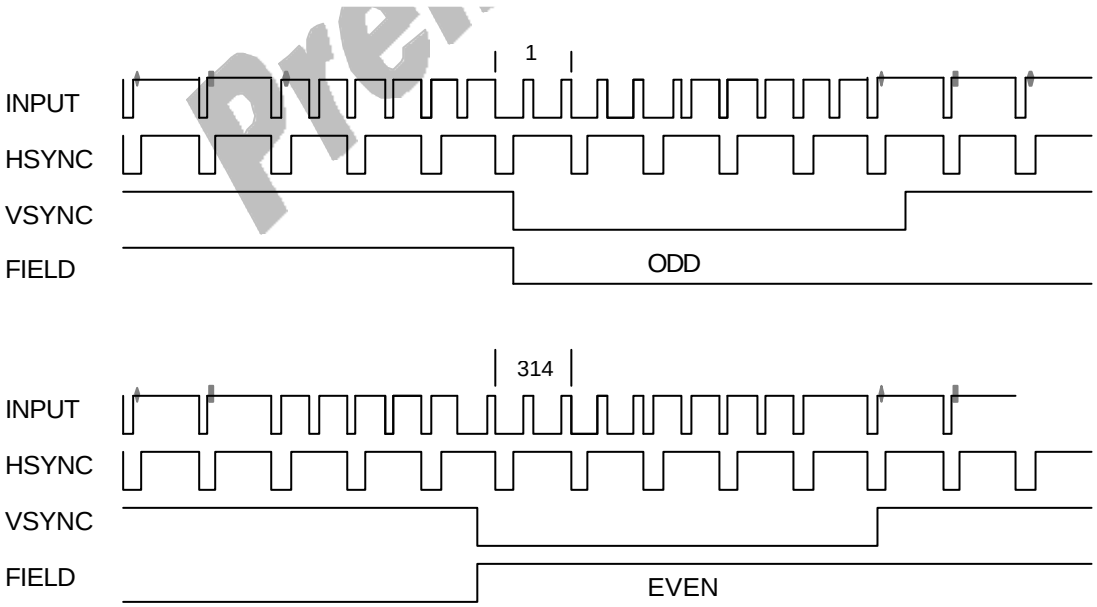


Figure 7b. HSYNC, VSYNC and FIELD timing for PAL(B,D,G,H,I) field transition

HACTIVE

TW9903 outputs two type of HACTIVE signal on HACTIVE pin. TW9903 maintains video HACTIVE and VBI HACTIVE internally. If VBI EN(Reg0x19[7]) is set to "1", TW9903 outputs VBI HACTIVE on VBI output line. TW9903 outputs VBI HACTIVE on the line that LVALID is high and VACTIVE is low. If RTSEL(Reg0x19[2:0]) is set to 0x7,LVALID signal can be observed on MPOUT pin. TW9903 outputs video HACTIVE except VBI line on HACTIVE pin. TW9903 outputs video HACTIVE in whole line per frame or some lines selected by HA_EN(Reg0x19[4]) and VSCTL(Reg0x03[3]). During the lines that VACTIVE is low, if HA_EN is set to "1", TW9903 outputs video HACTIVE, if HA_EN is set to "0", TW9903 doesn't output video HACTIVE. During those lines that VACTIVE is high and LVALID is low, if VSCTL is set to "1", TW9903 outputs video HACTIVE. If VSCTL is set to "0", TW9903 doesn't output video HACTIVE. In VBI enable mode (Reg0x19[7]=1), VBI HACTIVE has higher priority than video HACTIVE in VBI output line. The video HACTIVE is asserted at the start of the active video synchronous to the rising edge of CLKX2. . When the horizontal count of CLKX1 cycles matches the setting of HDELAY register, video HACTIVE is asserted. It will be asserted for a period matches the setting of HACTIVE register before it is de-asserted. HACTIVE signal changes when CLKX1 goes to high. If BYPASS Register bit is set to "0", the number of CLKX2 clocks from the leading edge of HSYNC to the leading edge of video HACTIVE is always fixed during active video lines. Figure 8 shows video HACTIVE timing. Figure 9a shows VBI HACTIVE timing at the first VBI line. Figure 9b shows VBI HACTIVE timing during VBI output line. Figure 9c shows VBI HACTIVE timing at the last VBI line.

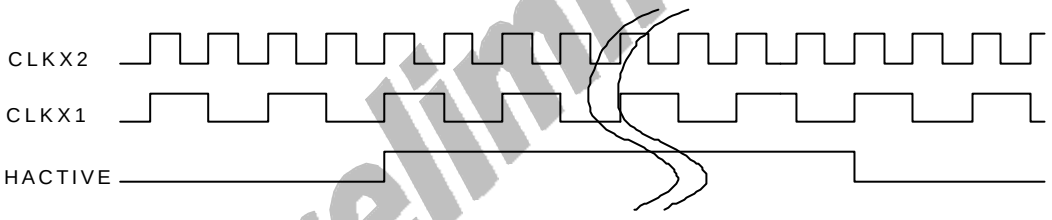


Figure 8. VIDEO HACTIVE timing

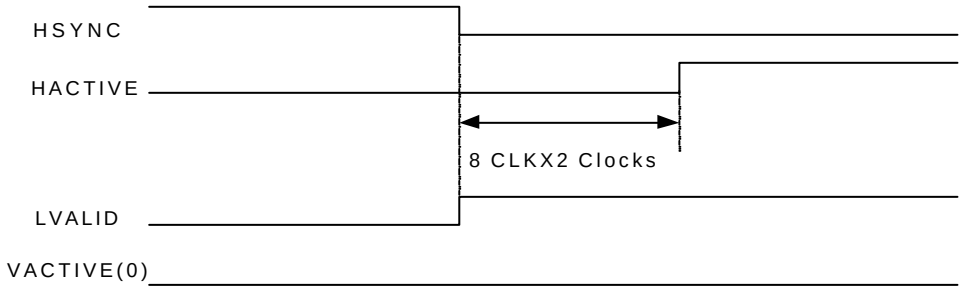


Figure 9a . VBI HACTIVE timing at the first VBI line

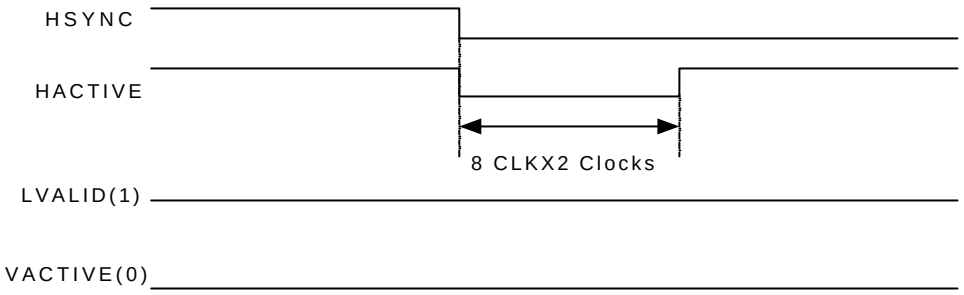


Figure 9b. VBI HACTIVE timing during VBI lines

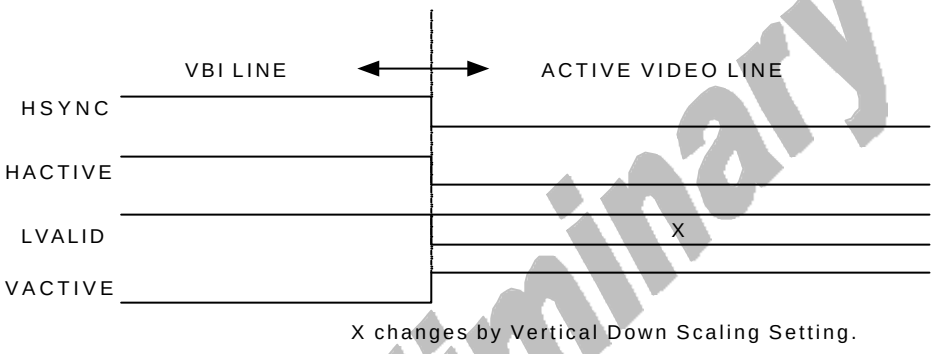


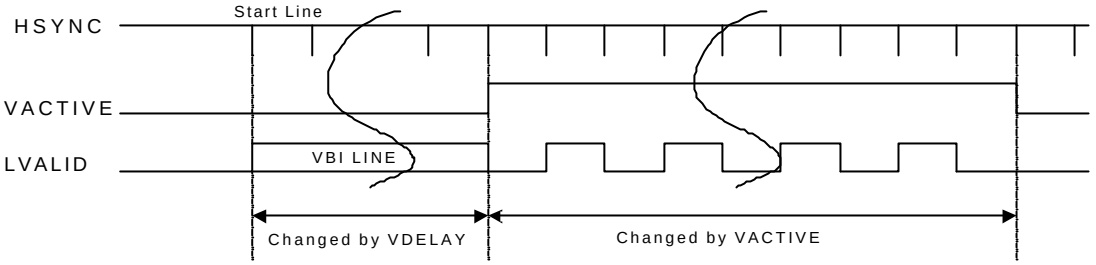
Figure 9c. VBI HACTIVE timing at the last VBI line

VACTIVE

VACTIVE is used to indicate the start of active video line. When the line count in each field matches the VDELAY register setting, VACTIVE is asserted. It will remain asserted for the number of scan lines that match the setting of VACTIVE register before it is de-asserted. VACTIVE changes at the leading edge of HSYNC as illustrated in Figure 9c. Figure 10 also shows VACTIVE timing.

LVALID

LVALID is used to indicate the valid line of video line. If VBI EN(Reg0x19[7]) is set to "1', LVALID goes high from VBI start line(line 10 in 525 line video system and line 6 in 625 line video system) to the start line of active video line. If VBI EN(Reg0x19[7]) is set to "0', LVALID keeps low during the same lines. When VACTIVE is asserted and active video line is a valid line as determined by Vertical down scaling, LVALID stays high for the line. If active video line is not a valid line as determined by Vertical down scaling, LVALID stays low for the line. LVALID changes at the leading edge of HSYNC as shown in Figure 9a and 9c. Figure 10 also shows LVALID timing of typical vertical down scaling output mode.



Start Line in both odd and even field : 6(625 line video system)

10(525 line video system)

LVALID in VBI LINE is always high if VBI EN is "1".

Figure 10. VACTIVE and LVALID timing

DVALID and VCLK

In a 601 pixel format, the active video resolutions are either 720 x 480 for the 525/60 video systems or 720 x 576 for the 625/50 systems. In a square pixel operation, the active video resolutions are either 640 x 480 for the 525/60 video systems or 768 x 576 for the 625/50 systems. The DVALID is used to indicate the valid active pixels data output during a active video line. DVALID is also used to indicate valid VBI data. If VBI EN(Reg0x19[7]) is set to "1",DVALID always has valid timing while HACTIVE is active .

The DVALID can be configured to output in three different formats. This is determined by the DVALID (0x03[5:4]) register.

In the first format, the DVALID output is asserted for valid pixel during the valid pixel time on video lines. The VCLK is gated by DVALID for proper pixel data strobing. For 8-bit output mode, VCLK is the inverted CLK2 and masked to "0" value while DVALID is invalid in order to indicate valid pixel data. For 16-bit output mode, CLKX1 is used instead of CLK2.

In the second format, the DVALID output has the same timing as the first formats. VCLK is inverted CLKX2 or CLKX1. In 8-bit output mode, LEN(Reg0x3[6]=0),VCLK is inverted CLKX2.In 16-bit output mode, LEN(Reg0x03[6]=1),VCLK is inverted CLKX1.

In the third format, the DVALID has the same timing as VCLK of the first format. VCLK has the same timing as the second formats.

VCLK wave changes by LEN(Reg0x03[6]) setting. If LEN is set to "1", its wave form will be similar to inverted CLKX1. If LEN is set to "0", its wave form will be similar to inverted CLKX2. In third format, DVALID signal also changes by LEN setting. DVALID signal and VCLK signal don't have any hazard pulse. Both DVALID and VCLK can be used as clock pulse.

If CNTL656(Reg0x19[3]) is set to "0" in down scaling mode, TW9903 outputs Y invalid data as 0x10 and CbCr invalid data as 0x80 during HACTIVE active time. If CNTL656 is set to "1" in down scaling mode, TW9903 outputs Y invalid data 0x00 and CbCr invalid data 0x00. In 8-bit output mode, the CbCr invalid data is output first and then Y invalid data. TW9903 outputs only even number invalid data in invalid period during HACTIVE active time. TW9903 always outputs CbCr and Y 2-byte pair format data as valid data or invalid data.

These are illustrated in Figure 11a, 11b, 11c, 11d, 11e, and 11f.

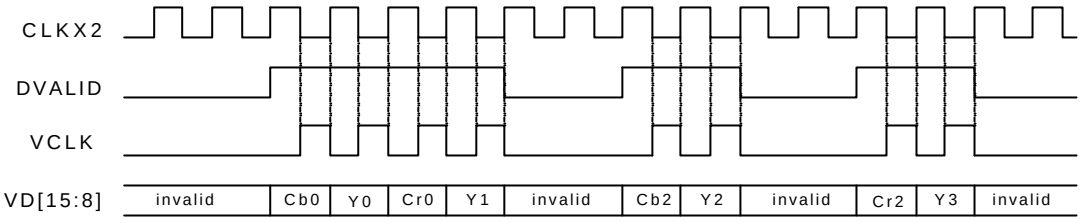


Figure 11a. 8-bit DVALID first format timing

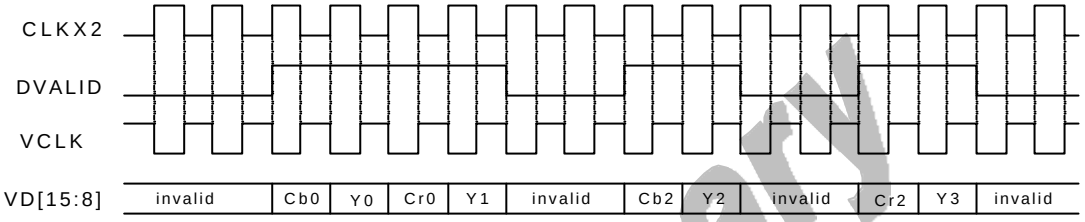


Figure 11b. 8-bit DVALID second format timing

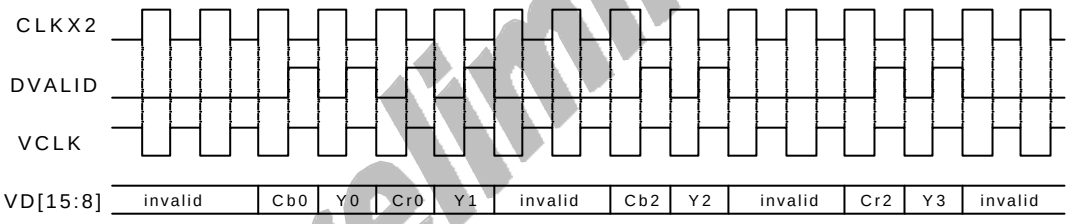


Figure 11c. 8-bit DVALID third format timing

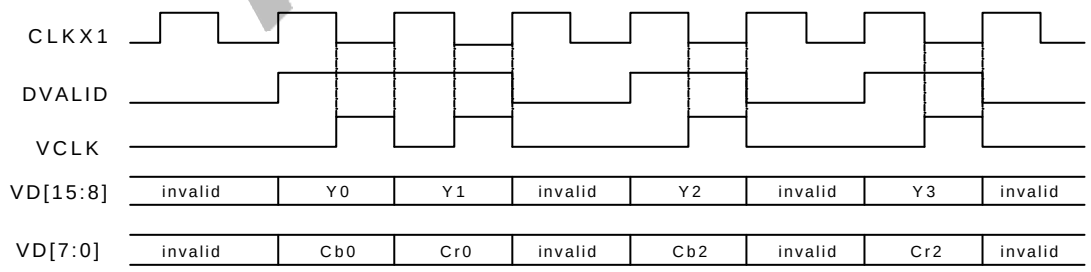


Figure 11d. 16-bit DVALID first format timing

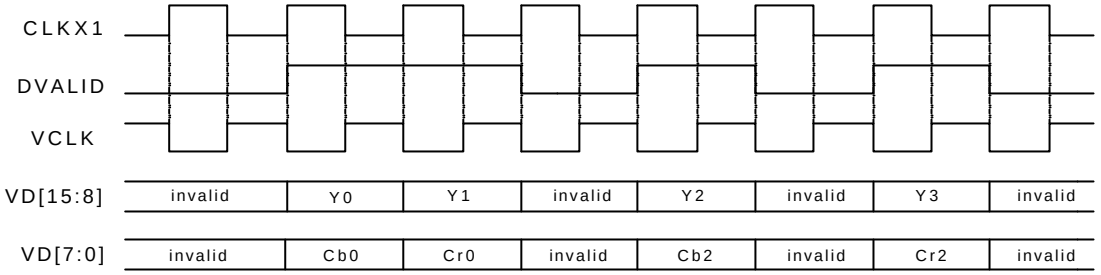


Figure 11e. 16-bit DVALID second format timing

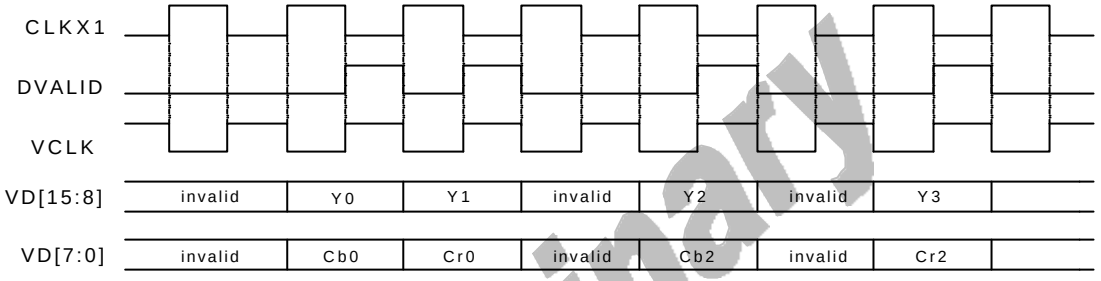


Figure 11f. 16-bit DVALID third format timing

CbCr data and CBFLAG

In 8-bit output mode, TW9903 always outputs CbCr data when CLKX1 is high in video HACTIVE active time as illustrated in Figure 3a. Even if TW9903 outputs H scaling down active pixel, CbCr data will be output when CLKX1 is high. Because TW9903 always outputs 2-byte pair format data on both valid pixel time and invalid pixel time. TW9903 outputs Cb data as the first valid CbCr data during video HACTIVE active time in 8-bit output mode. In 16-bit output mode, TW9903 outputs Cb data as the first valid CbCr data on VD[7:0] pins in video HACTIVE active time.TW9903 also has the optional CBFLAG signal. If CBFLAG is high during both DVALID and video HACTIVE active time, CbCr data is Cb data. If CBFLAG is low, then CbCr data is Cr data. Figure 12a shows 8-bit output mode CBFLAG timing. Figure 12b shows 16-bit output mode CBFLAG timing.

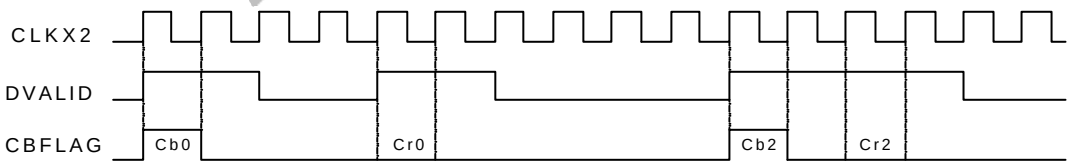


Figure 12a. 8-bit output mode CBFLAG timing

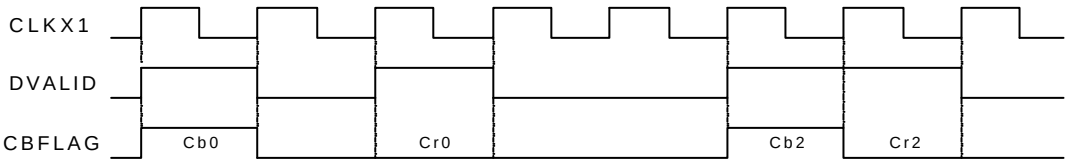


Figure 12b. 16-bit output mode CBFLAG timing

CLKX2 and CLKX1

CLKX2 is the delayed and buffered XTI clock signal. CLKX1 is 1/2 frequency clock signal of CLKX2. VCLK clock output is generally used as data strobing clock for down stream device with DVALID register setting as (Reg0x03[5:4]=01 or 10).

ITU-R BT.656

If MODE(Reg0x03[7]) is set to "1" , TW9903 outputs ITU-R BT.656 compatible data on VD[15:8] in 8-bit output mode and on VD[15:0] in 16-bit output mode. All of control signals, sync signals, and clock signals have the same timing regardless of MODE bit setting. Only VD[15:8] or VD[15:0] video data changes. If MODE bit is set to "1",All data between EAV code and SAV code are filled by 0x80 for CbCr data and 0x10 for Y data. If MODE is set to "1", this blanking data and SAV/EAV code are the only difference from CCIR601 mode(MODE=0). TW9903 doesn't output SAV/EAV code if the line doesn't have HACTIVE signal. SAV code is generated on 4 CLKX2 clock timing before the leading edge of HACTIVE. EAV code is generated on 4 CLKX2 clock timing after the trailing edge of HACTIVE. 8-bit output mode is normally used in ITU-R BT.656 mode. But even if TW9903 is in 16-bit output mode, if MODE is set to "1", TW9903 output 4 bytes SAV/EAV code on VD[15:0] pins and the rest of HACTIVE non active period will be filled by Y 0x10 data and CbCr 0x80 data optionally. The changing timing of F bit and V bit in forth byte of SAV/EAV code are decided by VDELAY and VACTIVE register setting. EAV code will change before SAV code changes to maintain the compatibility with ITU-R BT.656 standard. Forth byte of SAV/EAV code is comprised of the following 8 bytes eventually. ITU-R BT.656 sequence is consisted of the following one by (a)-(b)-(c)-(d)-(e)-(f)-(a)-(b)- …… If VIPCFG register bit is set to "1", MSB bit 7 of forth byte of SAV/EAV code is changed to "0' for special application.

	EAV	SAV	
(a)	0xB6	0xAB	Odd field V Blanking Line
(b)	0x9D	0x80	Odd field Active Video Line
(c)	0xB6	0xAB	Odd field V Blanking Line
(d)	0xF1	0xEC	Even field V Blanking Line
(e)	0xDA	0xC7	Even field Active Video Line
(f)	0xF1	0xEC	Even field V Blanking Line

The output timing is illustrated in Figure 13a,13b. The SAV and EAV sequences are shown in Table 3.

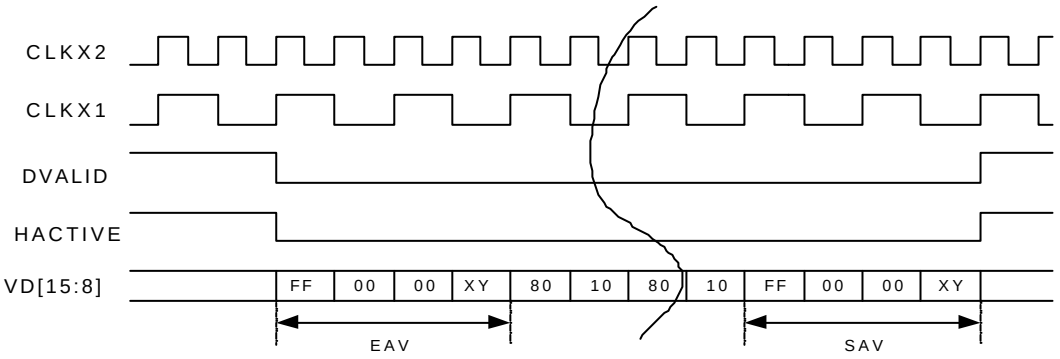


Figure 13a. 8-bit output mode ITU-R BT.656 Compatible Output timing

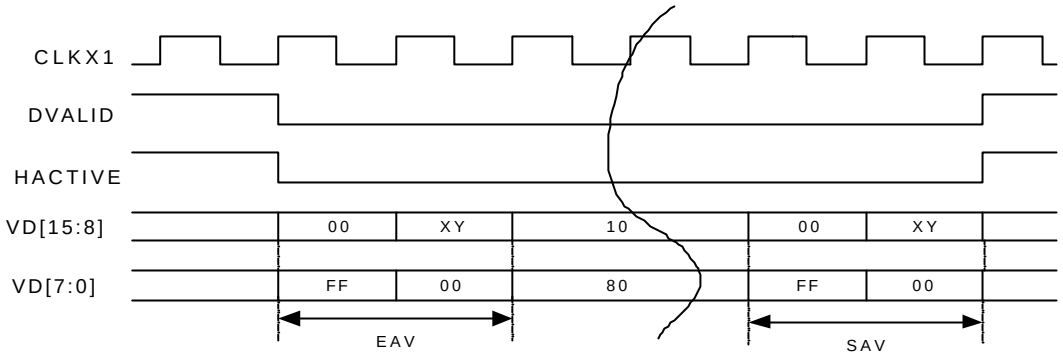


Figure 13b.Optional 16-bit output with ITU-R BT.656 control code

Table 3. ITU-R BT.656 SAV and EAV code sequence

	VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8
First byte	1	1	1	1	1	1	1	1
Second byte	0	0	0	0	0	0	0	0
Third byte	0	0	0	0	0	0	0	0
Forth byte	*C	F	V	H	V XOR H	F XOR H	F XOR V	F XOR V XOR H
H = 0 - SAV, 1 – EAV V = 1 - blanking, 0 – elsewhere F = 0 - field 1, 1 - field 2								

*C is set by VIPCFG register bit.

Down-scaling and Cropping

The TW9903 provides two methods to reduce the amount of output video pixel data, downscaling and cropping. The downscaling provides full video image at lower resolution. Cropping provides only a portion of the video image output. All these mechanisms can be controlled independently to yield maximum flexibility in the output stream.

TW9903 Down-Scaling

The TW9903 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses 2-tap to 5-tap 8-phase interpolation filter dynamically for luma depending on the horizontal and vertical scaling ratio. Besides its normal scaling function, the scaling logic can be doubled as additional line comb filter to either reduce crawling dot or cross color at the expense or resolution.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW9903 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register. The 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: $HSCALE = [720/N_{pixel\_desired}] * 256$

PAL: $HSCALE = [(720/N_{pixel\_desired})] * 256$

Where: $N_{pixel\_desired}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

$HSCALE = [(720/320)] * 256 = 576 = 0x0240$

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

$HSCALE = [(640/320)] * 256 = 512 = 0x200$

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW9903. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

60Hz system: $VSCALE = [240/ N_{line\_desired}] * 256$

50Hz system: $VSCALE = [288/ N_{line\_desired}] * 256$

Where: $N_{line\_desired}$ is the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table 4.

TW9903 Cropping

Cropping allows only subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the unscaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858. The HDELAY should be set to 106 and HACTIVE set to 720. For PAL output at 13.5 MHz rate, the total number of pixels is 864. The HDELAY should be set to 108 and HACTIVE set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

Table 4 shows some popular video formats and its recommended register settings. The CCIR601 format refers to the sampling rate of 13.5 MHz. The SQ format for 60 Hz system refers to the sampling rate of 12.27 MHz, and the SQ format for 50 Hz system refers to the use of sampling rate of 14.75 MHz.

Scaling Ratio	Format	Total Resolution	Output Resolution	HSCALE values	VSCALE (frame)
1:1	NTSC SQ	780x525	640x480	0x0100	0x0100
	NTSC CCIR601	858x525	720x480	0x0100	0x0100
	PAL SQ	944x625	768x576	0x0100	0x0100
	PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)	NTSC SQ	390x262	320x240	0x0200	0x0200
	NTSC CCIR601	429x262	360x240	0x0200	0x0200
	PAL SQ	472x312	384x288	0x0200	0x0200
	PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400
	NTSC CCIR601	214x131	180x120	0x0400	0x0400
	PAL SQ	236x156	192x144	0x0400	0x0400
	PAL CCIR601	216x156	180x144	0x0400	0x0400

Table 4. HSCALE and VSCALE value for some popular video formats.

VBI Data Processing

A frame of video is composed of 525 lines for NSTC and 625 for PAL. The time required for the electron beam to move from the bottom to the top of the screen is the vertical blanking period, and it requires the equivalent of 21 horizontal active video scan lines. This portion is normally not seen. During vertical blanking period, video lines before VBI Data are used for equalizing and synchronization. In 525 line video system, many TV channels have special VBI data from line 10 to line 21 or line22 in both odd and even fields. In 625 line video system, many TV channels have VBI data from line 6 or 7 to line 23 in both odd and even fields. They are normally regarded as the Vertical Blanking Interval or VBI portion of the video signal.

TW9903 VBI Overview

In the default configuration of the TW9903, the VBI region of the video signal is treated the same way as the real image signal. It will decode this region of signal as if it was video by Y/C separation and horizontal scaling. The TW9903 can also be configured in a mode known as VBI raw data mode. In this mode, the raw VBI region data (AD converter output data of input VIDEO signal) can be captured for later processing by software. It is done as follows. First, the analog composite video signal is digitized. Then, it is converted to 8-bit data stream at the input clock frequency, normally 27MHz for a 27MHz crystal. Finally, the data is output to the VD [15:8] data pins in 8-bit output mode. It can also be output as a 16-bit data stream on pins VD [15:0] at half of the crystal rate in 16-bit output mode.

There are three modes of operation for the VBI raw data output feature.

1) If VBI EN(Reg0x19[7]) is set to "0". VBI raw data output mode is disabled. This is the default mode of operation. In this mode, the decoder doesn't output valid data on VBI lines.

2) If VBI EN(Reg0x19[7]) is set to "1", VBI raw data output mode is enabled.TW9903 outputs a clock rate VBI data stream during VBI data lines from line 6 (in 625 line video system) or line10 (in 525 line video system) to the leading edge of VACTIVE. If LVALID is high and VACTIVE is low, the line is VBI data output line. When VACTIVE is high, the TW9903 outputs normal YCbCr data. Therefore, this mode can be used to capture both VBI raw data and normal YCbCr video data simultaneously.

3) If VBI Frame mode (Reg0x19[5]) is set to "1", VBI frame output mode is enabled. VBI Frame mode bit has the higher priority than VBI EN bit. In this mode, TW9903 treats every scan line of the signal as a vertical interval line and outputs clock rate raw data on every line. Therefore, no video image data is output. This mode can be used to capture raw data for later processing. This mode of operation is designed for use in still-frame capture/processing applications.

When the device is set to VBI raw data output mode, the VBI data is output during HACTIVE signal period. The DVALID or gated VCLK are used to indicate valid VBI data as in the normal video data output mode .

A video/graphic controller should be able to do the following to capture VBI data output. It should keep track of the line count in order to select specific lines for VBI data processing. It must be able to use DVALID or VCLK for data qualification, and load only the valid data.

VBI Frame Output Mode

In VBI frame output mode the TW9903 is generating VBI data all the time (i.e., there is no VBI active interval). In essence, the TW9903 is acting as an ADC continuously sampling the entire video signal at the crystal rate. The TW9903 generates HSYNC, VSYNC and FIELD timing signals in addition to the VBI data, but the DVALID, HACTIVE, and VACTIVE signals are all held high during VBI frame output operation. The behavior of the HSYNC, VSYNC, and FIELD timing signals is the same as normal YCbCr 4:2:2 output operation. The HSYNC, VSYNC, and FIELD timing signals are used by the video processor to detect the beginning of a video frame/field, at which point it can start to capture a full frame/field of VBI data.

VBI Byte Order

In 8-bit output mode, if VBI Byte Order (Reg0x19[6]) is set to "0", 8-bit VBI output data have the following order.

VBI2-VBI1-VBI4-VBI3-VBI6-VBI5-……

Even number VBI data is output at first and odd number VBI data is output next. This function is useful for Motorola type CPU or similar logic. If VBI Byte Order (0x19[6]) is set to "1", 8-bit VBI output data have the following order.

VBI1-VBI2-VBI3-VBI4-VBI5-VBI6-……

Odd number VBI data is output at first and even number VBI data is output next. This function is useful for Intel type CPU or similar logic.

In 16-bit output mode, if VBI Byte Order (Reg0x19[6]) is set to "0", above odd number VBI data is output on VD[15:8] pins and even number VBI data is output on VD[7:0] pins. If VBI Byte Order (Reg0x19[6]) is set to "1", above even number VBI data is output on VD[15:8] pins and odd number VBI data is output on VD[7:0] pins.

Closed Captioning and Extended Data Services

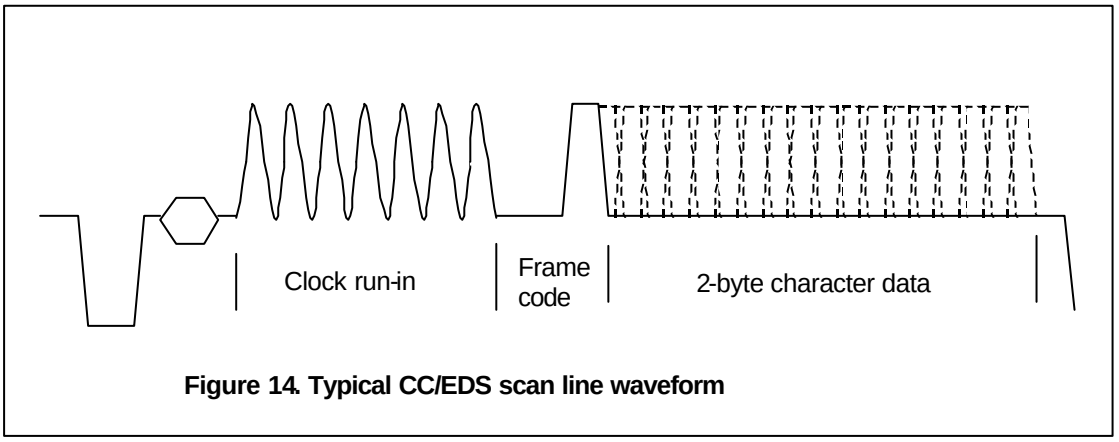


Figure 14. Typical CC/EDS scan line waveform

Line 21 Closed Captioning and line 284 Extended Data Service of 525-line video system is at a 0.5035MHz bit rate. Line 22, line 335 Closed Captioning of 625-line video system is at about 0.500MHz.It contains 14bits Clock Run-in by double bit rate, 3bits Start Bits, and 2 bytes data. Each of these 2 bytes is a 7 bit + odd parity ASCII character which represents text or control characters for positioning or display control. For the purposes of CC or EDS, only the Y component of the video signal is used. The TW9903 can be programmed to decode CC or EDS data by setting register 0x1A. Since the CC and EDS are independent, there could be one or both in a particular frame. A typical waveform is shown in Figure 14.

CC/EDS decoder uses the internal low pass filtered VBI data with ADC sampling rate. CC/EDS Bit rate frequency is generated internally.

In the CC/EDS decode mode, the decoder monitors the appropriate scan lines looking for the clock run-in and start bits pattern. If it s found, it starts tracking Clock Run-in Frequency and checks the status of Clock Run-in and start bits. Some programming may use these scan lines for other purpose. The caption data is sampled and loaded into shift registers, and the data is then transferred to the caption data FIFO. The TW9903 provides a 16 x 10 location FIFO for storing CC/EDS data. Once the video decoder detects the correct status of Clock Run-in, Start Bits in the CC/EDS signal, it captures the low byte of CC/EDS data at first and high byte next. Data is stored in the FIFO low byte first and high byte next sequentially. Captioned data is available to the user through the CC_DATA register (0x1B). Upon being placed in the 10-bit FIFO, two additional bits are attached to the CC/EDS data byte by TW9903' s CC/EDS decoder. These two bits indicate whether the given byte stored in the FIFO corresponds to CC or EDS data and whether it is the high or low byte of CC/EDS. These two bits are available to the user through the CC_STATUS register bits CC_EDS and LO_HI (0x1A[1:0]), respectively. As stored in the FIFO, LO_HI is bit 8 and CC_EDS is bit 9. Additionally, the TW9903 reports the results of the parity check in the PARITY bit in the CC_STATUS register. FIFO can hold 17 data. Initially when the FIFO is empty, bit FF_EMP in the CC_STATUS register (0x1A[2]) is set low indicating that no data is available in the FIFO. Subsequently, when data has been stored in the FIFO, the FF_EMP bit is set to logical high. Once the FIFO has more than 8 bytes, the CC_VALID pin outputs low if CCVALID_EN bit in CC_STATUS register (0x1A[7]) is high and CCVALID bit in CSTATUS register(0x01[2]) also becomes high. If CC_VALID pin is used, CCVALID pin must have external pull-up resister of 4.75 ..10kohm typically. While FIFO has less than 7data, if CCVALID_EN bit is disabled (0x1A[7]=0), CCVALID pin always outputs high by external pull-up resister. If there is no pull-up resister, CVALID pin outputs tri-state unstable signal. CCVALID pin is used when hardware handshaking with Micro controller is needed. In many applications, only CCVALID bit in CSTATUS register(0x01[2]) is used normally. If the FIFO read cycle time is long, then FIFO overflow condition may happen. After 17 data are stored in FIFO, FF_OVF bit in CC_STATUS register(0x1A[3]) becomes high. After FF_OVF becomes high, any incoming data causes only 17th location data to be overwritten. After FIFO is read and FIFO has less than 16 data, FF_OVF bit becomes low. However, once FF_OVF bit becomes high some data loss may happen. In this case, FIFO must be reset by the following way (a) or (b). Method (b) is most often used.

(a) Execute Software Reset (Write 0x06[7]=1)
(b) Write CC_STATUS register bits 0x1A[6:5]=00
16 times read CC_DATA register 0x1B continuously
Write CC_STATUS Register bits 0x1A[6:5] for the application again

There will routinely be asynchronous reads and writes to the CC/EDS FIFO. The writes will be from the CC/EDS circuitry and the reads will occur as the system controller reads the CC/EDS data from TW9903. These reads and writes will not occur until FIFO is in overflow condition. The average FIFO Read cycle time must be shorter than Closed Captioning byte transmitter cycle time. If either odd field Close Captioning or even field Closed Captioning is enabled, the average FIFO read cycle time must be shorter than 2 times write per 1 frame cycle. If both odd field Closed Captioning

and even field Closed Captioning are enabled, it must be shorter than 4 times write per 1 frame cycle. Otherwise, FIFO will be in overflow condition theoretically.

Typical FIFO Read flows are as follows. These flows are written similar to C language type.

Case 1: typical I2C Master with normal read cycle speed

```
CONT1:  Write CC_STATUS register bits 0x1A[6:5]=00
        Read  16 times CC_DATA register 0x1B
        Write CC_STATUS register bits 0x1A[6:5] for the application
CONT2: Read CC_STATUS register 0x1A
       If(FF_OVF bit==1)  goto CONT1
       else if(FF_EMP bit ==0) goto CONT2 or goto CONT3
       else {
            if(PARITY bit==1)  {
                 read CC_DATA register 0x1B
                Abandon this CC_DATA
                goto CONT2 or goto CONT3
            }
            else {
                Check CC_EDS bit and store field information
                read CC_DATA register 0x1B(store 1 data)
            }
       }
CONT3: execute another program routine
       goto CONT2
```

Case2 : Too slow speed I2C Master or program with too big waiting time to cause overflow often.
CC_STATUS Register bits 0x1A[6:5]=01 or10.

```
CONT4: Write CC_STATUS register bits 0x1A[6:5]=00
       Read  16 times CC_DATA register 0x1B
       Write CC_STATUS register bits 0x1A[6:5] for the application
CONT5:  Read CSTATUS register 0x01
       If(CCVALID bit==0)  goto CONT5 or goto CONT6
       Read CC_STATUS register
       If(FF_OVF bit ==1) goto CONT4
       Read 8times CC_DATA register 0x1B(Store 8 data)
       while (1)  {
                  Read CC_STATUS Register 0x1A
                   If(FF_EMP bit==0) break or goto CONT6
                   else  Read 0x1B (store1 data)
                  continue
       }
CONT6: execute another program routine
       goto CONT5
```

Two Wire Serial Bus Interface

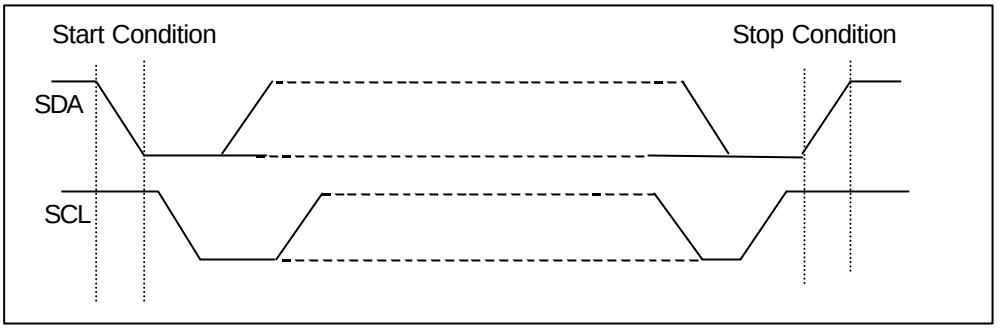
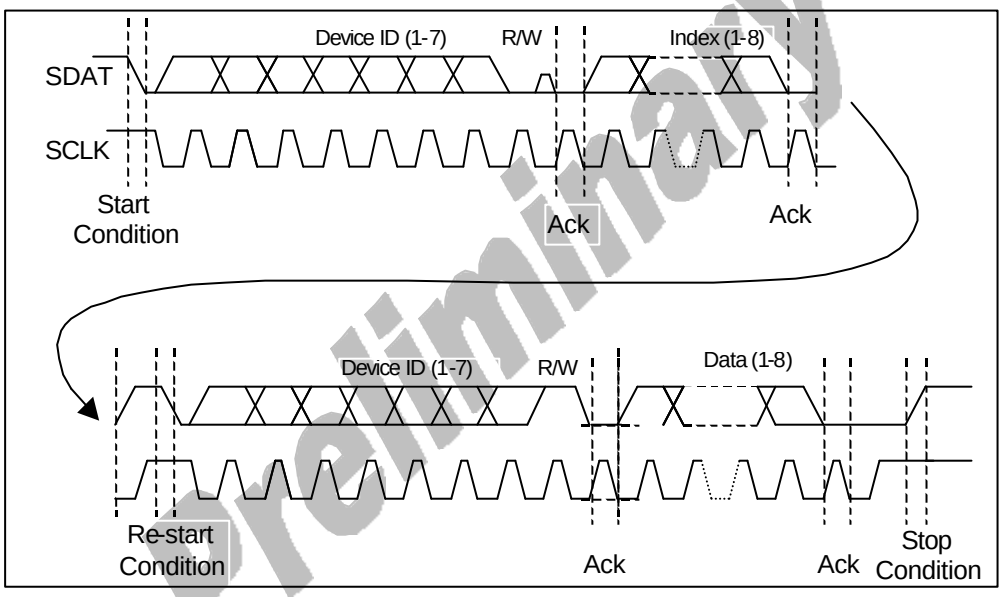


Figure 15. Definition of the serial bus interface bus start and stop

Figure 16. One complete register read sequence via the serial bus interface



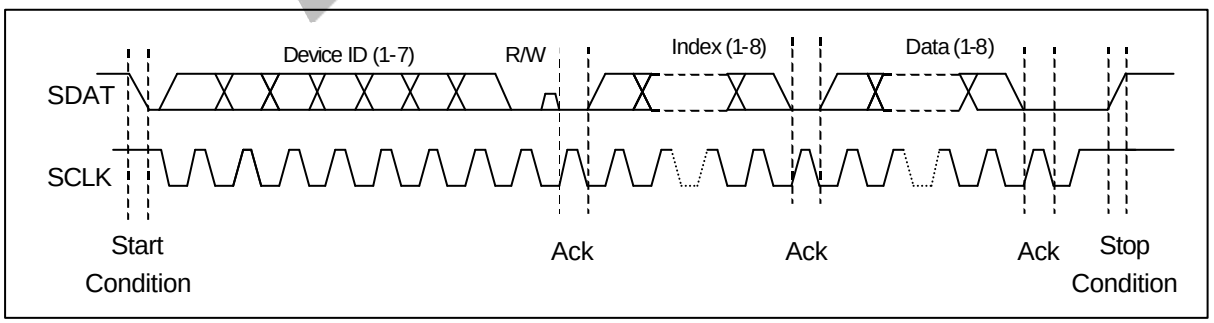


Figure 17. One complete register write sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW9903 registers. SCLK is the serial clock and

SDAT is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW9903 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD (Serial Interface ADdress) pin ether to VDD or GND (See Table 5.). If the SIAD pin is tied to VDD, then the least significant bit of the 7-bit address is a "1". If the SIAD pin is tied to GND then the least significant bit of the 7-bit address is a "0". The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDA from high to low, while SCL is high, this is defined to be a start condition (See Figure 15.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 16. (For the TW9903, the next byte is normally the index to the TW9903 registers and is a write to the TW9903 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theTW9903, the master sends another 8-bits of data, the TW9903 loads this to the register pointed by the internal index register. The TW9903 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW9903 if they are in ascending sequential order. After each 8bit transfer the TW9903 will acknowledge the receipt of the 8bits with an acknowledge pulse. To end all transfers to the TW9903 the host will issue a stop condition.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	SIAD1	SIAD0	1=Read 0=Write

Table 5 TW9903 serial bus interface 7-bit slave address and read write bit

A TW9903 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 16). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Test Modes

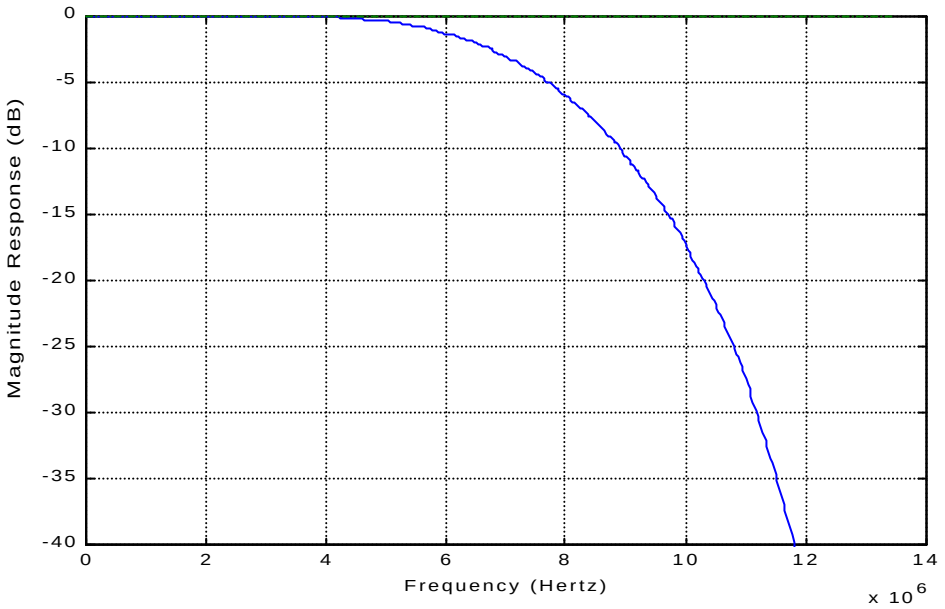
The test mode is provided by the TMODE input pin. If this pin is de-asserted (low), the TW9903 is in its normal operating mode. When this pin is asserted (high), the TW9903 is in test mode, and the mode is controlled by TEST1 and TEST2 input pins as shown in Table 6.

Table 6. Test mode selection and description

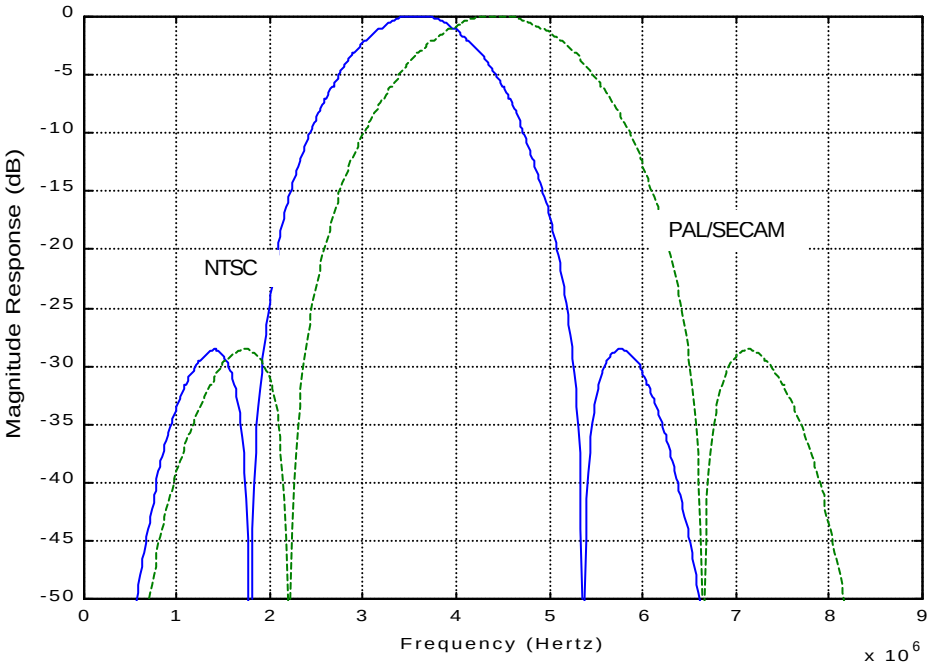
Test mode	TEST2	TEST1	Description
Reserved	0	0	
Pin tri-state	0	1	In this mode, all pin output drivers are tri-stated. Pin leakage current parameters can be measured.
Outputs high	1	0	In this mode, all pin output drivers are forced to the high output state. Pin output high voltage, V_{OH} and I_{OH}, can be measured.
Outputs low	1	1	In this mode, all pin output drivers are forced to the low output state. Pin output high voltage, V_{OL} and I_{OL}, can be measured.

Filter Curves

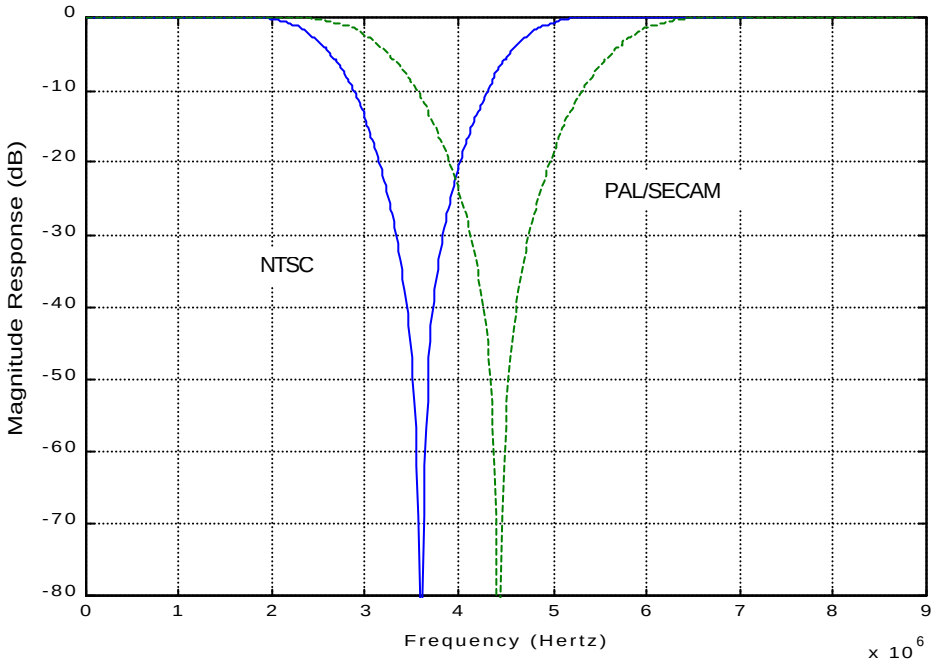
Decimation filter



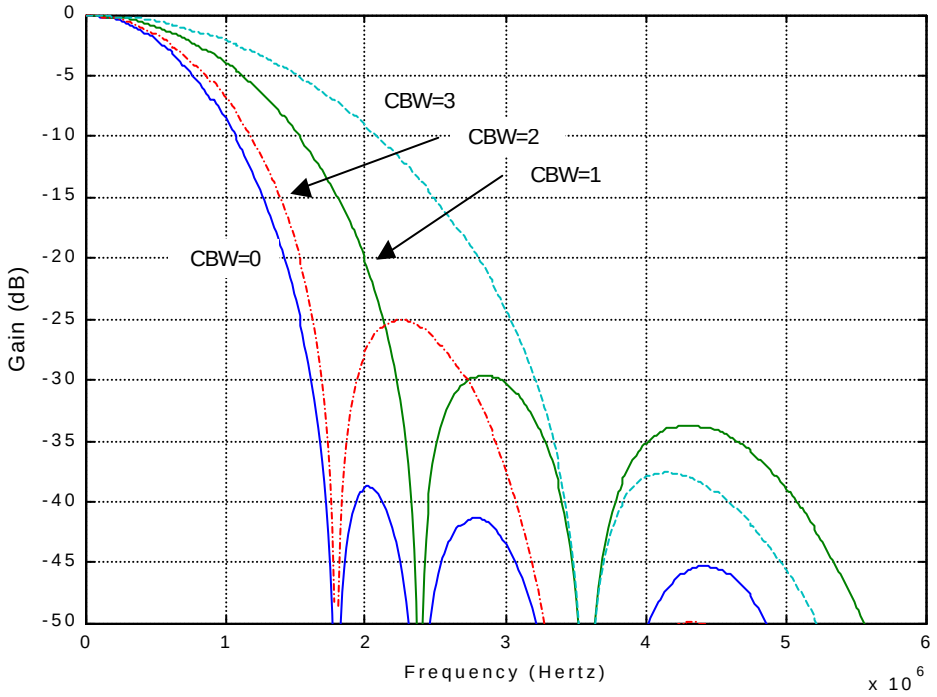
Chroma Band Pass Filter Curves



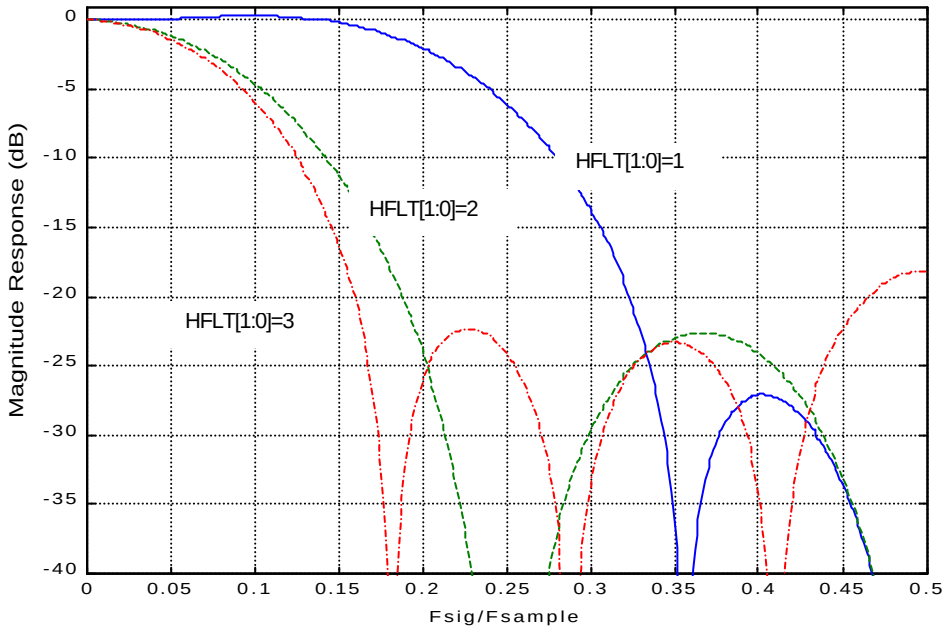
Luma Notch Filter Curve for NTSC and PAL/SECAM



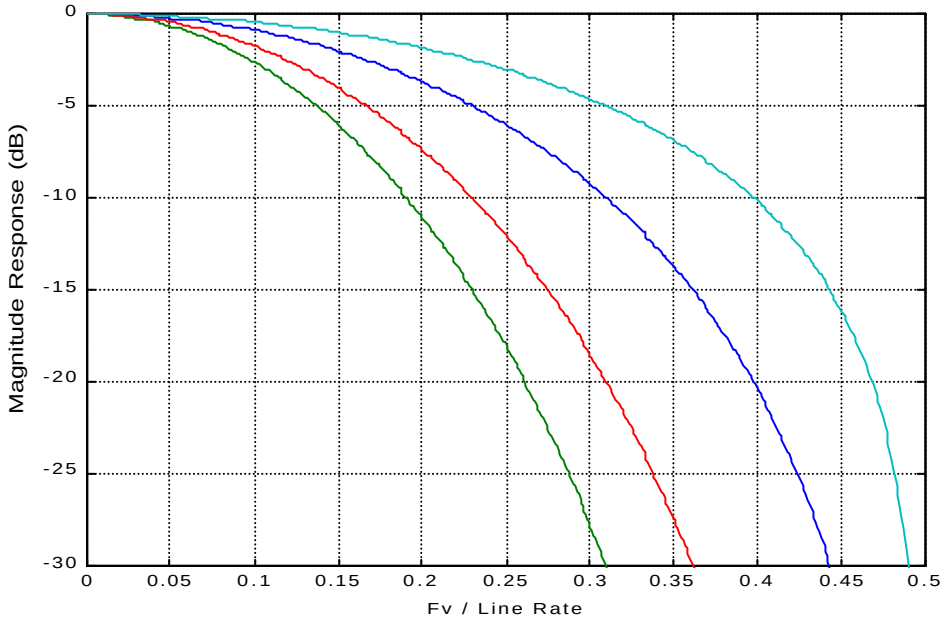
Chrominance Low-Pass Filter Curve



Horizontal Scaler Pre-Filter curves

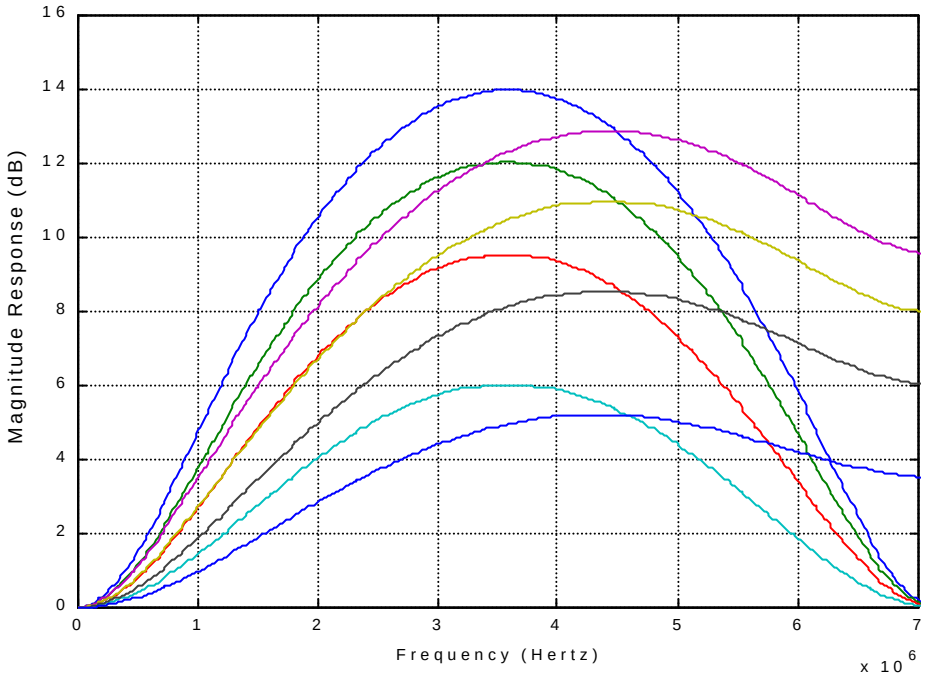


Vertical Interpolation Filter curves

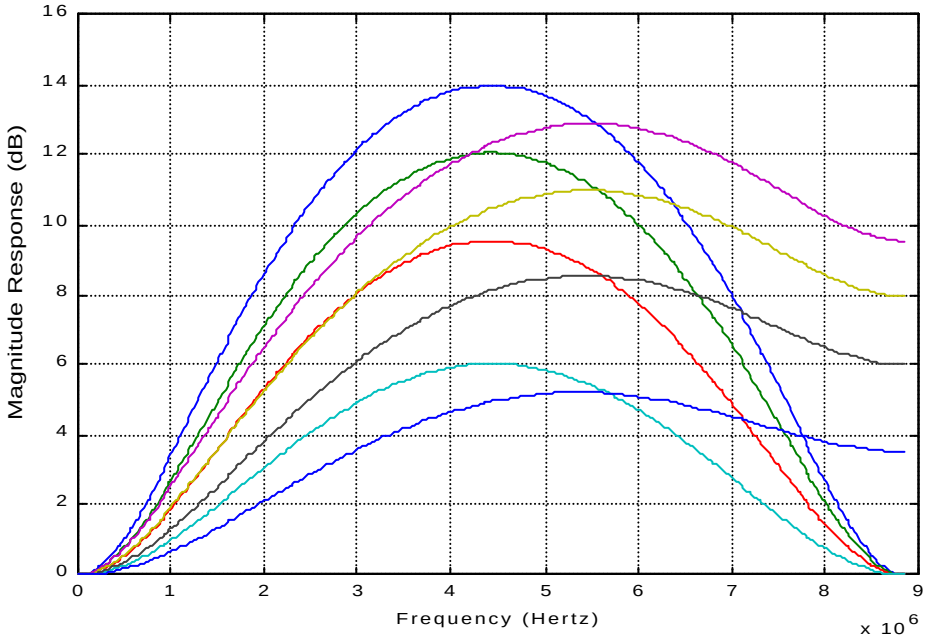


Peaking Filter Curves

NTSC



PAL



Control Register

TW9903 Register SUMMARY

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
00	ID					REV			**19h**
01	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	CCVALID	MONO	DET50	**00h**
02	*	FC27	IFSEL		YSEL		CSEL	SEL	**40h**
03	MODE	LEN	DVALID		VSCTL	OEN	TRI_SEL		**04h**
04	*	*	HSDLY						**00h**
05	LVALID_POL	DVALID_POL	VACTIVE_POL	CBFLAG_POL	FIELD_POL	HACTIVE_POL	HSYNC_POL	VSYNC_POL	**00h**
06	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	*	**03h**
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		**02h**
08	VDELAY_LO								**13h**
09	VACTIVE_LO								**F0h**
0A	HDELAY_LO								**78h**
0B	HACTIVE_LO								**D0h**
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	CCOMB	**8Ch**
0D	VSCALE_LO								**00h**
0E	VSCALE_HI				HSCALE_HI				**11h**
0F	HSCALE_LO								**00h**
10	BRIGHTNESS								**00h**
11	CONTRAST								**60h**
12	SCURVE	*	*		SHARPNESS				**01h**
13	SAT_U								**7Fh**
14	SAT_V								**5Ah**
15	HUE								**00h**
16	SHLMT				SHCOR				**C3h**
17	*				*				**80h**
18	*		CCOR		*		BKCOR		**44h**
19	VBI_EN	VBI_BYT	VBI_FM	HA_EN	CTL656	RTSEL			**58h**
1A	CCVALID_EN	EDS_EN	CC_EN	PARITY	FF_OVF	FF_EMP	CC_EDS	LO_HI	**80h**
1B	CC_DATA								**X**
1C	DTSTUS	STDNOW			ATREG	STANDARD			**00h**
1D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	**00h**
1E	**IN**				**OUT**				**X0h**
1F	**TEST**								**00h**

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
20	CLPEND				CLPST				A0h
21	NMGAIN				WPGAIN			Agcgain8	22h
22	AGCGAIN[7:0]								F0h
23	PEAKWT								FEh
24	CLMPLD	CLMPL							3Ch
25	SYNCTD	SYNCT							38h
26	MISSCNT				HSWIN				44h
27	PCLAMP								20h
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00h
29	BSHT			CCEVENLINE(VSHT)					15h
2A	CKILMAX		CKILMIN						A0h
2B	HTL				VTL				44h
2C	CKLM	YDLY			HSLEN				38h
2D	EVCNT	HFLT			TBC_EN	BYPASS	SYOUT	HADV	00h
2E	HPM		ACCT		SPM		CBW		A5h
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0h
30	sf	pf	ff	kf	CSBAD	MCVSN	CSTRIPE	CTYPE	00h
31	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00h
32	FILLDATA								A0h
33	VBILPF		SDID						22h
34	NODTEN	SYRM	WSSEN	DID					11h
35	ANCEN	TOUTHA	VIPCFG	CCODDLINE					35h
36	SLICELEVEL								72h
37	CRCERR	WSSFLD	WSS[13:8]						X
38	WSS[7:0]								X
39	*	*	WKAIR	VSTD	NINTL	WSSDET	EDSDET	CCDET	0
3A	HREF								x
3B	*	*	*	*	CLMD		PSP		5

0x00 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	The TW9903 Product ID code is 00011.	03h
2-0	Revision	R	The revision number.	1

0x01 – Chip Status Register (CSTATUS)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	CCVALID	R	This bit indicates that valid closed caption or extended data service data pairs have been stored in the CC_DATA register and the FIFO is half full.	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x02 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	Reserved			
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	10 = Component video decoding 01 = S-video decoding 00 = Composite video decoding	00
3-2	YSEL	R/W	These two bits control the input video selection. It selects between all composites source, or three composites and one S-video source. 00 = Route MUX0 input to MXOUT 01 = Route MUX1 input to MXOUT 10 = Route MUX2 input to MXOUT 11 = Route MUX3 input to MXOUT	00
1	CSEL	R/W	This bit selects the chroma channel input. 0 = C_PBIN0 1 = C_PBIN1	0
0	SEL	R/W	This bit determine the method of Y input MUX control 0 = by YSEL 1 = by pin SEL1, SEL0	0

0x03 – Output Format Control Register (OPFORM)

Bit	Function	R/W	Description	Reset
7	MODE	R/W	0 = CCIR601 compatible YCrCb 4:2:2 format with separate syncs and flags. 1 = ITU-R-656 compatible data sequence format.	0
6	LEN	R/W	0 = 8-bit YCrCb 4:2:2 output format based on CLKX2. 1 = 16-bit YCrCb 4:2:2 output format based on CLKX1.	0
5-4	DVALID	R/W	00 = DVALID is in the first format with VCLK used as data strobe. 01 = DVALID is in the second format with DVALID indicating the valid data period. 10 = DVALID is in the third format with DVALID used as data strobe.	0
3	VSCTL	R/W	1 = Vertical scale-downed output controlled by DVALID only. 0 = Vertical scale-downed output controlled by both HACTIVE and DVALID.	0
2	OEN	R/W	0 = Enable outputs. 1 = Tri-state outputs defined by Tri-state select bits of this register.	1
1-0	TRI_SEL	R/W	These bits select the outputs to be tri-stated when the OEN bit is asserted high. There are three major groups that can be independently tri-stated: timing group (HSYNC, VSYNC, HACTIVE, VACTIVE, CBFLAG, DVALID, MPOUT, FIELD), data group (VD[15:0]), and clock group (CLKX1, CLKX2, VCLK) according to following definition. If OE# pin is asserted high, all of these pins are tri-stated regardless of this setting. 00 = Timing and data group only. 01 = Data group only. 10 = All three groups. 11 = Clock and data group only.	00b

0x04 – GAMMA and HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W		0
6-5	Reserved	R/W		0
4-0	HSDLY	RW	These bits control the position of the HSYNC pin output relative to the internal reference in 4 CLKX1 step. 5h is recommended.	0

0x05 – Output Polarity Register (POLARITY)

Bit	Function	R/W	Description	Reset
7	LVALID	R/W	0 = LVALID pin is active high. 1 = LVALID pin is active low.	0
6	DVALID	R/W	0 = DVALID pin is active high. 1 = DVALID pin is active low.	0
5	VACTIVE	R/W	0 = VACTIVE pin is active high. 1 = VACTIVE pin is active low.	0
4	CBFLAG	R/W	0 = CBFLAG pin is active high. 1 = CBFLAG pin is active low.	0
3	FIELD	R/W	0 = FIELD pin is low for the odd field. 1 = FIELD pin is low for the even field.	0
2	HACTIVE	R/W	0 = HACTIVE pin active high. 1 = HACTIVE pin active low.	0
1	HSYNC	R/W	0 = HSYNC pin active low. 1 = HSYNC pin active high.	0
0	VSYNC	R/W	0 = VSYNC pin active low. 1 = VSYNC pin active high.	0

0x06 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	An 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	1 = Internal voltage reference. 0 = external voltage reference using VCOM, VREFP and VREFN.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKX1 and CLKX2) are still active.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	1
0	Reserved	R/W		0

0x07 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	10b

0x08 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	13h

0x09 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0h

0x0A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	78h

0x0B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x0C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Slock sensitivity	0
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. 0 = mode 0.	1
1	YCOMB	R/W	This bit controls the Y comb. 1 = Y output is the averaging of two adjacent lines. 0 = No comb.	0
0	CCOMB	R/W	This bit controls the UV comb. 1 = UV output is the averaging of two adjacent lines. 0 = No comb.	0

0x0D – Vertical Scaling Register, Low (VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00h

0x0E – Scaling Register, High (SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	01h
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	01h

0x0F – Horizontal Scaling Register, Low (HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	HSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00h

0x10 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	Brightness	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00h

0x11 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	Contrast	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 1 (`100_0000`) has no effect on the video data.	60h

0x12 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the sharpness filter center frequency. 0 = Normal 1 = High	0
6	Reserved	R/W		0
5-4	Reserved	R/W		0
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 7 provides sharpness enhancement with '7' being the strongest. Value 8 through 15 are provided for noise reduction purpose.	1

0x13 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	7Fh

0x14 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	5Ah

0x15 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue. They have value from +96^{o} (7Fh) to -96^{o} (80h) with an increment of 0.75^{o}. The default value is 0^{o} (00h).	00h

0x16 – Sharpness Control Register II

Bit	Function	R/W	Description	Reset
7-4	SHLMT	R/W	These bits limit the maximum enhancement level regardless of the SHARP setting. The internal step size is 8.	C
3-0	SHCOR	R/W	These bits provide coring function for the sharpness control.	3

0x17 – Reserved

Bit	Function	R/W	Description	Reset
7-4	*	R/W		0
3-0	*	R/W		0

0x18 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W		0
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0h
3-2	Reserved	R/W		0h
1-0	BKCOR	R/W	These bits control the black level coring function.	0h

0x19 – VBI Control Register (VBICNTL)

Bit	Function	R/W	Description	Reset
7	VBI EN	R/W	0 = VBI capture disabled. 1 = VBI capture enabled.	0
6	VBI Byte Order	R/W	If LEN(Reg0x03[6]) is "1" 0 = Pixel 1, 3, 5 …on the VD[15:8] data bus, and pixel 2, 4, 6, … on the VD[7:0] data bus. 1 = Pixel 1, 3, 5, …on the VD[7:0] data bus, and pixel 2, 4, 6, .. on the VD[15:8] data bus. If LEN is"0" 0 = Pixel 2,1,4,3,6,5, … on the VD[15:8] data bus. 1 = Pixel 1,2,3,4,5,6, … on the VD[15:8] data bus.	1
5	VBI Frame Mode	R/W	0 = VBI Frame output mode disabled. VBI capture is controlled by bit 7 of this register. 1 = VBI Frame output mode enabled. VBI capture is always enabled.	0
4	HA_EN	R/W	0 = HACTIVE output is disabled during vertical blanking period. 1 = HACTIVE output is enabled during vertical blanking period.	1
3	CNTL656	R/W	0 = 0x80 and 0x10 code will be output as invalid data during active video line. 1 = 0x00 code will be output as invalid data during active video line.	1
2-0	RTSEL	R/W	These bits control the real time signal output from the MPOUT pin. 000 = Video loss 001 = H-lock 010 = S-lock 011 = V-lock 100 = MONO 101 = Det50 110 = Mcvsn 111 = LVALID	0

0x1A – CC/EDS Status Register (CC_STATUS)

Bit	Function	R/W	Description	Reset
7	CCVALID_EN	R/W	0 = Disable CCVALID interrupt pin. 1 = Enable CCVALID interrupt pin.	1
6	EDS_EN	R/W	0 = EDS data is not transferred to the CC_DATA fifo. 1 = EDS data is transferred to the CC_DATA fifo.	0
5	CC_EN	R/W	0 = CC data is not transferred to the CC_DATA fifo. 1 = CC data is transferred to the CC_DATA fifo.	0
4	PARITY	R	0 = Data in CC_DATA has no error. 1 = Data in CC_DATA has odd parity error.	X
3	FF_OVF	R	0 = An overflow has not occurred. 1 = An overflow has occurred in the CC_DATA fifo.	0
2	FF_EMP	R	0 = CC_DATA fifo is empty. 1 = CC_DATA fifo has data available.	0
1	CC_EDS	R	0 = Closed caption data is in CC_DATA register. 1 = Extended data service data is in CC_DATA register.	X
0	LO_HI	R	0 = Low byte of the 16-bit word is in the CC_DATA register. 1 = High byte of the 16-bit word is in the CC_DATA register.	X

0x1B – CC/EDS Data Register (CC_DATA)

Bit	Function	R/W	Description	Reset
7-0	CC Data	R	These bits store the incoming closed caption or even field closed caption data.	80h

0x1C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	Standard	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	0h

0x1D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6		R/W	1 = enable recognition of PAL60. 0 = disable recognition.	0
5		R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	0
4		R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	0
3		R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	0
2		R/W	1 = enable recognition of SECAM. 0 = disable recognition.	0
1		R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	0
0		R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	0

0x1E – General Programmable I/O Register (GPIO)

Bit	Function	R/W	Description	Reset
7-4	IN[3:0]	R	These input bits can be used to monitor external signals from VD[7:4] while in 8-bit output mode (Length bit of OPFORM register equals 0). If not in the 8-bit output mode, the values of these bits are not valid.	X
3-0	OUT[3:0]	R/W	These output bits can be programmed to output additional signals on VD[3:0] while in 8-bit output mode. If not in the 8-bit output mode, these bits have no effect on the pins.	0h

0x1F – Test Control Register (TEST)

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 1 = Analog test mode. Y and C channel portion of the device can be tested in this mode. The Y channel ADC output can be obtained from HACTIVE, HSYNC and VD[15:8] for bit1, bit0 and bit9-2, respectively. The C channel ADC output can be obtained from VACTIVE, VSYNC and VD[7:0] for bit1, bit0 and bit9-2, respectively. 2 = Digital test mode1. The sync portion of the device should be tested in this mode. The 8-bit input corresponds to TISVN, TEST1, TEST2, TDO, TCK, TRST#, TMS, and TDI in the order of bit 7 to 0. 3 = Analog test mode 1. It is same as the previous analog test mode except that the C channel ADC inputs come from TADCP and TADCN instead of C_PBIN. 4 = Digital test mode 2. In addition to digital test mode 1, this test mode allows the C channel data to be inputted from VD[7:0]. In this mode, only 8-bit output format is allowed. 5 = Closed Caption test mode. 6 = Analog test mode 2. The "C channel portion of the device can be tested in this mode. The C channel ADC output can be obtained from VACTIVE, VSYNC and VD[7:0] for bit1, bit0 and bit9-2, respectively. 7 = Analog DAC output mode. The 6-bit Sync output corresponds to TDI, TMS, TRST#, TCK, TISVN and TDO in the order of bit 5 to 0. Y and Cb/Cr outputs correspond to VD[15:8] and VD[7:0], respectively. In this mode, HACTIVE pin will be BGOUT and VACTIVE pin will be VSDLY.	0

0x20 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	A
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x21 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x22 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0h

0x23 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	FEh

0x24– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	0
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3Ch

0x25– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	0
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38h

0x26 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4h
3-0	HSWIN	R/W	These bits determine the Hsync detection window.	4h

0x27 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	20h

0x28 – Vertical Control Register

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x29 – Vertical Control II

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control.	0
5-0	VSHT	R/W	Delayed Vsync position control in the increment of half line length or CC decoding line number for even field.	15h

0x2A – Color Killer Level Control

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis.	2
5-0	CKILMIN	R/W	These bits control the color killer trip point.	20h

0x2B – Comb Filter Control

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Reserved	4
3-0	VTL	R/W	Adaptive Comb filter combing strength control. Higher value provides stronger comb filtering.	4

0x2C – Luma Delay and HSYNC Control

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provide –4 to +3 unit delay control.	3h
3-0	HSLEN	R/W	It sets the pin output HSYNC pulse width in increment of 8 CLKX1 clock period. The minimum width is 8 CLKX1 period.	7h

0x2D – Miscellaneous Control Register I (MISC1)

Bit	Function	R/W	Description	Reset
7	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
6-4	HFLT	R/W	Pre-filter selection for scaler 1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image 010 = Recommended for QCIF size image 011 = Recommended for ICON size image	0
3	TBC_EN	R/W	1 = Internal TBC enabled.(test purpose only) 0 = TBC off.	0
2	BYPASS	R/W	1 = Bypass output FIFO 0 = No bypass.	0
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	HADV	R/W	This bit advances the HACTIVE and DVALID pin output by one data clock when set.	0

0x2E – Miscellaneous Control Register II (MISC2)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto 1 = Mid 0 = Slow	2
5-4	ACCT	R/W	ACC time constant 00 = No ACC 01 = slow 10 = medium 11 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0x2F – Miscellaneous Control III (MISC3)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x30 – Macrovision Detection

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6	Reserved	R		0
5	Reserved	R		0
4	Reserved	R		0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0x31 – Clamp Cntl2

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debugging use.	0
6	YCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x32 – FILL DATA

Bit	Function	R/W	Description	Reset
7-0	FILLDATA	R/W	Fill data value for missing data byte in double word sliced VBI data output.	A0h

0x33 – VBI CNTL1

Bit	Function	R/W	Description	Reset
7-6	VBILPF	R/W	VBI low pass filter selection. 00 = Disabled. 01 = type1. 10 = type2. 11 = type3	0
5-0	SDID	R/W	Sliced VBI data identification code.	22h

0x34 – VBI CNTL2

Bit	Function	R/W	Description	Reset
7	NODTEN	R/W	1 = Enabled embedded 'Vdloss' feature in 656 stream. 0 = Disabled.	0
6	SYRM	R/W	1 = VBI output with sync removed. 0 = Raw VBI data output.	0
5	WSSEN	R/W	1 = Enable WSS decoding. 0 = Disabled.	0
4-0	DID	R/W	ANC header framing code	11h

0x35 – MISC 4

Bit	Function	R/W	Description	Reset
7	ANCEN	R/W	1 = Enable ANC code output of sliced VBI data. 0 = Disabled.	0
6	TOUTHA	R/W	1 = Sliced VBI (CC/EDS or WSS) data output during HACTIVE high period. 0 = Disabled.	0
5	VIPCFG	R/W	1 = VIP task A control code. 0 = VIP task B control code.	1

4-0	CCODDLINE	R/W	These bits control the CC decoding line number in the case of Odd field.	15h

0x36 – Slice Level

Bit	Function	R/W	Description	Reset
7-0	SLICE	R/W	These bits define the VBI data initial slice level.	72h

0x37 – WSS1

Bit	Function	R/W	Description	Reset
7	CRCERR	R	This is the CRC error indicator for 525-line WSS. 1:CRC error.0:no error	0
6	WSSFLD	R	These bit indicates the detected WSS field information, 0=odd and 1=even.	X
5-0	WSS1	R	These bits represent the sliced WSS data bit 13 to 8.	X

0x38 – WSS2

Bit	Function	R/W	Description	Reset
7-0	WSS2	R	These bits represent the sliced WSS bit 7 to 0.	X

0x39 – CSTATUS III

Bit	Function	R/W	Description	Reset
5	WKAIR	R	1 = Weak signal 0 = Nomal	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	0
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	0
0	CCDET	R	1 = CC data detected. 0 = Not detected.	0

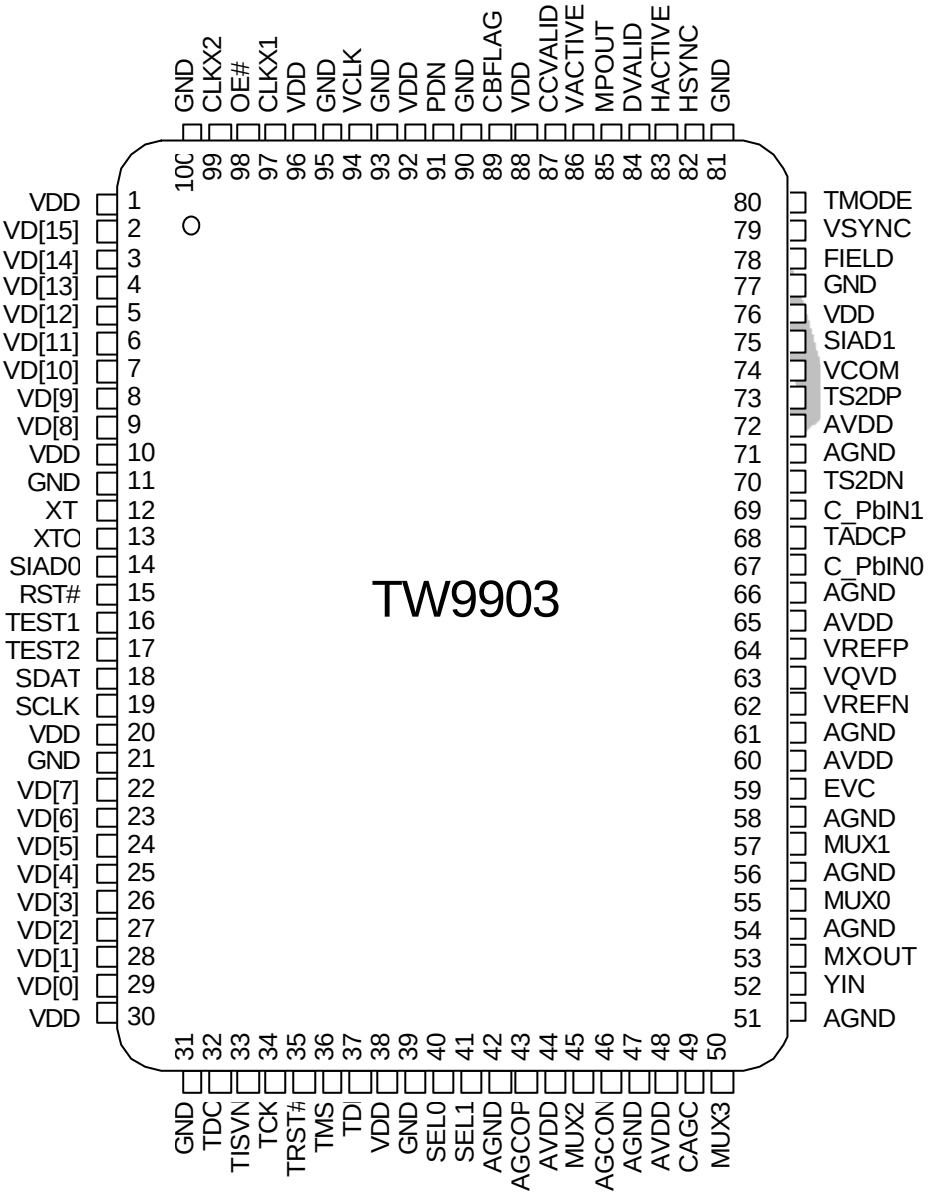
0x3A – HFREF

Bit	Function	R/W	Description	Reset
7-0	HFREF	R	Horizontal line frequency indicator	X

0x3B – CLAMP MODE

Bit	Function	R/W	Description	Reset
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = Med 2 = high	1

Pin Diagram


TW9903
1 VDD
2 VD[15]
3 VD[14]
4 VD[13]
5 VD[12]
6 VD[11]
7 VD[10]
8 VD[9]
9 VD[8]
10 VDD
11 GND
12 XT
13 XTO
14 SIAD0
15 RST#
16 TEST1
17 TEST2
18 SDAT
19 SCLK
20 VDD
21 GND
22 VD[7]
23 VD[6]
24 VD[5]
25 VD[4]
26 VD[3]
27 VD[2]
28 VD[1]
29 VD[0]
30 VDD
31 GND
32 TDC
33 TISVN
34 TCK
35 TRST#
36 TMS
37 TDI
38 VDD
39 GND
40 SEL0
41 SEL1
42 AGND
43 AGCOP
44 AVDD
45 MUX2
46 AGCON
47 AGND
48 AVDD
49 CAGC
50 MUX3
51 AGND
52 YIN
53 MXOUT
54 AGND
55 MUX0
56 AGND
57 MUX1
58 AGND
59 EVC
60 AVDD
61 AGND
62 VREFN
63 VQVD
64 VREFP
65 AVDD
66 AGND
67 C_PbIN0
68 TADCP
69 C_PbIN1
70 TS2DN
71 AGND
72 AVDD
73 TS2DP
74 VCOM
75 SIAD1
76 VDD
77 GND
78 FIELD
79 VSYNC
80 TMODE
81 GND
82 HSYNC
83 HACTIVE
84 DVALID
85 MPOUT
86 VACTIVE
87 CCVALID
88 VDD
89 CBFLAG
90 GND
91 PDN
92 VDD
93 GND
94 VCLK
95 GND
96 VDD
97 CLKX1
98 OE#
99 CLKX2
100 GND

Pin Description

This section provides a detailed description of each pin for the TW9903. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

The pin description also includes the buffer type used for that pin.

I input pin

O output pin

OD open drain output pin

I/O bi-directional input/output pin

Analog analog signal pin

LVTTL low voltage TTL compatible signals with 3.3V outputs and 5V tolerant inputs.

Analog Interface Pins

Pin#	I/O	Pin Name	Description
45, 50, 55, 57	I, analog	MUX3, MUX2, MUX1, MUX0	These are the analog composite video inputs pins to the input selector. Four composite sources or three composites and one S-video source can be selected as the input. Unused pins should be connected to AGND.
53	O, analog	MXOUT	The output of the on-chip 4-to-1 selector. It should be connected to the YIN pin. The input selected can be programmed through INFORM register.
52	I, analog	YIN	The analog composite or luma input to the Y-ADC.
67	I, analog	C_PbIN0	The analog chroma input to the C-ADC.
43, 46	O, analog	AGCOP, AGCON	The buffered AGC differential outputs that correspond to the AGCIN. It is for test use only.
59	I, analog	EVC	Test pin. It should be left unconnected.
64	I/O, analog	VREFP	The positive reference voltage for the ADC. It should be connected to AGND through 0.1uF capacitor. It can be optionally forced by external voltage reference source.
62	I/O, analog	VREFN	The negative reference voltage for the ADC. It should be connected to AGND through a 0.1uF capacitor. It can be optionally forced by external voltage reference source.
74	O, analog	VCOM	The common mode voltage output. It should be connected to analog GND through a 0.1uF capacitor. It can be optionally forced externally.

Pin#	I/O	Pin Name	Description
63	I, analog	VQVD	De-coupling pin. It should be connected with 0.1uF to AGND.
49	I, Analog	CAGC	Test pin. It should be left unconnected.
68	I, analog	TADCP	Test pin. It should be connected to AGND during normal operation.
69	I, analog	C_PbIN1 / TADCN	The analog chroma input in the S-video mode or the analog Pr input in the component video input mode. It also doubles as a test pin.
70	O, analog	TS2DN	Test pin. It should be left unconnected during normal operation.
73	O, analog	TS2DP	Test pin. It should be left unconnected during normal operation.

Two Wire Interface Pins

Pin#	I/O	Pin Name	Description
19	I, LVTTL	SCLK	The MPU Serial interface Clock Line.
18	I/OD, LVTTL	SDAT	The MPU Serial interface Data Line.
14	I, LVTTL	SIAD0	The MPU interface address select pin 0. This pin is used to select one of the four addresses that chip will respond. It is internally pulled down to ground.
75	I, LVTTL	SIAD1	The MPU interface address select pin 1. This pin is used to select one of the four addresses that chip will respond. It is internally pulled down to ground.
15	I, LVTTL	RST#	Master Reset Input. A logical zero for a minimum of four consecutive clock cycles is required to reset the device to its default state.

Video Timing Unit Pins

Pin#	I/O	Pin Name	Description
82	O, LVTTL	HSYNC	Horizontal Sync Output. This signal indicates the beginning of a new line of video. This signal is typically 64 CLKx1 clock cycles wide, and can be programmed through HSLEN register. The falling edge of this output indicates the beginning of a new scan line of video. Note: The polarity of this pin is programmable through the POLARITY register.
79	O, LVTTL	VSYNC	Vertical Sync Output. This signal indicates the beginning of a new field of video. This signal is output coincident with the rising edge of CLKx2, and is normally six lines wide. The falling edge of VSYNC indicates the beginning of a new field ofvideo. Note: The polarity of this pin is programmable through the POLARITY register.
83	O, LVTTL	HACTIVE	Active Video Output. This pin can be programmed to output the composite active or horizontal active signal via the Hactive register. It is a logical high

Pin#	I/O	Pin Name	Description
	LVTTL		active or horizontal active signal via the Hactive register. It is a logical high during the active/viewable periods of the video stream. The active region of the video stream is programmable. Note: The polarity of this pin is programmable through the POLARITY register.
94	O, LVTTL	VCLK	Video Clock Output. This pin provides a clock for video data strobing. The clock is available only during valid data period. This output is generated from CLKx1 (or CLKx2 in 8-bit mode), DVALID and, if programmed, HACTIVE. The phase of VCLK is inverted from the CLKx1 (or CLKx2) to ensure adequate setup and hold time with respect to the data outputs.
98	I, LVTTL	OE#	Output Enable Control. This pin controls the outputs of all video timing unit output pins and all clock interface output pins. All outputs are valid only when this pin is asserted low. This function is asynchronous. The three-stated pins include: VD[15:0], HSYNC, VSYNC, HACTIVE, DVALID, CBFLAG, FIELD, VCLK, CLKx1, and CLKx2.
78	O, LVTTL	FIELD	Odd/Even Field Output. A high state on the FIELD pin indicates that an even field is being output. Note: The polarity of this pin is programmable through the POLARITY register.
89	O, LVTTL	CBFLAG	Cb Data Flag. A high state on this pin indicates that the current chroma byte contains Cb chroma information. Note: The polarity of this pin is programmable through the POLARITY register.
2–9	O, LVTTL	VD[15:8]	Digitized Video Data Outputs. VD[0] is the least significant bit of the bus in 16-bit mode. VD[8] is the least significant bit of the bus in 8-bit mode. The information is output with respect to CLKx1 rising edge in 16-bit mode, and CLKx2 rising edge in 8-bit mode. It can be programmed to output CCIR-656 compliant format. When data is output in 8-bit mode using VD[15:8], VD[7:0] can be used as general purpose I/O pins.
22-29	I/O, LVTTL	VD[7:0]	
84	O, LVTTL	DVALID	Data Valid Output. This pin indicates when a valid pixel is being output onto the data bus. The format of this output pin can be programmed through the OPFORM register. Note: The polarity of this pin is programmable through the POLARITY register.
87	OD, LVTTL	CCVALID	A logical low on this pin indicates that the Closed Caption FIFO is half full (8 characters). This pin may be disabled. This open drain output requires a pullup resistor for proper operation. However, if closed captioning is not implemented, this pin may be left unconnected.
91	I, LVTTL	PDN	A logical high on this pin puts the device into power-down mode. This is equivalent to programming CLK_PDN high in the ADC register.
86	O, LVTTL	VACTIVE	Vertical Blanking Output. The falling edge of VACTIVE indicates the beginning of the active video lines in a field. This occurs VDELAY/2 lines after the rising edge of VSYNC. The rising edge of VACTIVE indicates the end of active video lines and occurs ACTIVE_LINES/2 lines after the falling edge of VACTIVE. VACTIVE is synchronized to the rising edge of CLKx1. Note: The polarity of the pin is programmable through the POLARITY register.

Pin#	I/O	Pin Name	Description
85	O, LVTTL	MPOUT	Multi-purpose output pin. The output function can be selected by RTSEL of register 0x19. Note: When LVALID is selected, the polarity of this pin is programmable through the POLARITY register.
80	I, LVTTL	TMODE	This pin is used to enable the in-circuit test mode. It should be connected to GND through a 10K ohm pull-down resistor for in-circuit test or tied to GND directly for others. When this pin is asserted (active high), pin TEST1 and TEST2 will determine the test to be performed.
16	I, LVTTL	TEST1	Test pin 1. See Test mode section for description.
17	I, LVTTL	TEST2	Test pin 2. See Test mode section for description.

Clock Interface Pins

Pin#	I/O	Pin Name	Description
12	I	XTI	Clock Zero pins. A 27MHz fundamental (or third harmonic) crystal can be connected directly to these pins, or a single -ended oscillator can be connected to XTI.
13	O	XTO	For Crystal 27MHz connection
97	O, LVTTL	CLKx1	1x clock output. The frequency of this clock is half of the crystal frequency, i.e. 13.5Mhz when 27Mhz crystal is used.
99	O, LVTTL	CLKx2	2x clock output. The frequency of this clock is the same as the crystal frequency, i.e. 27Mhz when 27Mhz crystal is used.

Test Pins

Pin#	I/O	Pin Name	Description
34	I/O, LVTTL	TCK	Test pin. It should be connected to GND during normal operation.
36	I/O, LVTTL	TMS	Test pin. It should be connected to GND during normal operation.
37	I/O, LVTTL	TDI	Test pin. It should be connected to GND during normal operation.
32	I/O, LVTTL	TDO	Test pin. It should be connected to GND during normal operation.
33	I/O, LVTTL	TISVN	Test pin. It should be connected to GND duringnormal operation.
35	I/O, LVTTL	TRST	Test pin. It should be connected to GND during normal operation.
41	I, LVTTL	SEL1	Y input MUX control 1.
40	I, LVTTL	SEL0	Y input MUX control pin 0.

Power and Ground Pins

Pin#	I/O	Pin Name	Description
1, 10, 20, 30, 38, 76, 88, 92, 96	P	VDD	+3.3 V Power supply for digital circuitry. All VDD pins must be connected together as close to the device as possible. A 0.1 μF ceramic capacitor should be connected between each group of VDD pins and the ground plane as close to the device as possible.
44, 48, 60, 65, 72	P	AVDD +3.3V	Power supply for analog circuitry. All AVDD pins must be connected together as close to the device as possible. A 0.1 μF ceramic capacitor should be connected between each group of AVDD pins and the ground plane as close to the device as possible.
11, 21, 31, 39, 77, 81, 90, 93, 95, 100	G	GND	Ground for digital circuitry. All GND pins must be connected together as close to the device as possible.
42, 47, 54, 56, 58, 61, 66, 71, 51	G	AGND	Ground for analog circuitry. All AGND pins must be connected together as close to the device as possible.

Parametric Information

AC/DC Electrical Parameters

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD (measured to AGND)	V_{DDAM}	-	-	4.8	V
V_{DD} (measured to DGND)	V_{DDM}		-	4.8	V
Voltage on any signal pin (See the note below)	-	DGND – 0.5	-	V_{DDAM} + 0.5	V
Analog Input Voltage	-	AGND – 0.5	-	V_{DDM} + 0.5	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering(15 Seconds)	T_{VSOL}	-	-	+220	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operationalsection of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

Table 8. characteristics

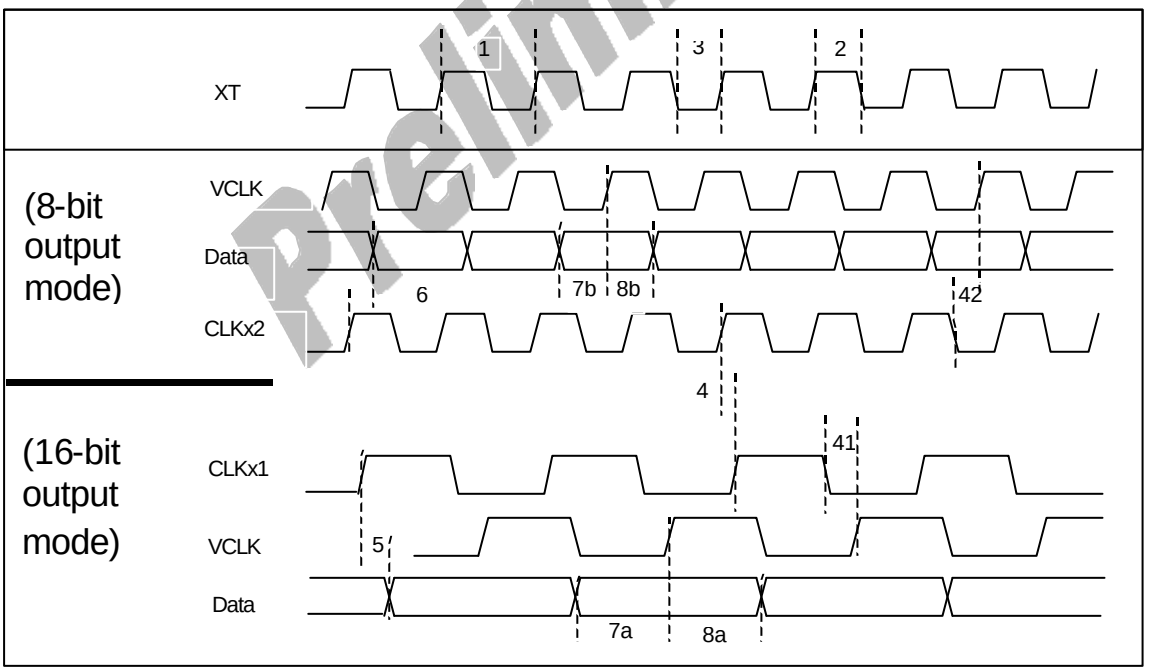
Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply —Analog	V_{DDA}	3.15	3.3	3.45	V
Power Supply —Digital	V_{DD}	3.15	3.3	3.45	V
Maximum $\|V_{DD} - AVDD\|$		-	-	0.3	V
MUX0, MUX1 and MUX2 Input Range (AC coupling required)		0.5	1.00	2.00	V
PRIN Amplitude Range (AC coupling required)		0.5	1.00	2.00	V
Ambient Operating Temperature	T_A	0		+70	°C
Analog Supply current	**Iaa**	**-**	**30**	**-**	**mA**
Digital Supply current	**Idd**	**-**	**90**	**-**	**mA**
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	V_{DDM} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDM} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	GND -0.5	-	1.0	V
Input High Current (V_{IN}=V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN}=GND)	I_{IL}	-	-	–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}	-	5	-	pF

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs					
Output High Voltage (I_{OH} = -4 mA)	V_{OH}	2.4	-	V_{DD}	V
Output Low Voltage (I_{OL} = 4 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	**ADCR**	-	10	-	bits
ADC integral Non-linearity	**AINL**	-	±1	-	LSB
ADC differential non-linearity	**ADNL**	-	±1	-	LSB
ADC clock rate	f_{ADC}	**24**	27	**30**	MHz
Video bandwidth (-3db)	**BW**	-	10	-	MHz
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	**6.2**	%
Subcarrier PLL					
subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±**400**	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
deviation		-	-	±**50**	ppm
Temperature range	**Ta**	**0**	-	**70**	°C
load capacitance	**CL**	-	20	-	pF
series resistor	**RS**	-	**80**	-	Ohm
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±**50**	ppm
duty cycle		-	-	**55**	%

Parameter	Symbol	Min	Typ	Max	Units

Output CLK					
CLKx1		**12**	13.5	**15**	MHz
CLKx2		**24**	27	**30**	MHz
CLKx1 Duty Cycle		-	-	55	%
CLKx2 Duty Cycle		-	-	55	%
CLKx2 to CLKx1 Delay	4	-	-	2	ns
CLKx1 to Data Delay	5	-	5	-	ns
CLKx2 to Data Delay	6	-	5	-	ns
CLKx1 (Falling Edge) to VCLK (Rising Edge)	41	-	0	-	ns
CLKx2 (Falling Edge) to VCLK (Rising Edge)	42	-	0	-	ns
Output Video Data					
8-bit Mode (1)					
Data to VCLK (Rising Edge) Delay	7b	-	18	-	ns
VCLK (Rising Edge) to Data Delay	8b	-	18	-	ns
16-bit Mode (1)					
Data to VCLK (Rising Edge) Delay	7a	**-**	37	-	ns
VCLK (Rising Edge) to Data Delay	8a	**-**	37	-	ns
OE# Asserted to Data Bus Driven		**0**	-	-	ns
OE# Asserted to Data Valid		**-**	-	100	ns
OE# Negated to Data Bus Not Driven		**-**	-	100	ns

Clock Timing Diagram



Application Information

Video Input Interface

The TW9903 has a built-in 4:1 input MUX for software controllable input selections. This MUX can be used to select three composite video sources and one S-Video source or two composite video sources, one S-video and one component video source. The output of the MUX (MUXOUT) should be connected to YIN directly or through a 0.1uF capacitor. The chroma of the S-Video input should be connected to C_PBIN0 or C_PBIN1 of the C-Channel A/D converter. For a typical application, a video input should be first terminated with a 75 ohm resistor before it is AC coupled by a 0.1uF capacitor to the input of the MUX.

A/D Converter

The TW9903 has three internal A/D converters to cover all possible analog video signal sources. The reference supply generator for the A/D converter is also on-chip. For a better noise immunity, VREFP, VREFN, VCOM and VQVD should be connected through a 0.1uF capacitor to AGND.

Clamping/AGC

The TW9903 has built-in automatic clamping control circuitry. No extra external component is needed for this operation. The clamping loop gain can be controlled through register setting. The TW9903 also has built-in automatic AGC control circuitry. The AGC loop gain can also be controlled by register. The AGC loop response time is also register programmable.

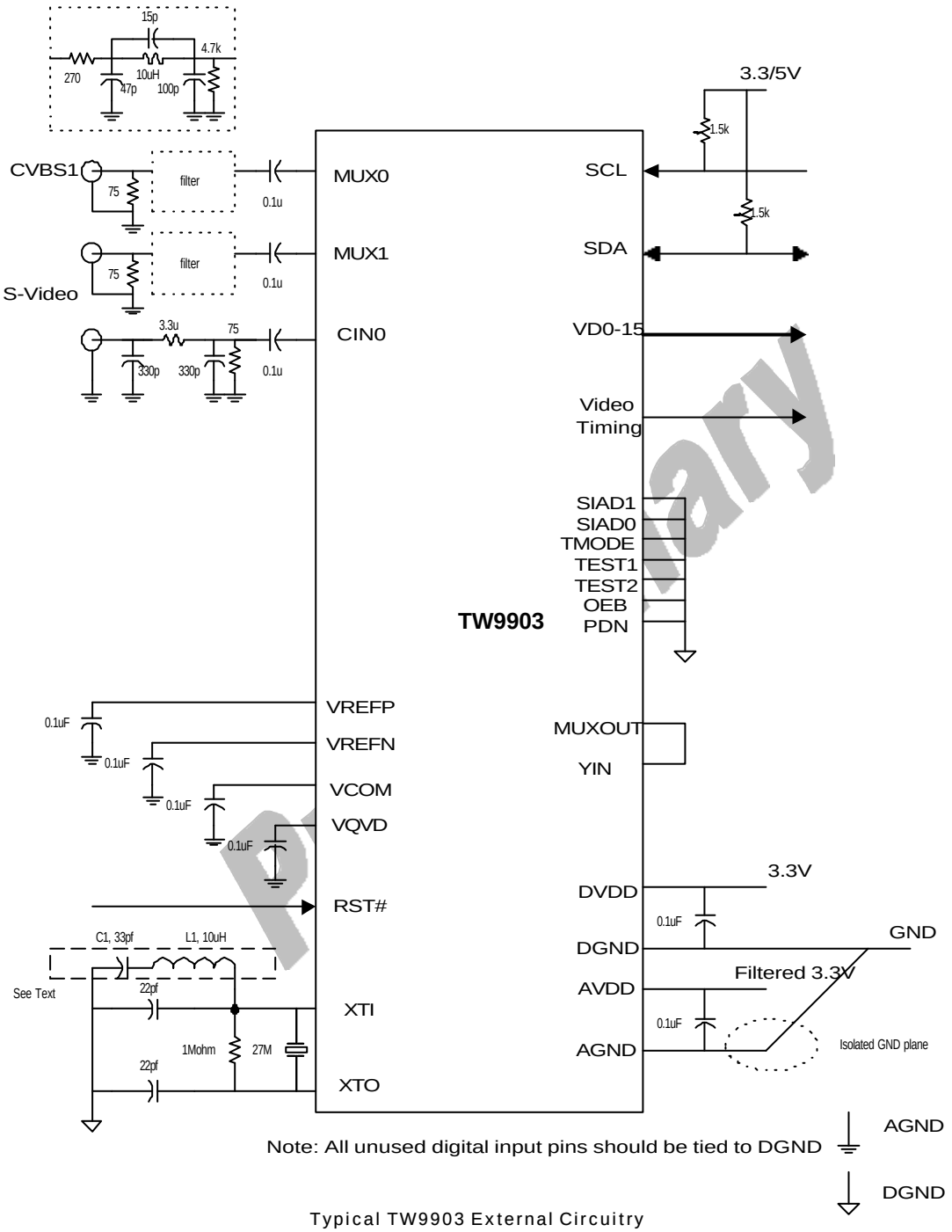
Clock Generation

The TW9903 requires one 27MHz crystal connected to XTI and XTO for all format decoding. The default crystal type should be 27MHz, fundamental mode, 20pF load capacitance or less, +- 50ppm, and with series resistance of 80 ohm or less. An external clock source of 27MHz can also be connected to the XTI input in place of the crystal. For True Square Pixel mode applications, a 24.54MHz crystal for 60Hz field rate source and a 29.5MHz crystal for 50Hz field rate source should be used. In this case, the bit FC27 of registers 0x02 should be set to '0' for proper operation. A typical 27MHz third overtone crystal circuit is shown in the following figure. In the case of using 27MHz fundamental mode crystal, the C1 and L1 can be omitted.

Power-Up

After power-up, the TW9903 registers have unknown values. The RST# pin must be asserted and released to bring all registers to its default values. After reset, the TW9903 data outputs are tri-stated. The OPFORM register should be written after reset to enable outputs desired.

Application Schematics

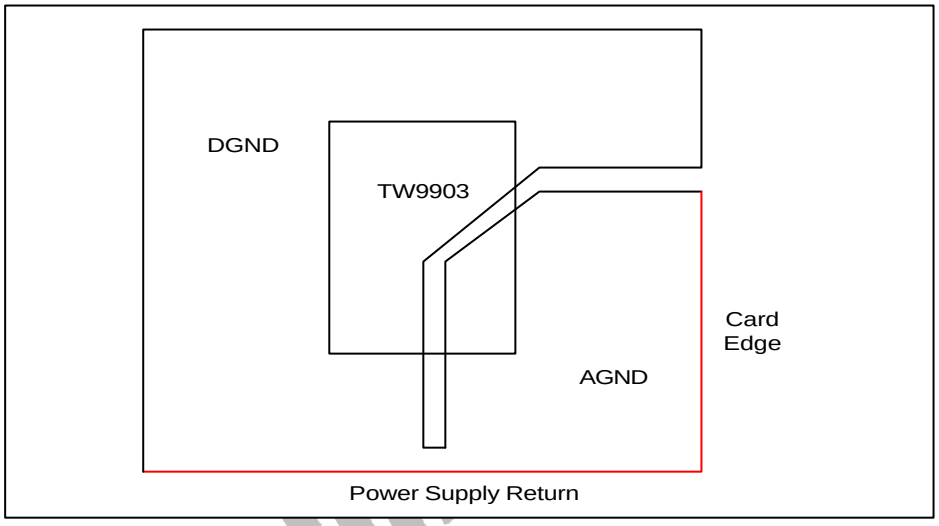


Typical TW9903 External Circuitry

PCB Layout Considerations

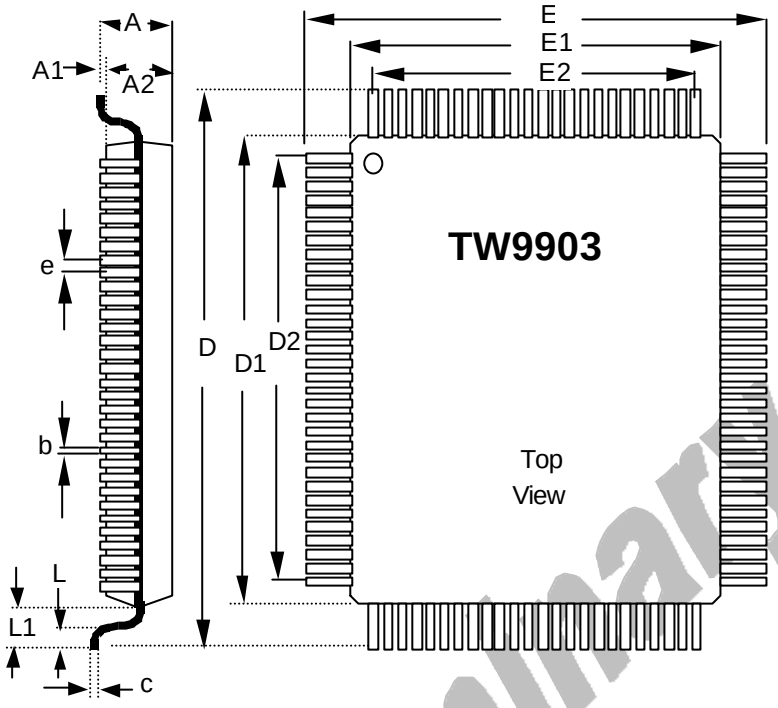
The PCB layout should be done to minimize the power and ground noise on the TW9903. This is done by good power de-coupling with minimum lead length on the de-coupling capacitors; well-filtered and regulated analog power input shielding and ground plane isolation.

The ground plane should cover most of the PCB area with separated digital and analog ground planes surrounding the chip. These two planes should be at the same electrical potential and connected together near the power supply. The following figure shows a ground plane layout example.



To minimize crosstalk, the digital signals of TW9903 should be separated from the analog circuitry. Moreover, the digital signals should not cross over the analog power and ground plane. Parallel running of digital lines for long distance should also be avoided.

100-pin PQFP Package Mechanical Drawing

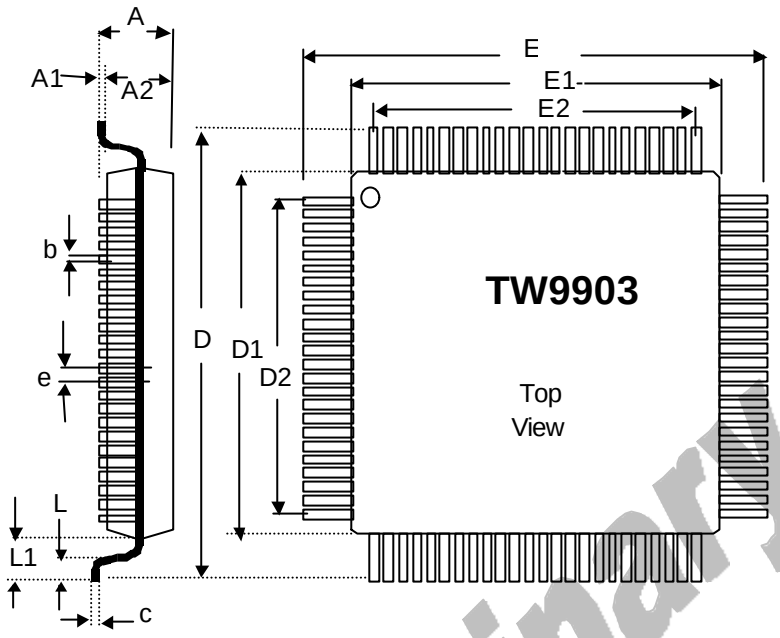


Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	3.40	---	---	0.134
A1	0.25	---	---	0.010	---	---
A2	2.55	2.72	3.05	0.100	0.107	0.120
b	0.22	0.30	0.38	0.009	0.012	0.015
c	0.11	0.15	0.23	0.004	0.006	0.009
e	0.65 Basic			0.026 Basic		
D	22.95	23.2	23.45	0.903	0.913	0.923
D1	20.00 Basic			0.787 Basic		
D2	18.85 Ref			0.742 Ref		
E	17.20 Basic			0.677 Basic		
E1	14.00 basic			0.551 Basic		
E2	12.35 Ref			0.486		
L	0.73	---	1.03	0.029	---	0.041
L1	1.60 Ref			0.063Ref		

Note: 1. Dimension of D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do include mold mismatch and are determined at datum plane.

2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed. The maximum b dimension by more than 0.08mm dambar cannot be located on the lower radius or the lead root.

100-pin LQFP Package Mechanical Drawing



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.09	0.10	0.20	0.004	---	0.008
e	0.4 Basic			0.016 Basic		
D	14.0 Basic			0.551 Basic		
D1	12.00 Basic			0.472 Basic		
D2	9.60			0.378		
E	14.0 Basic			0.551Basic		
E1	12.00 Basic			0.472 Basic		
E2	9.60			0.378		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 Ref			0.039Ref		

Note: 1. Dimension of D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do include mold mismatch and are determined at datum plane.

2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed. The maximum b dimension by more than 0.08mm dambar cannot be located on the lower radius or the lead root.