SiS302LV Datasheet

Preliminary

Contents

1 General Description

SiS302LV, which is an accompany chip of SiS VGA chip, integrates

- A NTSC/PAL video encoder with Macrovision Ver.7.1.L1 option for TV display.
- A dual link LVDS transmitter with bi-linear scaling capability for TFT LCD panel display.

All the above functions can support dual-display features. It means that the second display device driven by SiS302LV can display independent resolutions, color depths and frame rates different from the traditional CRT monitor driven by primary VGA chip. SiS302LV receives digital video signals and control signals from the primary VGA chip then transforms them into composite, S or component video output for TV display, LVDS signals for LCD display. The output display combination can be one of the three : (1) Primary CRT+SiS302LV TV, (2) Primary CRT+SiS302LV LCD,(3) SiS302LV TV + SiS302LV LCD.

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The package type of SiS302LV is 128-pin LQFP.

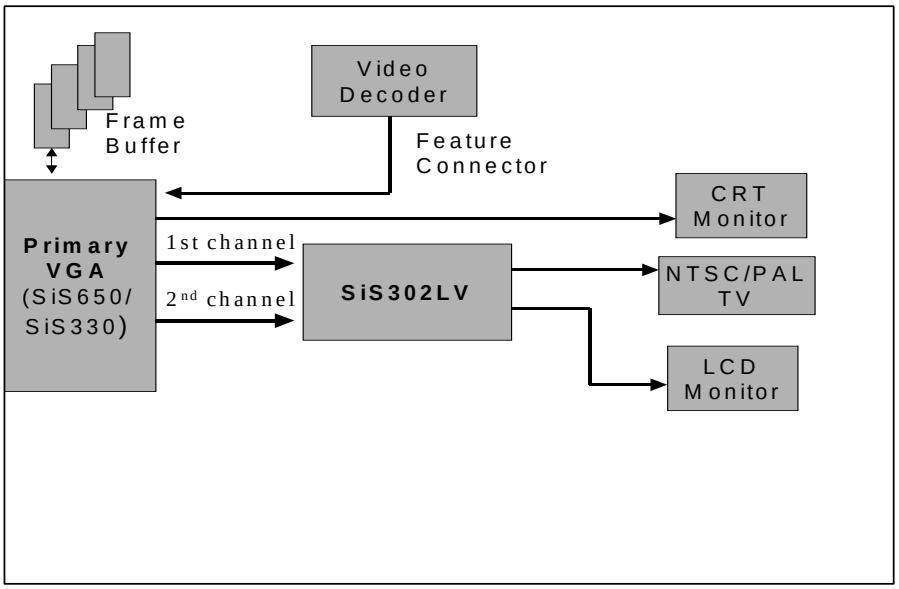

Figure 1 SiS302LV Application Block Diagram

2 Features

2.1 TV Display

- Supports PAL and NTSC Systems.
- Supports Composite, S-Video, and Component RGB(SCART) Output Signals
- Supports Macrovision Copy Protection Process Rev. 7.1.L1
- Support Progressive TV 525P YPbPr Output Signals.
- Support Macrovision Copy Protection Waveforms for 525p Progressive Scan Output
- Supports TV/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode
- Provides Adaptive 6-Line Anti-Flicker Filtering.
- Provides Hardware Interpolation for Programmable Under-Scan/Over-Scan Adjustment.
- Provides Programmable Display Position Adjustment.
- Provides Programmable Notch Filter for Cross Color Elimination.
- Provides Chrominance Filter for Cross Luminance Elimination
- Provides Color Saturation Adjustment for Vivid TV Output.
- Provides Gamma Correction Independent of That of Primary VGA.
- Auto-Sense of TV Connection

2.2 LVDS Interfaced LCD Panel Display

- Supports LVDS Transmitter Function.
- Support dual link LVDS up to WUXGA.
- Compatible with TIA/EIA-644 LVDS standard.
- Provides Bi-Linear Scaling to Scale VGA Low Resolution Mode up for LCD Display—up to 1600*1200.
- Supports LCD/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode.
- Support 2D dither for 18-bit panels.
- Provides Programmable Display Centering.
- Compliant with VESA DDC2B
- Compliant with VESA Plug & Display, Hot Plugging Function.

- Provides Gamma Correction Independent of That of Primary VGA

3 Functional Description

Before describing the detailed function, let's introduce the two data operation paths of SiS302LV. SiS302LV data operation paths:

Channel B path: SiS302LV provides clock, horizontal sync, vertical sync signals to primary VGA. The CRT timing at primary VGA is gen-locked to these clock and control signals. This path is selected when SiS302LV performs TV or LCD only display function. The CRT timing at primary VGA indicates the 1st (traditional CRT) at standard VGA modes and indicates the 2nd CRT (an extra CRT at SiS primary VGA) at enhanced modes.

There's scaling hardware in this path. In LCD display mode, this hardware can make lower VGA resolution display to fit up to 1600*1200 LCD panel. In TV display mode, this scaler can provide overscan and underscan option for TV.

Channel A path: SiS302LV accepts pixel clock, horizontal sync and vertical sync signals from primary VGA. The video data coming from primary VGA's 1st CRT passes the LVDS encoding data path to panel display. This mode is active when SiS302LV performs TV and LCD simultaneous display mode.

At TV and LCD simultaneous display mode, TV data stream run through Channel B and LCD data stream run through Channel A.

3.1 Input Data Formats

3.1.1 Two Data Stream, 12-bit , Dual-Edge Data Rate Transfer

- Two 24-bit data per pixel clock from VAD[11:0] (LCD display) and VBD[11:0] (TV display).
- Maximum pixel rate is 270M pixels/sec with 270MHz pixel clock
- TV and LCD simultaneous display.

LCD Input Data Stream				
Pixel	LCDP0		LCDP1	
	Clk Fall	Clk Rise	Clk Fall	Clk Rise
VAD[11:8]	LCDP0_G[3:0]	LCDP0_R[7:4]	LCDP1_G[3:0]	LCDP1_R[7:4]
VAD[7:4]	LCDP0_B[7:4]	LCDP0_R[3:0]	LCDP1_B[7:4]	LCDP1_R[3:0]
VAD[3:0]	LCDP0_B[3:0]	LCDP0_G[7:4]	LCDP1_B[3:0]	LCDP1_G[7:4]

TV Input Data Stream				
Pixel	TVP0		TVP1	
	Clk Fall	Clk Rise	Clk Fall	Clk Rise
VBD[11:8]	TVP0_G[3:0]	TVP0_R[7:4]	TVP1_G[3:0]	TVP1_R[7:4]
VBD[7:4]	TVP0_B[7:4]	TVP0_R[3:0]	TVP1_B[7:4]	TVP1_R[3:0]
VBD[3:0]	TVP0_B[3:0]	TVP0_G[7:4]	TVP1_B[3:0]	TVP1_G[7:4]

3.1.2 TV Encoder

SiS302LV integrates video encoder which supports NTSC/PAL and 525P TV format. The output signal formats for NTSC/PAL system can be composite, S-video(Y/C), or RGB-component. The output signal format for 525P TV is progressive YPbPr-component output. The DAC resolution is 10-bits per channel. There are three sets of DAC implemented in SiS302LV.

The display on TV can be under-scan or over-scan mode. This function is supported by a flexible horizontal/vertical hardware scaling capability. The scaling factor is programmable. The maximum source resolution can be 1024x768.

The Y/C filter implemented can reduce the cross-color and cross-luminance intervention. A SiS patented adaptive anti-flicker technology is implemented to remove the flicker but still retain the sharp profile.

Four analog comparators are integrated to detect the status of the TV connection. BIOS and software utility can set the video encoder configuration intelligently based on the read-back value. DAC power-down mode is automatically set according to the sense result.

The display at TV can be simultaneous and independent of the CRT output of primary VGA.

4 LVDS Interfaced LCD Display

SiS302LV supports LVDS interfaced LCD panel display by implementing the transmitter inside. SiS302LV receives parallel digital video data from a primary VGA. Through the use of optional DC balanced and internal low jitter PLL, SiS302LV encodes and serializes the input video data. The serialized data is then transmitted to the receiver chip over the Low Voltage Differential Signal interconnection layer.

The output from SiS302LV composes of eight high-speed data channels and two low speed clock channel. The maximum output data pixel rate is 270M pixels/sec in dual link mode, the corresponding display resolution is 1920x1600@60Hz. There is built-in bi-linear scaling and centering function for low resolution image display.

When supporting LCD monitor display only, LCD display data stream runs through Channel B path to implement scaling-up. SiS302LV outputs the pixel clock, horizontal sync and vertical sync to the primary VGA.

When supporting TV and LCD simultaneous display mode, LCD display data stream runs through Channel A path without scaling-up option.

4.1 Display Modes

4.1.1 TV Output Modes

The table below lists part of the display modes supported by SiS302LV. The maximum input active resolution at PAL and NTSC system is 1024x768. Because of the flexible scaling hardware, the over/under-scan (Active TV lines) modes supported by SiS302LV are far beyond of these listed below.

System	Input(Active) Resolution	Active TV lines	Over/Under scan
NTSC	320x200	480 ~ 400	+
NTSC	640x480	480 ~ 400	+
NTSC	720x480	480 ~ 400	+
NTSC	720x400	480 ~ 400	+
NTSC	800x600	480 ~ 420	+
NTSC	1024x768	480	Over

System	Input(Active) Resolution	Active TV lines	Over/Under scan
PAL	320x200	540 ~ 500	+
PAL	640x480	540 ~ 500	+
PAL	720x400	540 ~ 500	+

PAL	720x576	576 ~ 510	+
PAL	800x600	600 ~ 510	+
PAL	1024x768	520	Under

System	Input(Active) Resolution	Active TV Lines	Over/Under scan
525P	320x200	480 ~ 400	+
525P	640x480	480 ~ 400	+
525P	720x480	480 ~ 400	+
525P	720x400	480 ~ 400	+
525P	800x600	480 ~ 420	+
525P	1024x768	480	Over

4.1.2 LCD Output Modes

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Display Panel Size	Data Path	
	Channel B (302LV Scale-up)	Channel A (302LV does not Scale-up)
1920x1600	-	#
1600x1200	+	#
1400x1050	+	#
1280x1024	+	#
1024x768	+	#
800x600	+	#

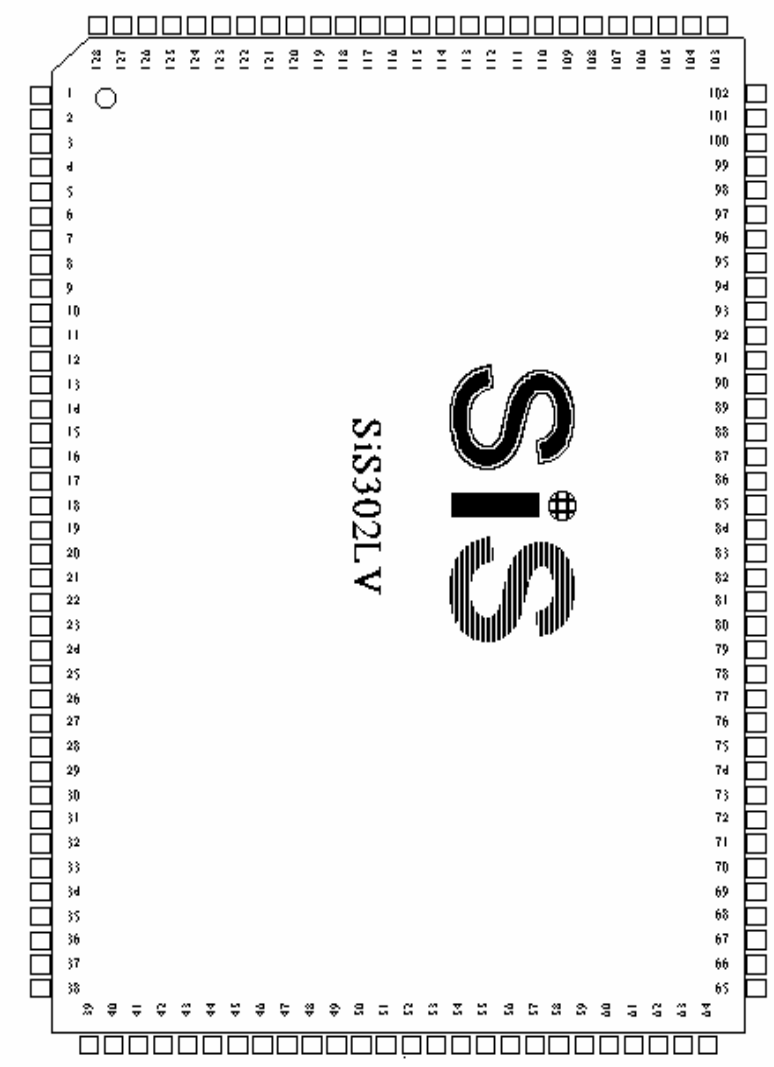
Note: "+" means LCD display only mode

"#" means TV and LCD simultaneous display mode.

"-" means no scaling

5 Pin Description

5.1 Pin Outline



5.2 Pin Description

Pin #	Pin Name	I/O Type	Description
108	VBHCLK	I	Register programming serial bus: clock
107	VBCAD	I/O	Register programming serial bus: command/address/data. External pull high.
99	VAD[11]	I	LCD/TV video data input: R[7]
98	VAD[10]	I	LCD/TV video data input: R[6]
97	VAD[9]	I	LCD/TV video data input: R[5]
96	VAD[8]	I	LCD/TV video data input: R[4]
95	VAD[7]	I	LCD/TV video data input: R[3]
94	VAD[6]	I	LCD/TV video data input: R[2]
90	VAD[5]	I	LCD/TV video data input: R[1]
89	VAD[4]	I	LCD/TV video data input: R[0]
88	VAD[3]	I	LCD/TV video data input: G[7]
87	VAD[2]	I	LCD/TV video data input: G[6]
86	VAD[1]	I	LCD/TV video data input: G[5]
85	VAD[0]	I	LCD/TV video data input: G[4]
82	VBD[11]	I	LCD/TV video data input: G[3]
81	VBD[10]	I	LCD/TV video data input: G[2]
80	VBD[9]	I	LCD/TV video data input: G[1]
79	VBD[8]	I	LCD/TV video data input: G[0]
78	VBD[7]	I	LCD/TV video data input: B[7]
77	VBD[6]	I	LCD/TV video data input: B[6]
73	VBD[5]	I	LCD/TV video data input: B[5]
72	VBD[4]	I	LCD/TV video data input: B[4]
71	VBD[3]	I	LCD/TV video data input: B[3]
70	VBD[2]	I	LCD/TV video data input: B[2]
69	VBD[1]	I	LCD/TV video data input: B[1]
68	VBD[0]	I	LCD/TV video data input: B[0]
93	VAGCLK	I	Channel A pixel clock input. Input from primary VGA.
101	VAHSYNC	I	Channel A HSYNC. Input from primary VGA.
102	VAVSYNC	I	Channel A VSYNC. Input from primary VGA.

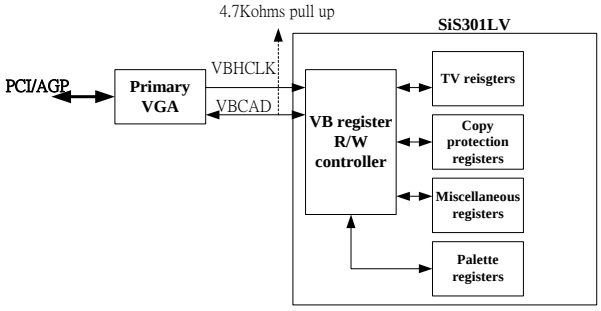
104	VADE	I	Channel A display enable. Input from primary VGA. VADE is high when input video stream data are valid.
76	VBGCLK	I	Channel B pixel clock input.. Input from primary VGA.
59	VBCLK	I/O	Clock output to primary VGA
66	VBHSYNC	I/O	Channel B Horizontal SYNC output to primary VGA. Active high.
65	VBVSYNC	I/O	Channel B Vertical SYNC output to primary VGA. Active high.
63	VBDE	I/O	Channel B display enable. Input from primary VGA. VBDE is high when input video stream data are valid.
67	VBCTL0	I/O	Video control bit 0. Input from primary VGA.
62	VBCTL1	I/O	Video control bit 1. Input from primary VGA
Miscellanies			
52	VBRCLK	I	Crystal input/External reference clock input. A parallel resonant 14.31818 MHz crystal (+/- 20 ppm) should be attached between this pin and VBOSCO, or an external CMOS compatible clock can drive this pin.
53	VBOSCO	O	Crystal output. A parallel resonant 14.31818 MHz crystal (+/- 20 ppm) should be attached between this pin and VBRCLK. However, if an external CMOS clock is attached to VBRCLK, this pin should be left open.
121	LCDSENSE	I/O	Reserve
122	INTERRUPN	I/O	Interrupt request. Active low.
123	EXTRSTN	I	External Reset
112	GPIOA	I/O	GPIO Pin. Default Tri-state.
113	GPIOB	I/O	GPIO Pin. Default Tri-state.
114	GPIOC	I/O	GPIO Pin. Default Tri-state
115	GPIOD	I/O	GPIO Pin. Default Tri-state.
116	DDCDATA	I/O	DDC Data.
117	DDCCLK	I/O	DDC Clock.
127	GPIOG	I/O	GPIO Pin. Default Output Low.
128	GPIOH	I/O	GPIO Pin. Default Output Low..
Pins for LVDS Interface			
36	EXTSWING	A I	LVDS external voltage reference
34	LX0N	A O	LVDS transmitter out : Channel 0

33	LX0P	A O	LVDS transmitter out : Channel 0
31	LX1N	A O	LVDS transmitter out : Channel 1
30	LX1P	A O	LVDS transmitter out : Channel 1
28	LX2N	A O	LVDS transmitter out : Channel 2
27	LX2P	A O	LVDS transmitter out : Channel 2
25	LXC1N	A O	LVDS transmitter out : Clock channel
24	LXC1P	A O	LVDS transmitter out : Clock channel
22	LX3N	A O	LVDS transmitter out : Channel 3
21	LX3P	A O	LVDS transmitter out : Channel 3
Pins for TV DAC			
38	V2RSET	A I	DAC reference resistor
40	V2COMP	A I	DAC compensation
41	IOCOMP	A O	DAC output Composite output at standard PAL/NTSC TV mode. R output at SCART TV. Pb output at progressive TV mode.
43	IOY	A O	DAC output : Y output at standard PAL/NTSC S-Video TV mode. G output at SCRT TV. Y output at progressive TV.
45	IOC	A O	DAC output : C output at standard PAL/NTSC S-Video TV. B output at SCRT TV. Pr output at progressive TV.
49	IOCS	A O	DAC output : TV CSYNC output at SCART TV.
Pins for analog power/ground			
1,19	LVDSPLLVDD		AVDD: for LVDS PLL
3,16	LVDSPLLVSS		AVSS : for LVDS PLL
54	PLL1VDD		AVDD: for internal PLL
51	PLL1VSS		AVSS: for internal PLL
7,13, 20,26 ,32	LAVDD		AVDD: for LVDS transmitter
4,10, 23,29 35	LAVSS		AVSS: for LVDS transmitter
37,47	DACVDD		DAC VDD
39,48	DACVSS		DAC ground
Pins for digital power/ground			

110, 103, 91, 74, 64, 55	DVDD		Internal digital power.
109, 105, 92, 75, 61, 58	DVSS		Internal digital ground
60	OVDD		Power supply for I/O pins 3.3V or 1.8V. This OVDD need 1.8V when the data interface with primary VGA using low voltage swing, else 3.3V is applied
111	OVDD35V		Power supply for I/O pins using 3.3V power but with 5 V tolerance. This OVDD35V is always 3.3V.
100	OVSS		Ground pins for all I/O pins.
118	VDD5V		Power supply for 5V tolerance I/O pins
Pins for Test			
119	V2HSYNC	I/O	Reserved.
120	V2VSYNC	I/O	Reserved.
56	TSCLKI	I	Reserved
57	TVCLKO	I/O	Reserved
124	PFTEST1	I	For testing . Default pull low.
125	PFTEST2	I	For testing. Default pull low
126	PFTESTO	I/O	For testing output. Default pull low.

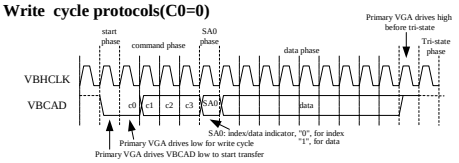
6 Register Programming Interface

SiS301LV Register Programming Block Diagram



Transfer Protocol

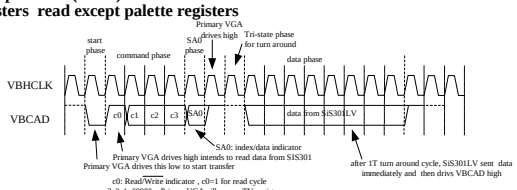
Write cycle protocols(C0=0)



c0: Read/Write indicator , c0=0 for write cycle
c3c2c1: "000" : Primary VGA will access TV registers
"001" : Primary VGA will access Copy protection registers
"010" : Primary VGA will access Miscellaneous registers
"011" : Primary VGA will access palette registers

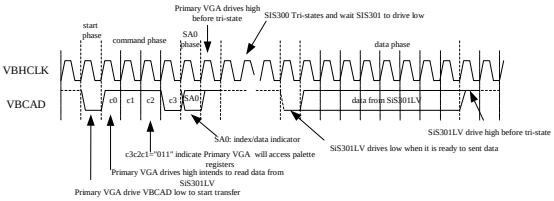
Read cycle protocols(C0=1)

a. registers read except palette registers



c0: Read/Write indicator , c0=1 for read cycle
c3c2c1: "000" : Primay VGAwill access TV registers
"001" : Primary VGA will access Copy protection registers
"010" : Primary VGA will access Miscellaneous registers

b. palette registers read



7 Electrical Characteristics

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7.1 DC Characteristic

Table 1 Absolute Maximum Conditions

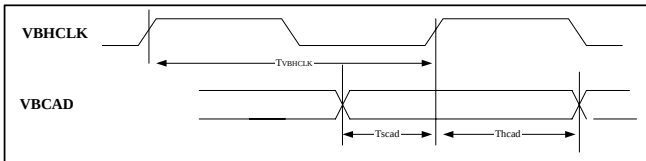
Symbol	Parameter	Min.	Max.	Units
Ta	Ambient Temperature	0	70	℃
Vcc	Supply Voltage 3.3V	-0.3	Vcc + 0.3	V
Vin	Input Voltage	-0.3	Vcc + 0.3	V
Vo	Output Voltage	-0.5	Vcc + 0.3	V
Pd	Package Power Dissipation	-	1.8	W

Table 2 DC Digital Specifications

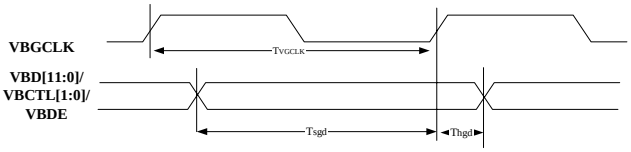
Symbol	Parameter	Min.	Max.	Units
Vil	Input Low Voltage	-0.5	0.8	V
Vih	Input High Voltage	2.2	Vcc + 10%	V
Vol	Output Low Voltage	-	0.4	V
Voh	Output High Voltage	2.4	-	V
Ili	Input Leakage Current	-	±10	uA
Ito	Tristate Leakage Current	-	±20	uA

7.2 AC Characteristic

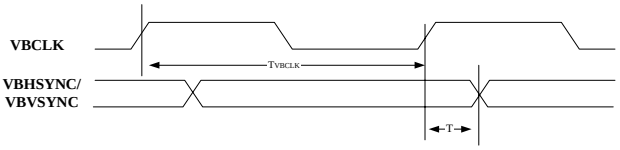
Symbol	Parameter	Min.	Max.	Units
T_{VBHCLK}	VBHCLK period	15	-	ns
T_{VGCLK}	VBGCLK period	9.0	-	ns
T_{VBCLK}	VBCLK period	9.0	-	ns
Tscad	VBCAD valid delay time	-	9	ns
Thcad	VBCAD valid preset time	-	3	ns
Tsgd	VBD[11:0], VBCTL[1:0], VBDE setup time	2	-	ns
Thgd	VBD[11:0], VBCTL[1:0], VBDE hold time	2	-	ns
Tdctl	VBHSYNC, VBVSYNC output delay at master mode	-	4	ns



VBCAD timing relative to VBHCLK

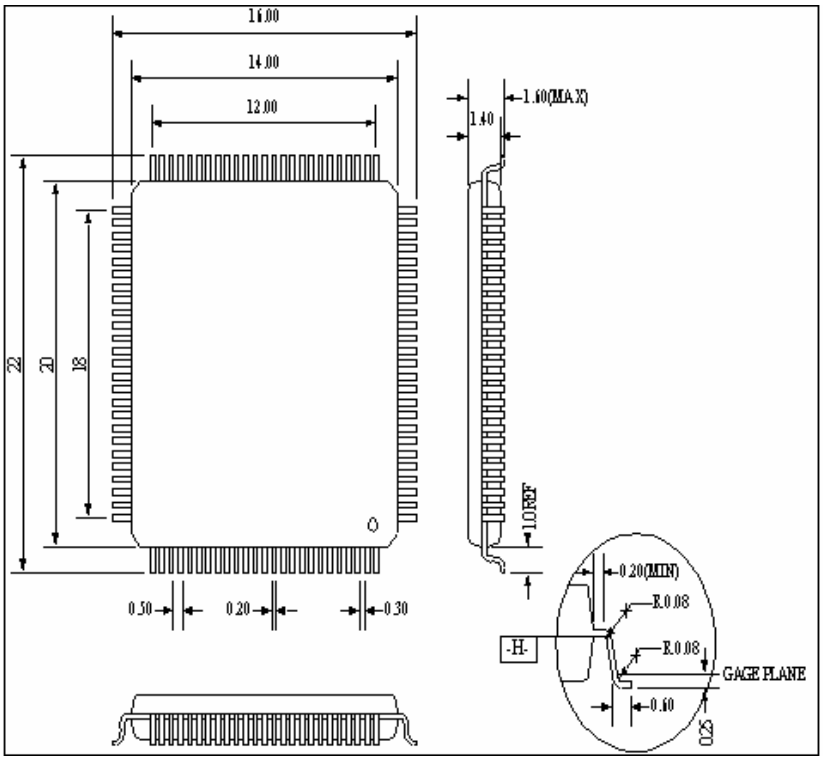


VBD[11:0]/VBCTL[1:0]/VBDE timing



VBHSYNC/VBVSYNC timing relative to VBCLK at SiS301 master mode

8 Mechanical Dimension



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