MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Advance Information

1.2 A 15 V H-Bridge Motor Driver IC

17510

1.2 A 15 V H-BRIDGE MOTOR DRIVER IC

The 17510 is a monolithic H-Bridge designed to be used in portable electronic applications such as digital and SLR cameras to control small DC motors.

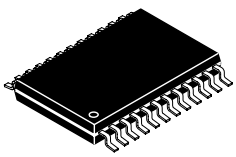
The 17510 can operate efficiently with supply voltages as low as 2.0 V to as high as 15 V. Its low $R_{DS(ON)}$ H-Bridge output MOSFETs (0.45 Ω typical) can provide continuous motor drive currents of 1.2 A and handle peak currents up to 3.8 A. It is easily interfaced to low-cost MCUs via parallel 5.0 V compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

The 17510 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

Features

- 2.0 V to 15 V Continuous Operation
- Output Current 1.2 A (DC), 3.8 A (Peak)
- 450 mΩ $R_{DS(ON)}$ H-Bridge MOSFETs
- 5.0 V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown
- Cross-Conduction Suppression
- Pb-Free Packaging Designated by Suffix Code EJ

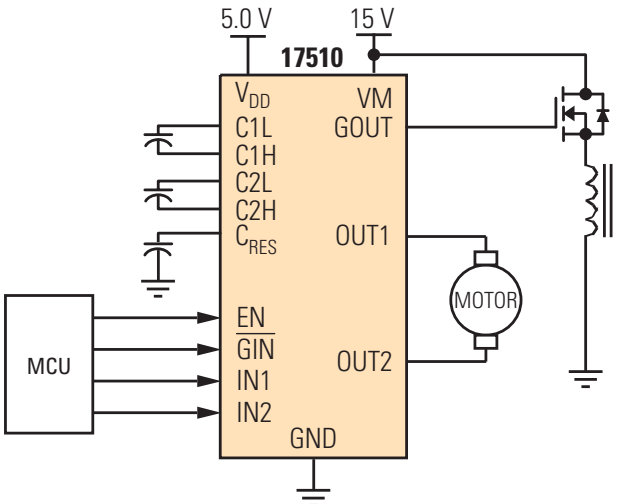


MTB SUFFIX
EJ (Pb-FREE) SUFFIX
CASE 948K-01
24-LEAD TSSOP

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MPC17510EJ/R2	-30°C to 65°C	24 TSSOPW

17510 Simplified Application Diagram



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Specifications and information herein are subject to change without notice.

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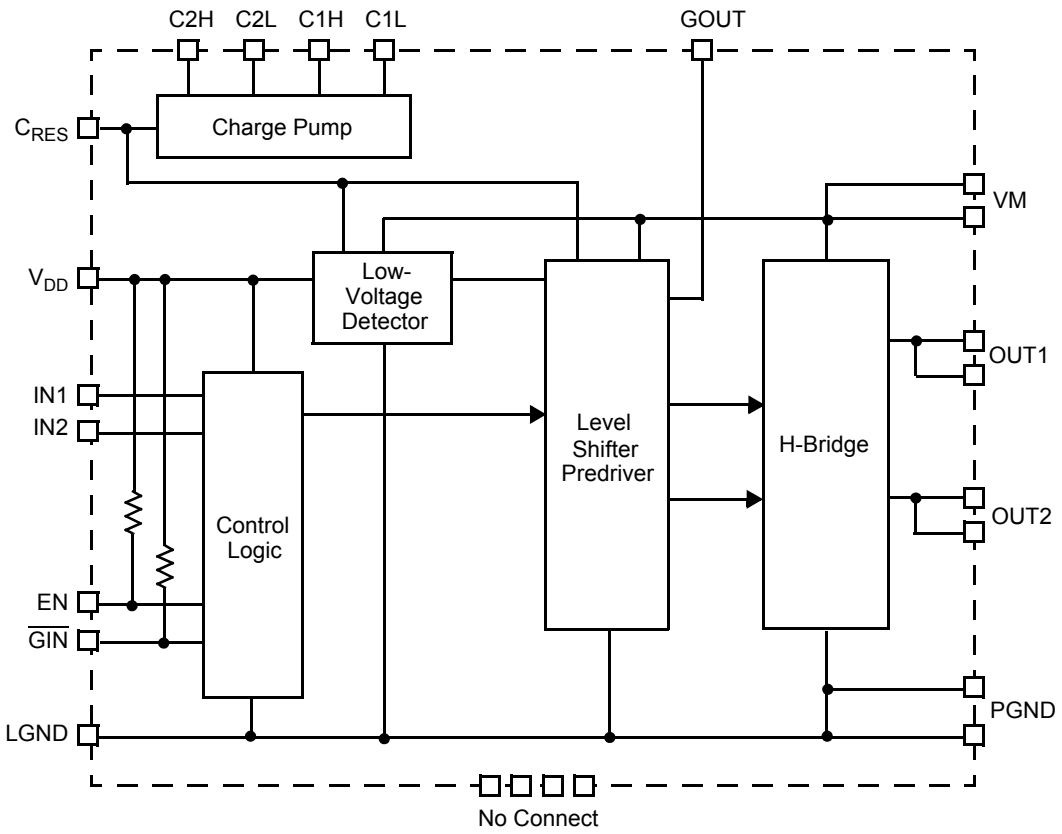
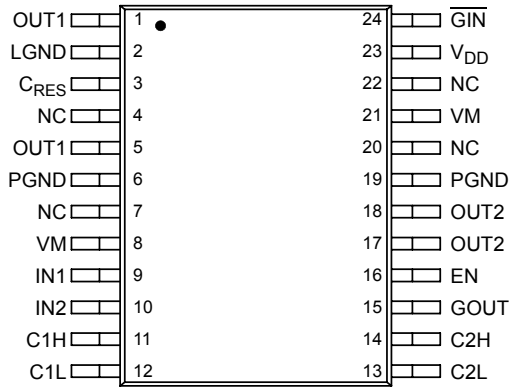


Figure 1. 17510 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1, 5	OUT1	Output 1	Driver output 1 terminals.
2	LGND	Logic Ground	Logic ground.
3	C_{RES}	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor terminal.
4, 7, 20, 22	NC	No Connect	No connection to these terminals.
17, 18	OUT2	Output 2	Driver output 2 terminals.
6, 19	PGND	Power Ground	Power ground.
8, 21	VM	Motor Drive Power Supply	Motor power supply voltage input terminals.
9	IN1	Input Control 1	Control signal input 1 terminal.
10	IN2	Input Control 2	Control signal input 2 terminal.
11	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
12	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
13	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
14	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
15	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
16	EN	Enable Control	Enable control signal input terminal.
23	V_{DD}	Logic Supply	Control circuit power supply terminal.
24	$\overline{GIN}$	Gate Driver Input	LOW = True control signal for GOUT terminal.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 16	V
Charge Pump Output Voltage (Note 1)	$V_{C_{RES}}$	-0.5 to 13	V
Logic Supply Voltage	V_{DD}	-0.5 to 6.0	V
Signal Input Voltage (EN, IN1, IN2, $\overline{GIN}$)	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (Note 2)	 I_O I_{OPK}	 1.2 3.8	A
ESD Voltage Human Body Model (Note 3) Machine Model (Note 4)	 V_{ESD1} V_{ESD2}	 ±1900 ±130	V
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Junction Temperature	T_J	-30 to 150	°C
Operating Ambient Temperature	T_A	-30 to 65	°C
Power Dissipation (Note 5)	P_D	1.0	W
Thermal Resistance	$R_{\theta JA}$	120	°C/W
Soldering Temperature (Note 6)	T_{SOLDER}	260	°C

Notes

1. When supplied externally, connect via 3.0 kΩ resistor.
2. T_A = 25°C, 10 ms pulse at 200 ms interval.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
4. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
5. T_A = 25°C, $R_{\theta JA}$ = 120°C/W, 37 mm x 50 mm Cu area (1.6 mm FR-4 PCB).
6. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_M = 15 V, V_{DD} = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage	V_M	2.0	–	15	V
Logic Supply Voltage	V_{DD}	4.0	–	5.5	V
Capacitor for Charge Pump	C1, C2, C3	0.001	–	0.1	μF
Standby Power Supply Current (Note 7)					
Motor Supply Standby Current	$I_{V_{MSTBY}}$	–	–	1.0	μA
Logic Supply Standby Current	$I_{V_{DDSTBY}}$	–	0.3	1.0	mA
Logic Supply Current (Note 8)	$I_{V_{DD}}$	–	3.3	4.0	mA
Low-Voltage Detection Circuit					V
Detection Voltage (V_{DD}) (Note 9)	V_{DD}DET	1.5	2.5	3.5	
Detection Voltage (V_M)	V_MDET	4.0	5.0	6.0	
Driver Output ON Resistance (Note 10)	$R_{DS(ON)}$				Ω
V_M = 2.0 V, 8.0 V, 15 V		–	0.45	0.55	
GATE DRIVE					
Gate Drive Voltage (Note 11)	$V_{C_{RES}}$				V
No Current Load		12	13	13.5	
Gate Drive Ability (Internally Supplied)	$V_{C_{RESload}}$				V
$I_{C_{RES}}$ = -1.0 mA		10	11.2	–	
Gate Drive Output					V
I_{OUT} = -50 μA	$V_{GOUThigh}$	$V_{C_{RES}}$-0.5	$V_{C_{RES}}$-0.1	$V_{C_{RES}}$	
I_{IN} = 50 μA	$V_{GOUTlow}$	LGND	LGND+0.1	LGND+0.5	
CONTROL LOGIC					
Logic Input Voltage (EN, IN1, IN2, $\overline{GIN}$)	V_{IN}	0	–	V_{DD}	V
Logic Input Function (4.0 V < V_{DD} < 5.5 V)					
High-Level Input Voltage	V_{IH}	V_{DD} x 0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x 0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	μA
Low-Level Input Current	I_{IL}	-1.0	–	–	μA
EN/$\overline{GIN}$ Terminal	I_{IL}	-200	-50	–	μA

Notes

7. Excluding pull-up resistor current, including current of gate-drive circuit.
8. f_{IN} = 100 kHz.
9. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage $V_{C_{RES}}$ is applied from an external source, $V_{C_{RES}}$ = 7.5 V.
10. I_O = 1.2 A source + sink.
11. Input logic signal not present.

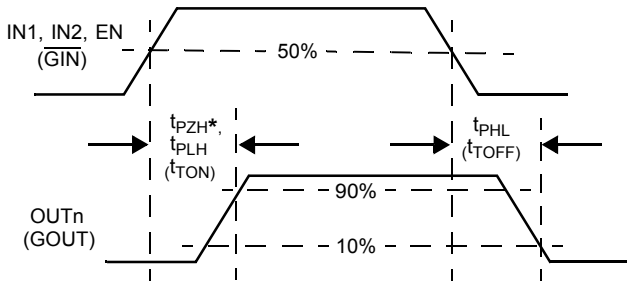
DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_M = 15 V, V_{DD} = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT (EN, IN1, IN2, $\overline{GIN}$)					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (Note 12)	t_R	–	–	1.0 (Note 13)	μs
Input Pulse Fall Time (Note 14)	t_F	–	–	1.0 (Note 13)	μs
OUTPUT					
Propagation Delay Time					μs
Turn-ON Time	t_{PZH}	–	0.3	1.0	
Turn-ON Time	t_{PLH}	–	1.2	2.0	
Turn-OFF Time	t_{PHL}	–	0.5	1.0	
GOUT Output Delay Time (Note 15)					μs
Turn-ON Time	t_{TON}	–	–	10	
Turn-OFF Time	t_{TOFF}	–	–	10	
Charge Pump Circuit					
Oscillator Frequency	f_{OSC}	100	200	400	kHz
Rise Time (Note 16)	$tV_{C_{RES}on}$	–	0.1	1.0	ms
Low-Voltage Detection Time	$t_{V_{DD}DET}$	–	–	10	ms

Notes
12. Time is defined between 10% and 90%.
13. That is, the input waveform slope must be steeper than this.
14. Time is defined between 90% and 10%.
15. Load is 500 pF.
16. Time to charge C_{RES} to 11 V after application of V_{DD}.

Timing Diagrams



***** The last state is “Z”.

Figure 2. t_{PLH}, t_{PHL}, and t_{PZH} Timing

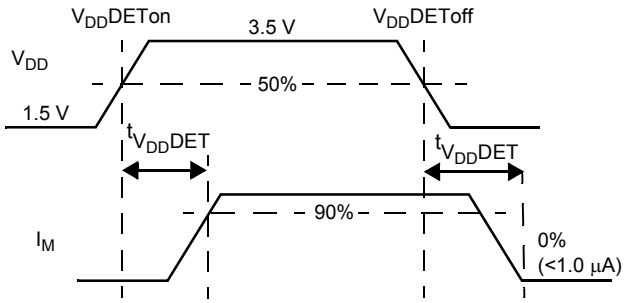


Figure 3. Low-Voltage Detection Timing

Table 1. Truth Table

INPUT				OUTPUT		
EN	**IN1**	**IN2**	**$\overline{\text{GIN}}$**	**OUT1**	**OUT2**	**GOUT**
H	L	L	X	Z	Z	X
H	H	L	X	H	L	X
H	L	H	X	L	H	X
H	H	H	X	L	L	X
L	X	X	X	L	L	L
H	X	X	L	X	X	H
H	X	X	H	X	X	L

H = High.
L = Low.
Z = High impedance.
X = Don’t care.
The $\overline{\text{GIN}}$ terminal and EN terminal are pulled up to V_{DD} with internal resistance.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 17510 is a monolithic H-Bridge power IC applicable to small DC motors used in portable electronics. The 17510 can operate efficiently with supply voltages as low as 2.0 V to as high as 15 V, and it can provide continuos motor drive currents of 1.2 A while handling peak currents up to 3.8 A. It is easily interfaced to low-cost MCUs via parallel 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17510 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

Basic protection and operational features (direction, dynamic braking, PWM control of speed and torque, main power supply undervoltage detection and shutdown, logic power supply undervoltage detection and shutdown), in addition to the 1.0 A rms output current capability, make the 17510 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 17510 devices can be used to control bipolar stepper motors. The 17510 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 1, 17510 Simplified Internal Block Diagram, page 2, the 17510 is a monolithic H-Bridge with built-in charge pump circuitry. For a DC motor to run, the input conditions need to be set as follows: ENable input logic HIGH, one INput logic LOW, and the other INput logic HIGH (to define output polarity). The 17510 can execute dynamic braking by setting both IN1 and IN2 logic HIGH, causing both low-side MOSFETs in the output H-Bridge to turn ON. Dynamic braking can also implemented by taking the ENable logic LOW. The output of the H-Bridge can be set to an open-circuit high-impedance (Z) condition by taking both IN1 and IN2 logic LOW. (refer to Table 1, Truth Table, page 7).

The 17510 outputs are capable of providing a continuous DC load current of up to 1.2 A. An internal charge pump supports PWM frequencies to 200 kHz. The EN terminal also controls the charge pump, turning it off when EN = LOW, thus allowing the 17510 to be placed in a power-conserving sleep mode.

FUNCTIONAL TERMINAL DESCRIPTION

OUT1 and OUT2

The OUT1 and OUT2 terminals provide the connection to the internal power MOSFET H-Bridge of the IC. A typical load connected between these terminals would be a small DC motor. These outputs will connect to either VM or PGND, depending on the states of the control inputs (refer to Table 1, Truth Table, page 7).

PGND and LGND

The power and logic ground terminals (PGND and LGND) should be connected together with a very low-impedance connection.

C_{RES}

The C_{RES} terminal provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively this terminal can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor. The voltage at the C_{RES} terminal will be approximately three times the V_{DD} voltage, as the internal charge pump utilizes a voltage tripler circuit. The $V_{C_{RES}}$ voltage is used by the IC to supply gate drive for the internal power MOSFET H-Bridge.

VM

The VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUT1 and OUT2. All VM terminals must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between terminals.

VM has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

IN1, IN2, and EN

The IN1, IN2, and EN terminals are input control terminals used to control the outputs. These terminals are 5.0 V CMOS-compatible inputs with hysteresis. The IN1, IN2, and EN work together to control OUT1 and OUT2 (refer to Table 1, Truth Table).

$\overline{GIN}$

The $\overline{GIN}$ input controls the GOUT terminal. When $\overline{GIN}$ is set logic LOW, GOUT supplies a level-shifted high-side gate drive signal to an external MOSFET. When $\overline{GIN}$ is set logic HIGH, GOUT is set to GND potential.

C1L and C1H, C2L and C2H

These two pairs of terminals, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

GOUT

The GOUT output terminal provides a level-shifted, high-side gate drive signal to an external MOSFET with C_{iss} up to 500 pF.

V_{DD}

The V_{DD} terminal carries the 5.0 V supply voltage and current into the logic sections of the IC. V_{DD} has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

APPLICATIONS

Typical Application

Figure 4 shows a typical application for the 17510.

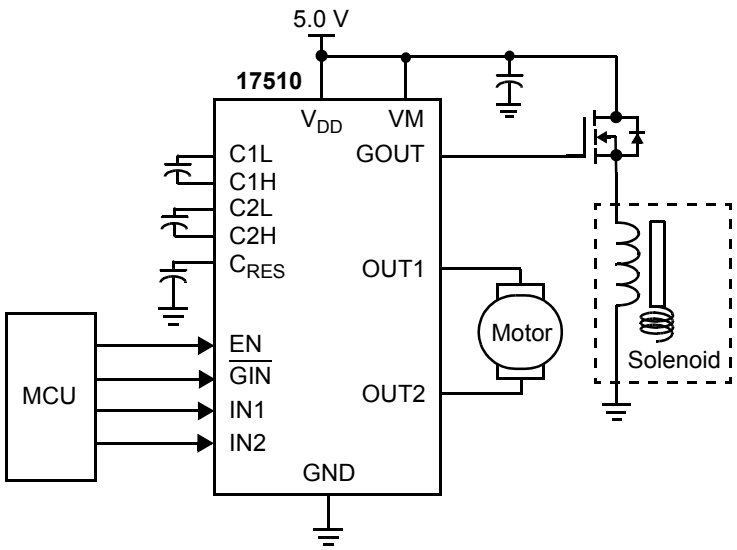


Figure 4. 17510 Typical Application Diagram

CEMF Snubbing Techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply terminal (VM) (see Figure 5).

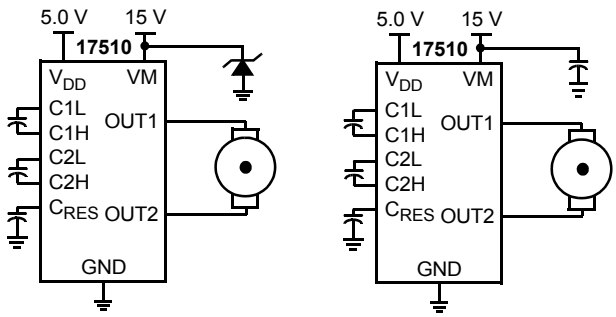
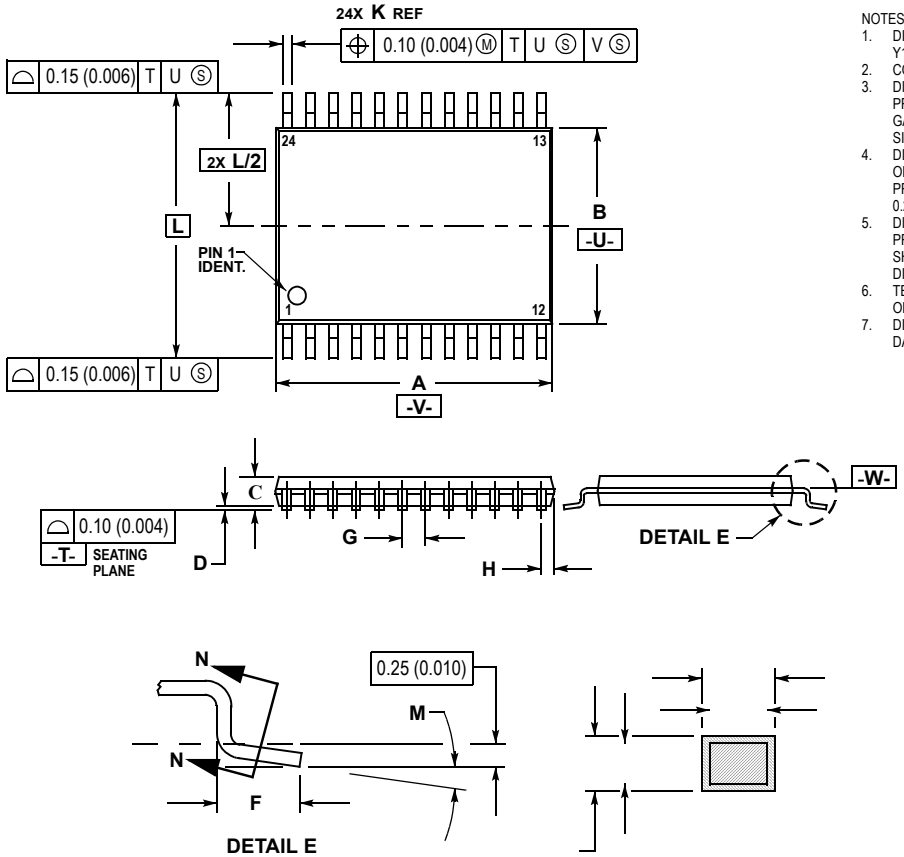


Figure 5. CEMF Snubbing Techniques

PACKAGE DIMENSIONS

MTB SUFFIX
EJ (Pb-FREE) SUFFIX
24-LEAD TSSOP WIDE BODY
PLASTIC PACKAGE
CASE 948K-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	5.50	5.70	0.216	0.224
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	7.60 BSC		0.299 BSC	
M	0°	8°	0°	8°

NOTES

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MPC17510

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