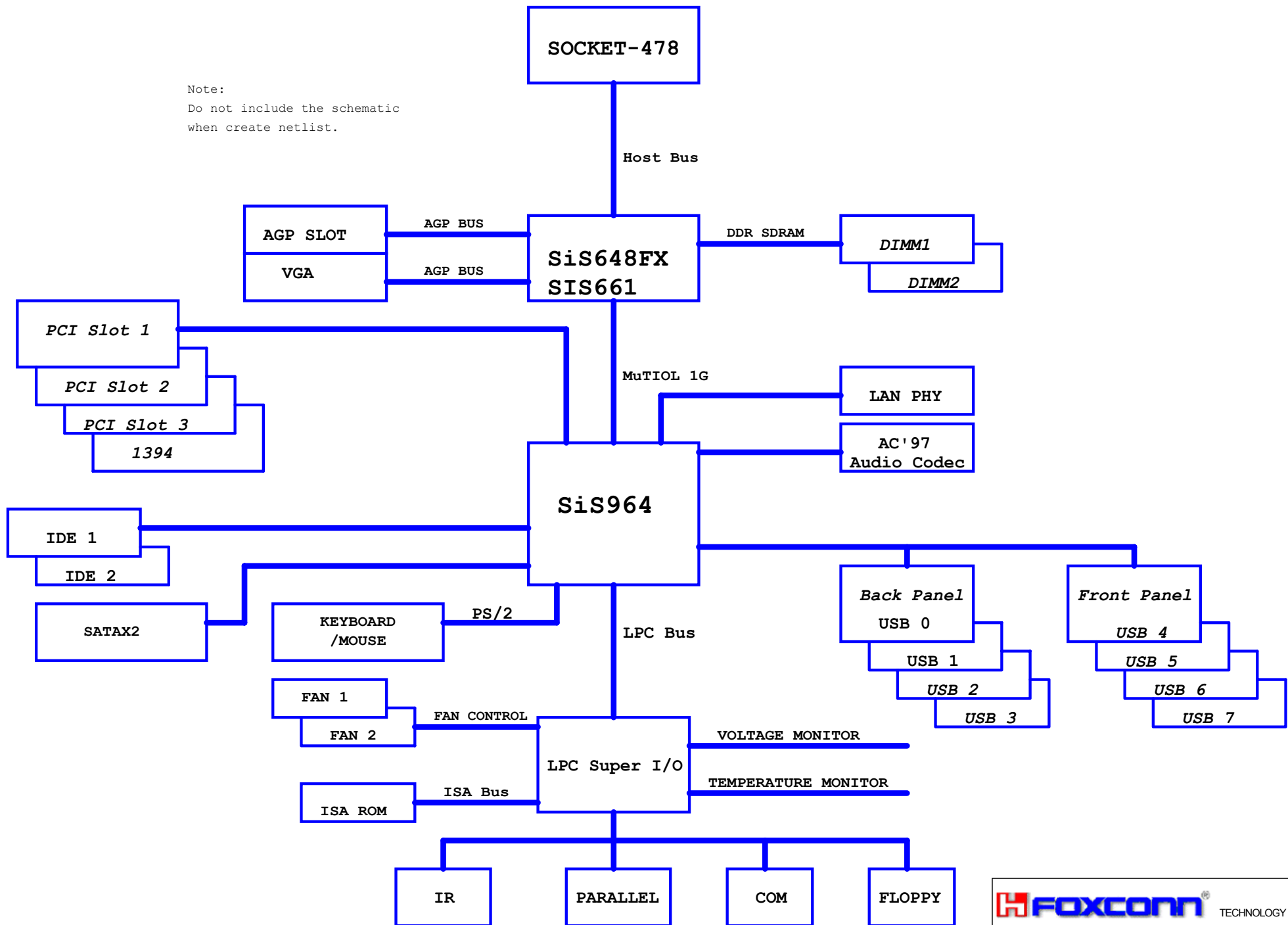
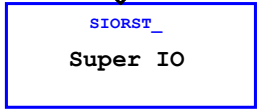
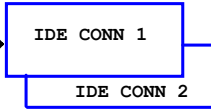
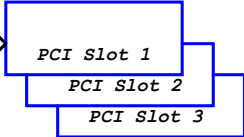
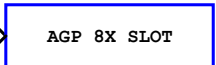
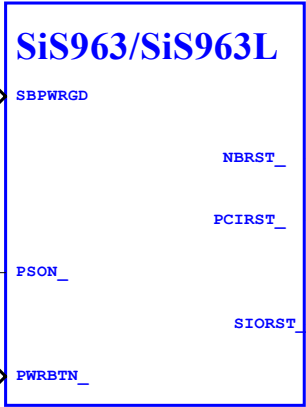
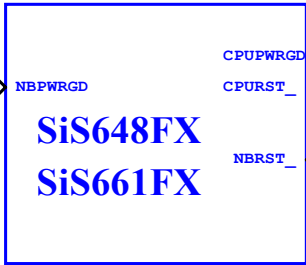
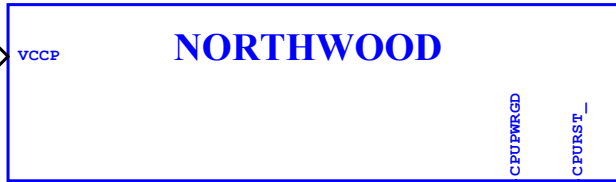
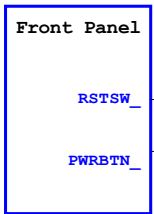
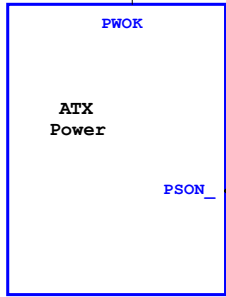
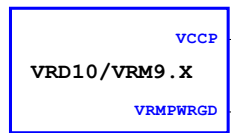
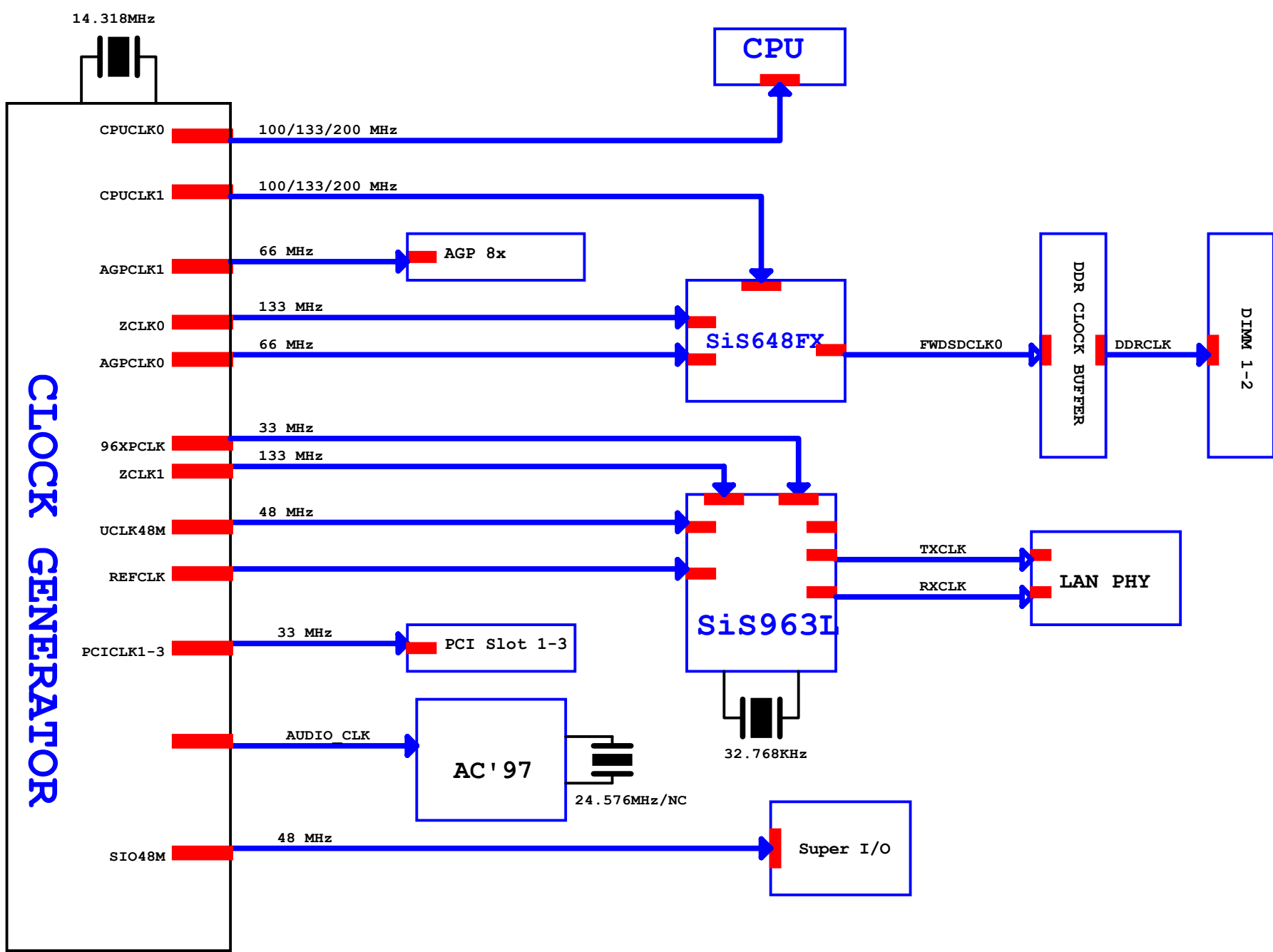
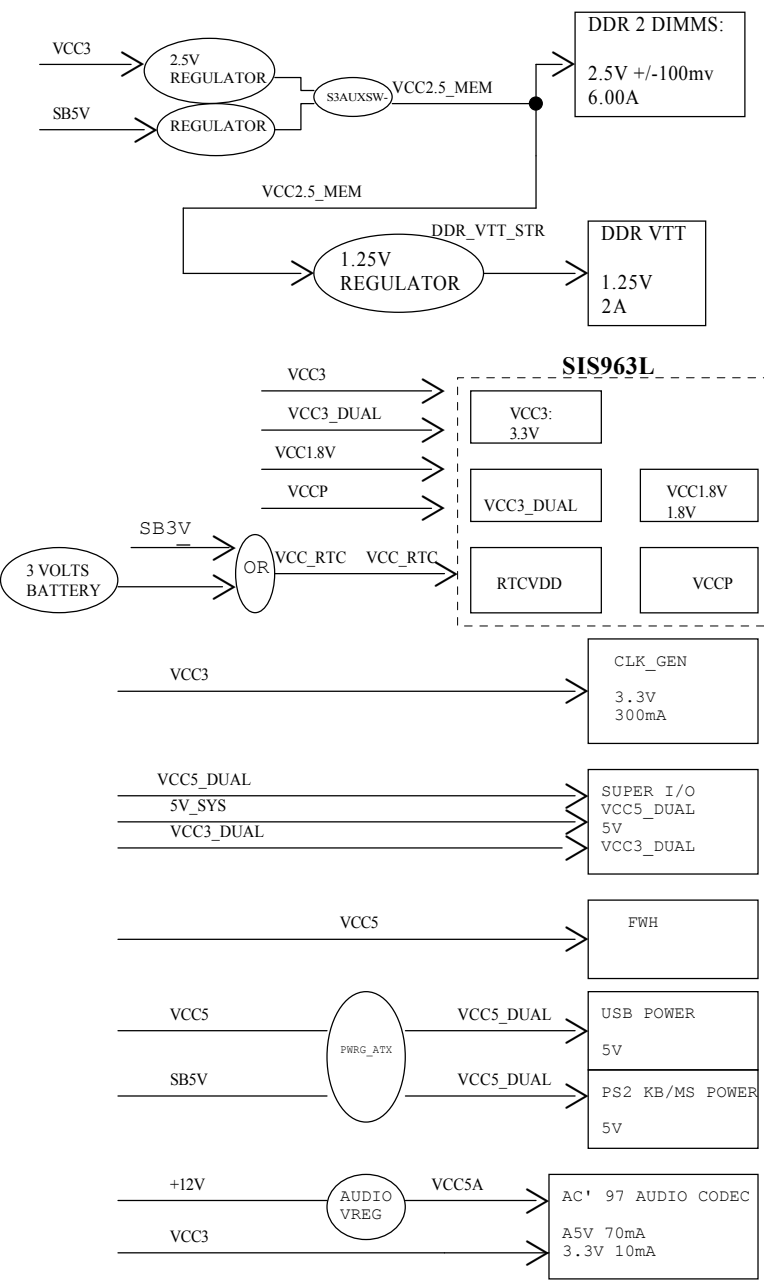
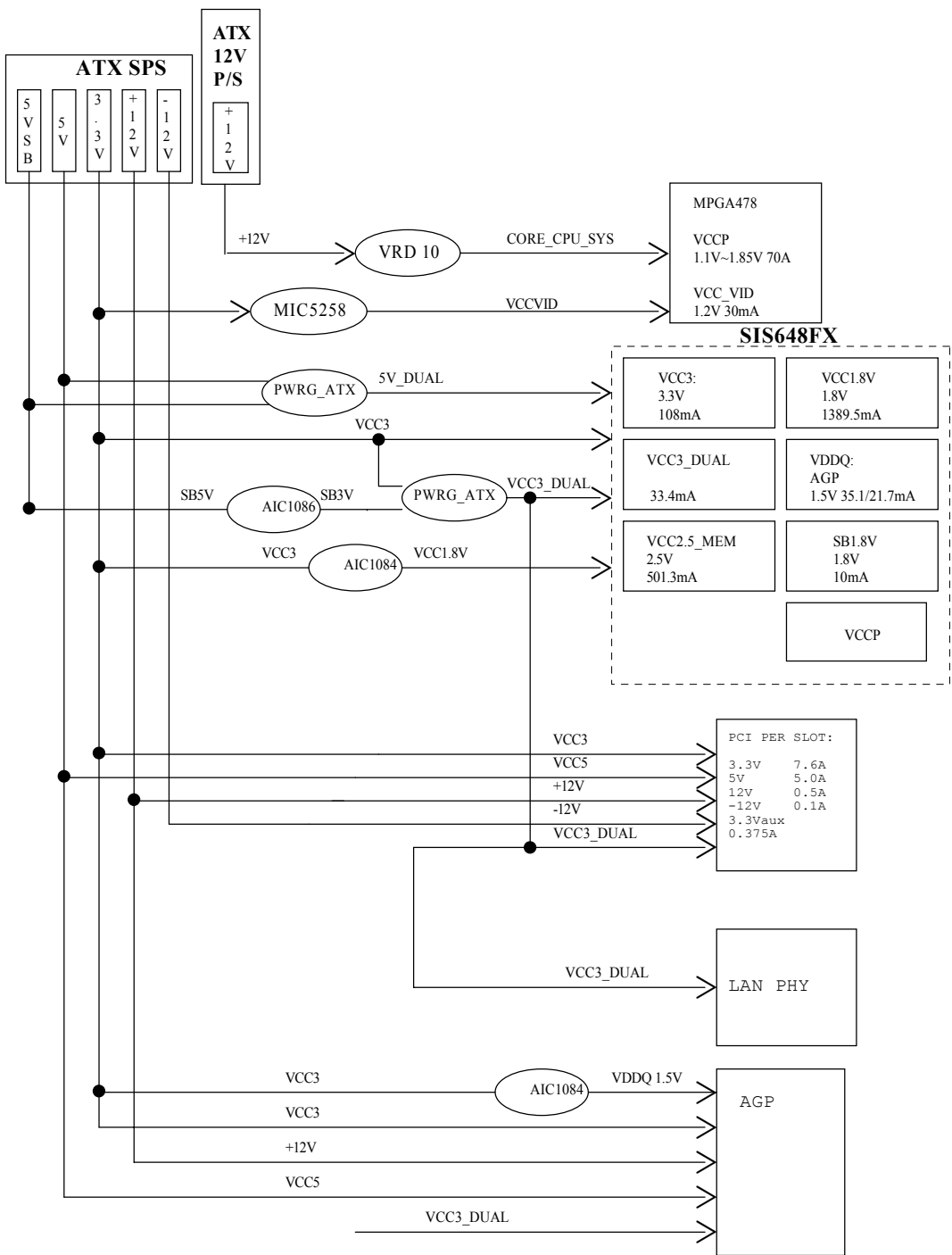


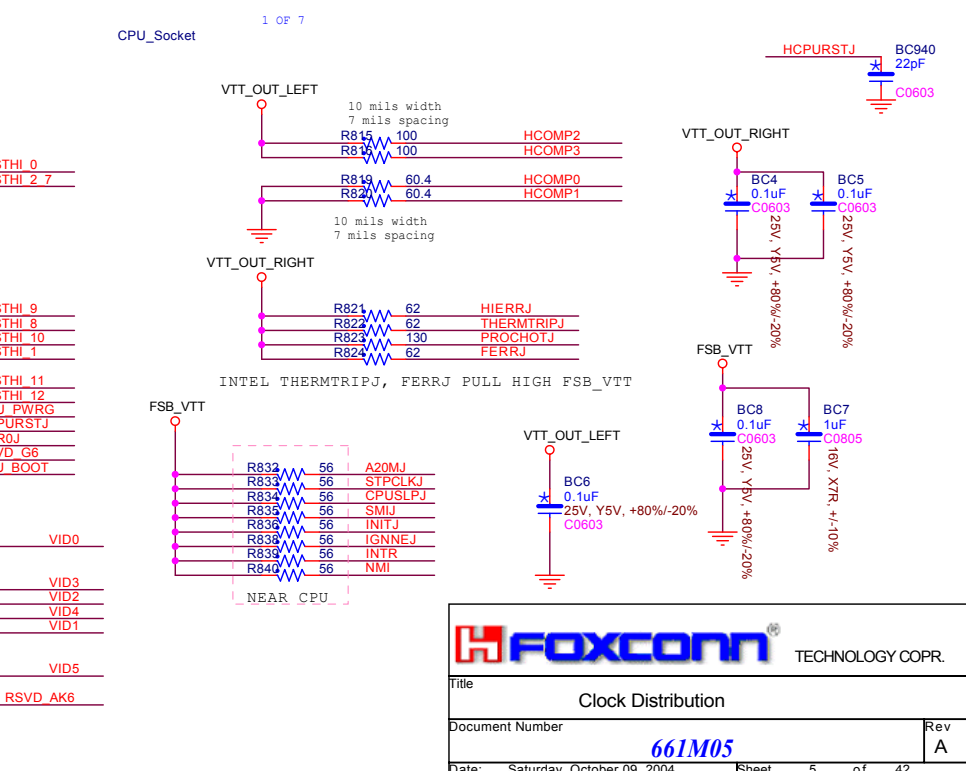
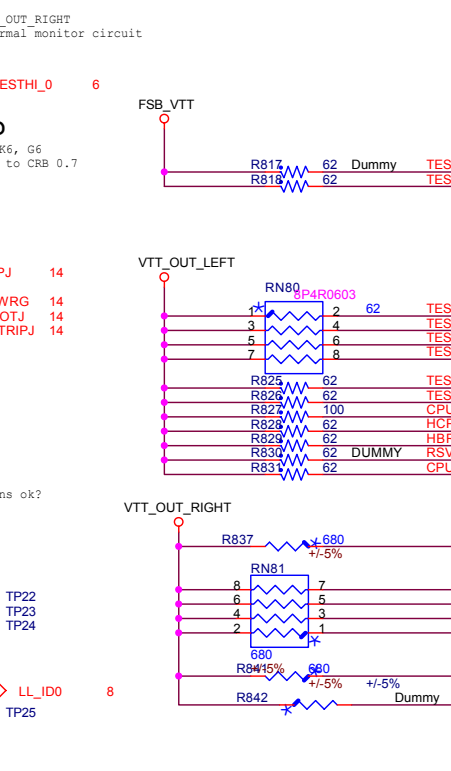
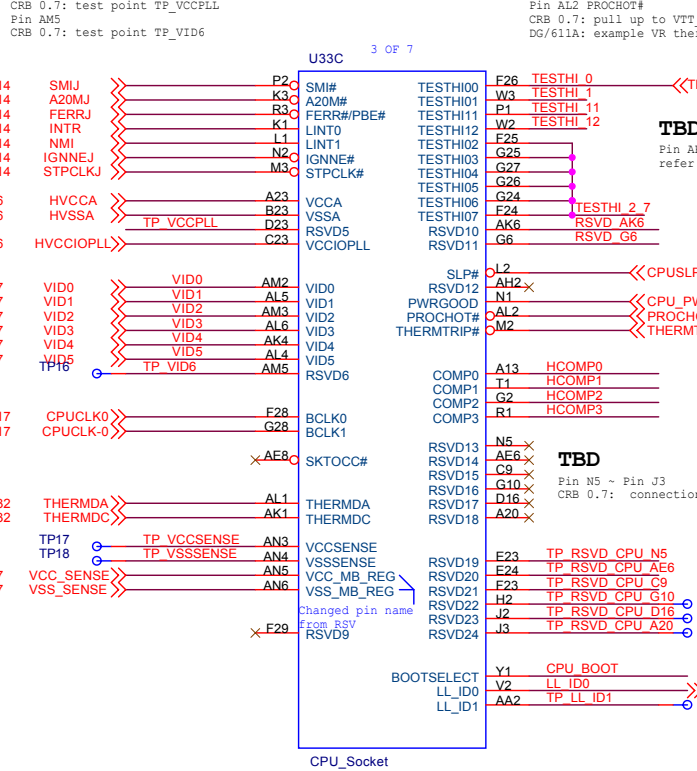
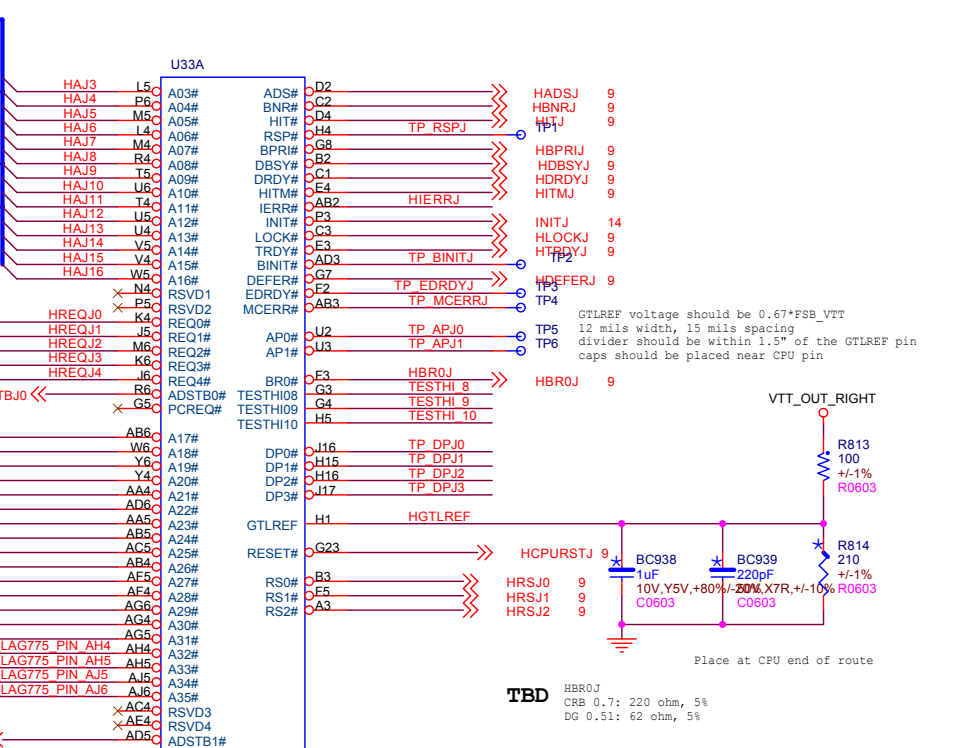
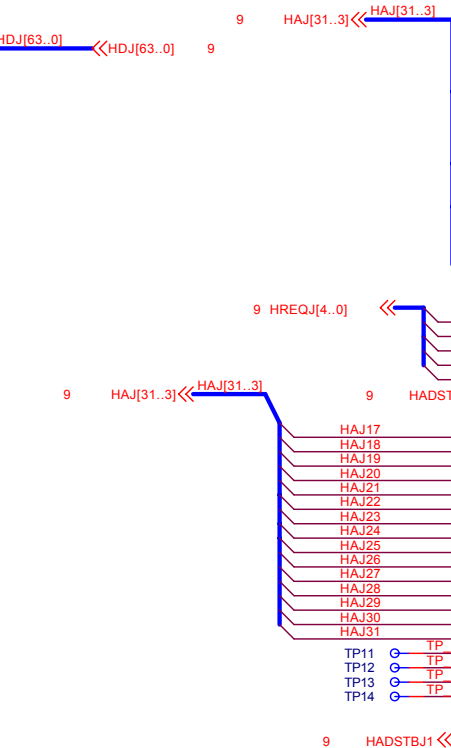
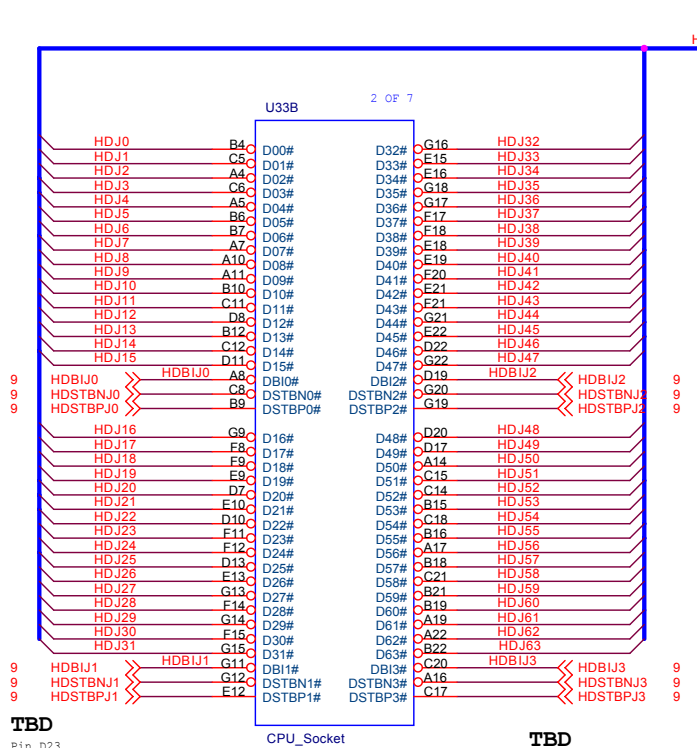
Note:
Do not include the schematic
when create netlist.











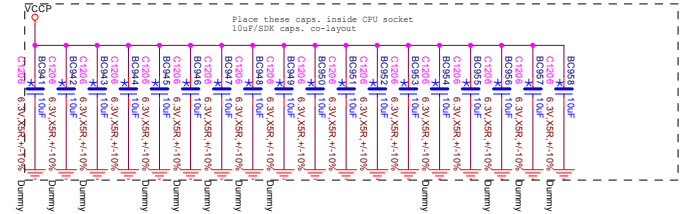
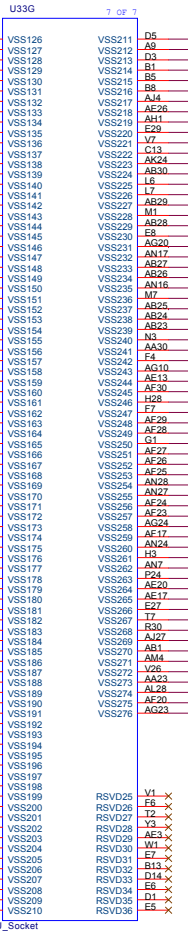
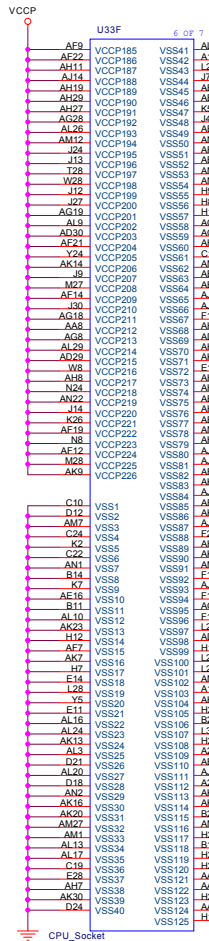
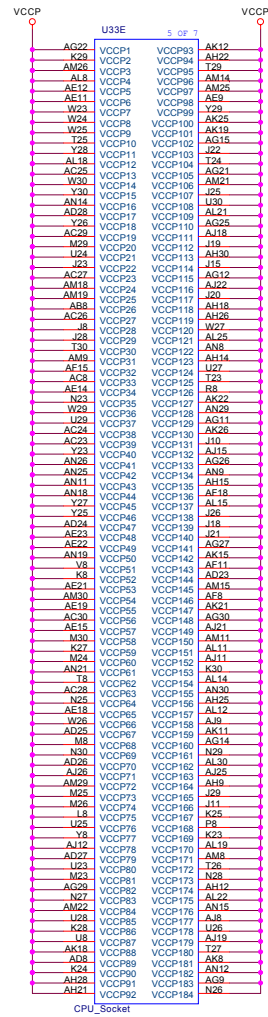
Clock Distribution

Document Number: **661M05**

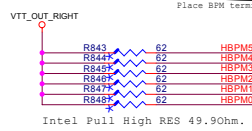
Date: Saturday, October 09, 2004

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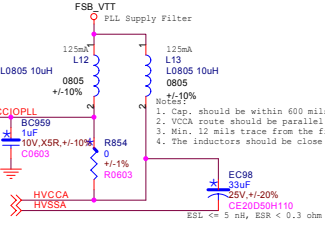
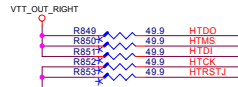
Rev A



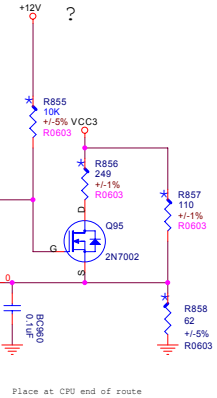
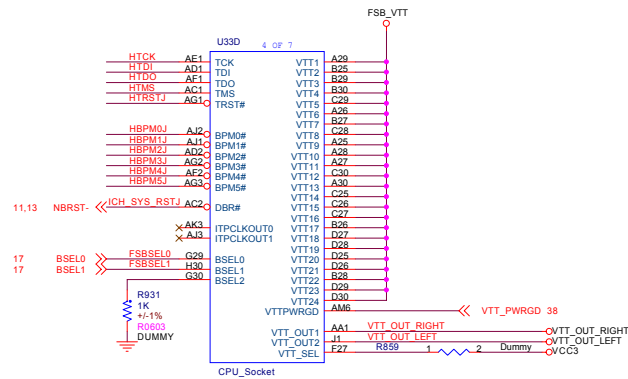
note: 7/6-change termination 49.9 to R8702 4)

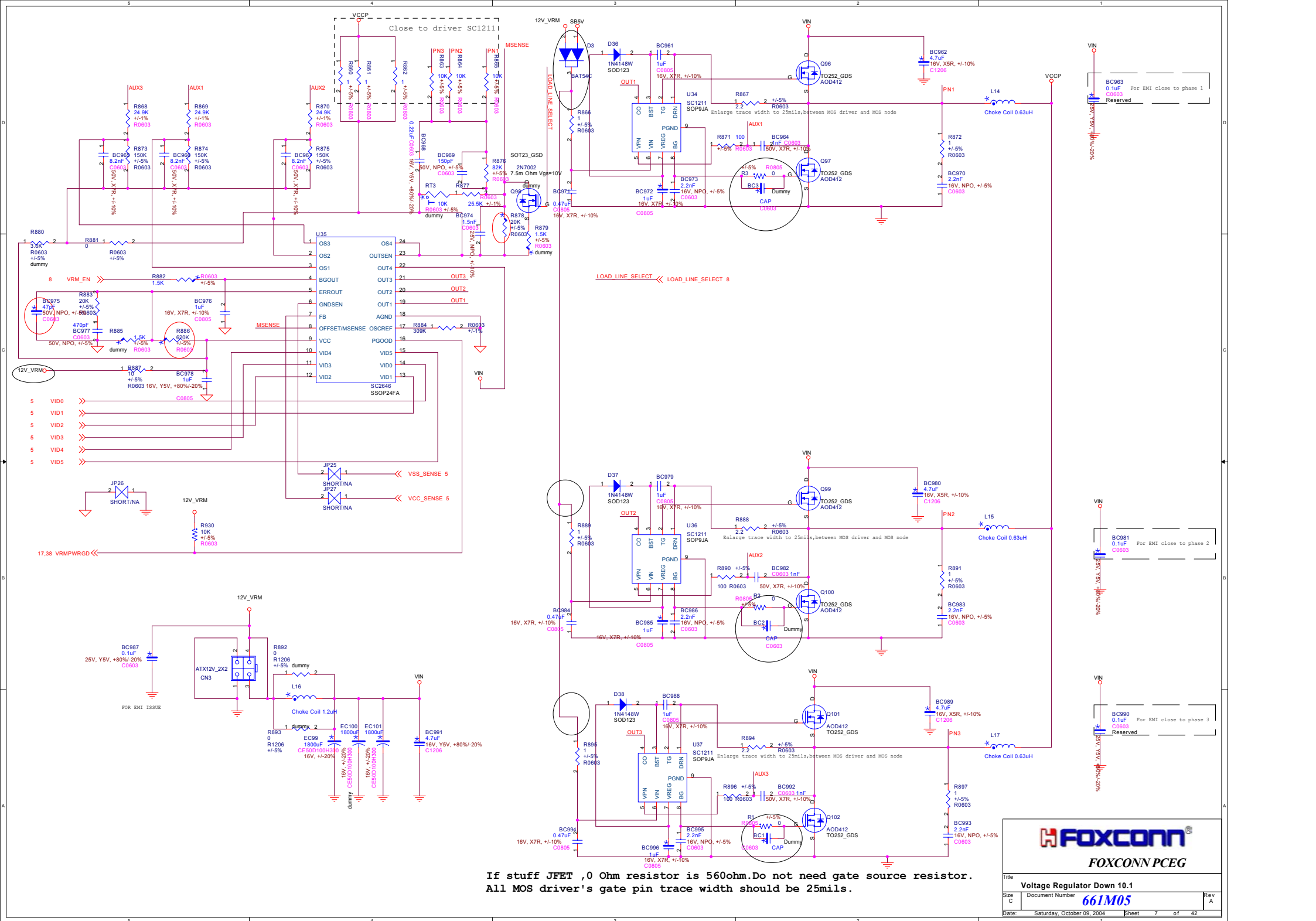


Intel Pull High RES 49.9ohm.



1. Cap. should be within 600 mils of the VCCA and VSSA pins
2. VCCA route should be parallel and next to VSSA route
3. Min. 12 mils trace from the filter to the processor pins
4. The inductors should be close to the cap.

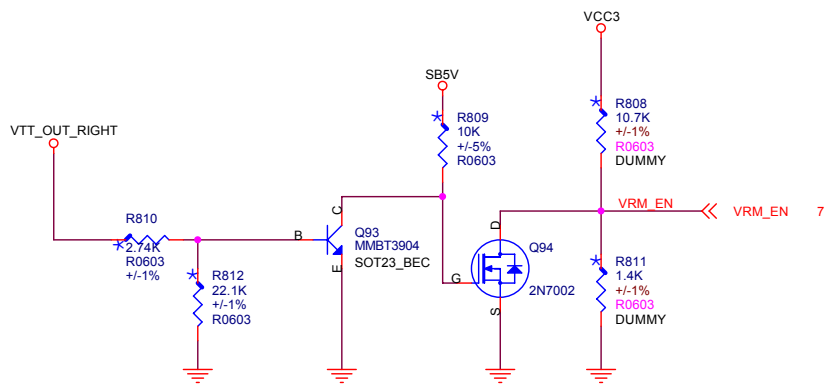
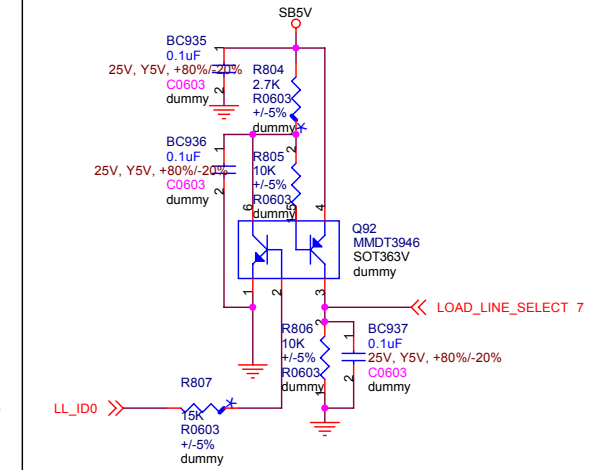
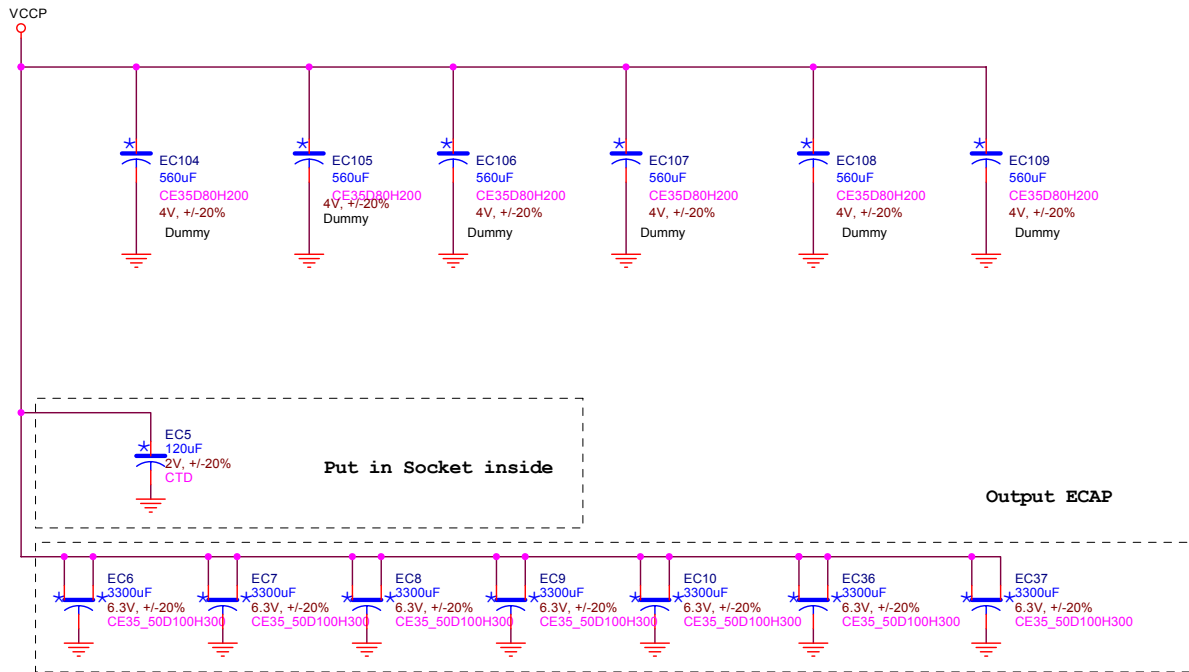




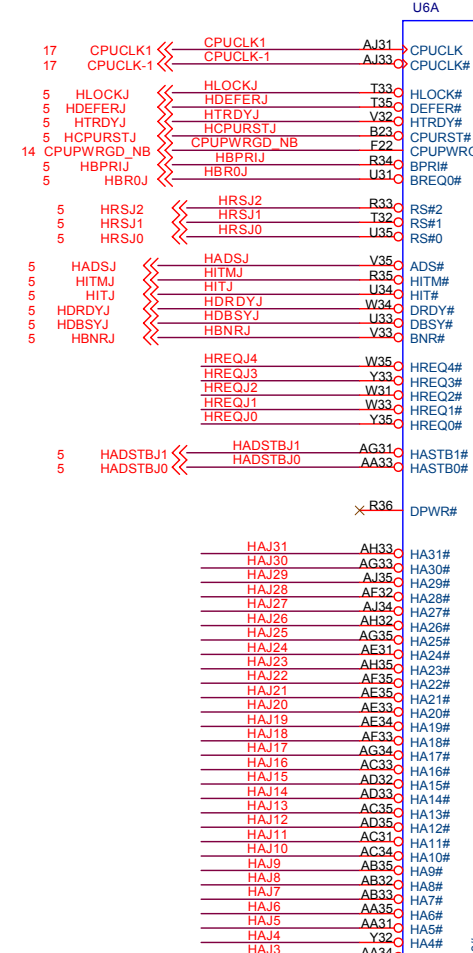
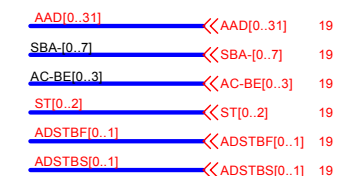
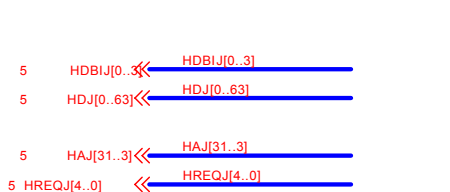
If stuff JFET ,0 Ohm resistor is 560ohm.Do not need gate source resistor.
 All MOS driver's gate pin trace width should be 25mils.

FOXCONN
 FOXCONN PCEG

Title: Voltage Regulator Down 10.1
 Size C Document Number: 661M05 Rev A
 Date: Saturday, October 09, 2004 Sheet 7 of 42



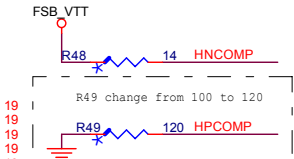
For delay VRD_EN that after VTT_PWRGD is OK.



661FX-1

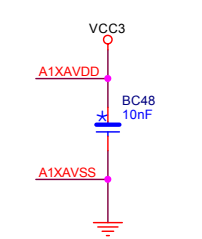
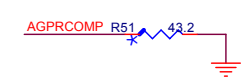
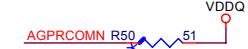
HOST

AGP

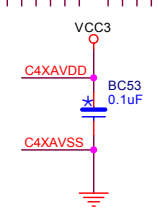
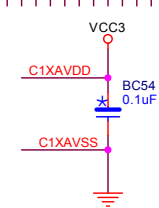
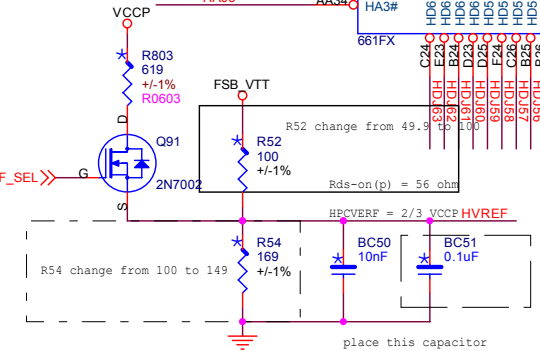


	R46	R48
648	20 1%	110 1%
648FX	14 1%	100 1%
661FX	14 1%	100 1%

AGP3.0 = 50 ohm



BC48, BC49 Change to 0.1uF?



under 661 solder side

FOXCONN TECHNOLOGY COPR.

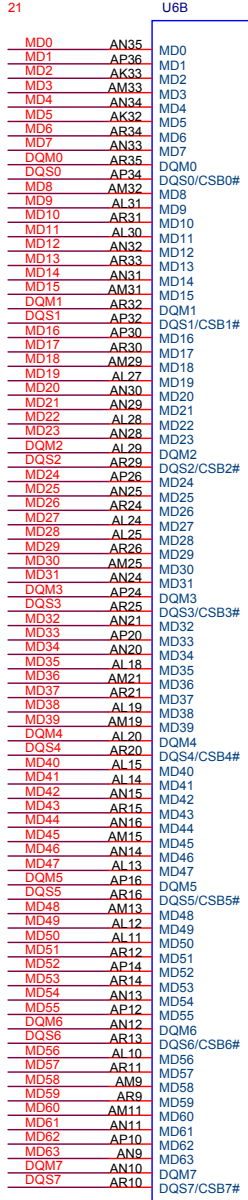
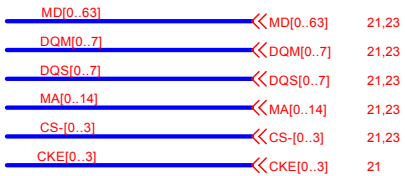
Title: 661FX-1 HOST & AGP

Document Number: 661M05

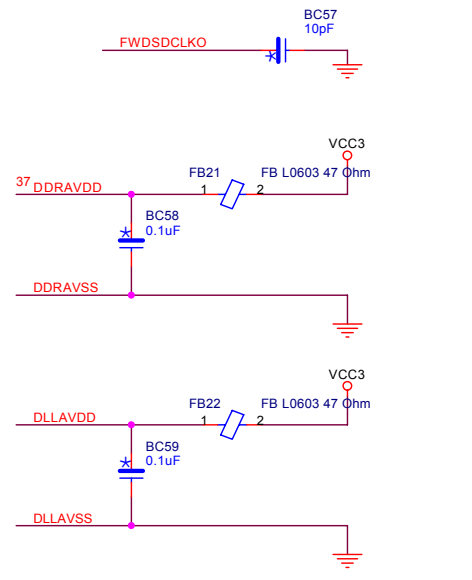
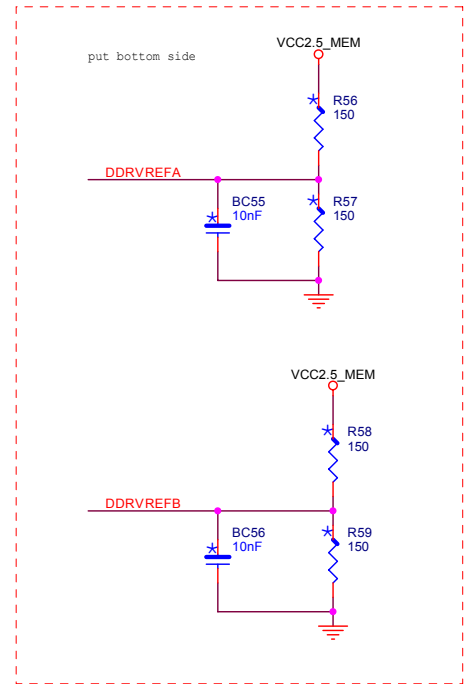
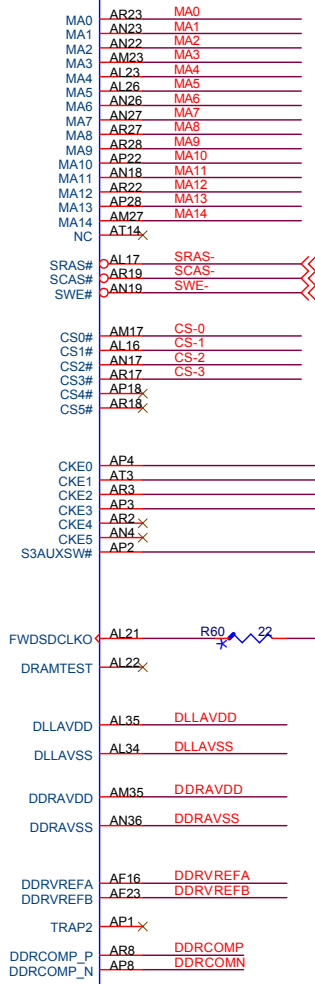
Date: Saturday, October 09, 2004

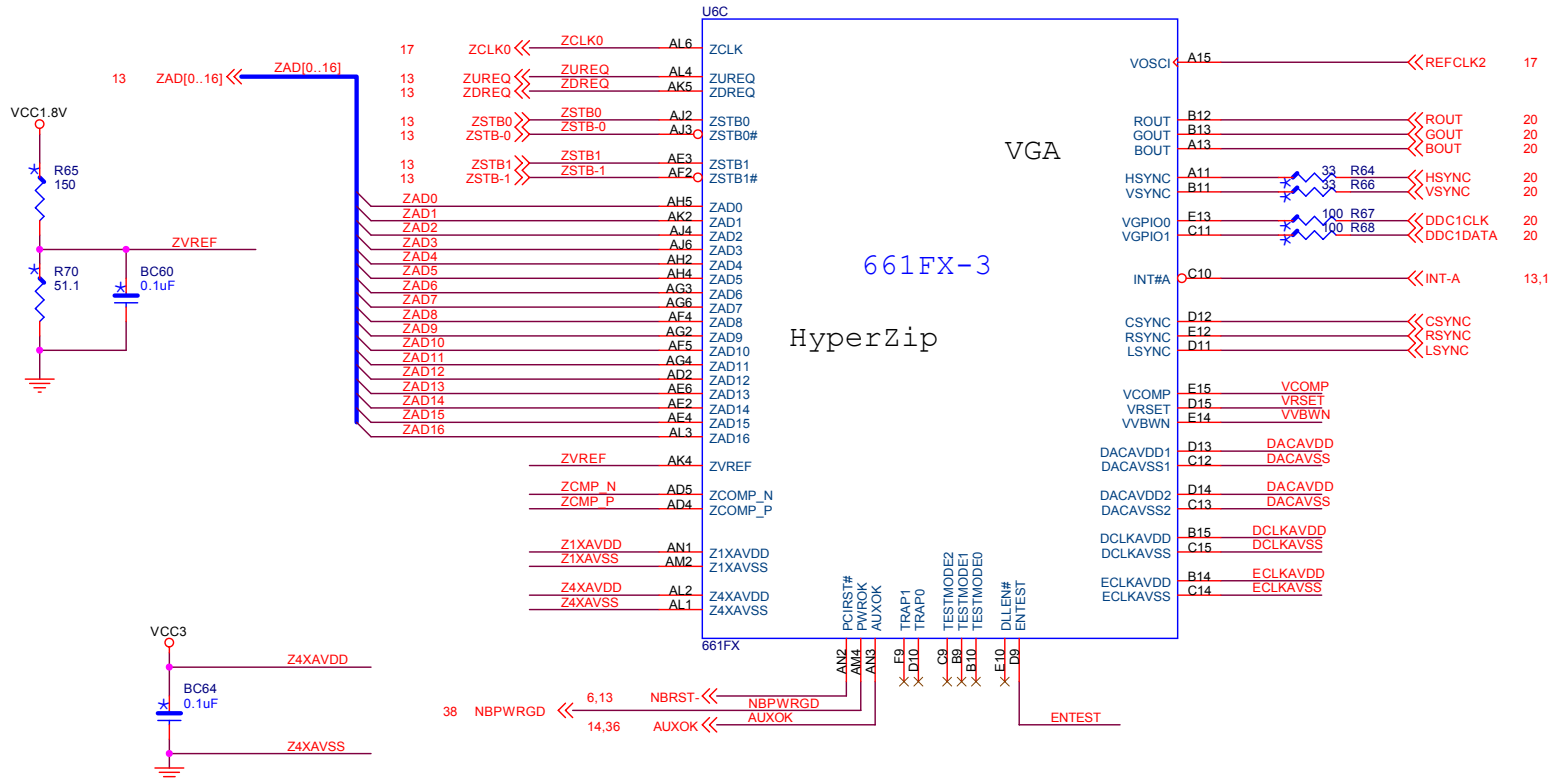
Sheet 9 of 42

Rev A

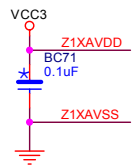
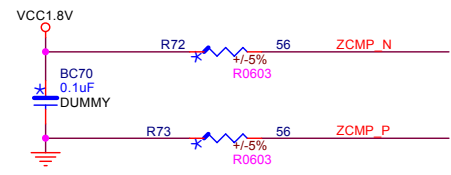
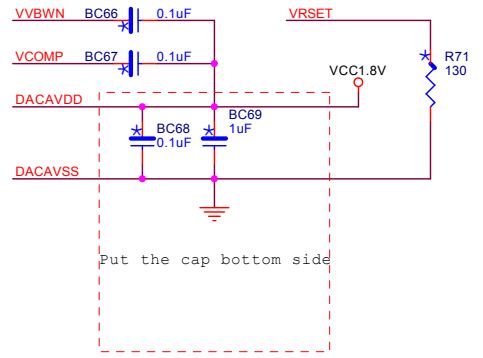
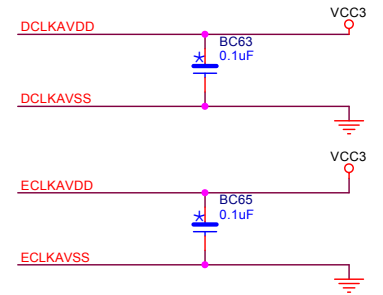
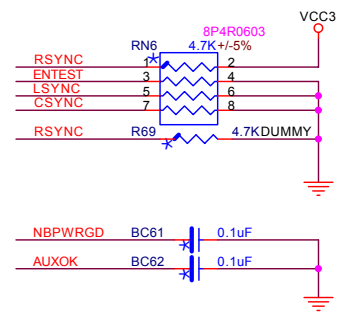


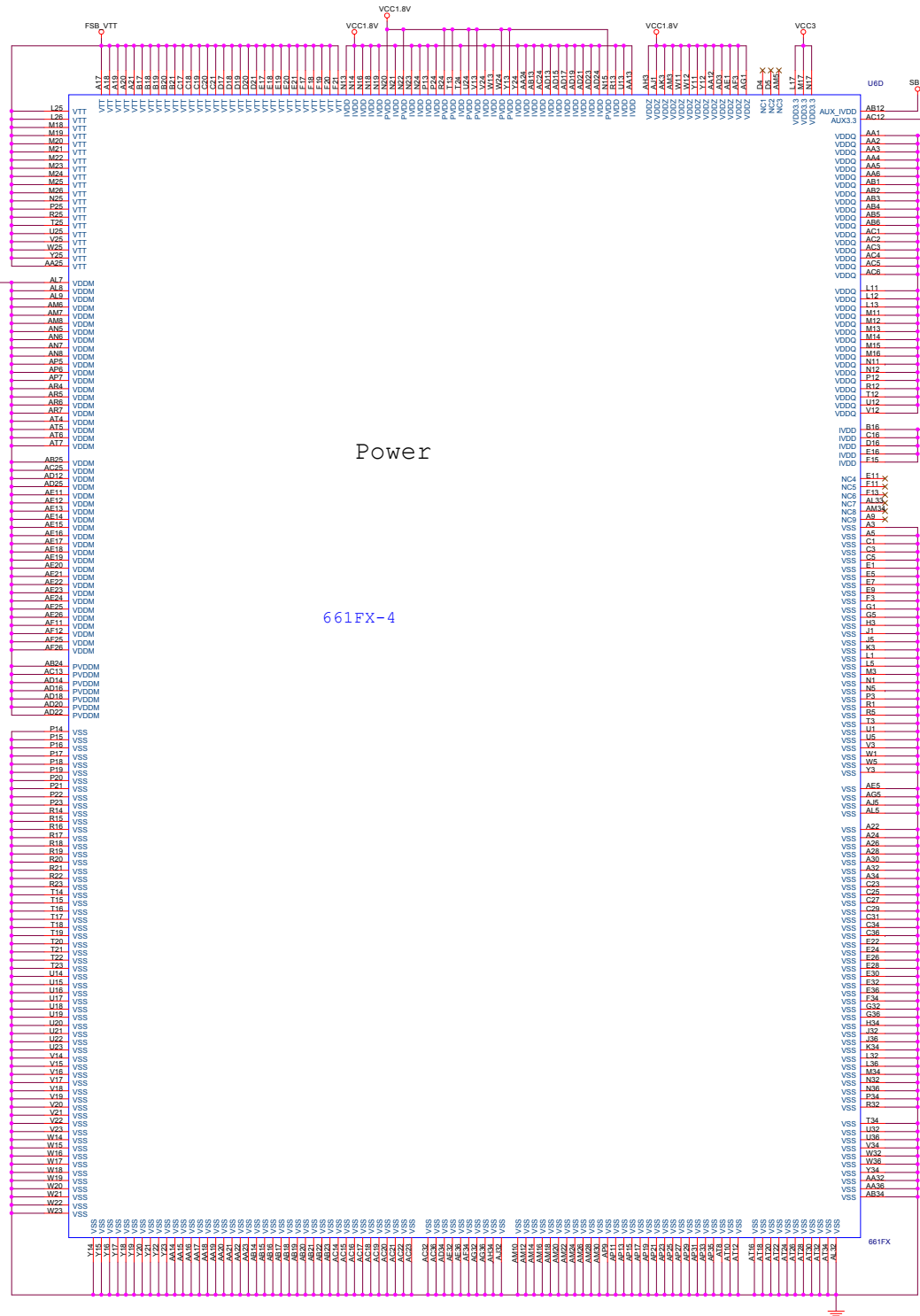
661FX-2





		Enable	Disable
RSYNC	VGA	1	0
LSYNC	panel link	1	0
CSYNC	VB	1	0

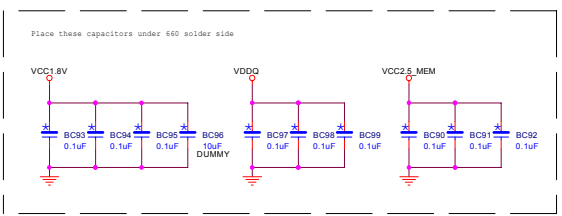
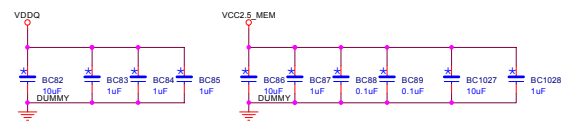
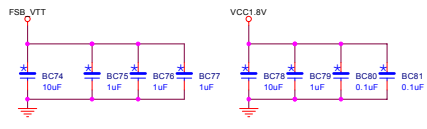
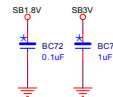


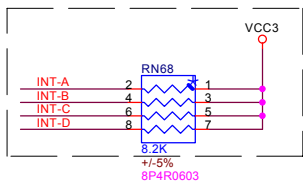


Power

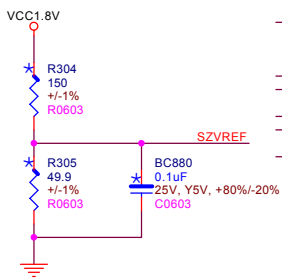
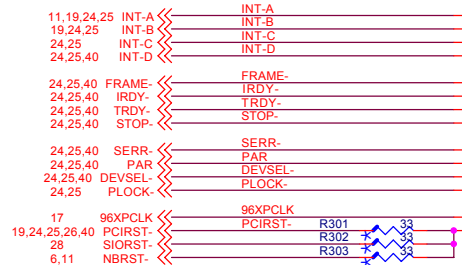
661FX-4

IVDD, AUX_IVDD 1.8V

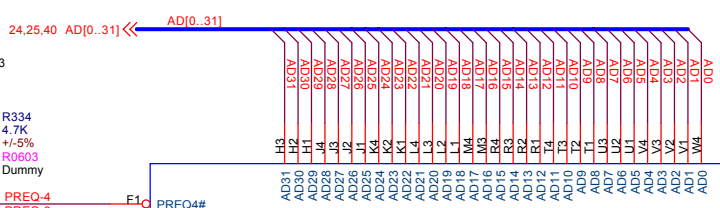




24,25,40 C/BE[0..3]



11 ZAD[0..16]

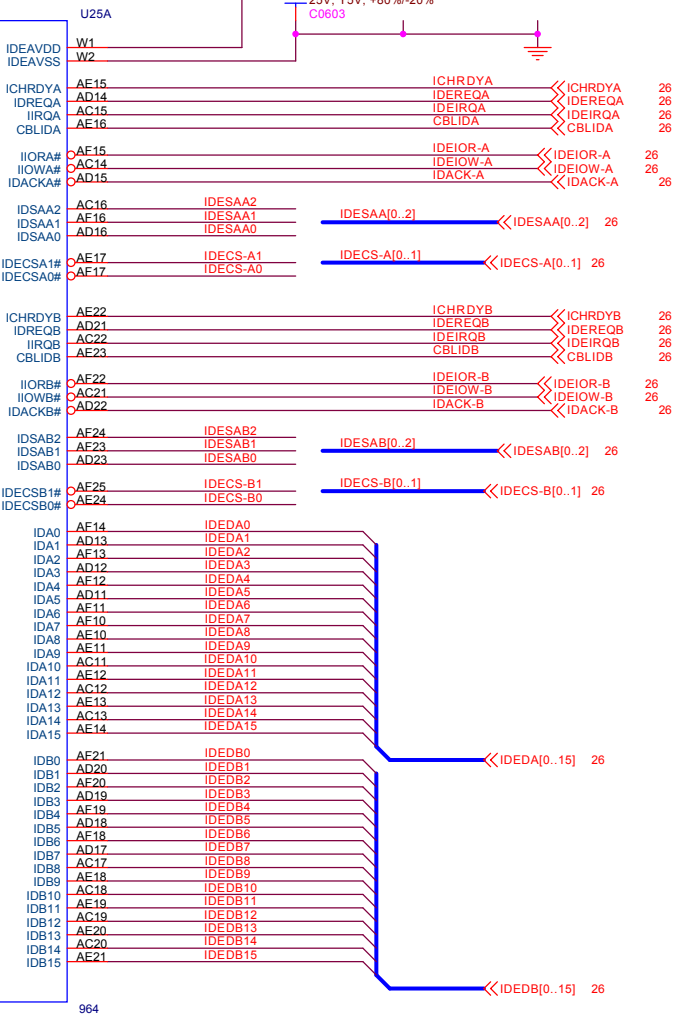
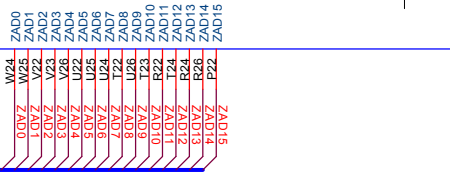


PCI

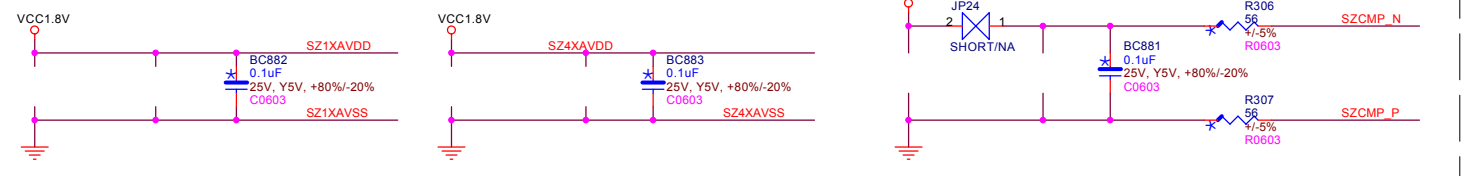
IDE

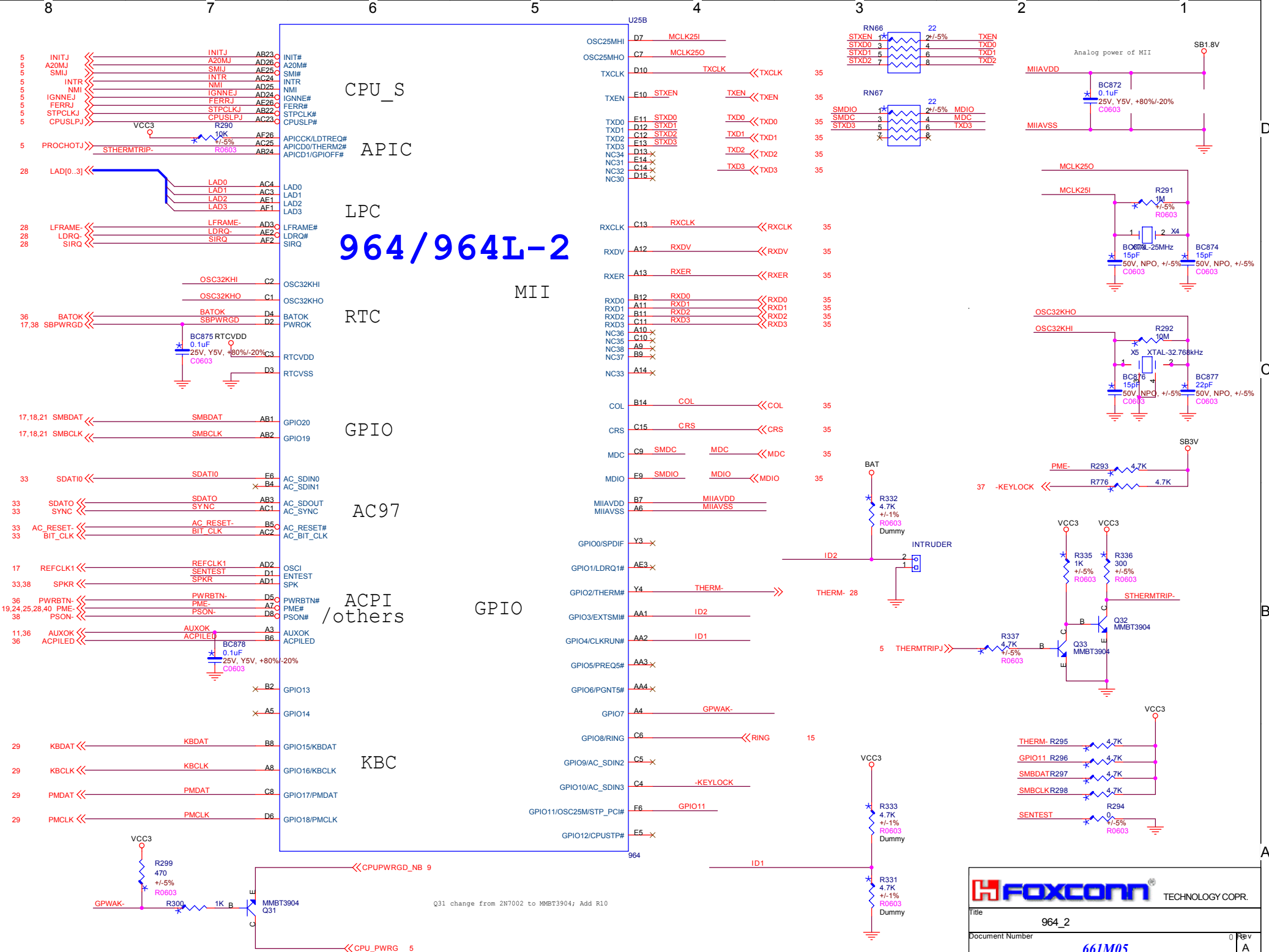
964/964L -1

HyperZip



Analog Power supplies of Transzip function for 96X Chip.





CPU_S 964/964L-2

MII

RTC

GPIO

AC97

ACPI / others

KBC

Q31 change from 2N7002 to MMBT3904; Add R10

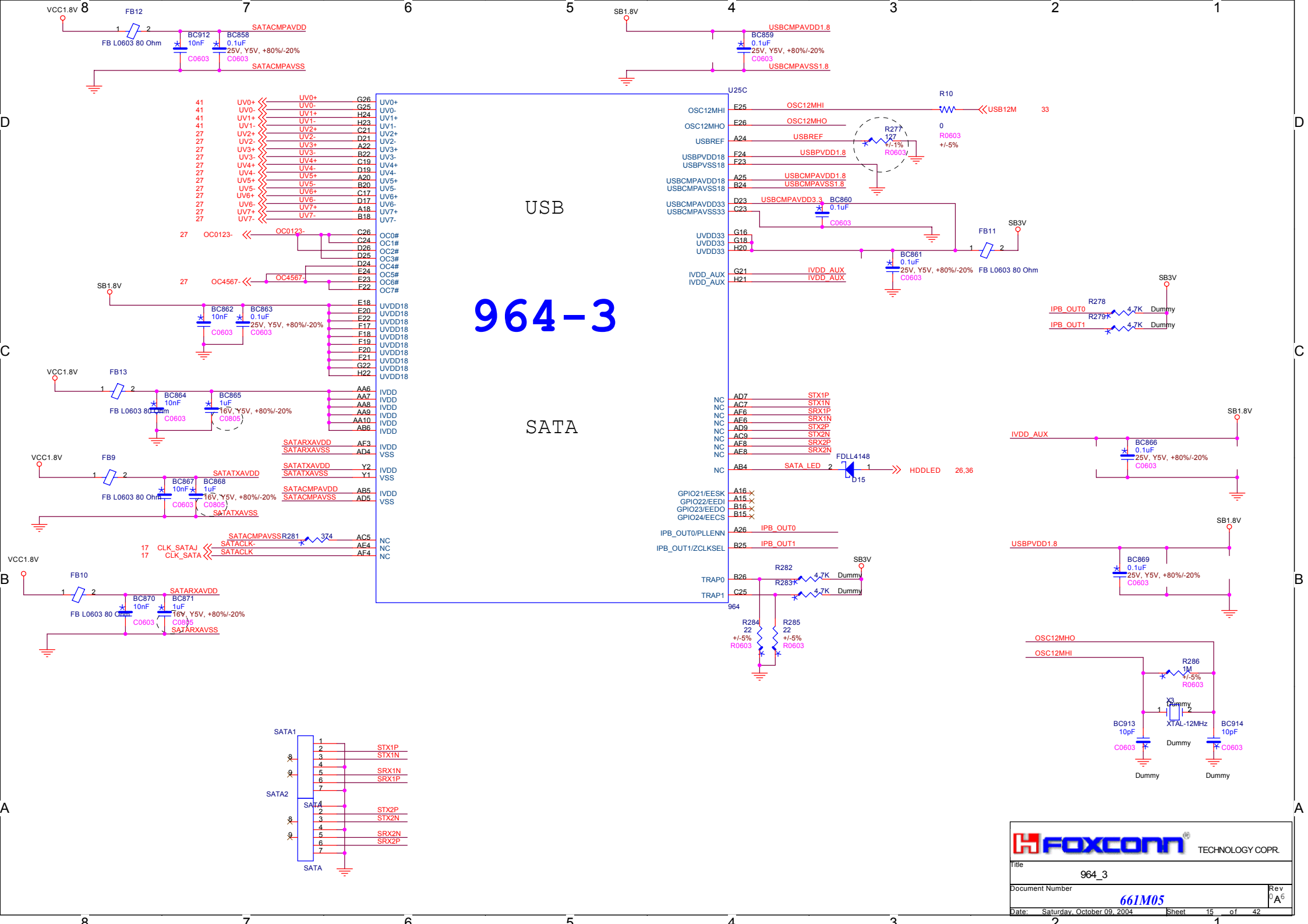
FOXCONN TECHNOLOGY COPR.

Title: 964_2

Document Number: 661M05

Date: Saturday, October 09, 2004 Sheet 14 of 42

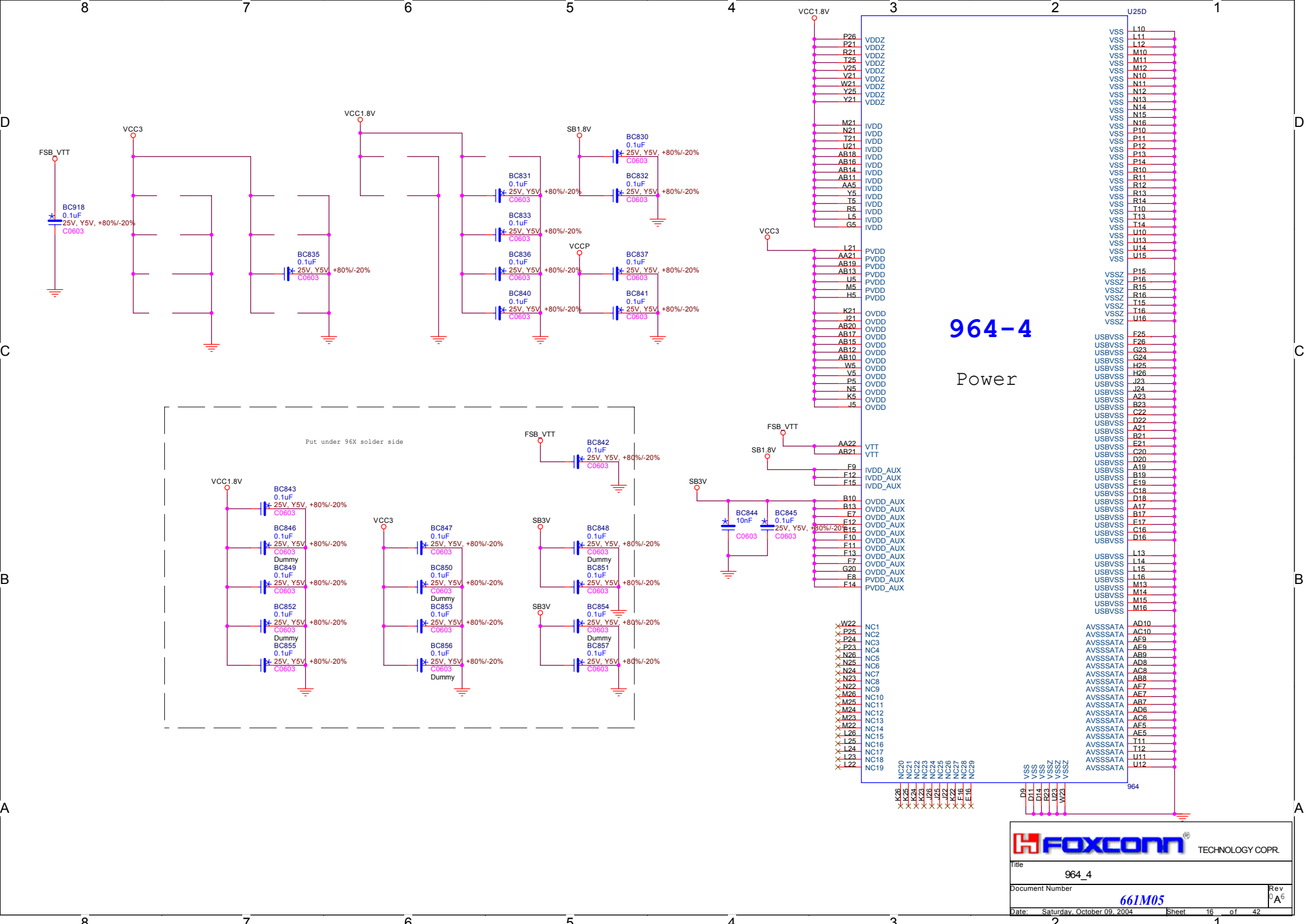
Rev: A



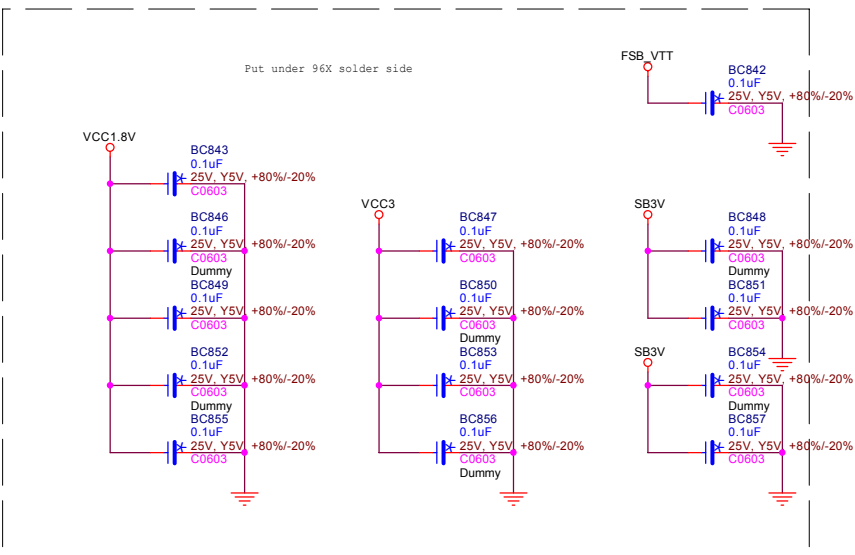
964-3

USB

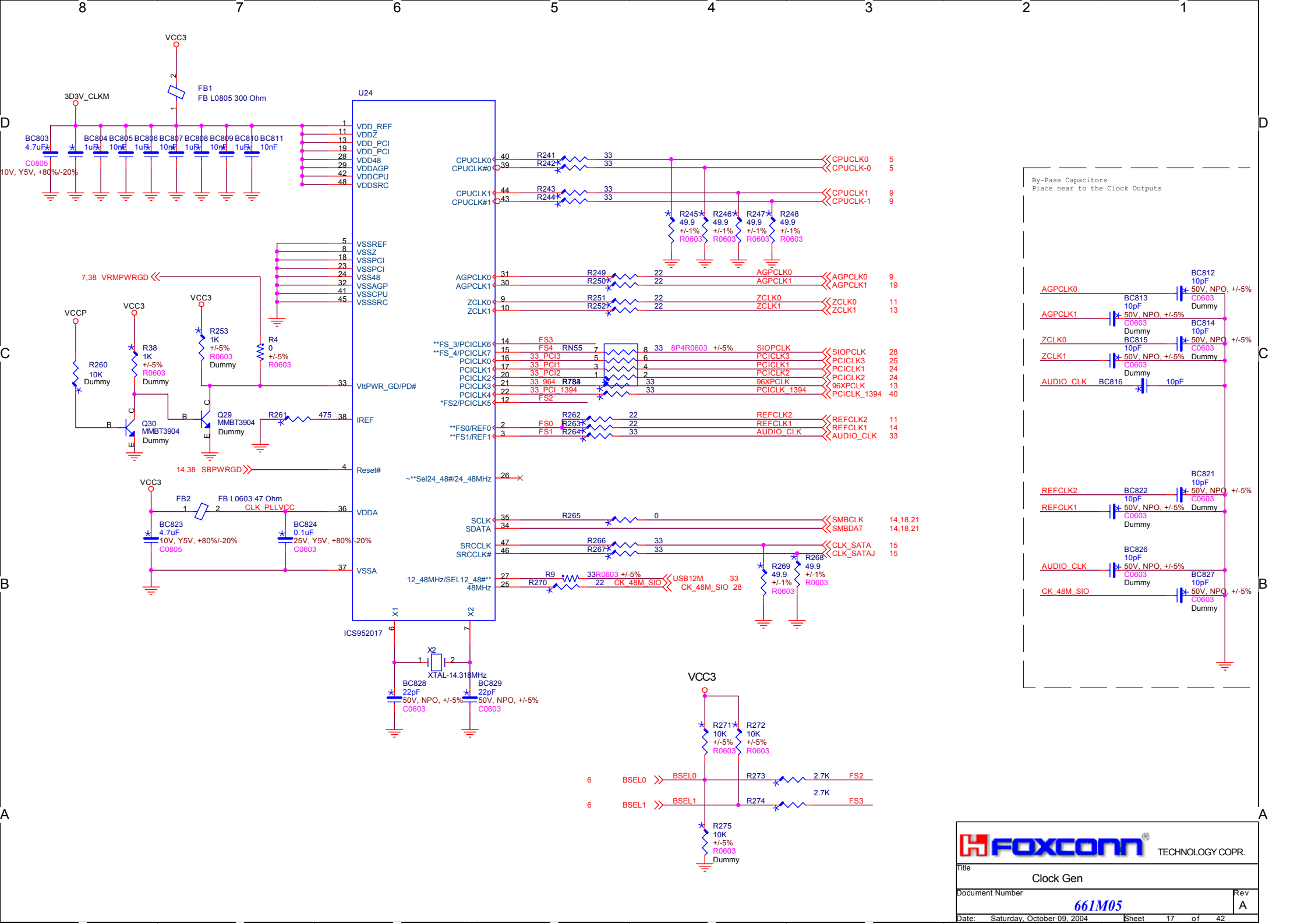
SATA

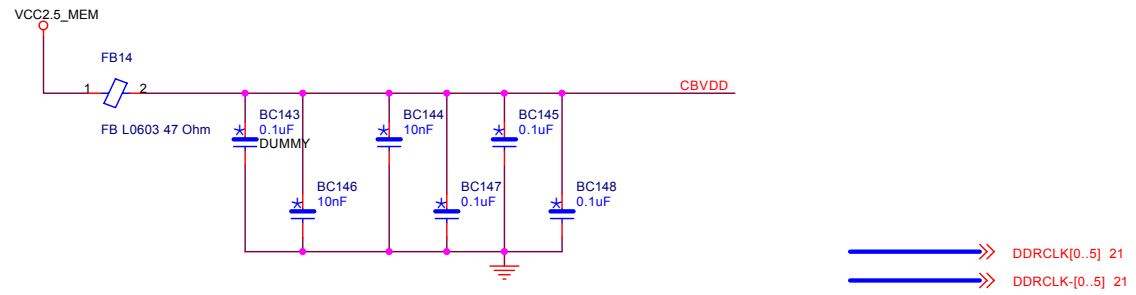


964-4
Power



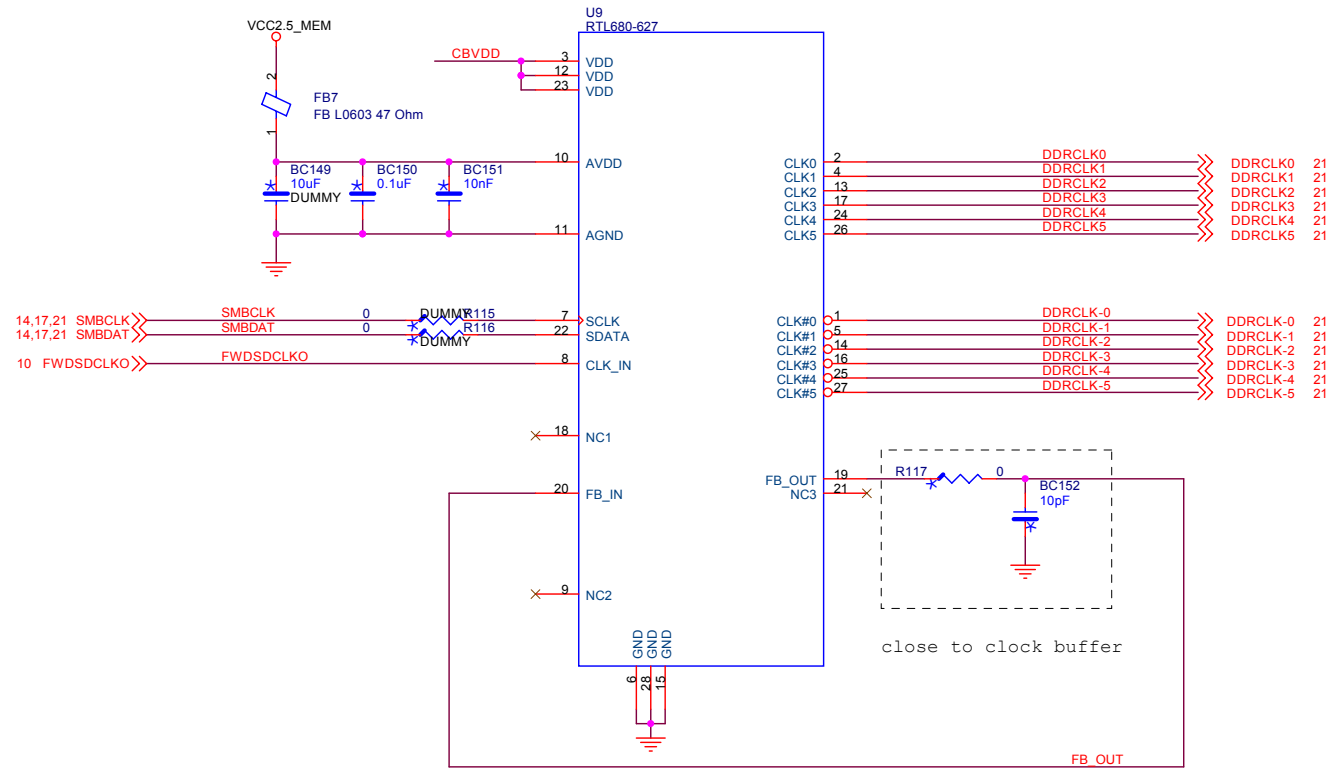
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	P21	VSS	L11
	R21	VSS	L12
	T25	VSS	M10
	V25	VSS	M11
	V21	VSS	M12
	W21	VSS	N10
	Y25	VSS	N11
	Y21	VSS	N12
	Y21	VSS	N13
		VSS	N14
		VSS	N15
		VSS	N16
		VSS	P10
		VSS	P11
		VSS	P12
		VSS	P13
		VSS	P14
		VSS	R10
		VSS	R12
		VSS	R13
		VSS	R14
		VSS	T10
		VSS	T13
		VSS	T14
		VSS	U10
		VSS	U11
		VSS	U14
		VSS	U15
		VSS	VSS
		VSSZ	P15
		VSSZ	P16
		VSSZ	R15
		VSSZ	R16
		VSSZ	T15
		VSSZ	T16
		VSSZ	U16
		VSSZ	VSSZ
		USBVSS	F25
		USBVSS	F26
		USBVSS	G23
		USBVSS	G24
		USBVSS	H25
		USBVSS	H26
		USBVSS	J23
		USBVSS	J24
		USBVSS	A23
		USBVSS	B23
		USBVSS	C22
		USBVSS	D22
		USBVSS	A21
		USBVSS	B21
		USBVSS	E21
		USBVSS	C20
		USBVSS	D20
		USBVSS	A19
		USBVSS	B19
		USBVSS	E19
		USBVSS	C18
		USBVSS	D18
		USBVSS	A17
		USBVSS	B17
		USBVSS	E17
		USBVSS	C16
		USBVSS	D16
		USBVSS	L13
		USBVSS	L14
		USBVSS	L15
		USBVSS	L16
		USBVSS	M13
		USBVSS	M14
		USBVSS	M15
		USBVSS	M16
		AVSSSATA	AD10
		AVSSSATA	AC10
		AVSSSATA	AF9
		AVSSSATA	AE9
		AVSSSATA	AB9
		AVSSSATA	AD8
		AVSSSATA	AC8
		AVSSSATA	AB8
		AVSSSATA	AE7
		AVSSSATA	AD7
		AVSSSATA	AD6
		AVSSSATA	AC6
		AVSSSATA	AE5
		AVSSSATA	AD5
		AVSSSATA	T11
		AVSSSATA	T12
		AVSSSATA	U11
		AVSSSATA	U12
		AVSSSATA	AVSSSATA
K26	NC20	D8	VSS
K25	NC21	D11	VSS
K24	NC22	D14	VSS
J26	NC23	L23	VSSZ
J25	NC24	J26	VSSZ
K26	NC25	L23	VSSZ
K25	NC26	J25	VSSZ
J26	NC27	K26	VSSZ
J25	NC28	E16	VSSZ
E16	NC29	E16	VSSZ
E16	NC29	E16	VSSZ
L22	NC19	L22	VSSZ
	NC1	W22	NC1
	NC2	P25	NC2
	NC3	P24	NC3
	NC4	P23	NC4
	NC5	N26	NC5
	NC6	N25	NC6
	NC7	N24	NC7
	NC8	N23	NC8
	NC9	N22	NC9
	NC10	M26	NC10
	NC11	M25	NC11
	NC12	M24	NC12
	NC13	M23	NC13
	NC14	M22	NC14
	NC15	L26	NC15
	NC16	L25	NC16
	NC17	L24	NC17
	NC18	L23	NC18
	NC19	L22	NC19





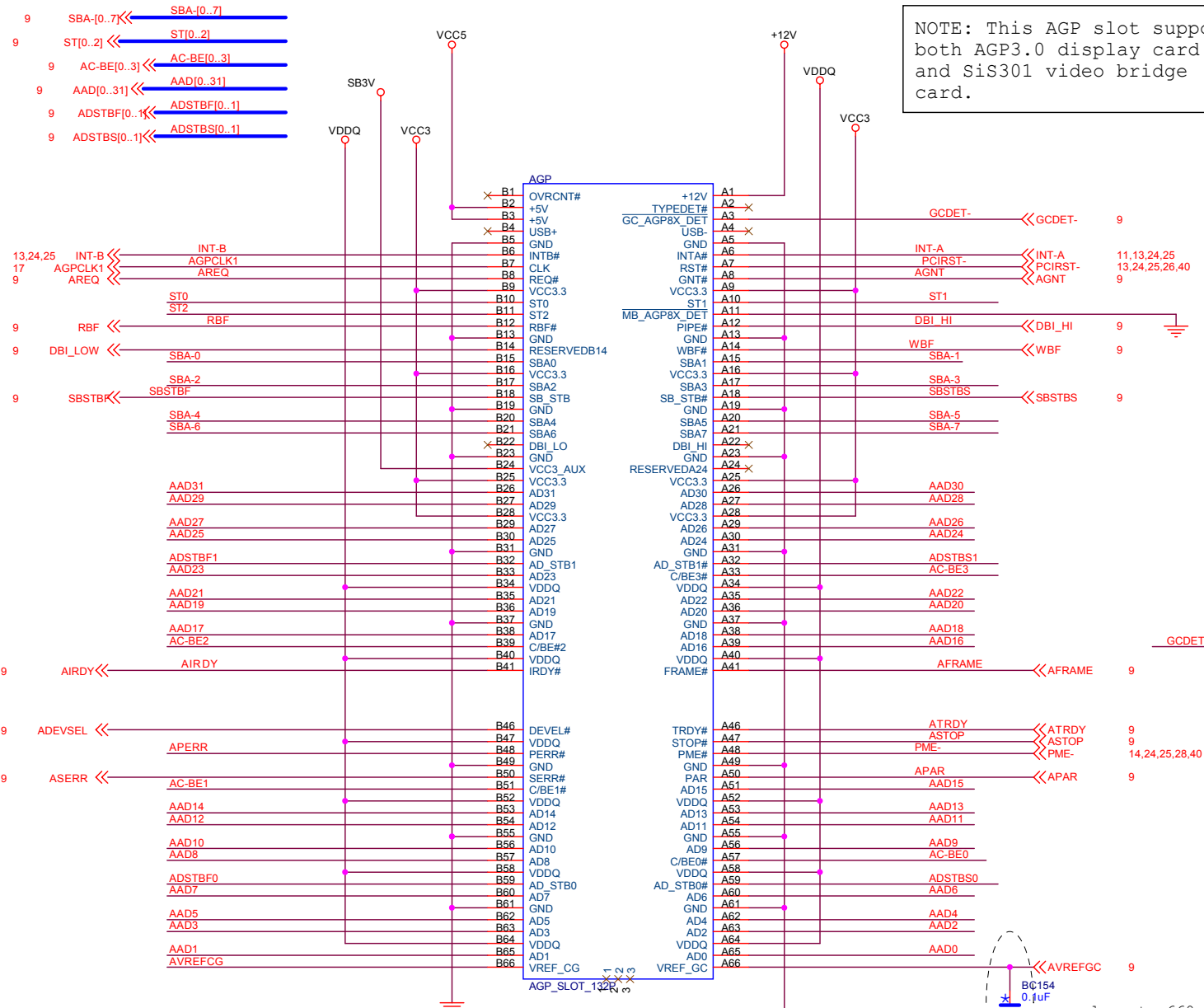
试用奥斯特的47uΩ电阻

Clock Buffer (DDR)

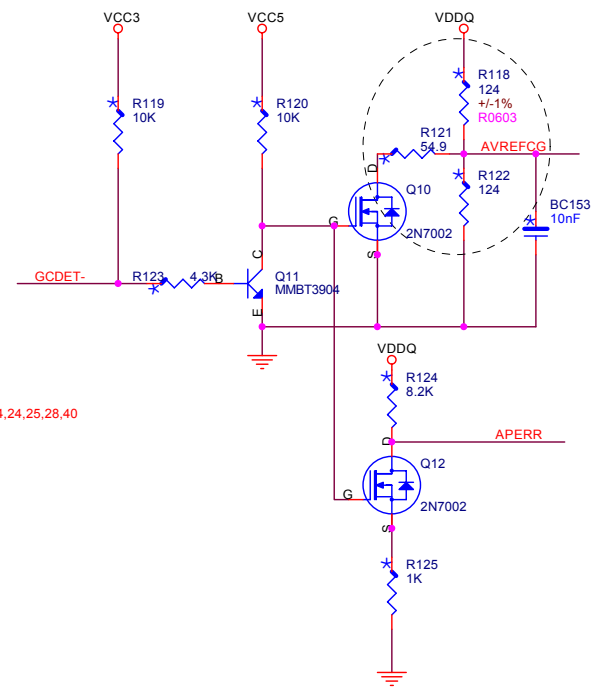


NOTE: This AGP slot support both AGP3.0 display card and SiS301 video bridge card.

GCDET- on card	GCDET-	AVREFCG	APERR
GND	0V	0.35V	0V
OPEN	1.47V	0.75V	1.5V



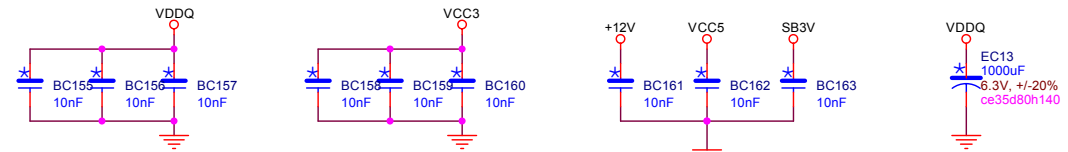
close to AGP SLOT



close to 660

AGP CONNECTOR DECOUPLING

put CAP close to AGP slot each POWER PIN



FOXCONN TECHNOLOGY COPR.

AGP

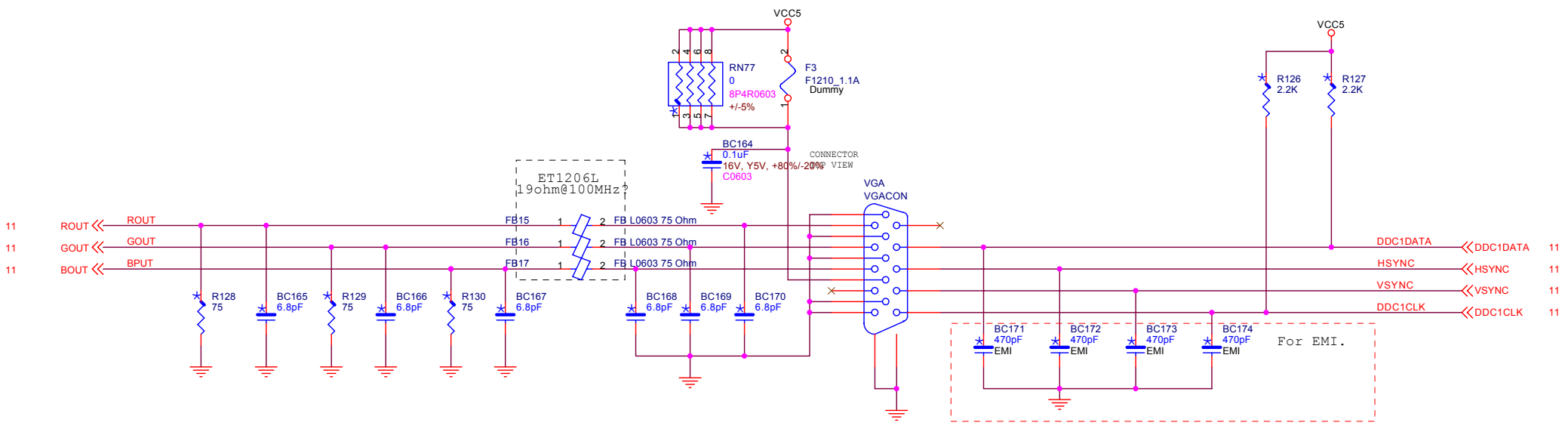
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VGA CONNECTOR



close to GND gap

10.23 MD[0..63] << MD[0..63]
 10.23 MA[0..14] << MA[0..14]
 10.23 DQM[0..7] << DQM[0..7]
 10.23 DQS[0..7] << DQS[0..7]

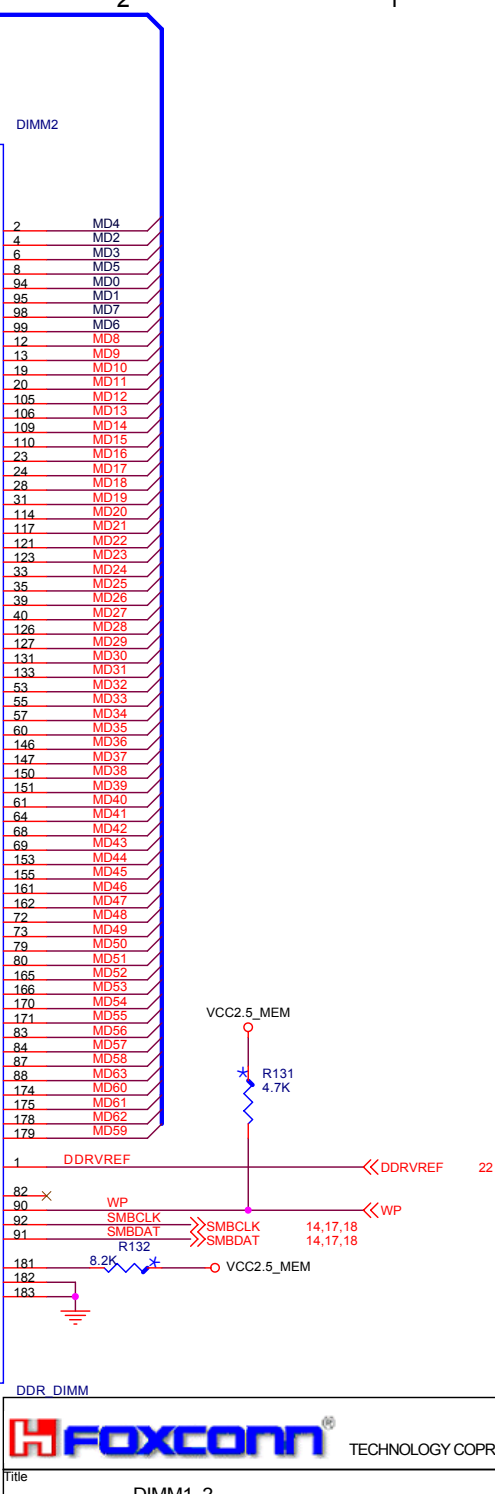
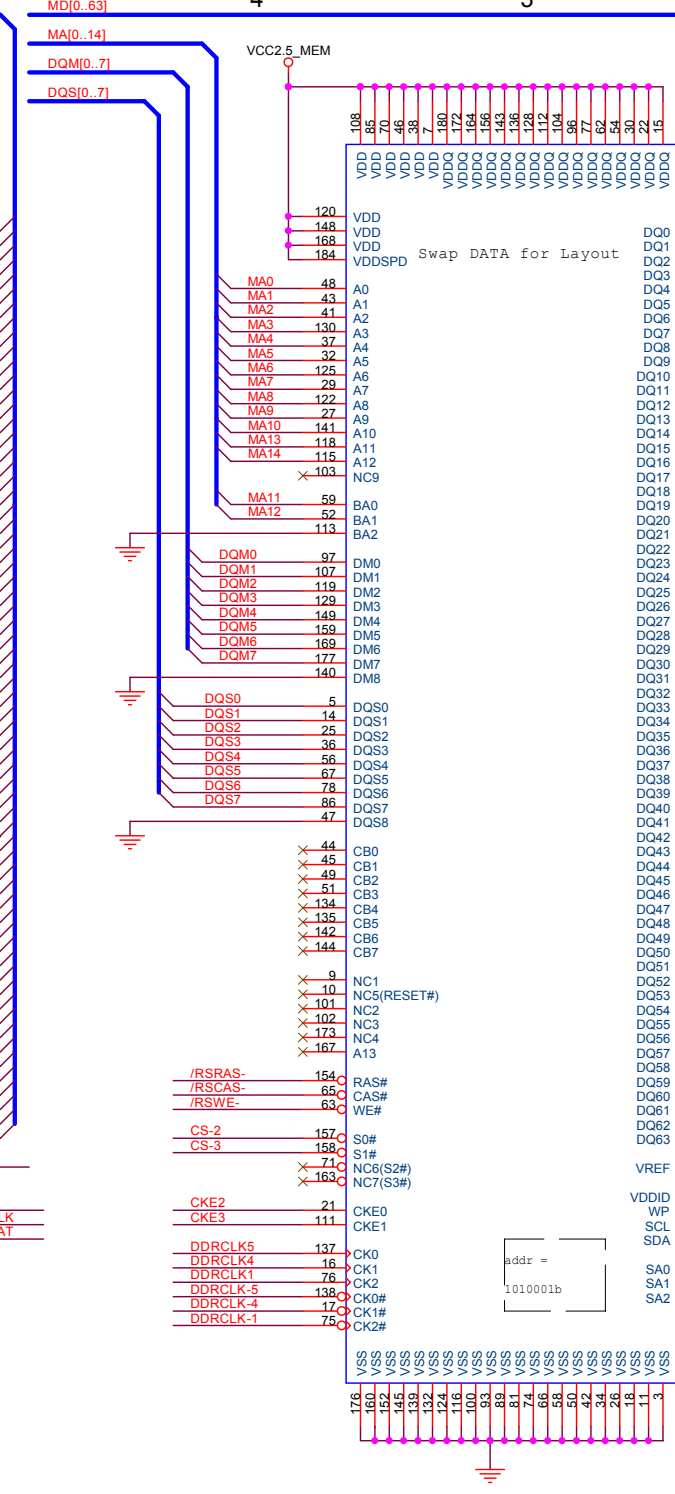
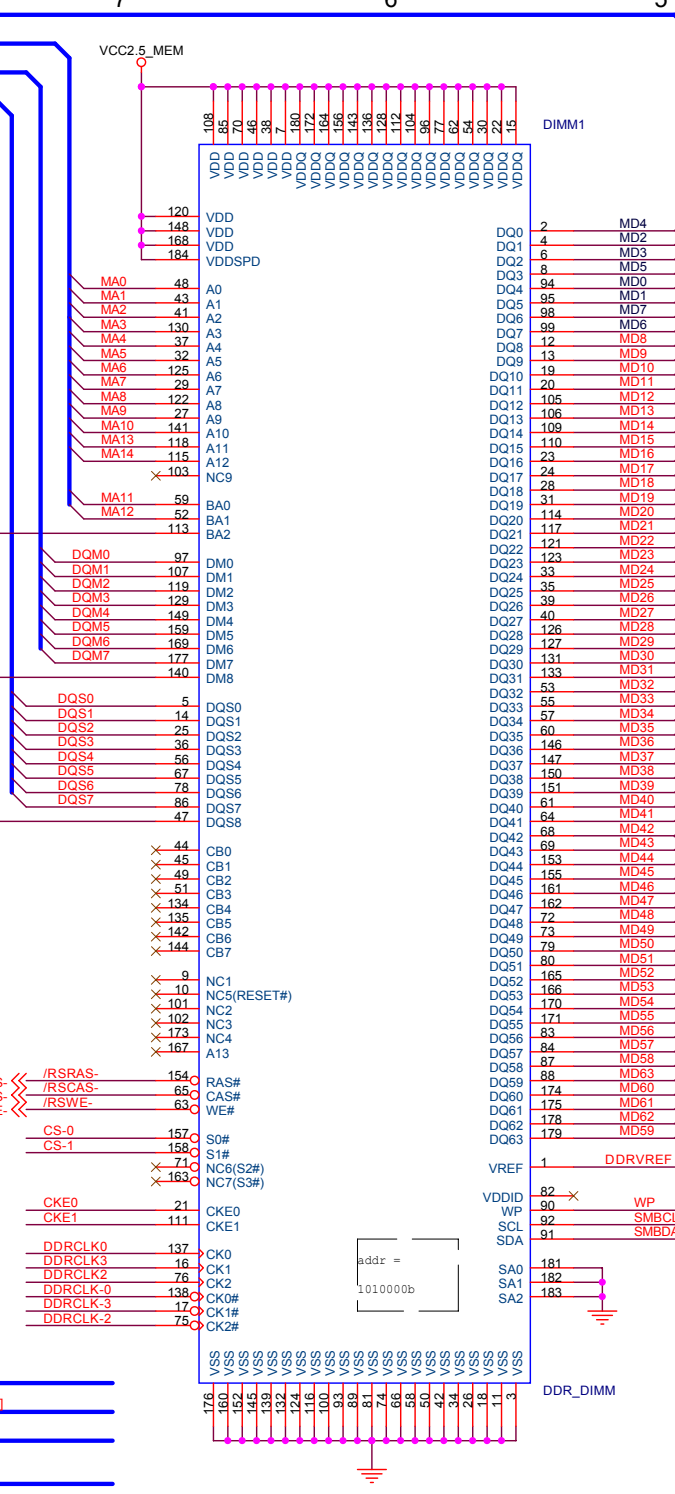
NOTE:
 VDDID IS A TRAP ON THE DIMM
 MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

10.23 CS-[0..3] << CS-[0..3]
 10 CKE[0..3] << CKE[0..3]
 18 DDRCLK[0..5] << DDRCLK[0..5]
 18 DDRCLK-[0..5] << DDRCLK-[0..5]

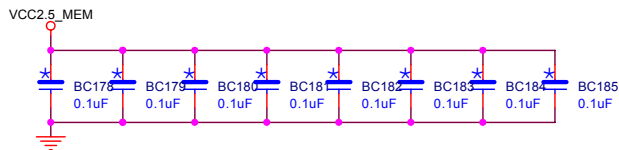
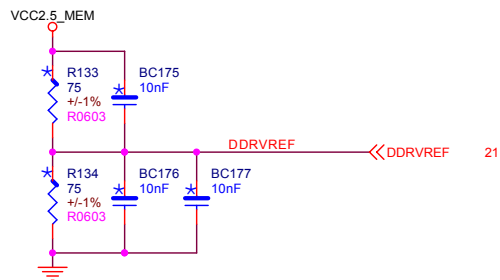


Title DIMM1, 2

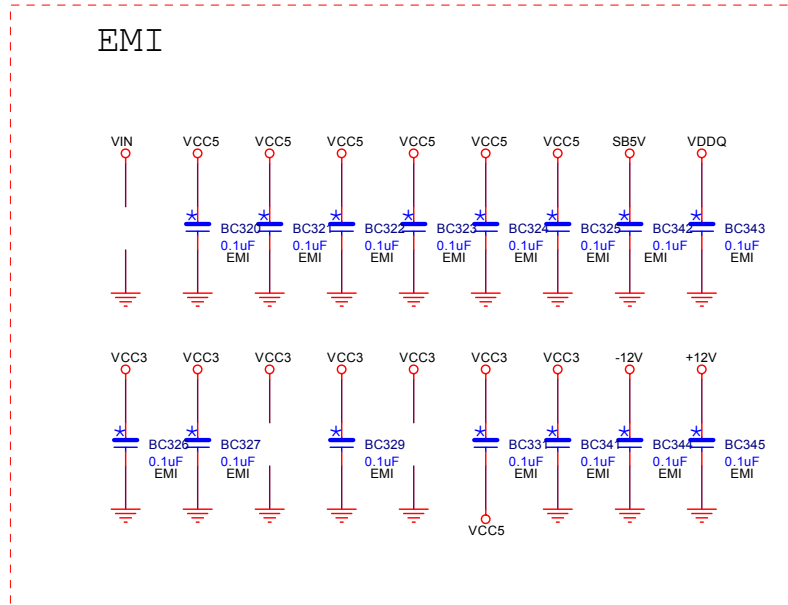
Document Number 661M05

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DDRVREF GEN. & DECOUPLING



EMI

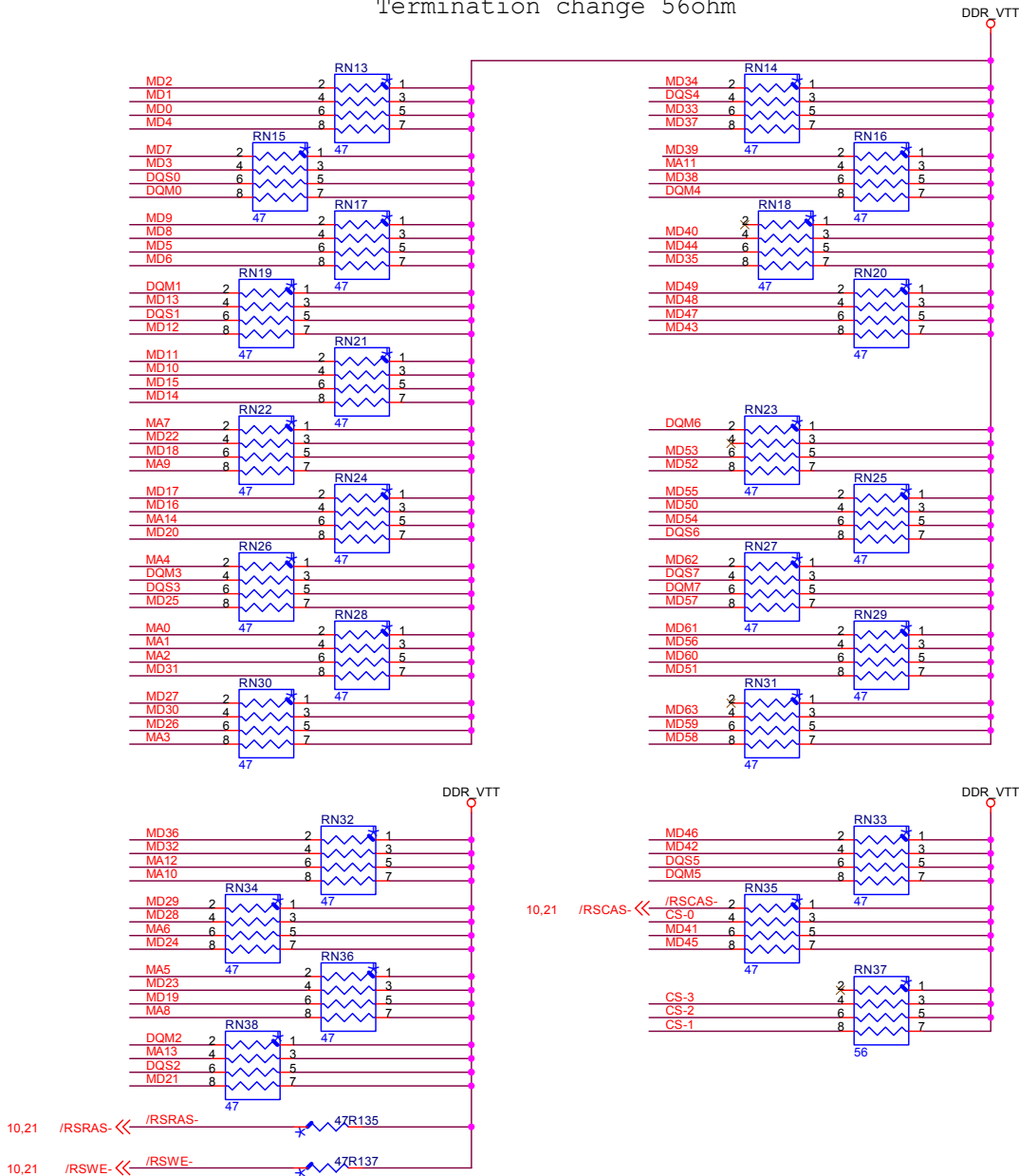


SSTL-2 Termination Resistors

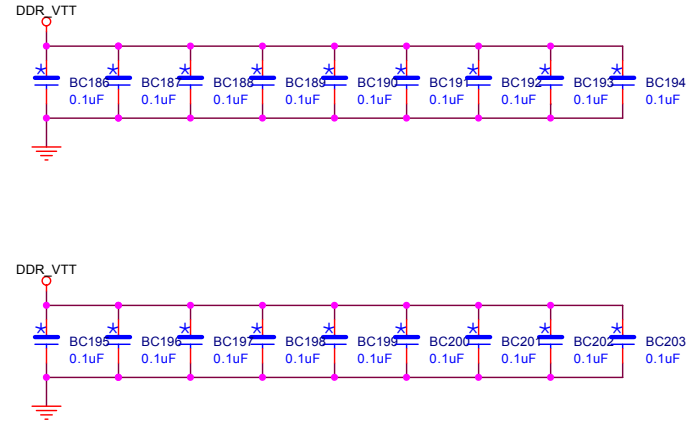
MD[0..63]	← MD[0..63]	10,21
DQM[0..7]	← DQM[0..7]	10,21
DQS[0..7]	← DQS[0..7]	10,21
MA[0..14]	← MA[0..14]	10,21
CS-[0..3]	← CS-[0..3]	10,21

	SDR		DDR		Rtt
MD/DQM (/DQS)	LV-CMOS	Rs	SSTL-2	10	33
MA/Control	LV-CMOS	0/10/-	SSTL-2	0	33
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V		DD 2.5V		

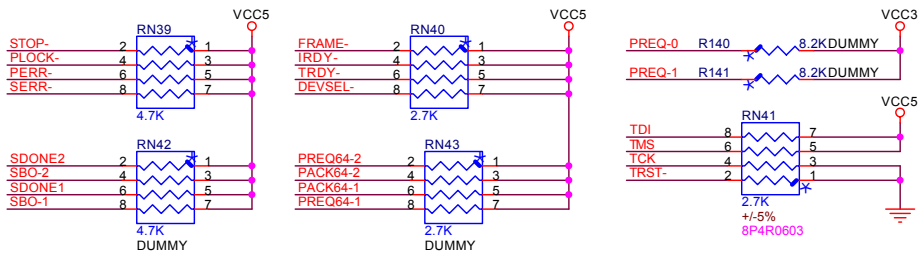
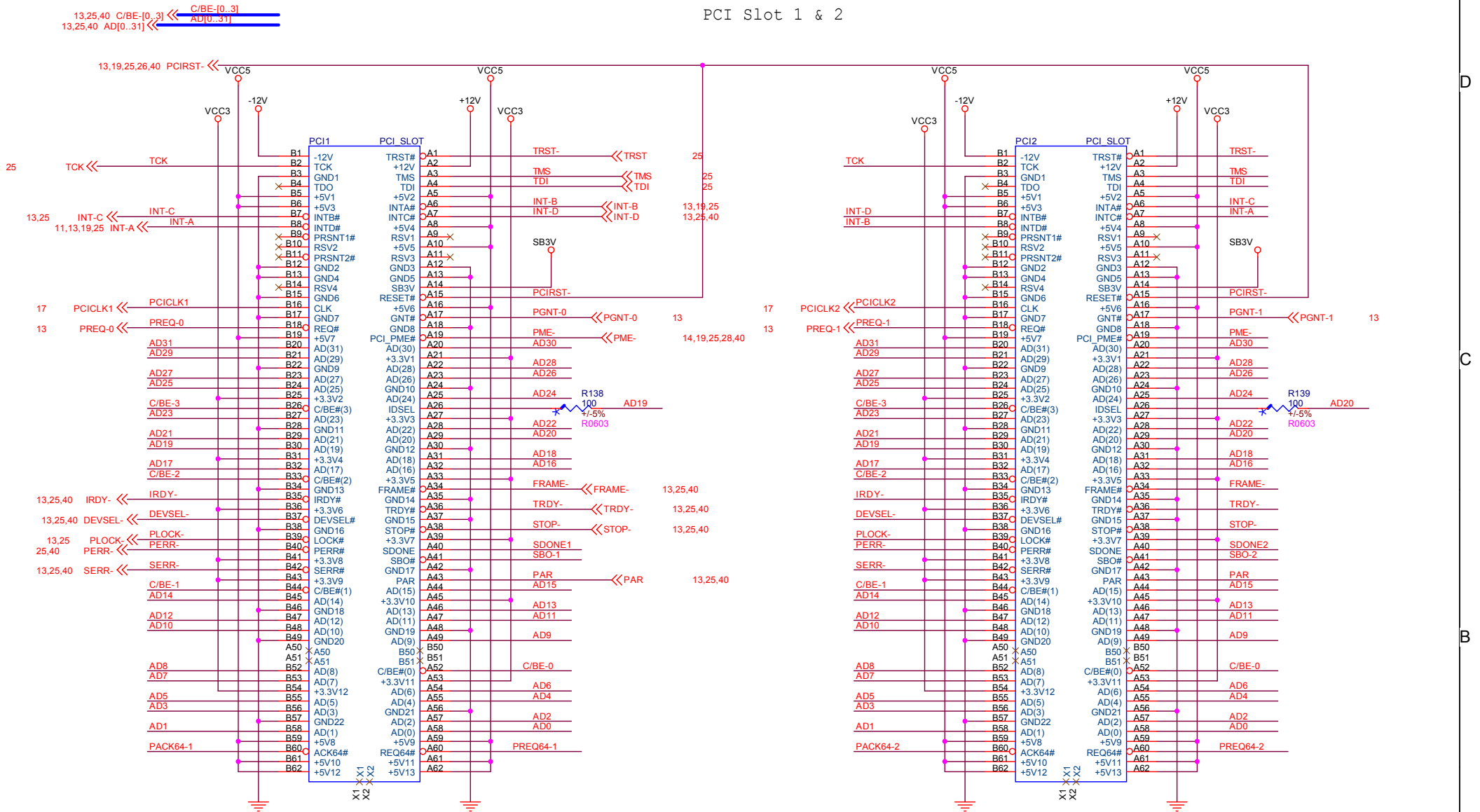
Termination change 56ohm



DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs



PCI Slot 1 & 2



FOXCONN TECHNOLOGY COPR.

Title: PCI 1, 2

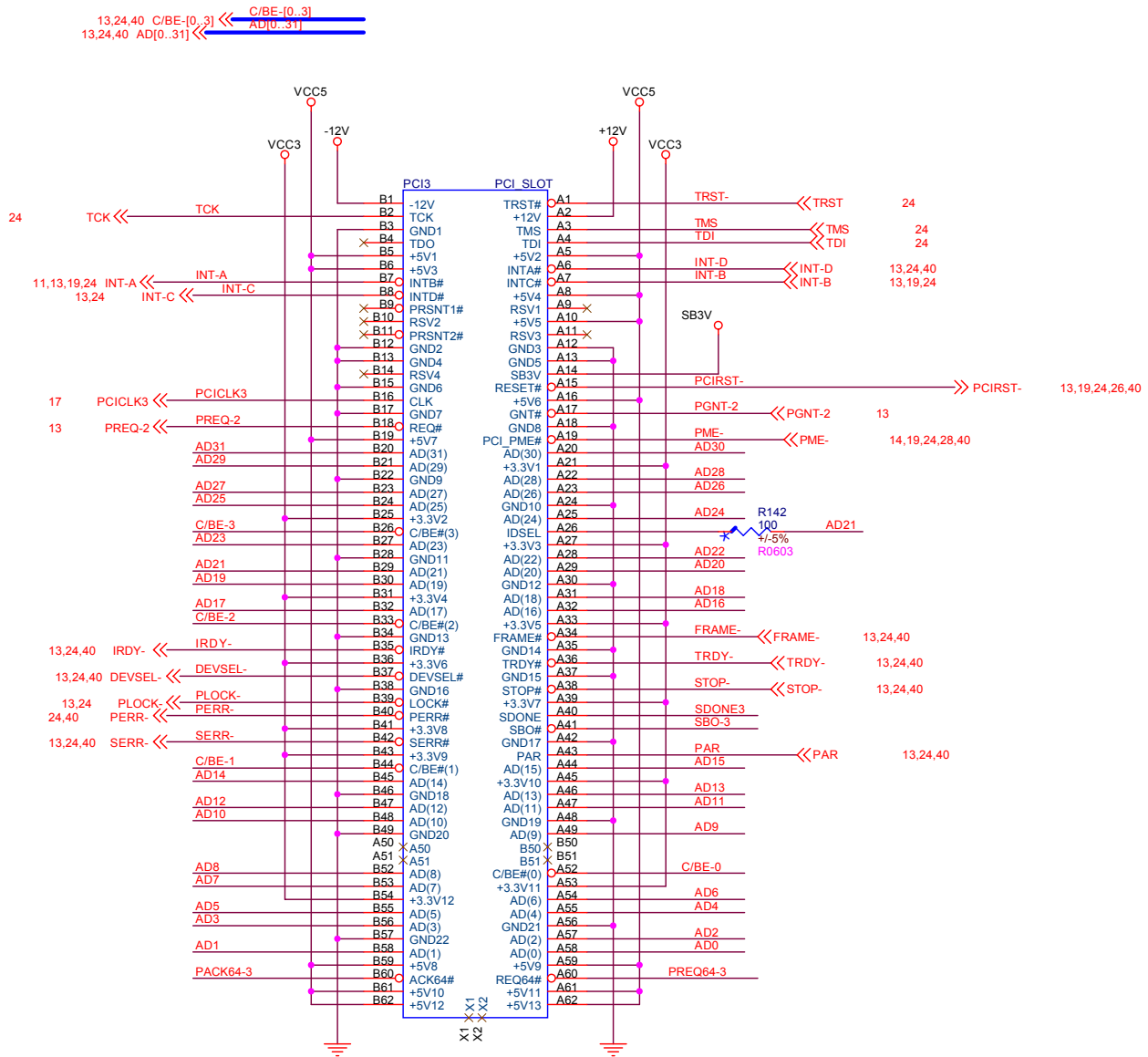
Document Number: 661M05

Date: Saturday, October 09, 2004

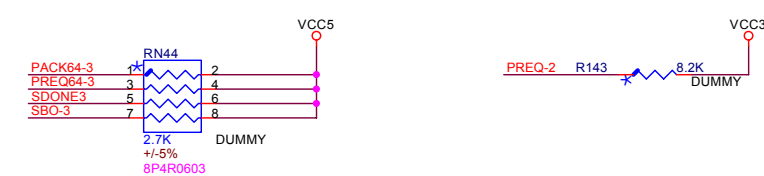
Sheet: 24 of 42

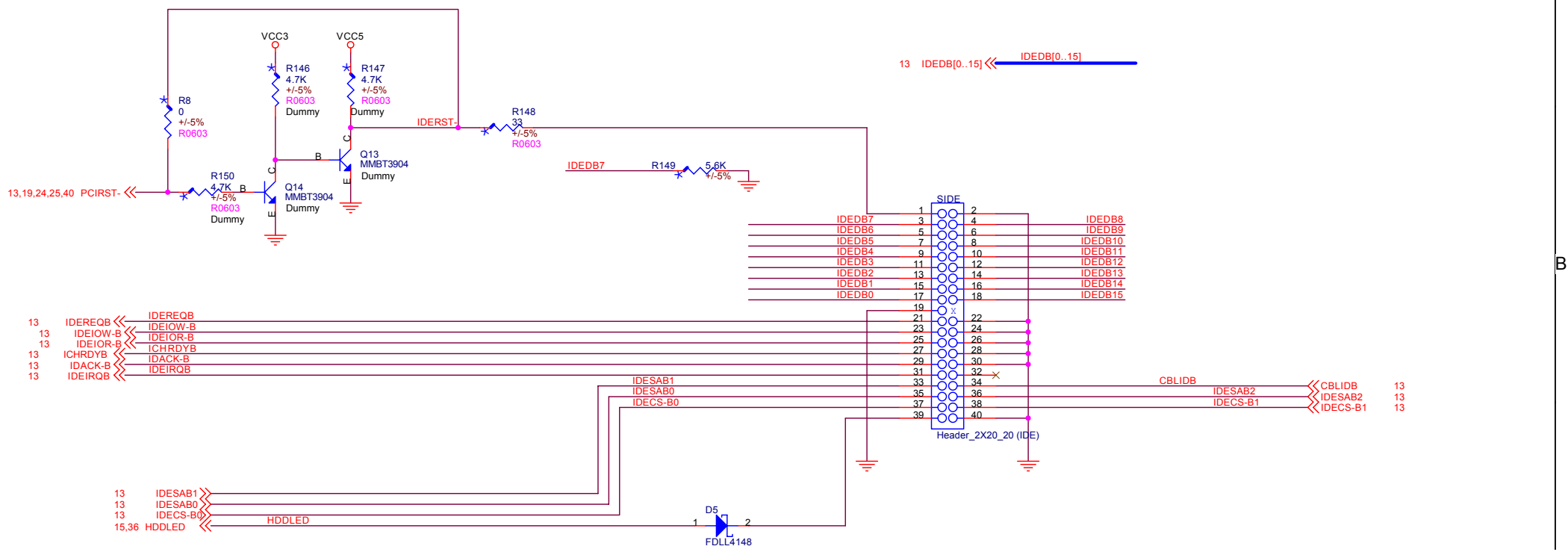
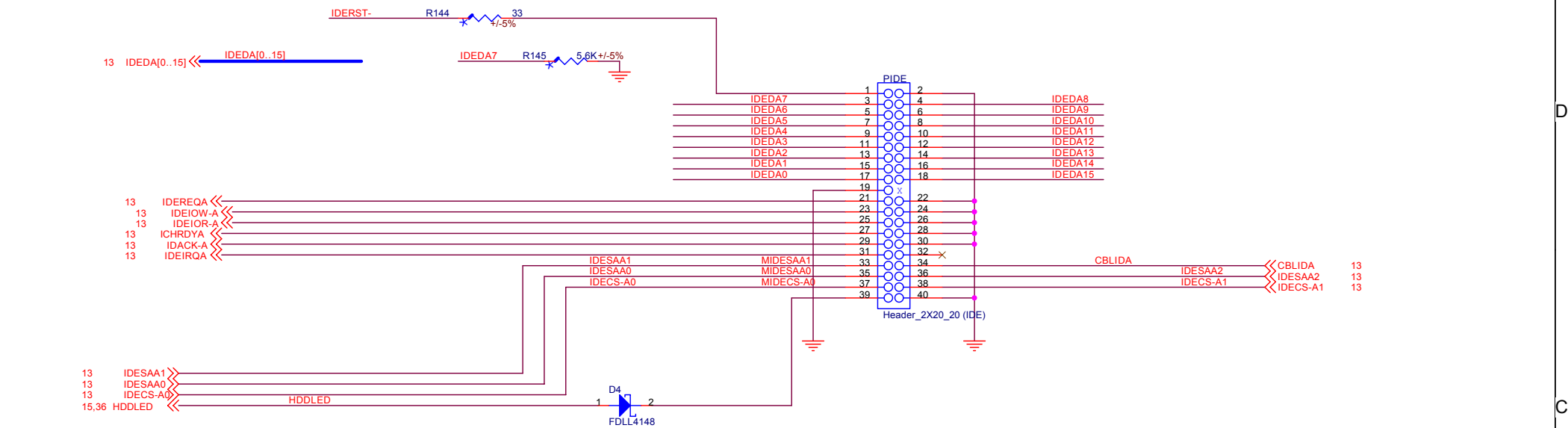
Rev: A

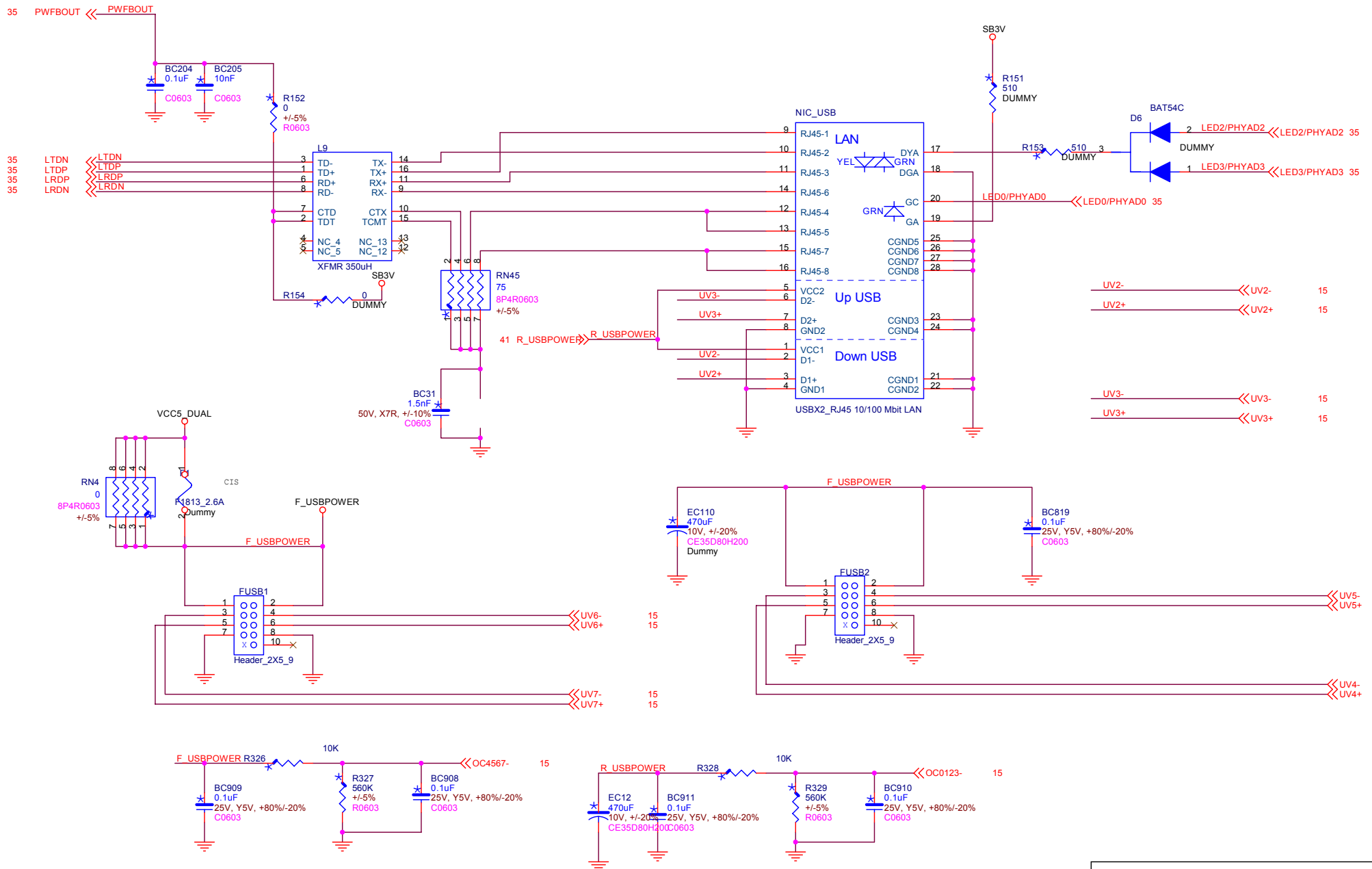
PCI Slot 3

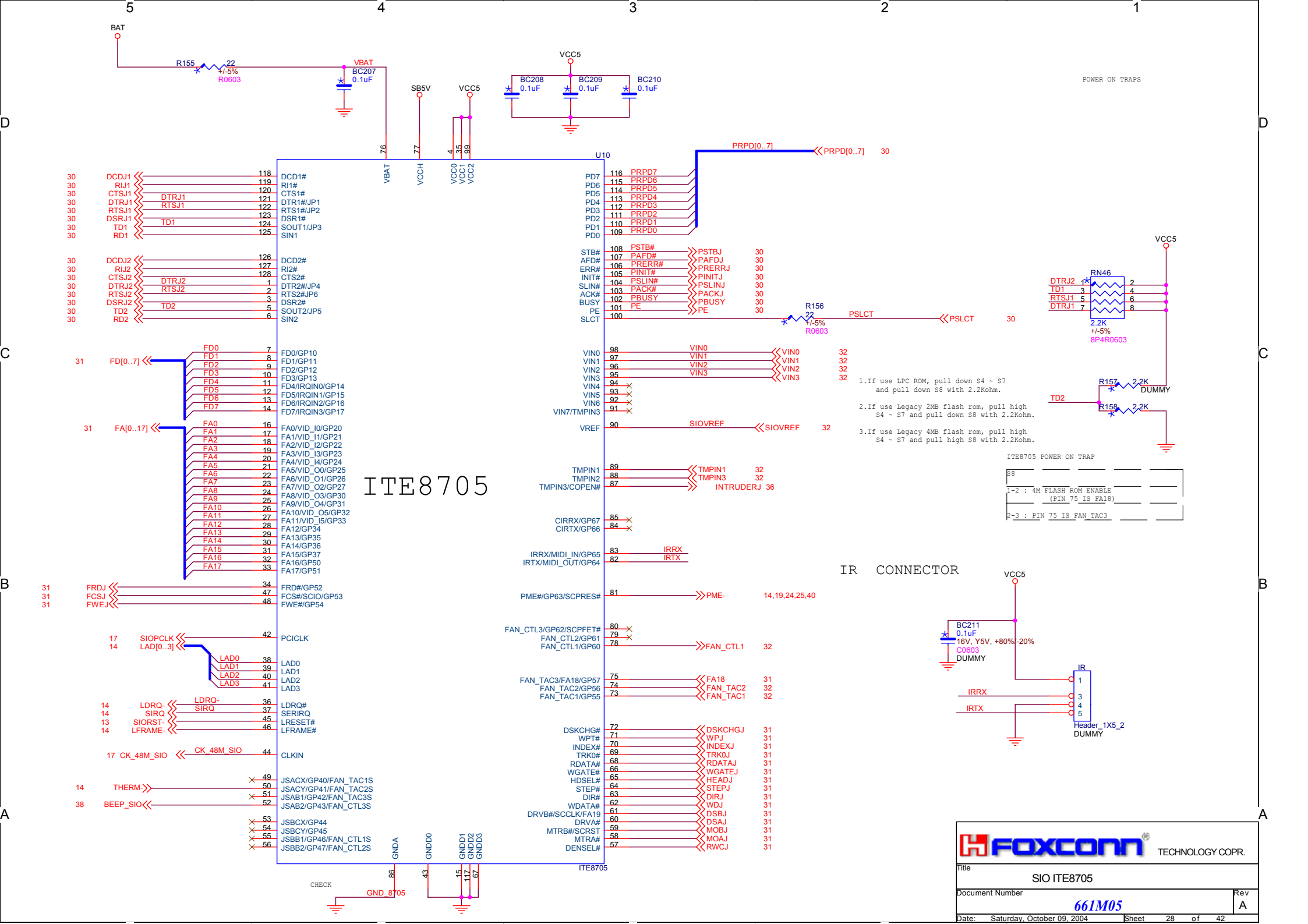


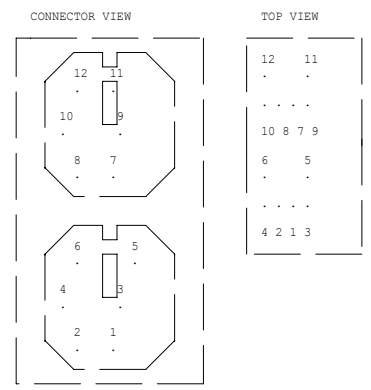
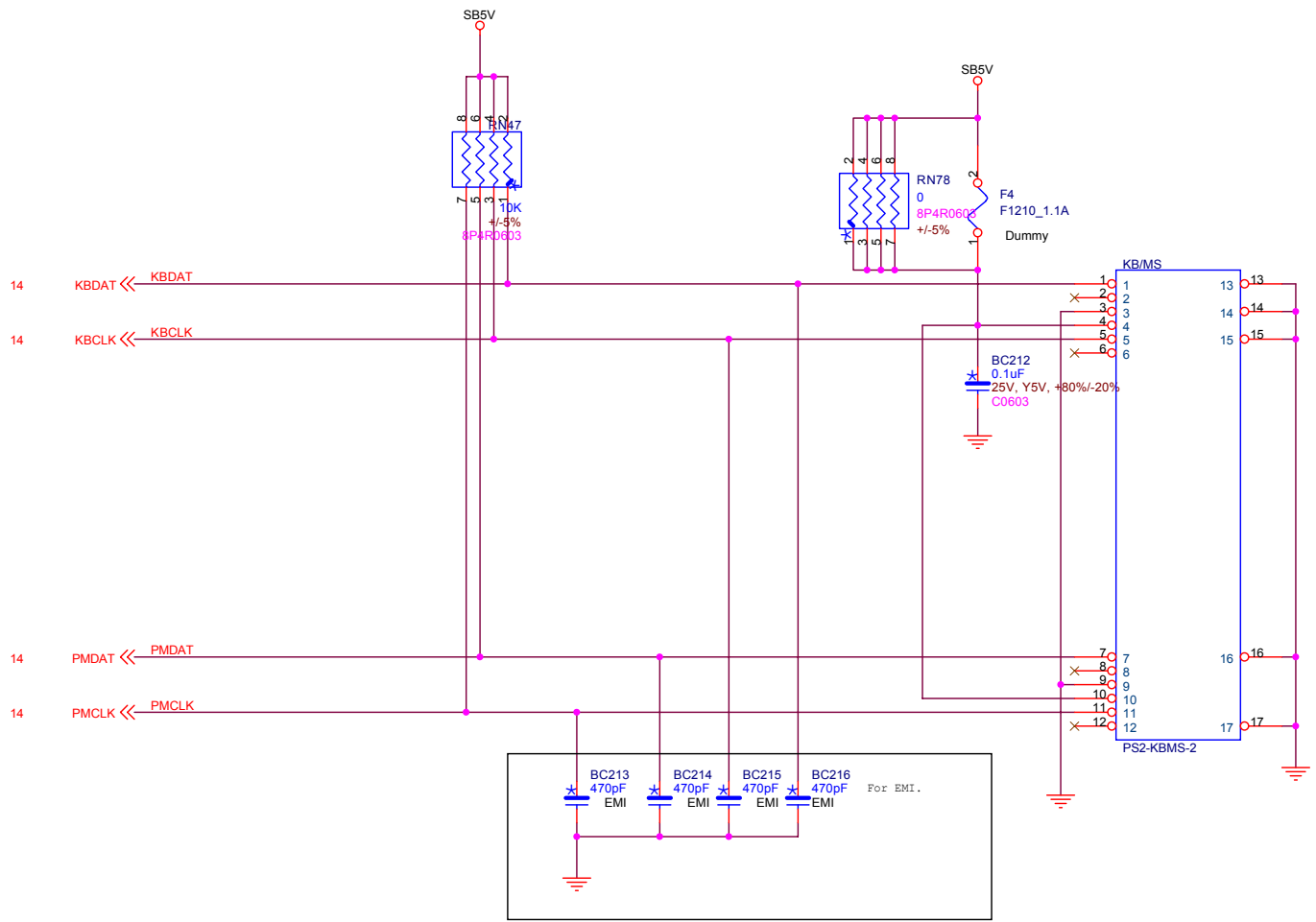
13,24,40 C/BE-[0..3] << C/BE-[0..3]
 13,24,40 AD[0..31] << AD[0..31]



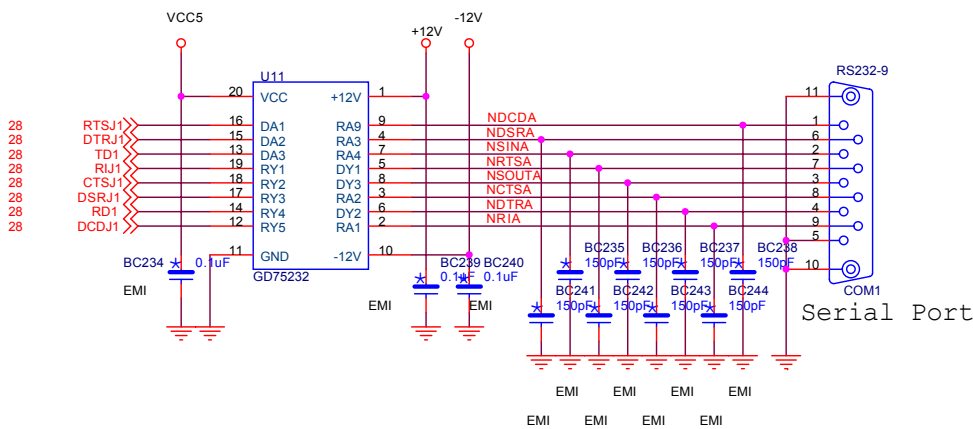
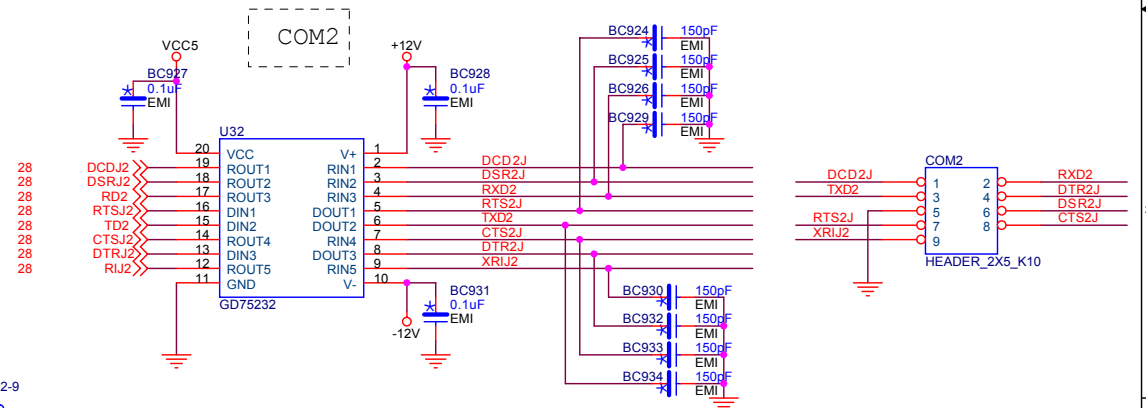
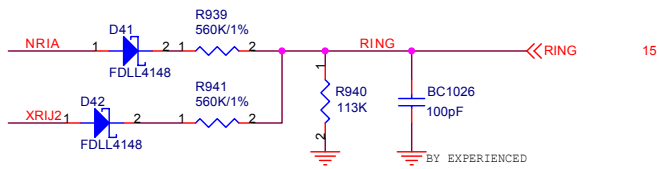
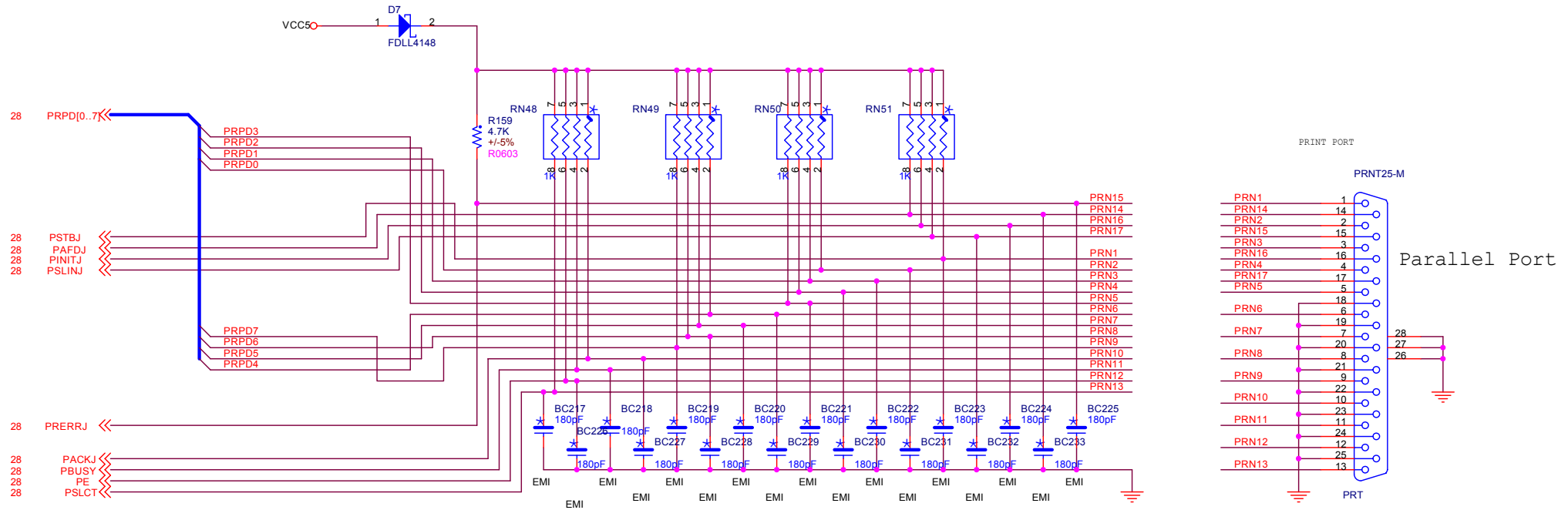




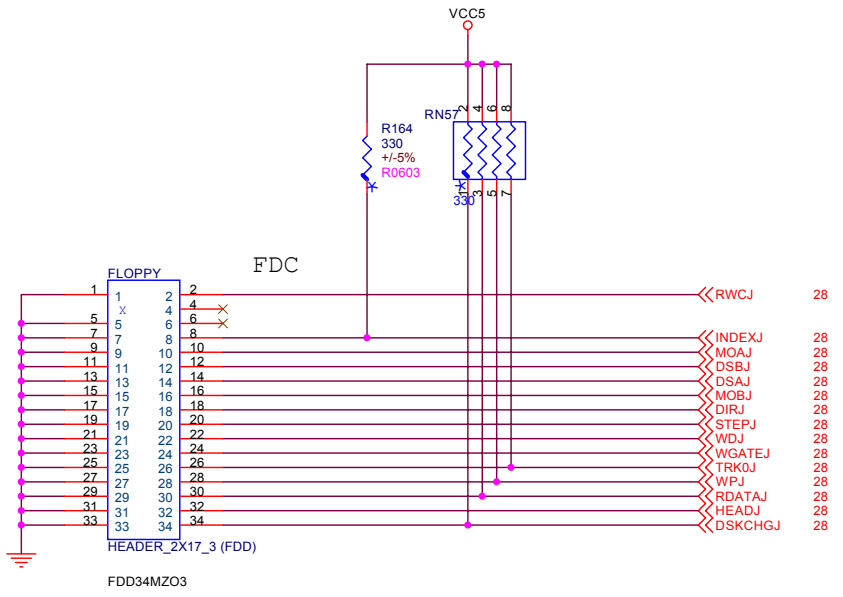
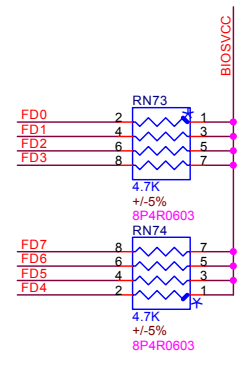
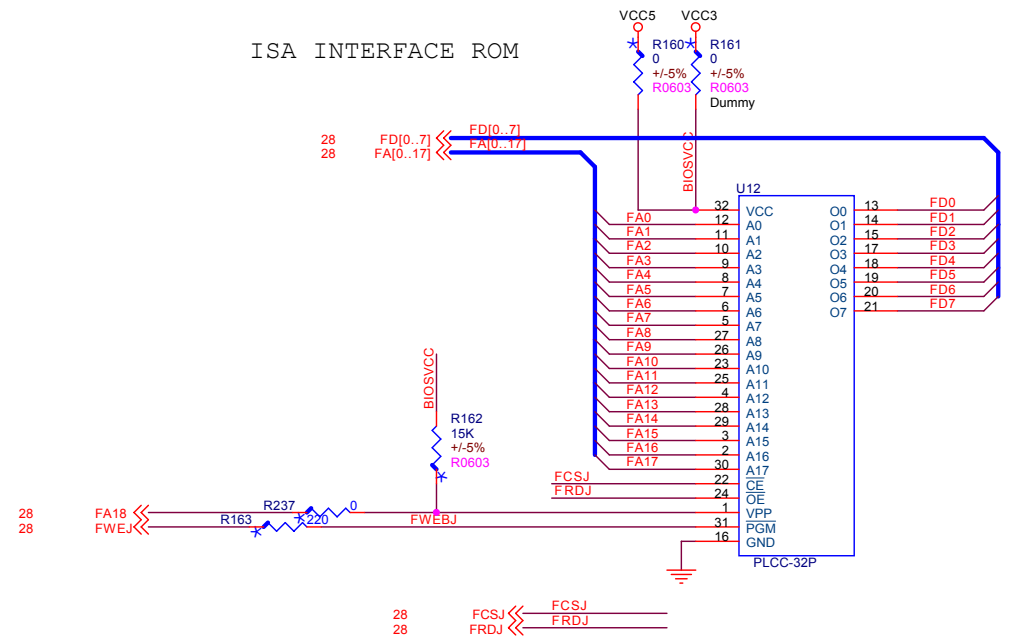




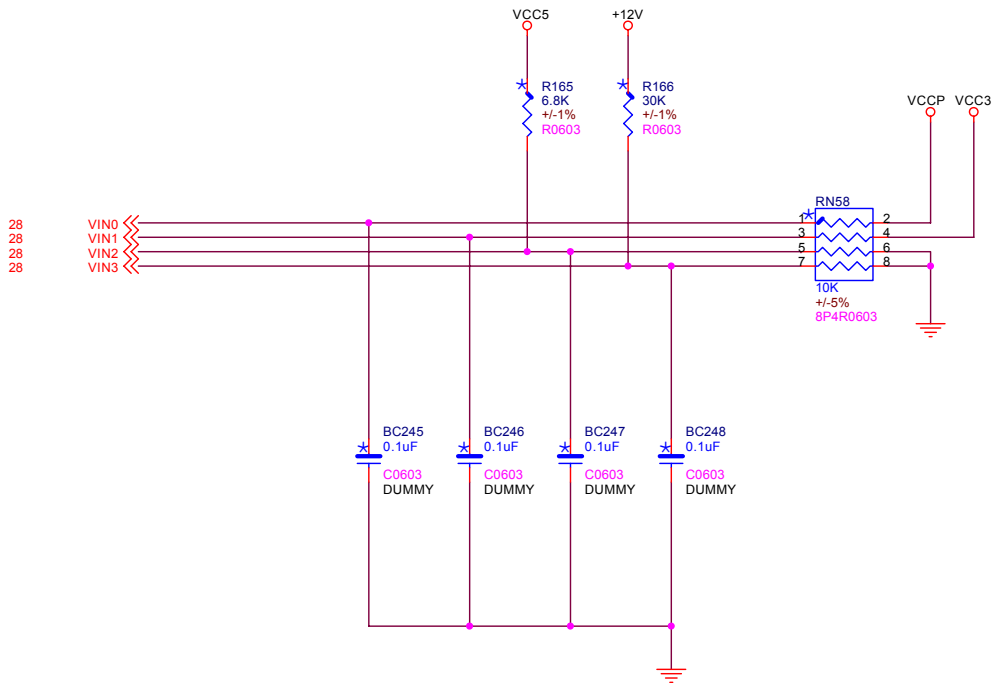
NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.



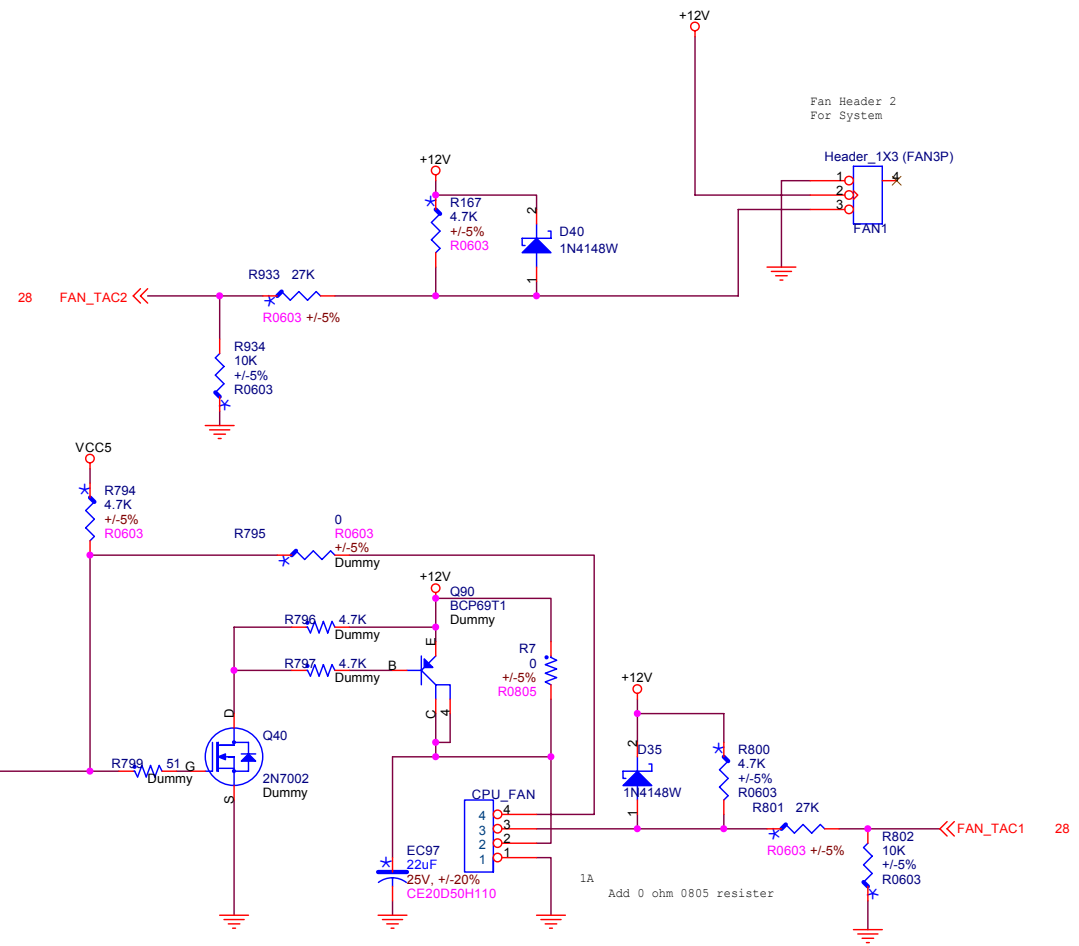
ISA INTERFACE ROM



Voltage Monitor

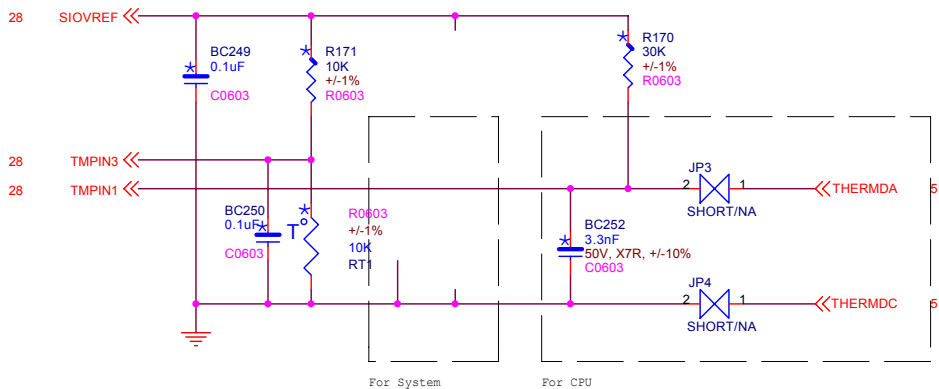


FAN Input and Output

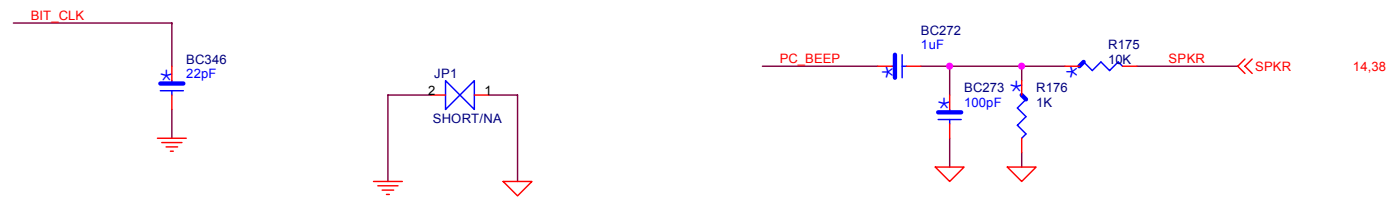
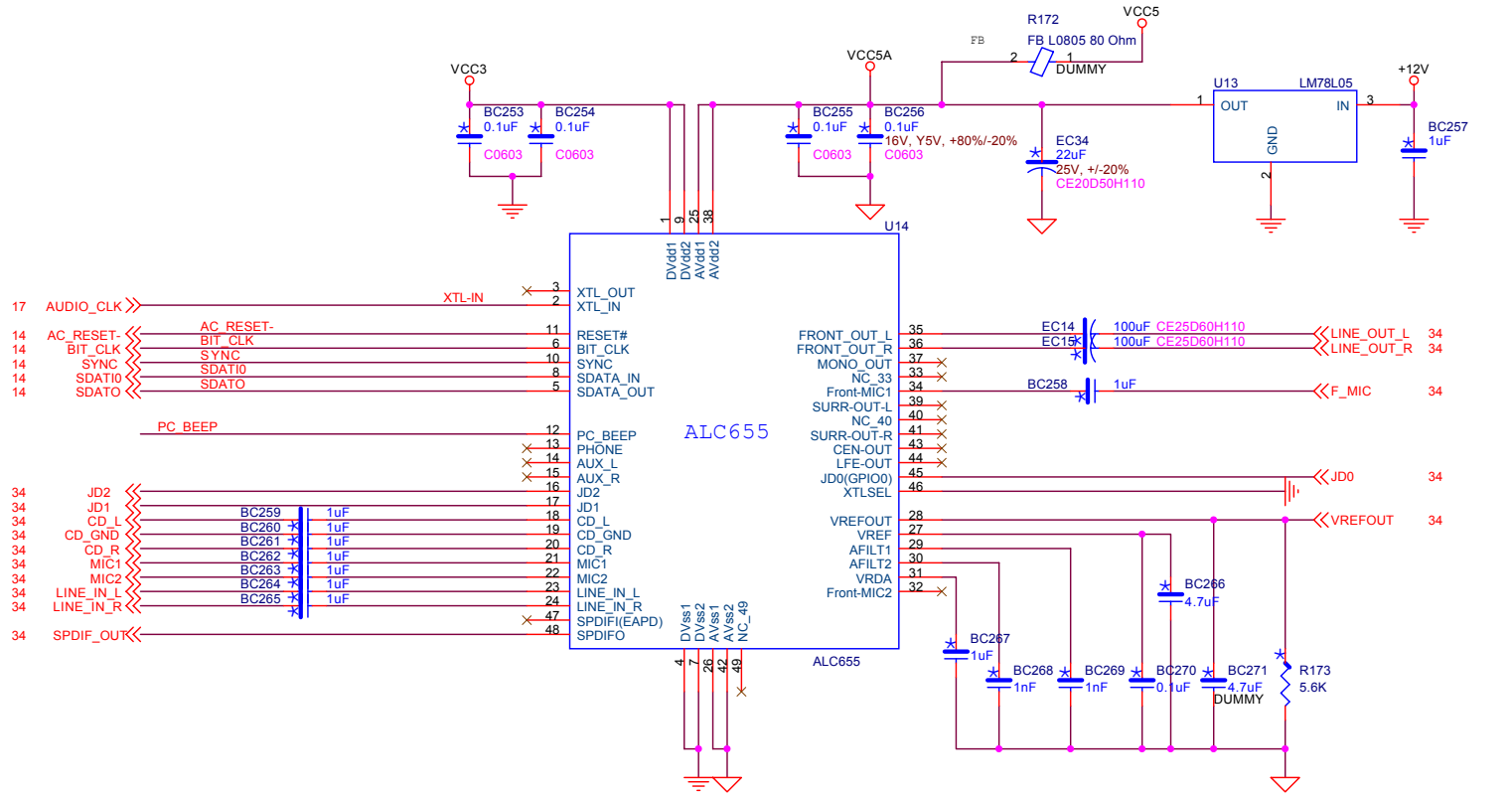


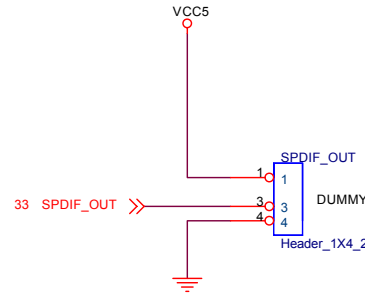
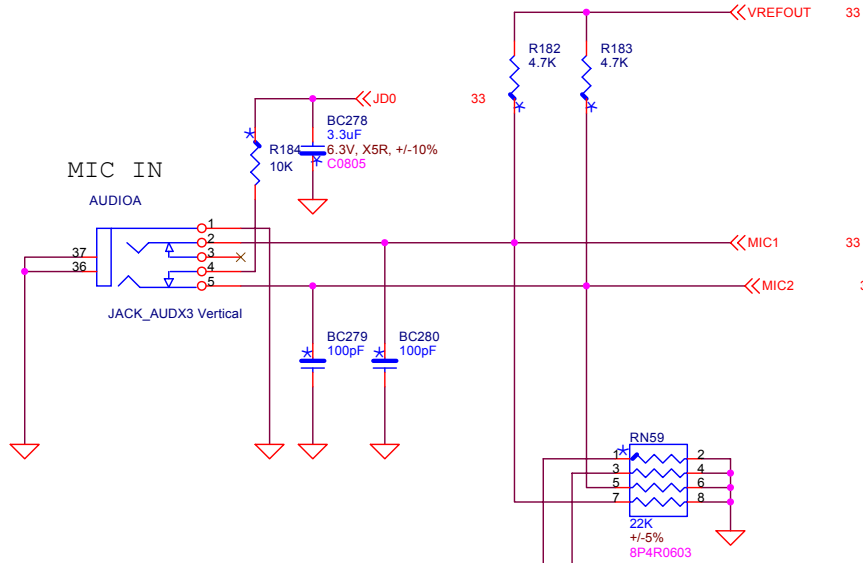
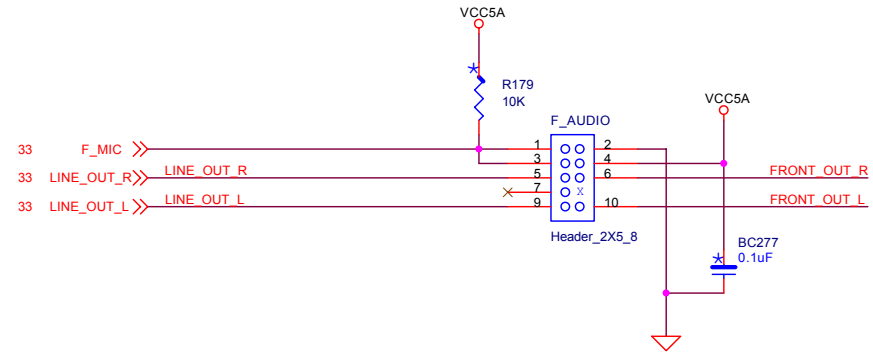
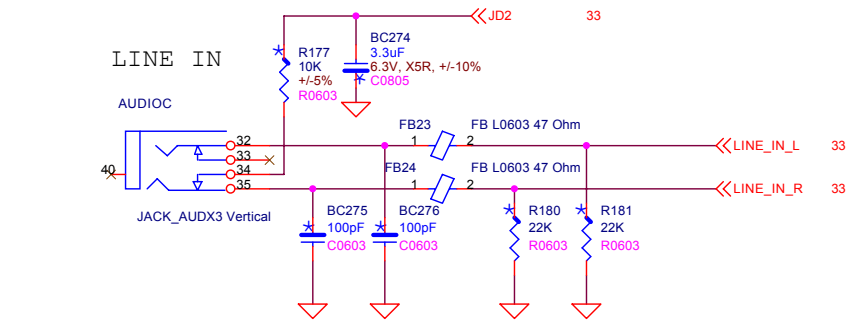
Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode

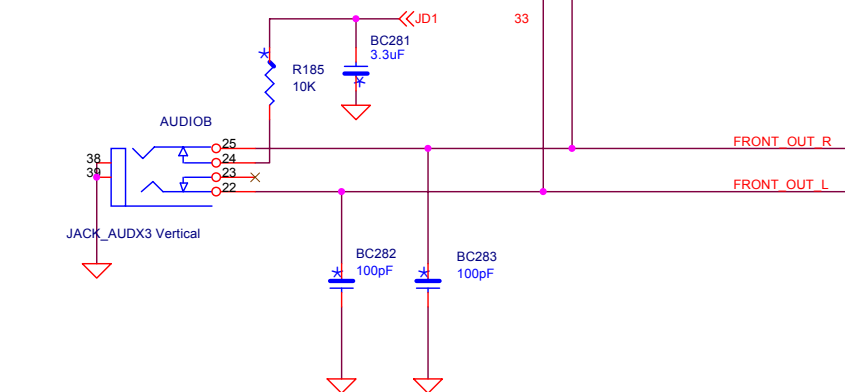


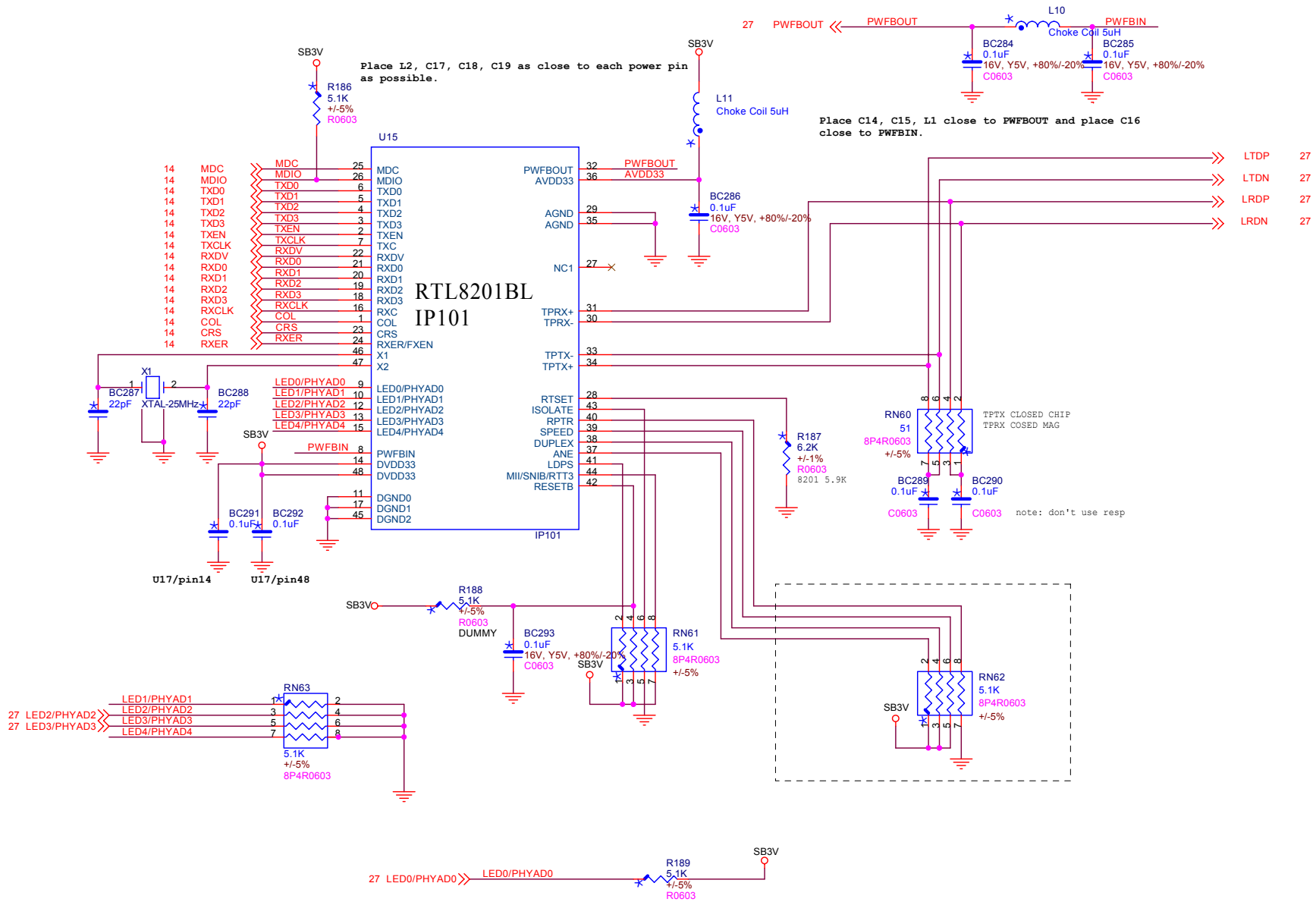
check CPU FAN

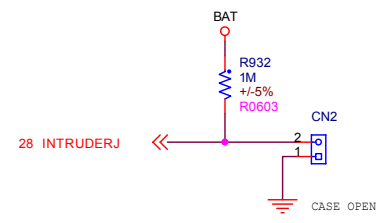
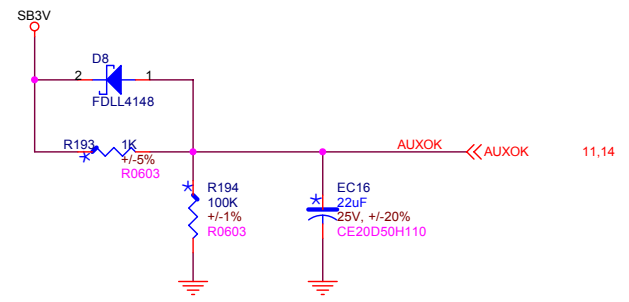
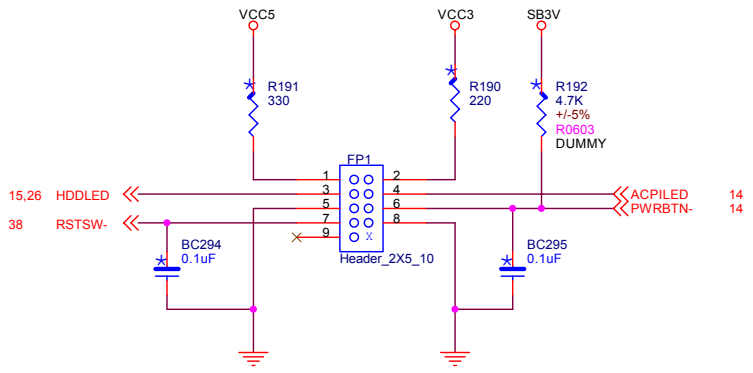




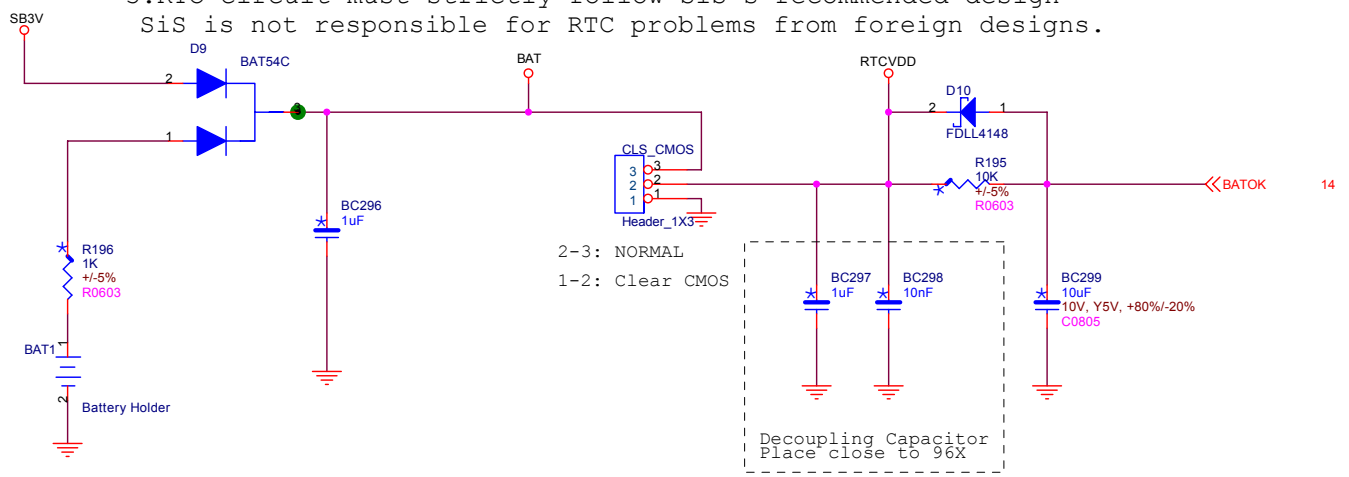
LINE OUT



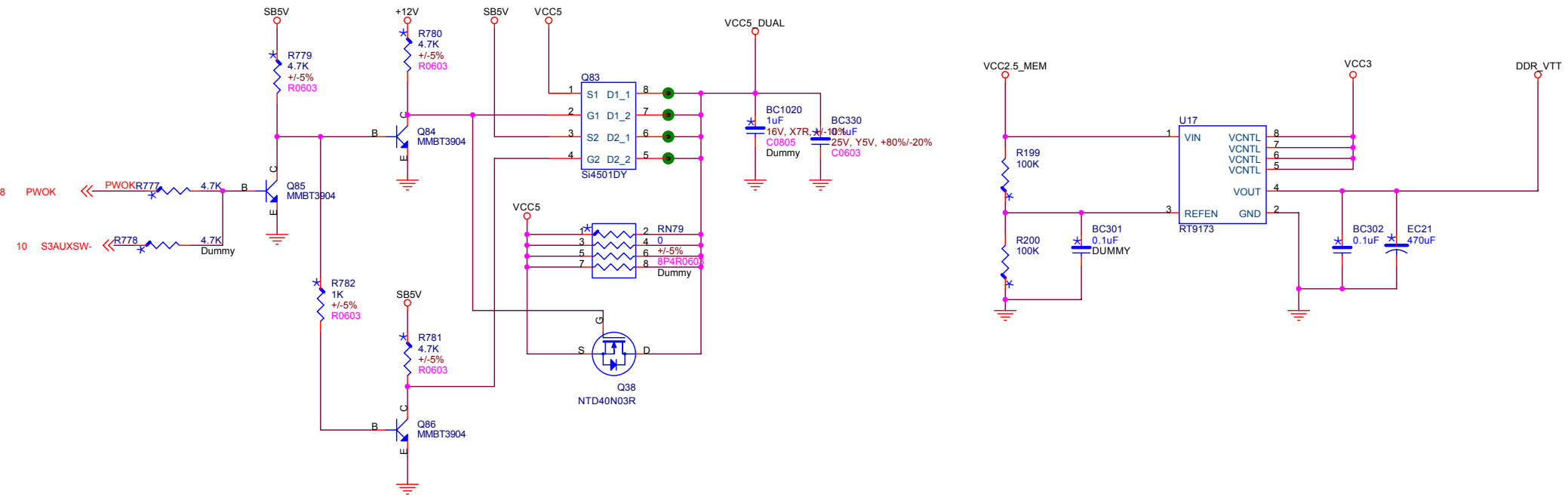




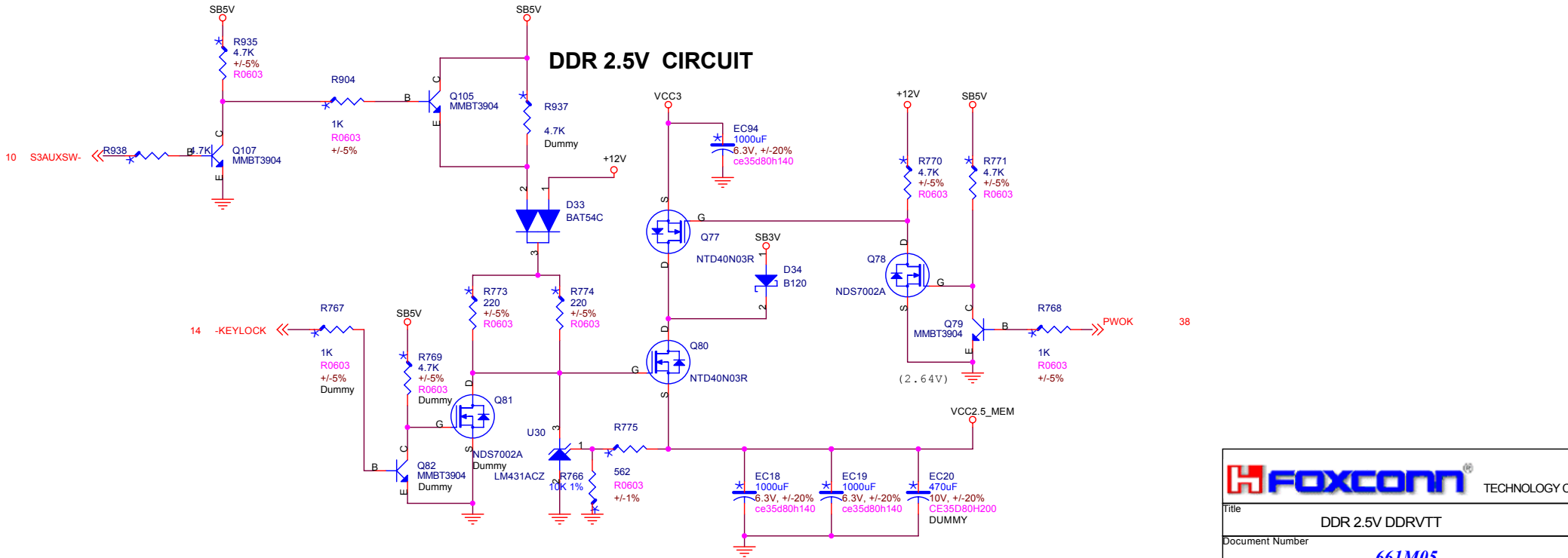
RTC
 NOTE!
 1.The RTCVDD is 3V
 2.Decoupling capacitor must be close to 96X RTCVDD pin.
 3.RTC circuit must strictly follow SiS's recommended design
 SiS is not responsible for RTC problems from foreign designs.

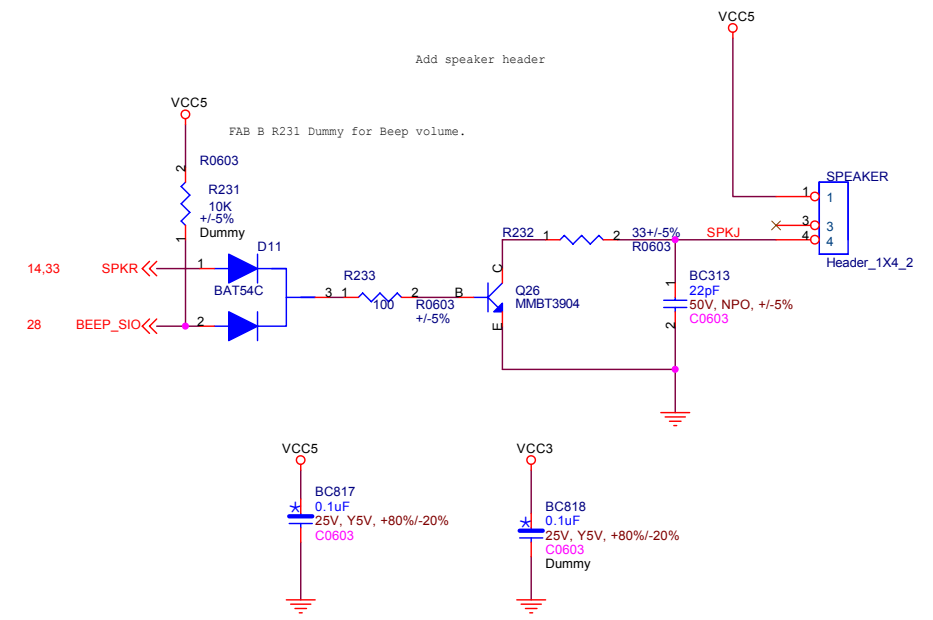
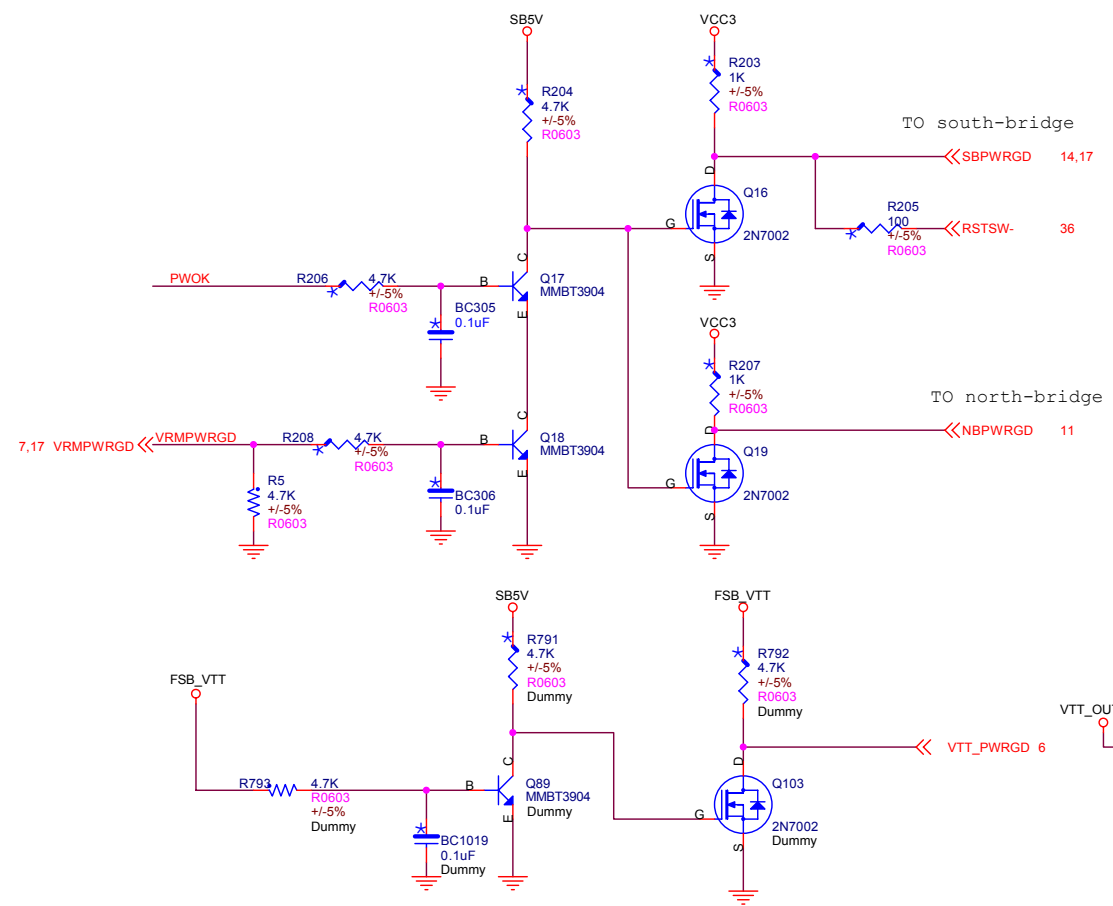
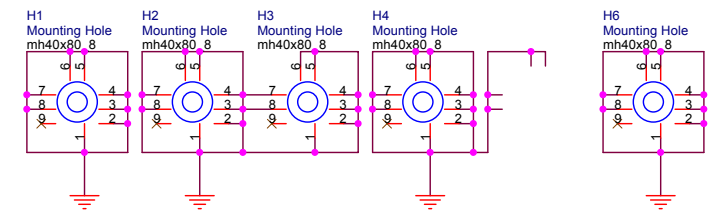
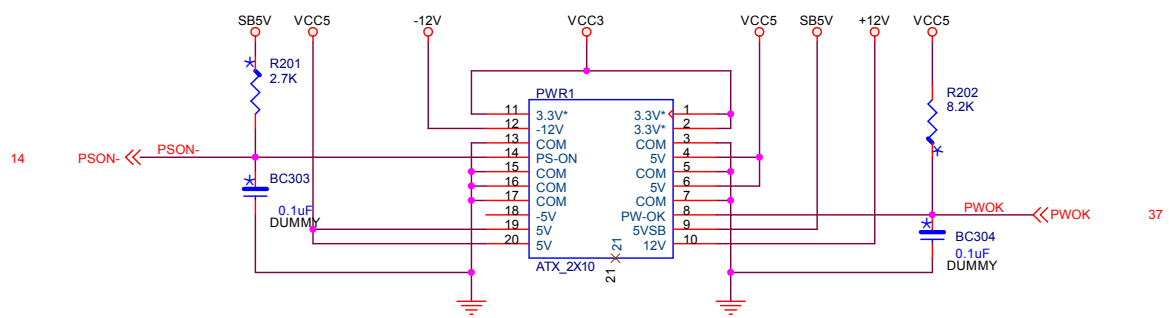


5V DUAL CIRCUIT

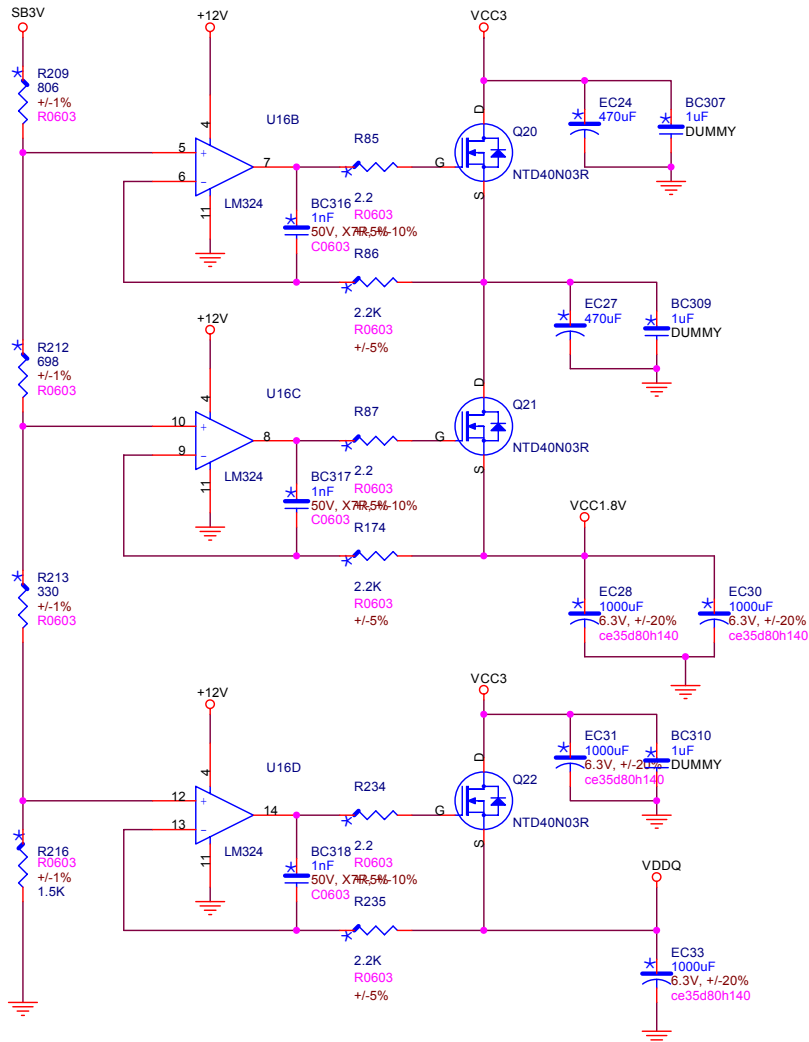


DDR 2.5V CIRCUIT

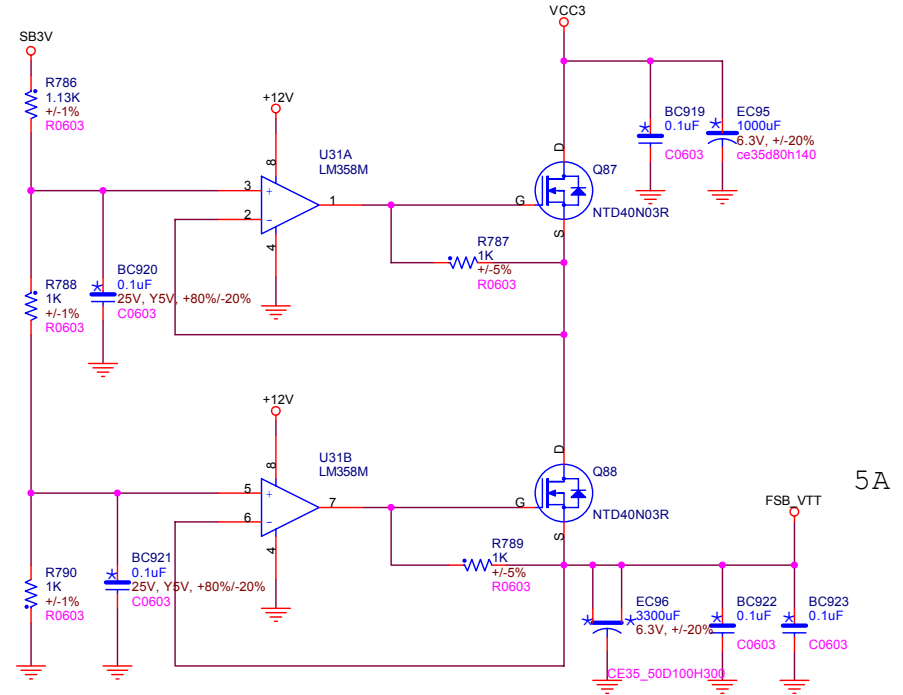




VCC1.8V and VDDQ

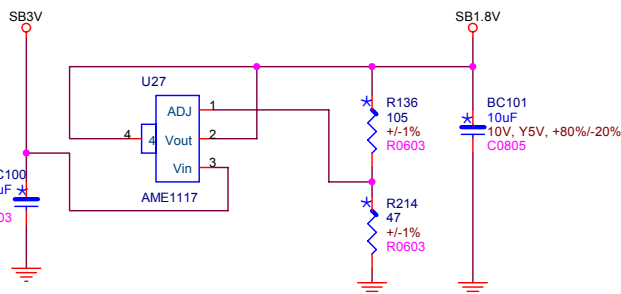


FSB_VTT

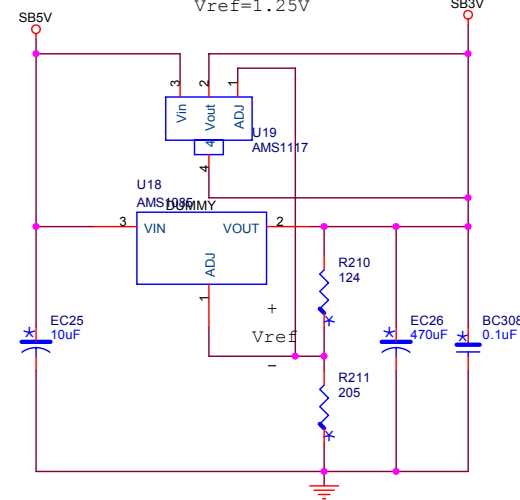


5A

SB1.8V for 964

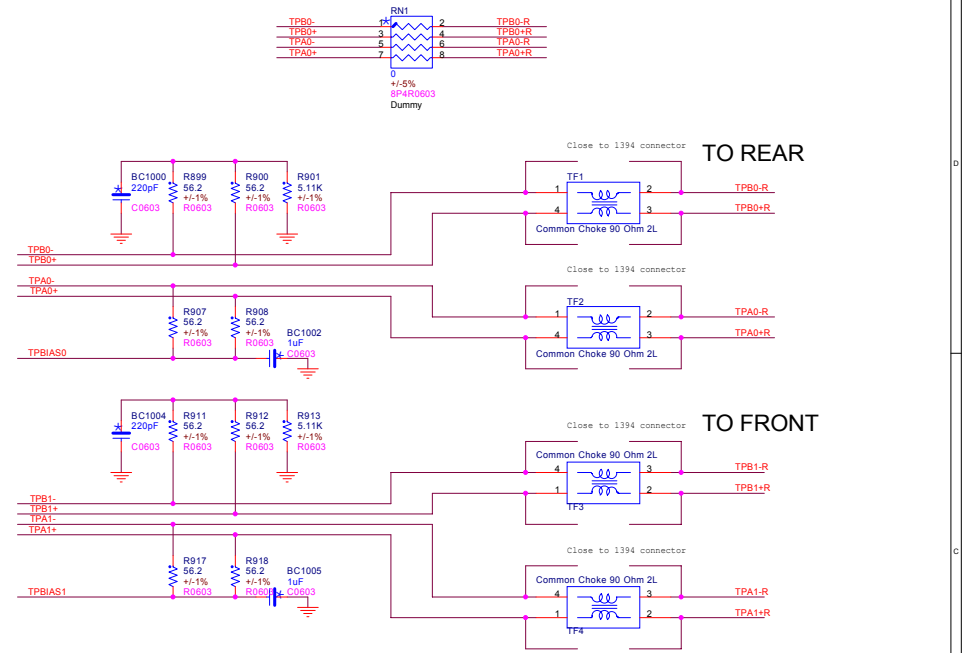
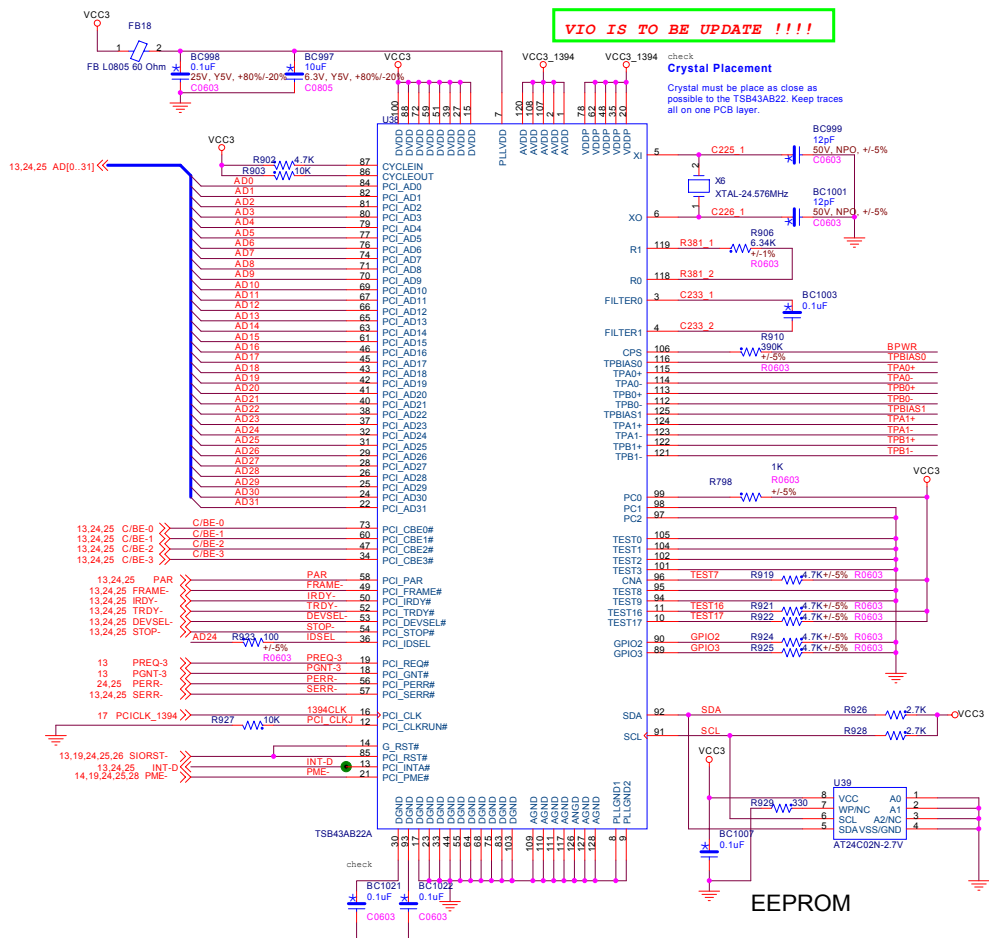


SB3.3V Vref=1.25V

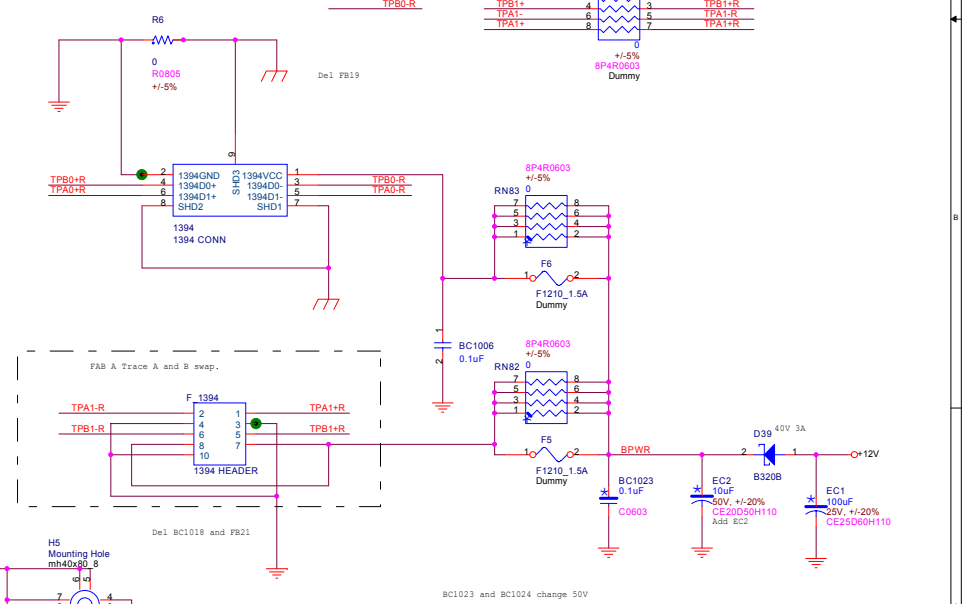


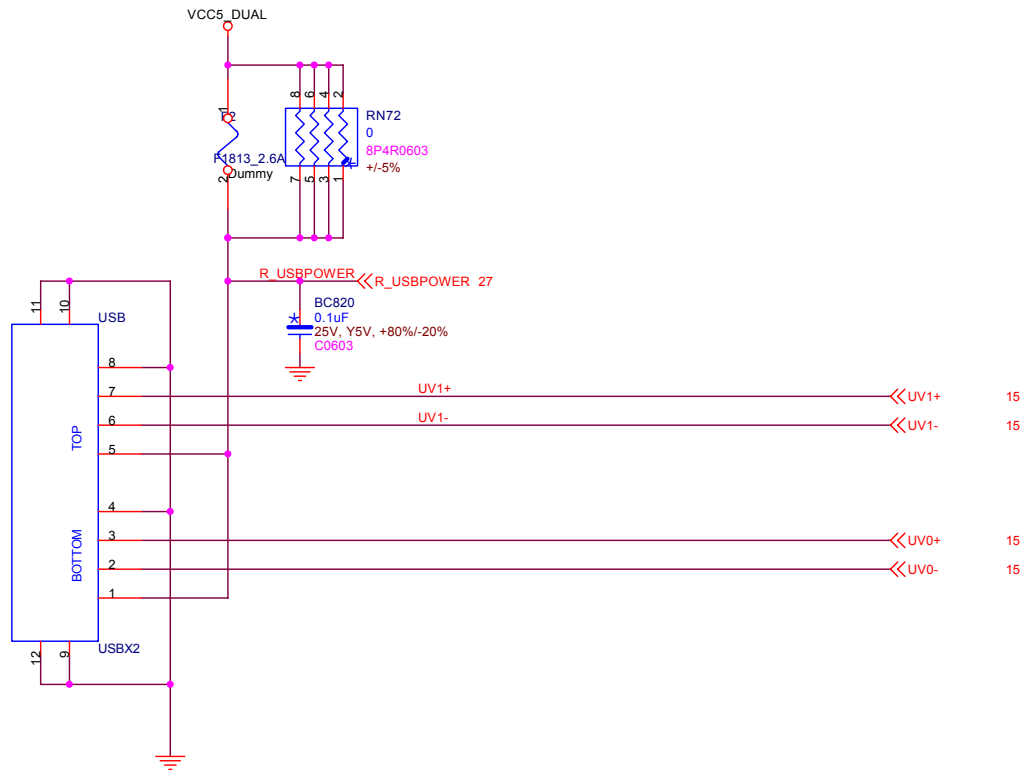
SB3.3V





- NOTES:**
1. Keep termination components close to TSB43AB22 device.
 2. Use Wide Copper Bus for Chassis ground and connect all 1394 connector shields directly to it. No thin trace leathers.







Title 661FX-1 HOST & AGP

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