
HA12187FP

Bus Interface Driver/Receiver IC

HITACHI

ADE-207-174A (Z)

2nd Edition
Jun. 1999

Description

The HA12187FP was developed to be used as a bus interface driver/receiver IC in automotive audio equipment controllers. It implements a two-wire serial bus.

Functions

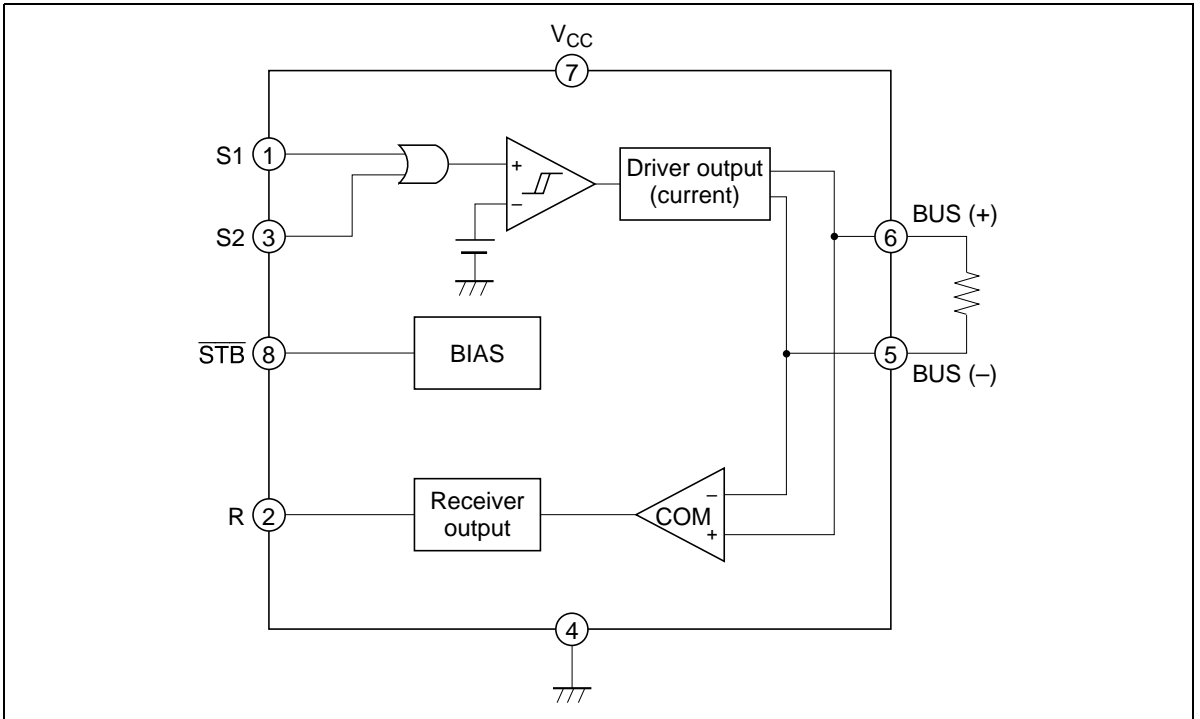
- Two-input OR circuit
- Input comparator circuit
- Current output driver circuit
- Receiver input comparator circuit
- Receiver output circuit
- Standby circuit

Features

- Supports two data inputs (Pins 1 and 3 are the input pins)
- Comparators with hysteresis characteristics were adopted for the inputs
- Current drive output drivers adopted (Output current: 3.8 mA typical)
- Comparators with hysteresis characteristics were adopted for the receivers
- Wide receiver common-mode input operating range (Common-mode input operating range: 0 to 5 V typical)
- The driver output and the receiver input can withstand high voltages (Maximum rating: 18 V)
- Standby function (The IC enters standby mode when pin 8 goes low)
- Operating power-supply voltage range: 5 V \pm 0.5 V

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Block Diagram



Pin Functions

Pin No.	Symbol	Function	Equivalent Circuit
1	S1	Data input	
2	R out	Receiver output	
3	S2	Data input	
4	GND	GND	
5	BUS (-)	Bus output (-) Receiver input (-)	
6	BUS (+)	Bus output (+) Receiver input (+)	
7	V _{CC}	Power supply	
8	STB	Standby control input	

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Power-supply voltage	V _{cc}	7	V	
Allowable power dissipation	Pd	400	mW	Ta ≤ 85°C
Operating temperature	Topr	-40 to 85	°C	
Storage temperature	Tstg	-55 to 125	°C	
Input voltage	Vin	-1.0 to 6.7	V	
Bus input voltage	Bus	18	V	

Note: Recommended operating power supply voltage range: 5 V ±0.5 V

Electrical Characteristics ($V_{CC} = 5.0\text{ V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Test Circuit	
S1	High-level input voltage	V_{IHS1}	3.5	—	—	V	$V1 = 0\text{ V} \rightarrow 5\text{ V}$, $V3 = 0\text{ V}$ With the potential difference between pin 5 and pin 6 120 mV or more	1	Figure 1
	Low-level input voltage	V_{ILS1}	—	—	1.5	V	$V1 = 5\text{ V} \rightarrow 0\text{ V}$, $V3 = 0\text{ V}$ With the potential difference between pin5 and pin 6 20 mV or less	1	
	High-level input current	I_{IHS1}	—	—	1	μA	$V1 = 5\text{ V}$, $V3 = 0\text{ V}$	1	
	Low-level input current	I_{ILS1}	—	—	1	μA	$V1 = 0\text{ V}$, $V3 = 0\text{ V}$	1	
S2	High-level input voltage	V_{IHS2}	3.5	—	—	V	$V3 = 0\text{ V} \rightarrow 5\text{ V}$, $V1 = 0\text{ V}$ With the potential difference between pin 5 and pin 6 120 mV or more	3	Figure 1
	Low-level input voltage	V_{ILS2}	—	—	1.5	V	$V3 = 5\text{ V} \rightarrow 0\text{ V}$, $V1 = 0\text{ V}$ With the potential difference between 5 and pin 6 20 mV or less	3	
	High-level input current	I_{IHS2}	—	—	1	μA	$V1 = 0\text{ V}$, $V3 = 5\text{ V}$	3	
	Low-level input current	I_{ILS2}	—	—	1	μA	$V1 = 0\text{ V}$, $V3 = 0\text{ V}$	3	
Driver	High-level output current	I_{OH}	3.0	3.8	4.8	mA	$I_{OH} = V_{OHD+} - V_{OHD-} / 62\ \Omega$	5, 6	Figure 1
	Low-level output leakage current	I_{OL}	—	—	1	μA	Pin 5 voltage = V_{OP-} $I_{OL} = V_{OP+} - V_{OP-} / R_I$	5, 6	
	Reference operating voltage (+)	V_{OP+}	2.3	2.5	2.7	V	$V1 = 0\text{ V}$, $V3 = 0\text{ V}$	6	
	Reference operating voltage (-)	V_{OP-}	2.3	2.5	2.7	V	$V1 = 0\text{ V}$, $V3 = 0\text{ V}$	5	
Current drain 1	$I_{CC}H$	5.5	7.3	9.5	mA	$V1 = 5\text{ V}$, $V3 = 0\text{ V}$	7	Figure 1	
Current drain 2	$I_{CC}L$	1.7	2.2	2.7	mA	$V1 = 0\text{ V}$, $V3 = 0\text{ V}$	7	Figure 1	

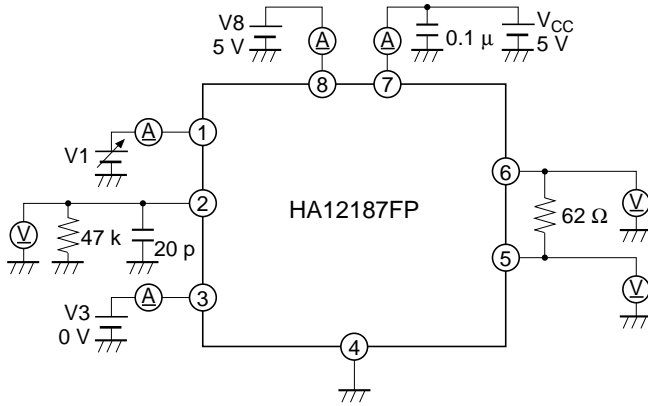
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Electrical Characteristics ($V_{CC} = 5.0 \text{ V}$, $T_a = 25^\circ\text{C}$) (cont)

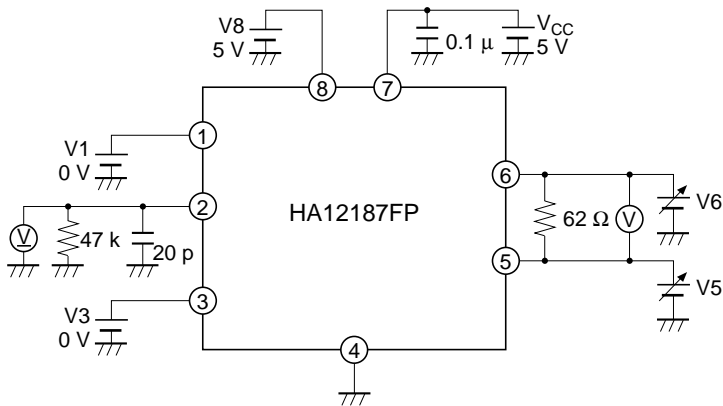
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Test Pin	Test Circuit
Receiver High-level input voltage (1)	V_{IH1}	—	80	120	mV	$V_6 = 0 \rightarrow 5 \text{ V}$, pin 2 = 4 V or more, $V_1 = 0 \text{ V}$, $V_3 = 0 \text{ V}$, $V_5 = V_{OP-}$, $V_{IH1} = V_6 - V_5$	2	Figure 2
Low-level input voltage (1)	V_{IL1}	20	45	—	mV	$V_6 = 5 \rightarrow 0 \text{ V}$, pin 2 = 1 V or less, $V_1 = 0 \text{ V}$, $V_3 = 0 \text{ V}$, $V_5 = V_{OP-}$, $V_{IL1} = V_6 - V_5$	2	Figure 2
Input hysteresis voltage (1)	V_{IHYS1}	10	35	60	mV	$V_{IHYS1} = V_{IH1} - V_{IL1}$		
High-level common-mode input voltage	V_{IHCOM}	4.5	—	—	V	$V_5 = 0 \rightarrow 5 \text{ V}$, pin 2 = 4 V or more, $V_1 = 0 \text{ V}$, $V_3 = 0 \text{ V}$, $V_6 - V_5 = 120 \text{ mV}$	5	Figure 2
Low-level common-mode input voltage	V_{ILCOM}	5	—	—	V	$V_5 = 0 \rightarrow 5 \text{ V}$, pin 2 = 1 V or less, $V_1 = 0 \text{ V}$, $V_3 = 0 \text{ V}$, $V_6 - V_5 = 20 \text{ mV}$	5	Figure 2
Receiver input resistance*1	RI	25	35	45	k Ω	$V_1 = 0 \text{ V}$, $RI = \frac{0.6 \text{ V}}{I_1 - I_2}$	5, 6	Figure 3
High-level output voltage	V_{OH}	4.5	—	—	V	$V_1 = 5 \text{ V}$, $V_3 = 0 \text{ V}$	2	Figure 1
Low-level output voltage	V_{OL}	—	—	1.0	V	$V_1 = 0 \text{ V}$, $V_3 = 0 \text{ V}$	2	Figure 1
Power supply off output leakage current	I_{OLEAK}	—	—	1	μA	V_{CC} off, $V_8 = 0 \text{ V}$, $V_6 = 5 \text{ V}$, $V_1 = 0 \text{ V}$, $V_3 = 0 \text{ V}$, SW1 on	5, 6	Figure 4
STB on voltage	VSTBon	—	—	1.5	V	$V_8 = 5 \rightarrow 0 \text{ V}$, $V_1 = 5 \text{ V}$, V_8 when $I_{CC} \leq 20 \mu\text{A}$	7	Figure 4
STB off voltage	VSTBoff	3.5	—	—	V	$V_8 = 0 \rightarrow 5 \text{ V}$, $V_1 = 5 \text{ V}$, V_8 when $I_{CC} \geq 4.5 \text{ mA}$	7	Figure 4
Standby mode current drain	I_{CCstb}	—	10	20	μA	$V_1 = 5 \text{ V}$, $V_3 = 0 \text{ V}$, $V_8 = 0 \text{ V}$	7	Figure 4
Standby mode leakage current	Istb-Leak	—	—	1	μA	$V_1 = 5 \text{ V}$, $V_3 = 0 \text{ V}$, $V_8 = 0 \text{ V}$, $V_6 = 5 \text{ V}$, SW1 on	5, 6	Figure 4
Delay time (L \rightarrow H)	DLY1	—	600	800	nS	See the operating waveform figure	2	Figure 5
Delay time (H \rightarrow L)	DLY2	—	450	800	nS	See the operating waveform figure	2	Figure 5

Note: 1. I_1 is the measured current when $V_6 = (V_{OP+}) + 0.3 \text{ V}$, and I_2 is the measured current when $V_6 = (V_{OP+}) - 0.3 \text{ V}$.

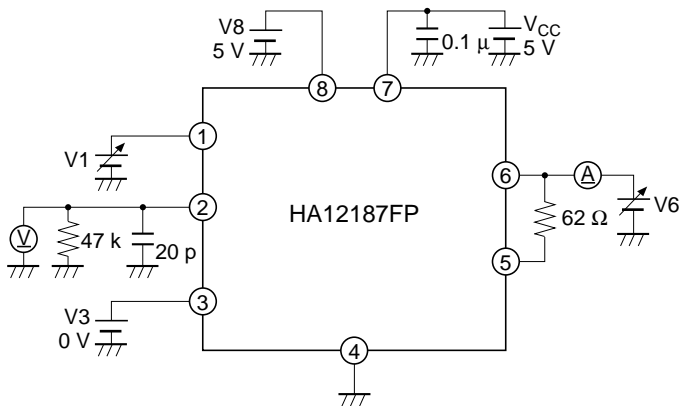
Test Circuits



Test Circuit 1

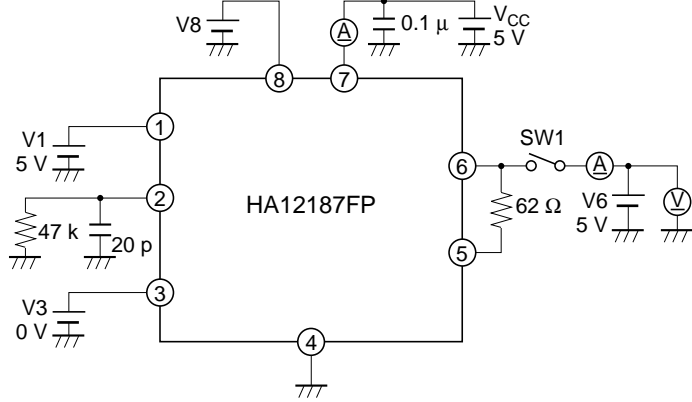


Test Circuit 2

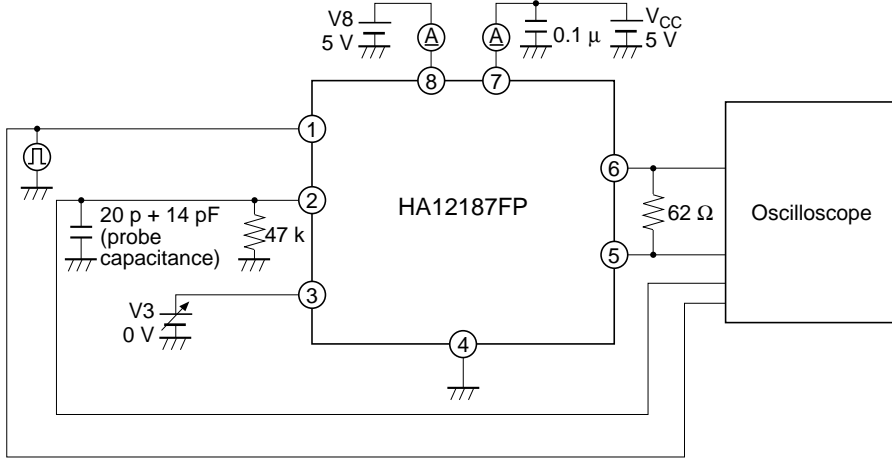


Test Circuit 3

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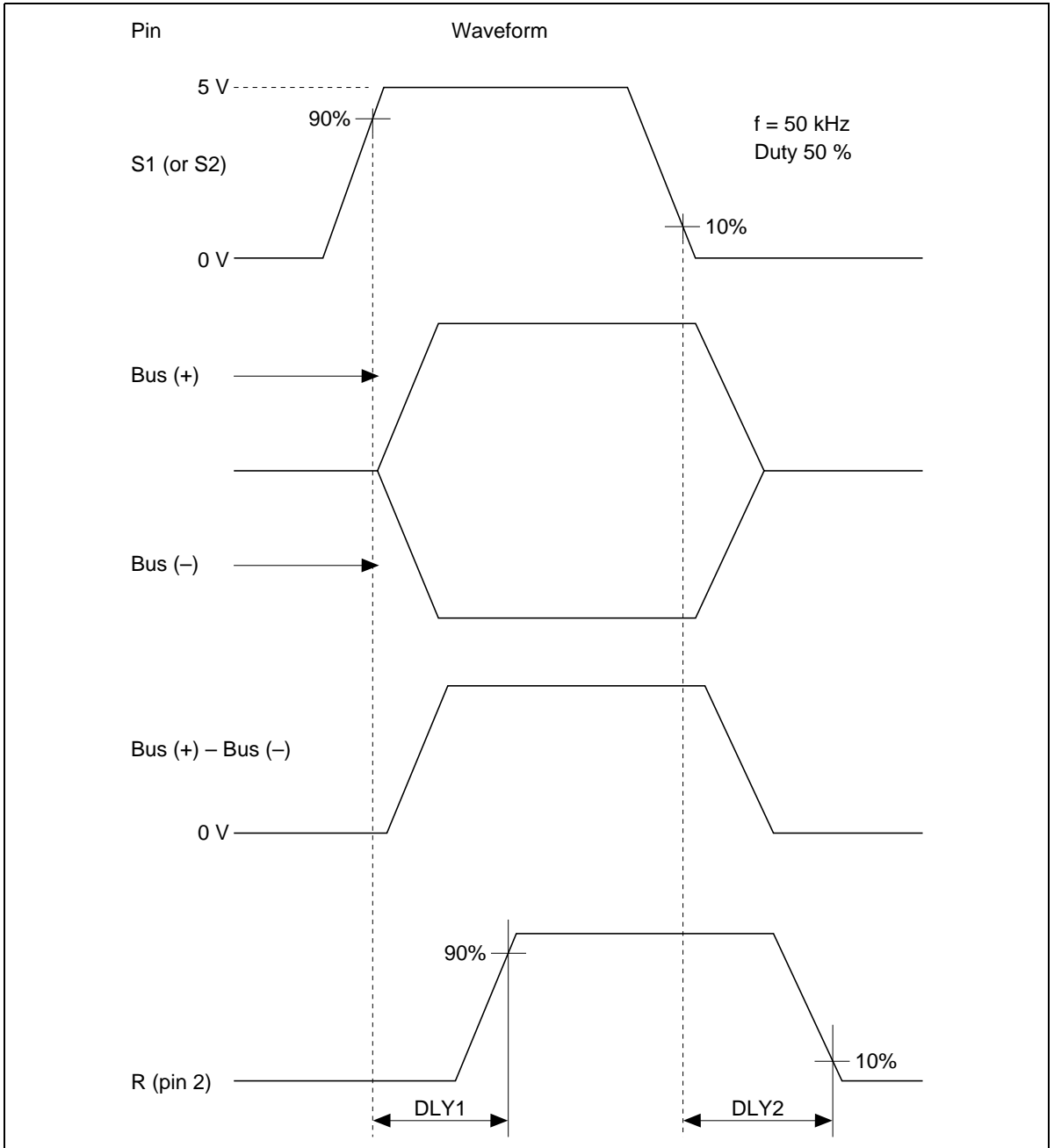


Test Circuit 4

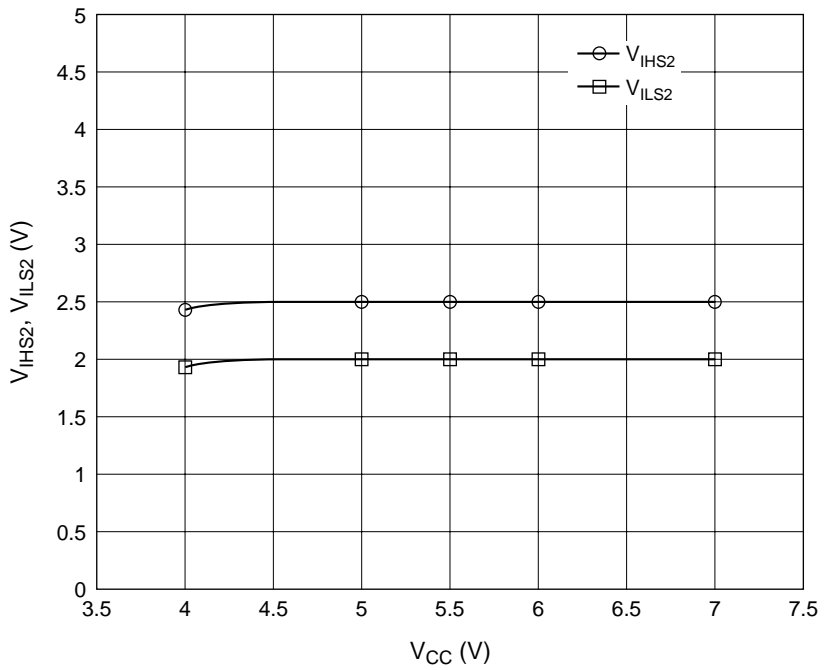
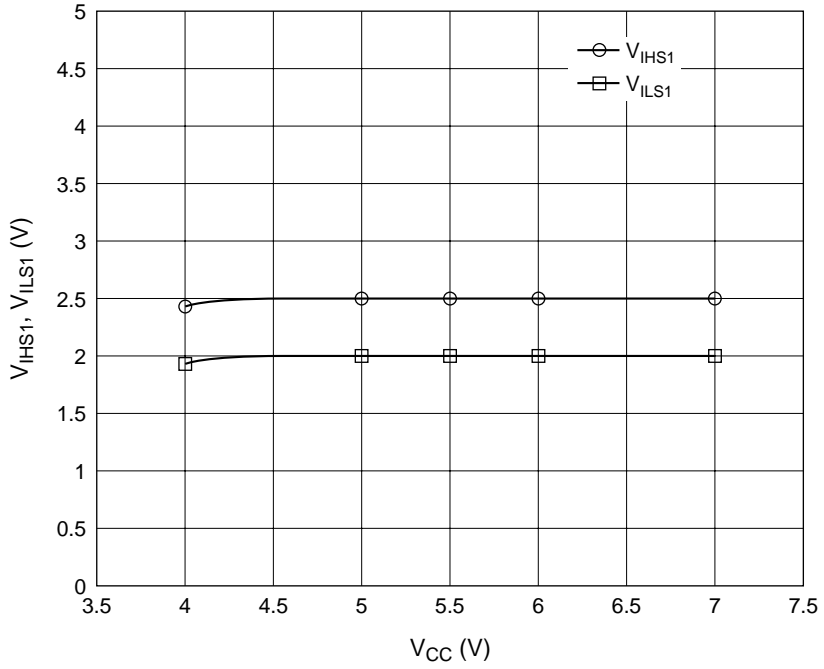


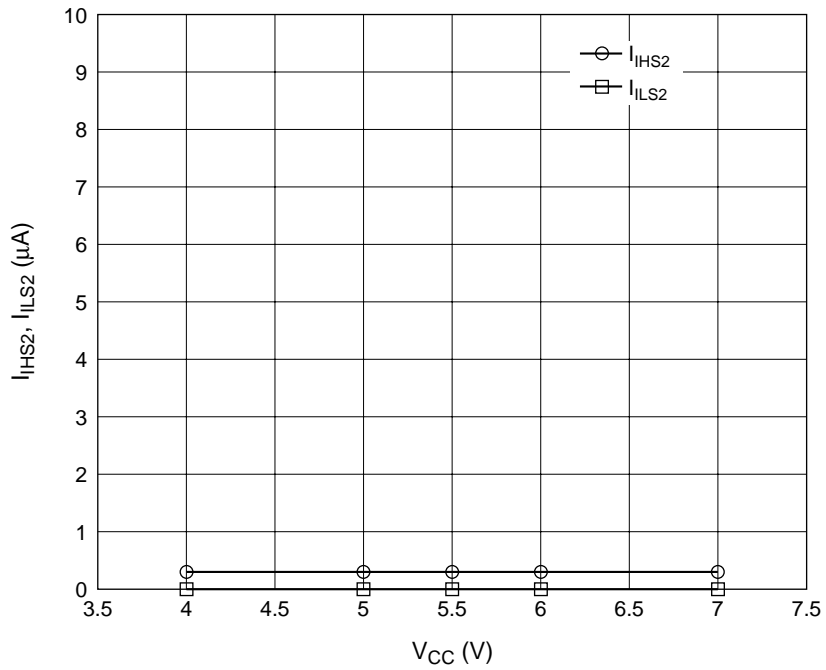
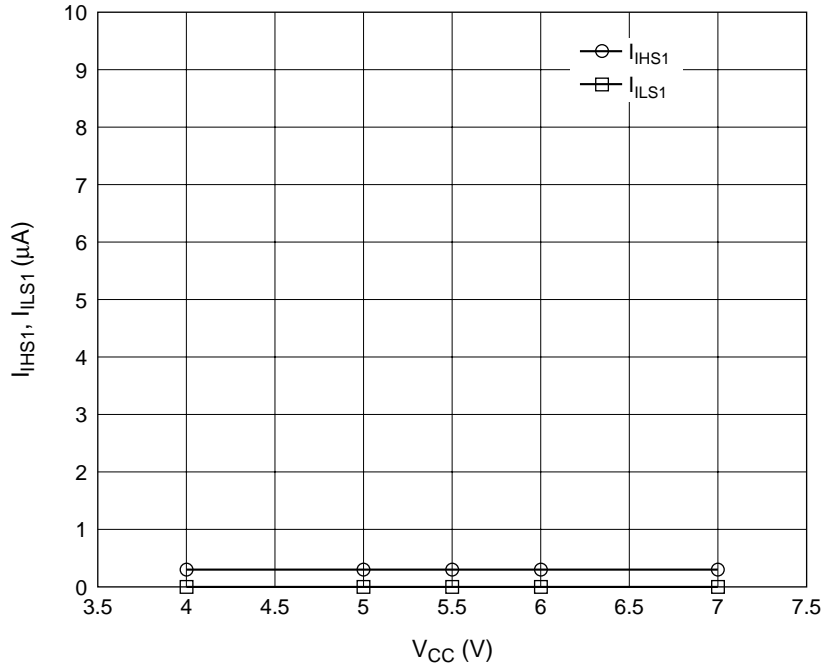
Test Circuit 5

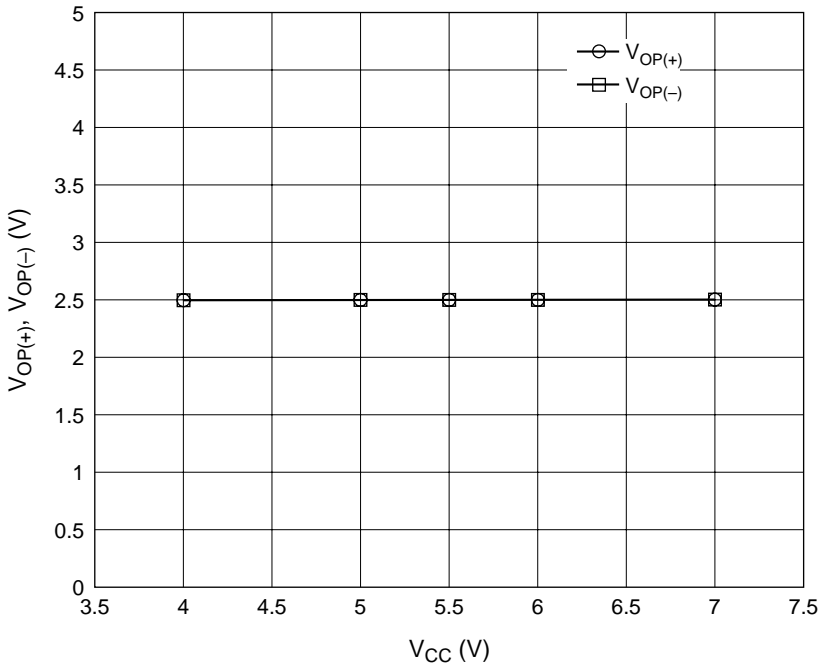
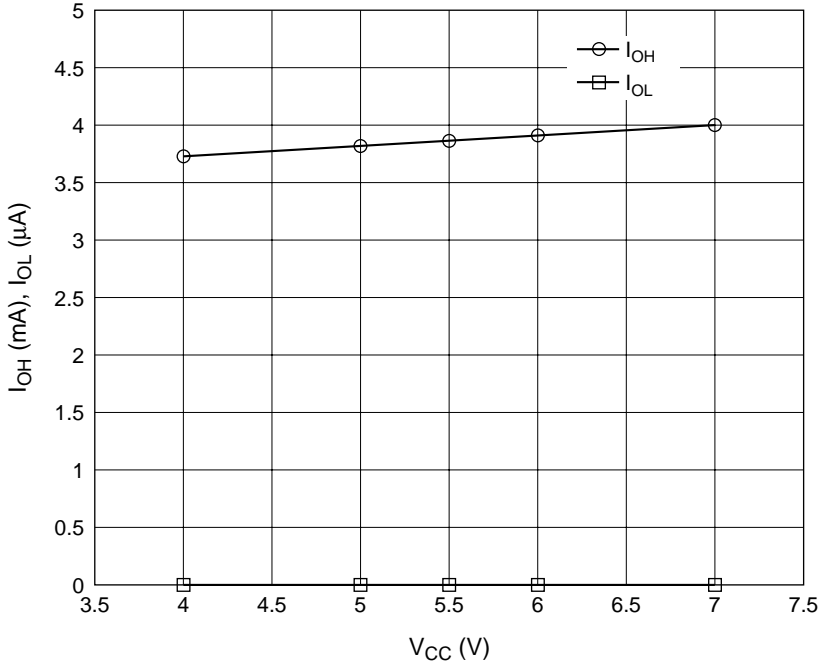
Operating Waveforms

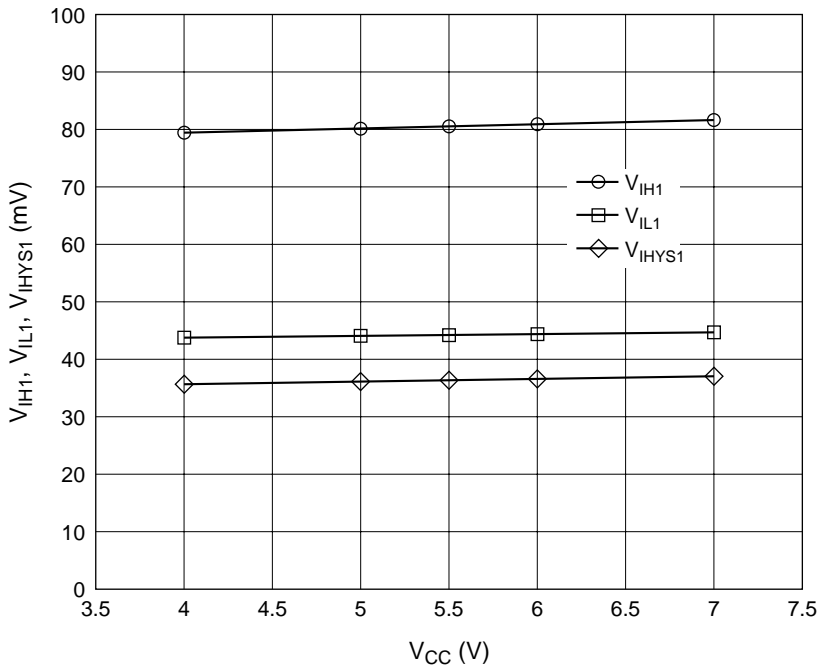
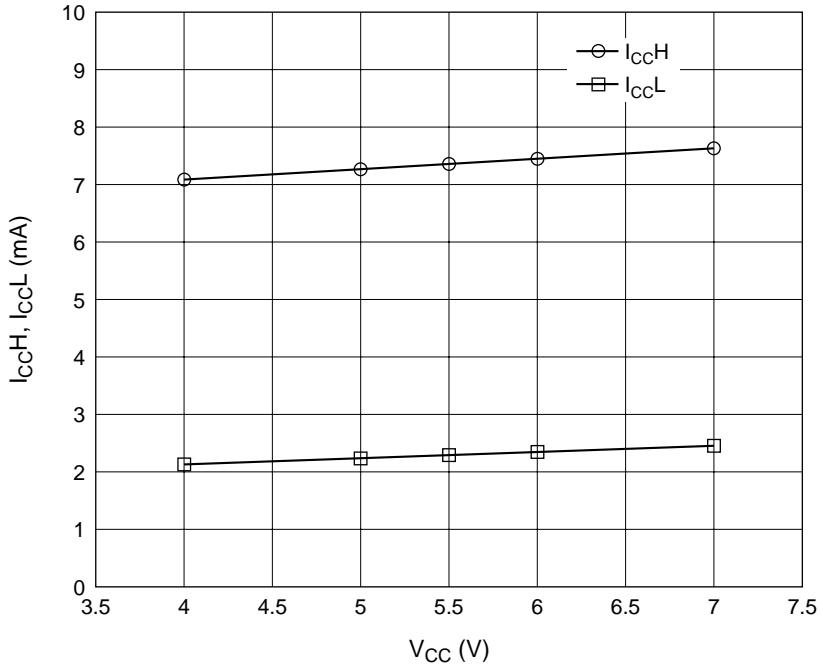


Main Characteristics

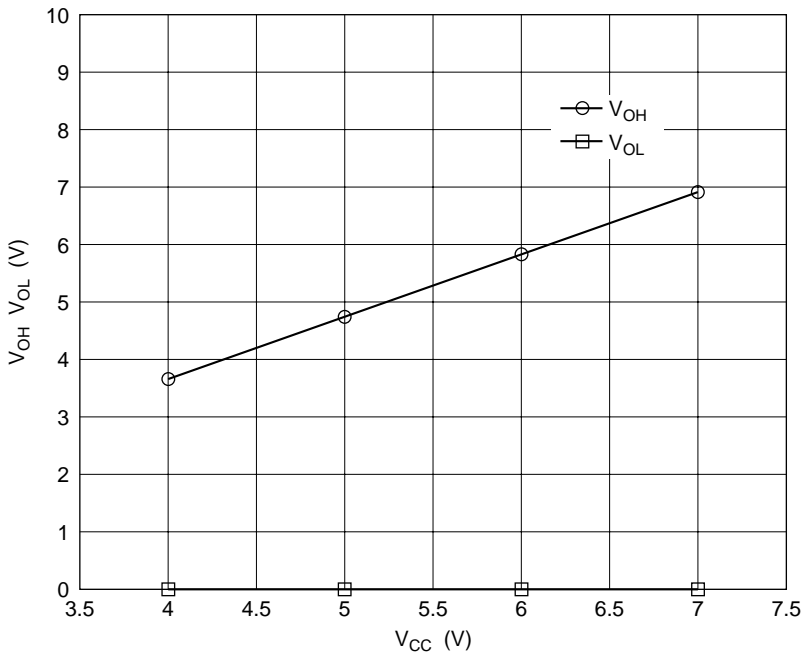
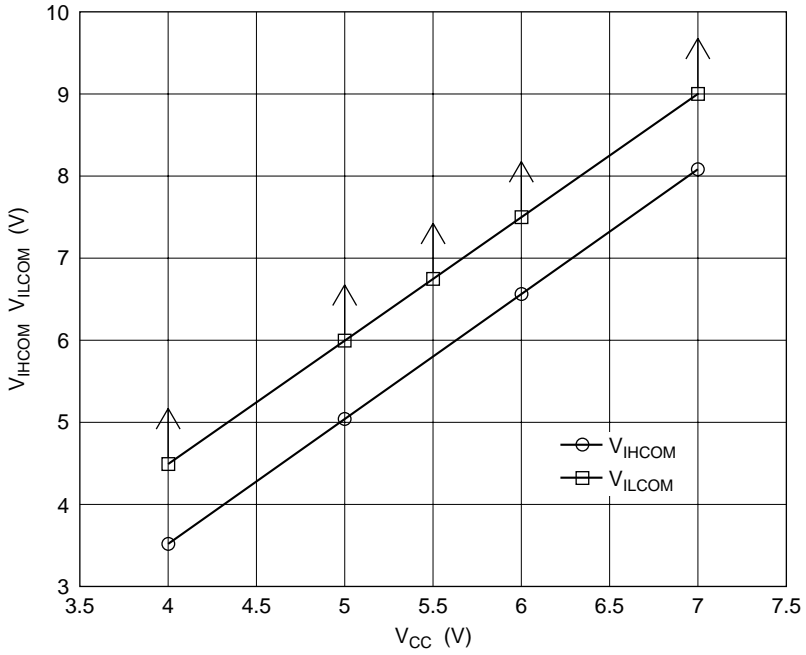


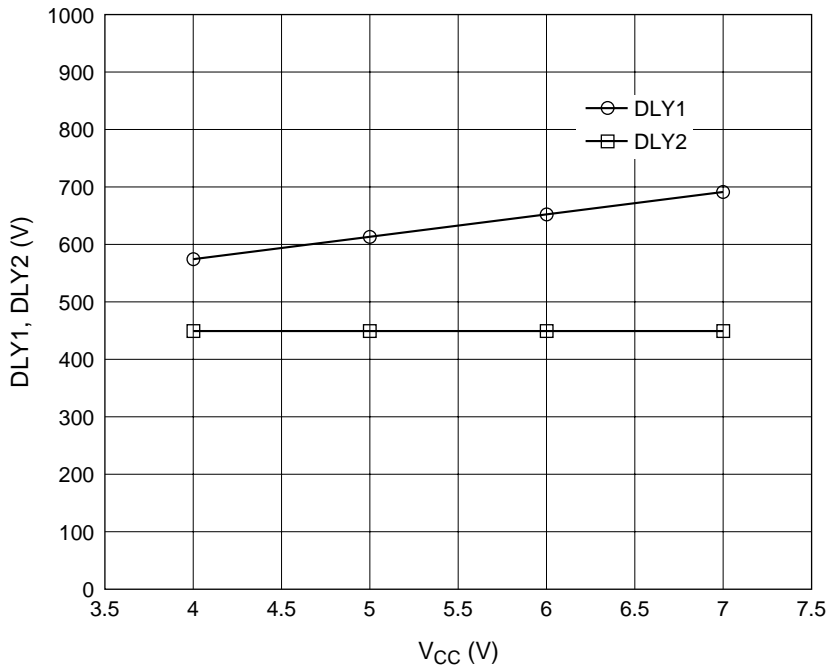
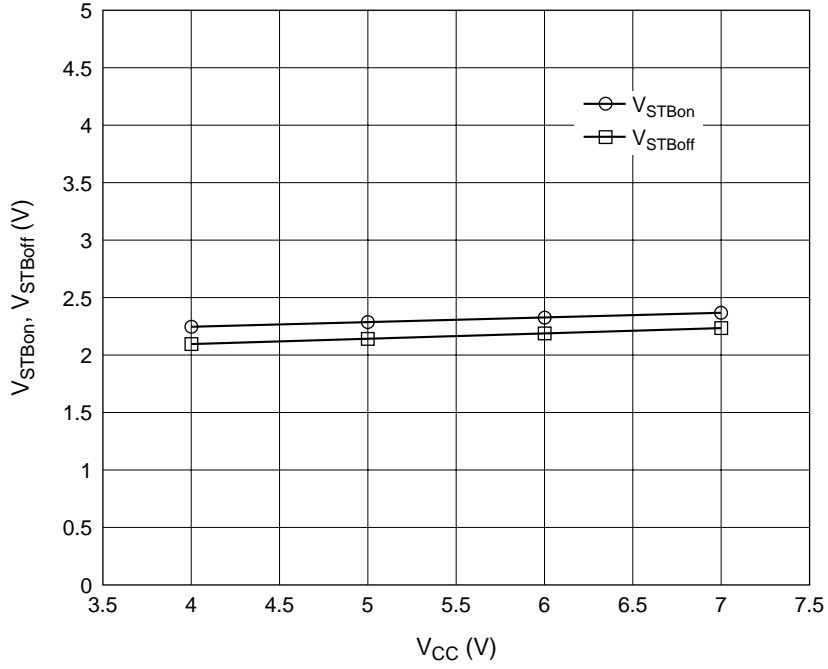


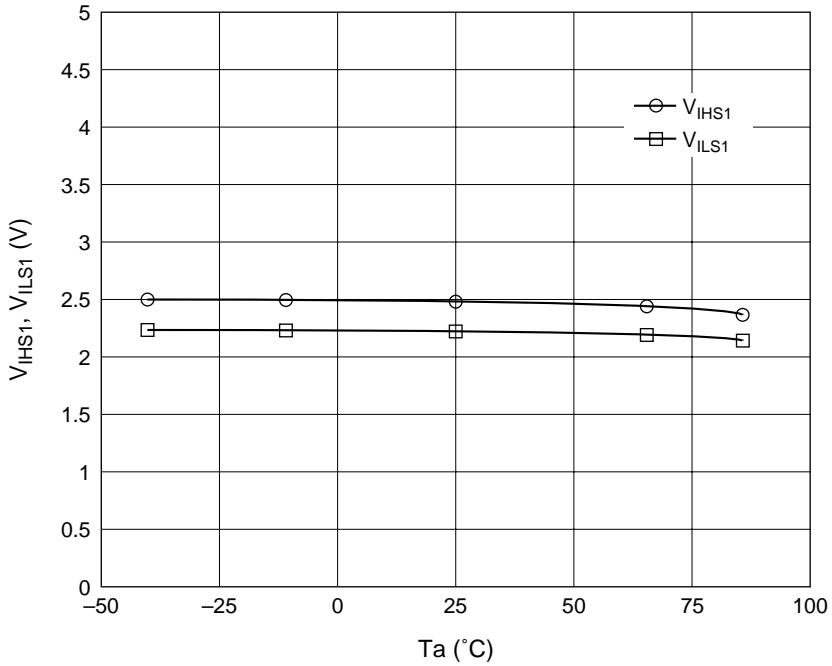
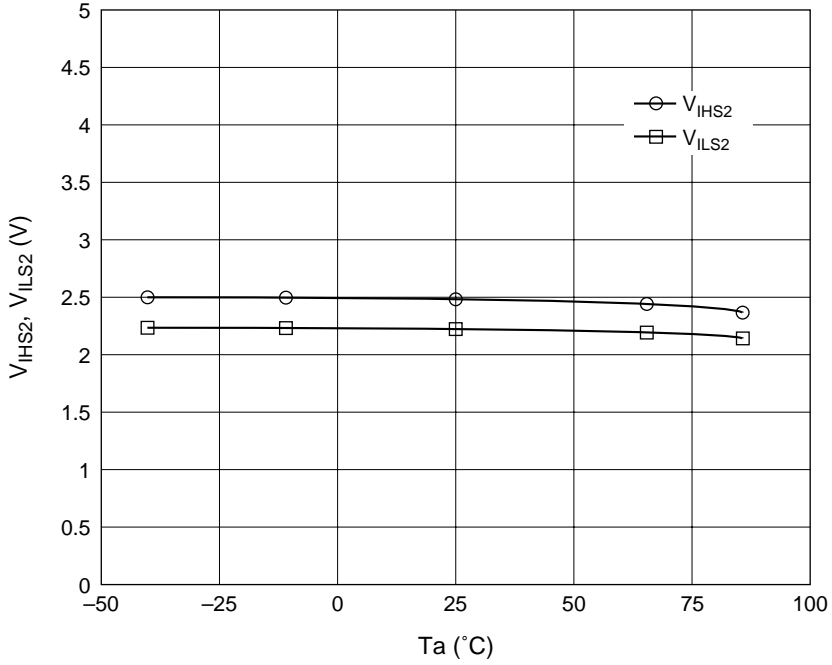


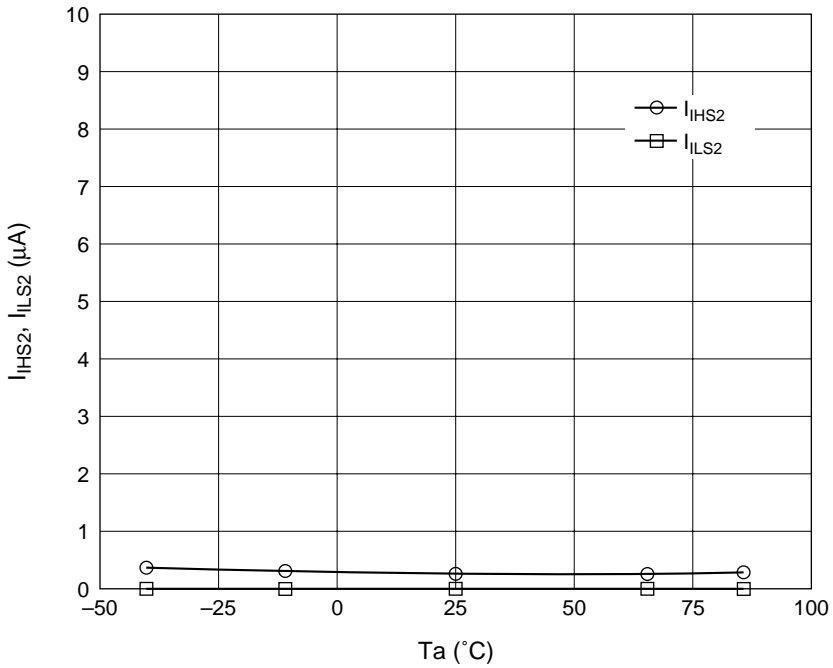
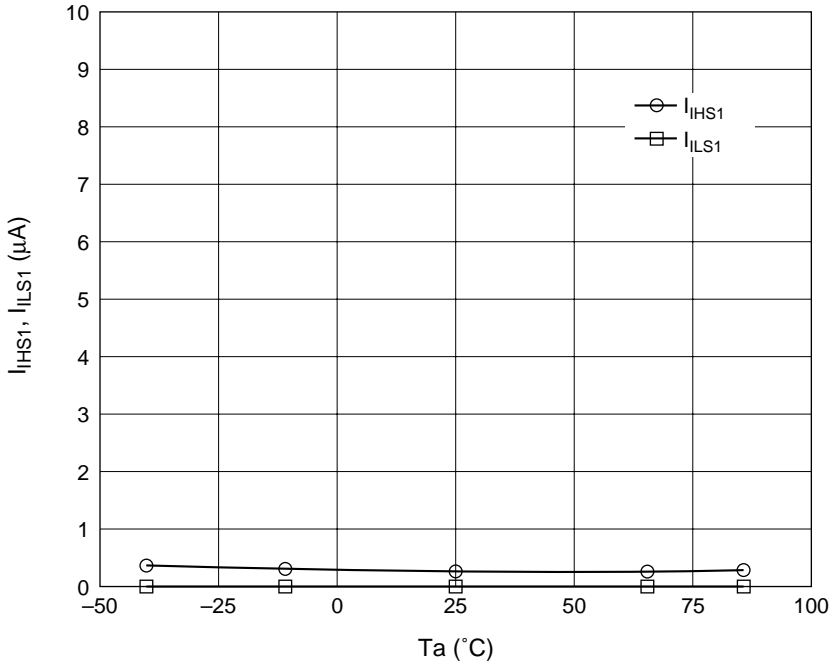


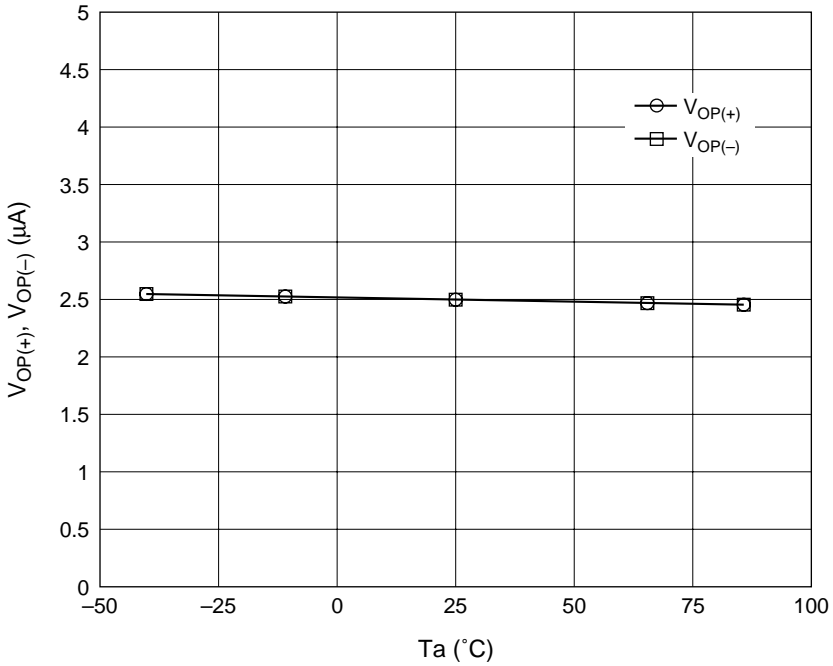
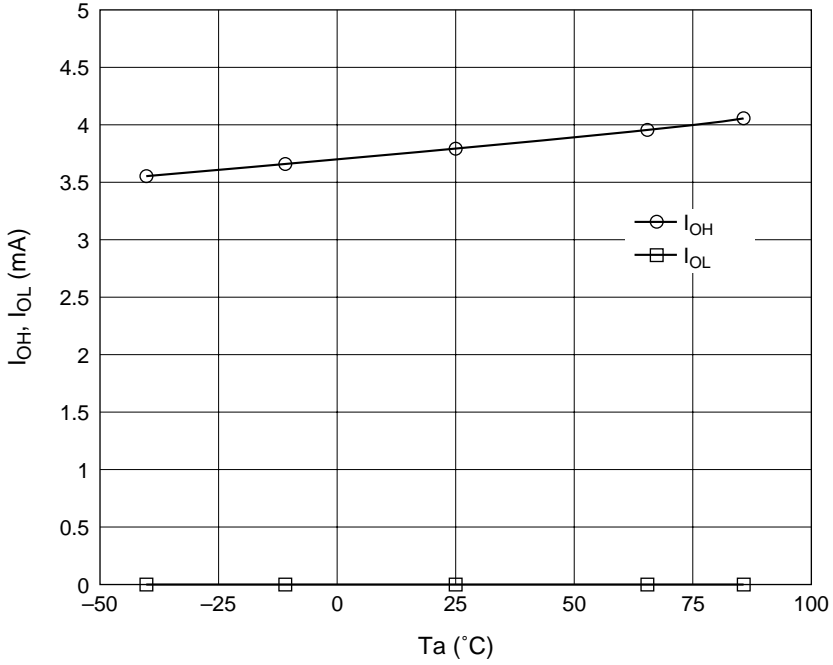
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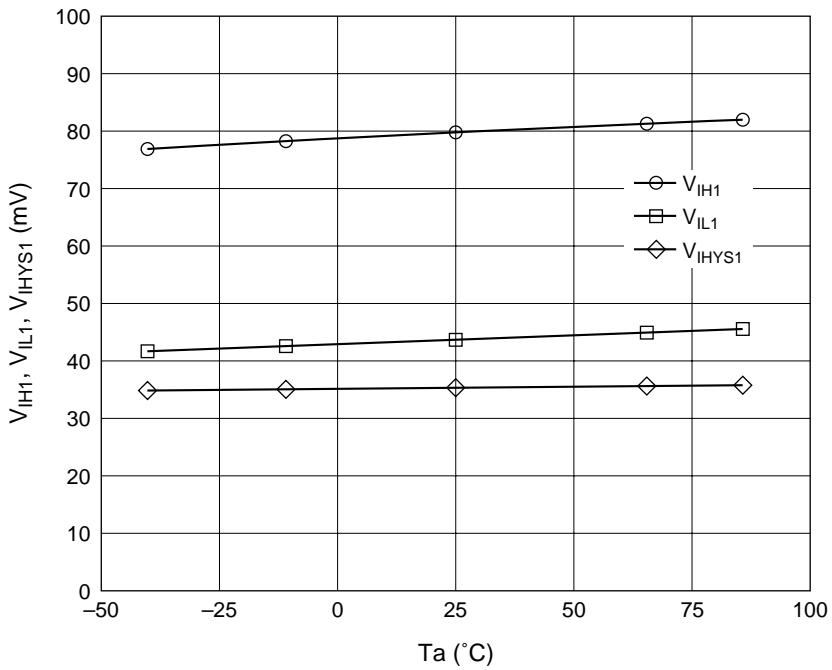
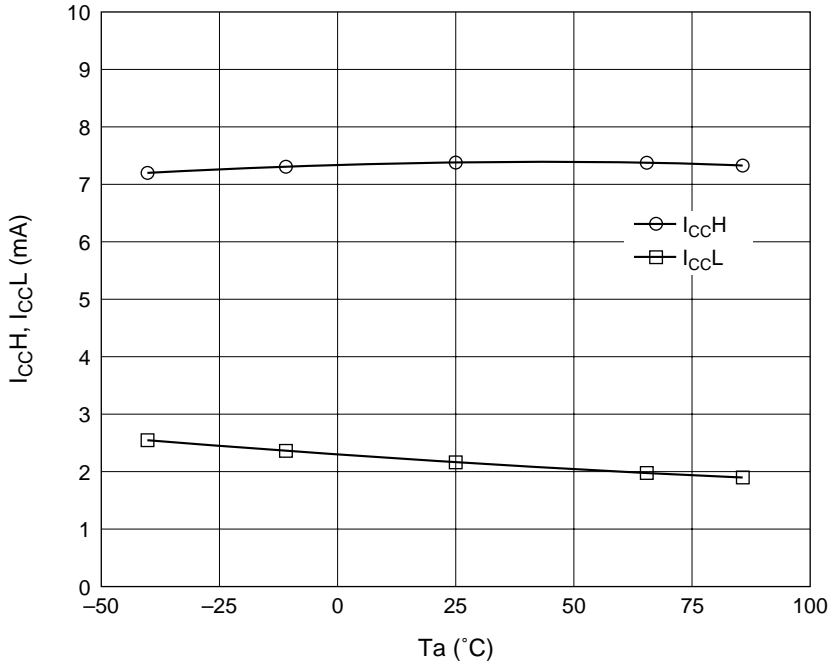




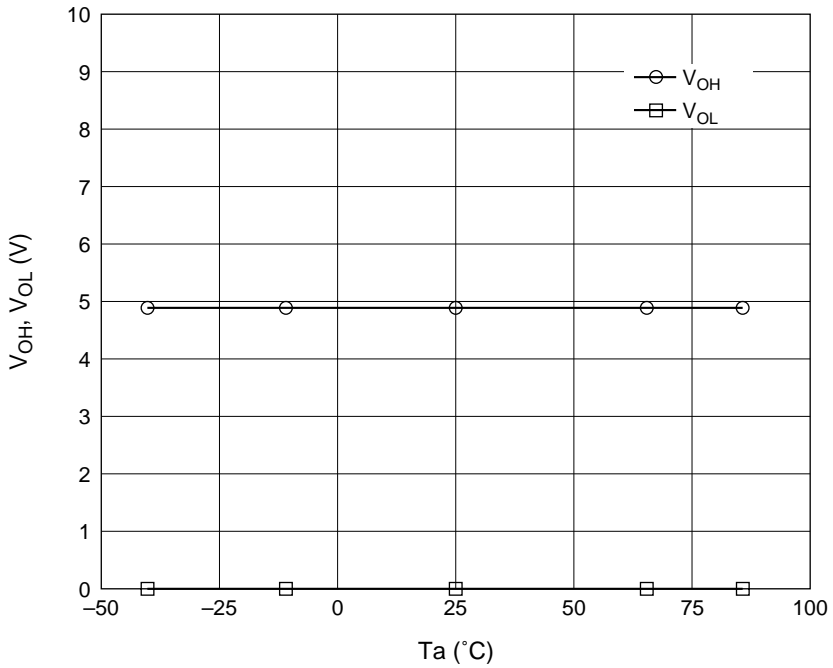
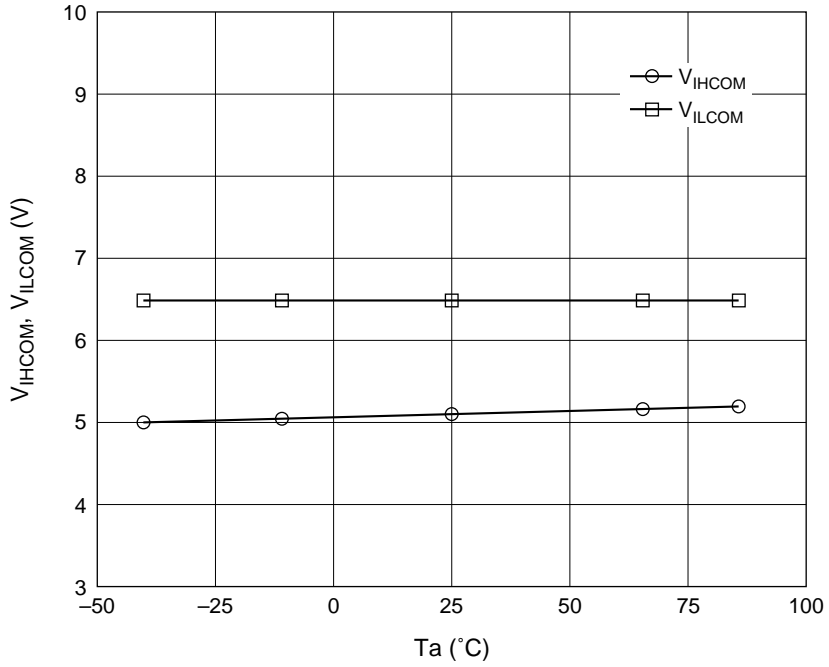


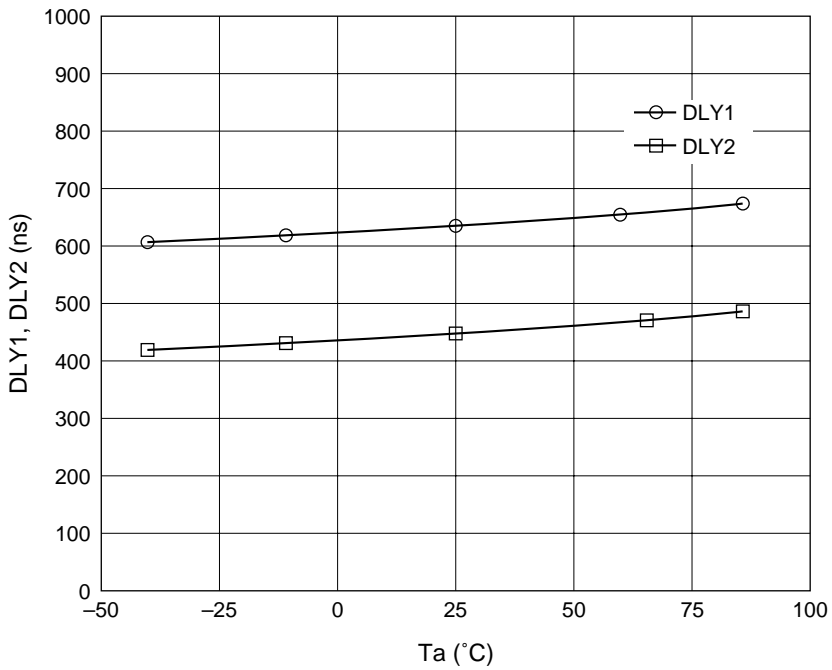
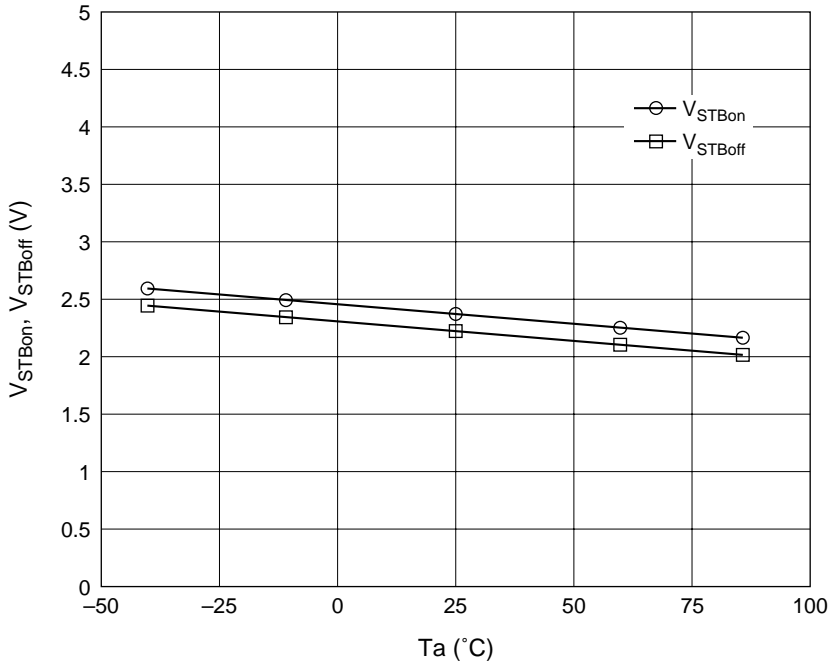






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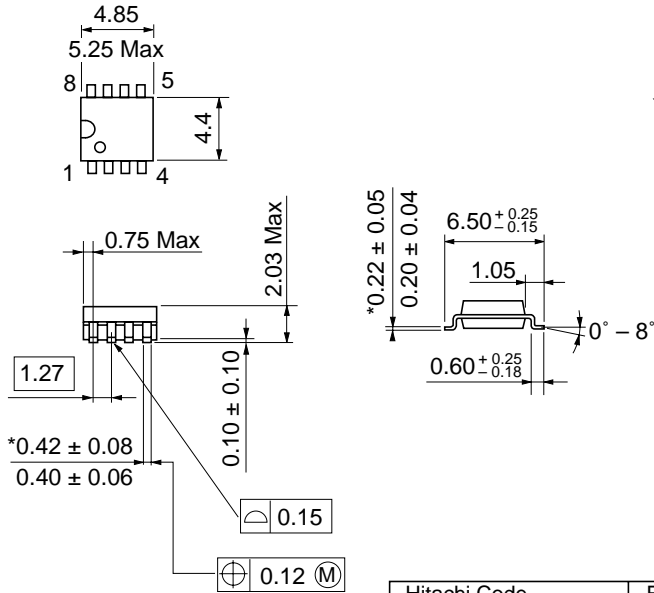




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Package Dimensions

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8D
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.10 g

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