PDP TELEVISION

SERVICE MANUAL

Chassis NO. PS08

Model No. PT4216

Please read this manual carefully before service.

CONTENTS

Part Ⅰ:PS08 Chassis Features and Circuit block diagram

1、 PT4216/PT4218 Panel Datas:

PT4216/ PT4218 and PT5016 are all belong to PS08 chassis. The used panel parameter is below:

PDP Panel Resolution	852×3(RGB)×480
Colors	16,777,216
Dot Pitch	1.095mm(H)×1.110mm(V)
Brightness	High brightness
Contrast	High contrast
Lifespan of Panel	20000 Hours
Viewing Angle	U/D：160 / L/R：160
Valid display area	933mm（H）×533mm(V)

Remarks: Brightness and contrast may vary because of different panels being used. PT4216 mainly uses LG PDP42V7 panel model or Panasonic MD42M7、MD42M8 panel model .

2、Main Features:

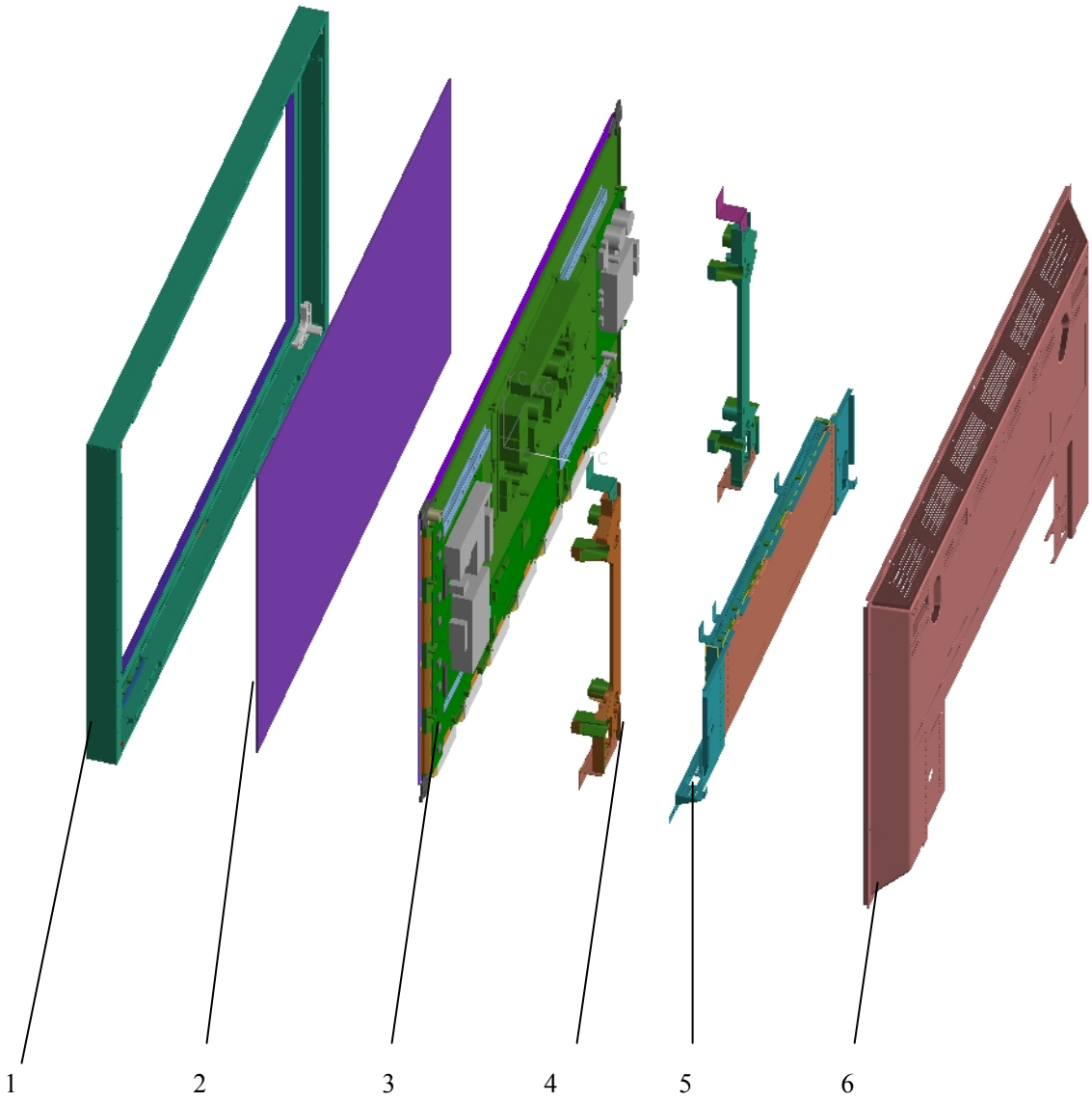
- Radio Frequency input; support CATV
  Capable to receive the full CATV programs.
- PIP function
- DVI digital RGB input
- VGA analog RGB input
- High definition YPbPr input
- AV input
  Capable to receive NTSC/PAL/SECAM AV signal. Convenient to watch VCR,DVR,DVD programs. Make you into perfect AV world.
- AV audio and video output
  Capable to output one way video, left and right audio signal each one.
- Y/C component video input
  S-video input, convenient to connect Y/C video input from DVD output.
- 236 programs preset
  In TV condition, capable to save 236 programs. Ready for future rich programs.
- Multi format
  Capable to receive NTSC/PAL/SECAM TV signal. Capable to receive D/K,I,B/G,M audio format TV signal.
- On/off on time
  Set PDP TV on or off at preset time.
- Blue background mute noise
  In TV, AV (S-Video), YCbCr, and YPbPr modes, screen displays gentle blue background if there is no signal input and into mute condition.
- Auto Off if no signal input
  In TV mode, the PDP TV will automatically power off within 15 minutes and enter into standby condition.
- Chinese/English menu
  Ordinary and graphical user interface makes the menu operation more convenient and intuitionistic
- Power Energy Saving Mode (power management mode)
  In PC mode, the PDD TV will automatically power off within 30 seconds and enter into the Power Energy Saving Mode if there is no signal input. It will automatically exit from the Power Energy Saving Mode and work again when it received a valid signal or press any button on the panel/remote control.
- Plug and Play
  It is no need to equip any installation software when the product is used as computer terminal display equipment. It

is real plug and play.

- Little weight, small dimension, low power consumption

3、CBU Content

3.1 PDP Inside Drawing:

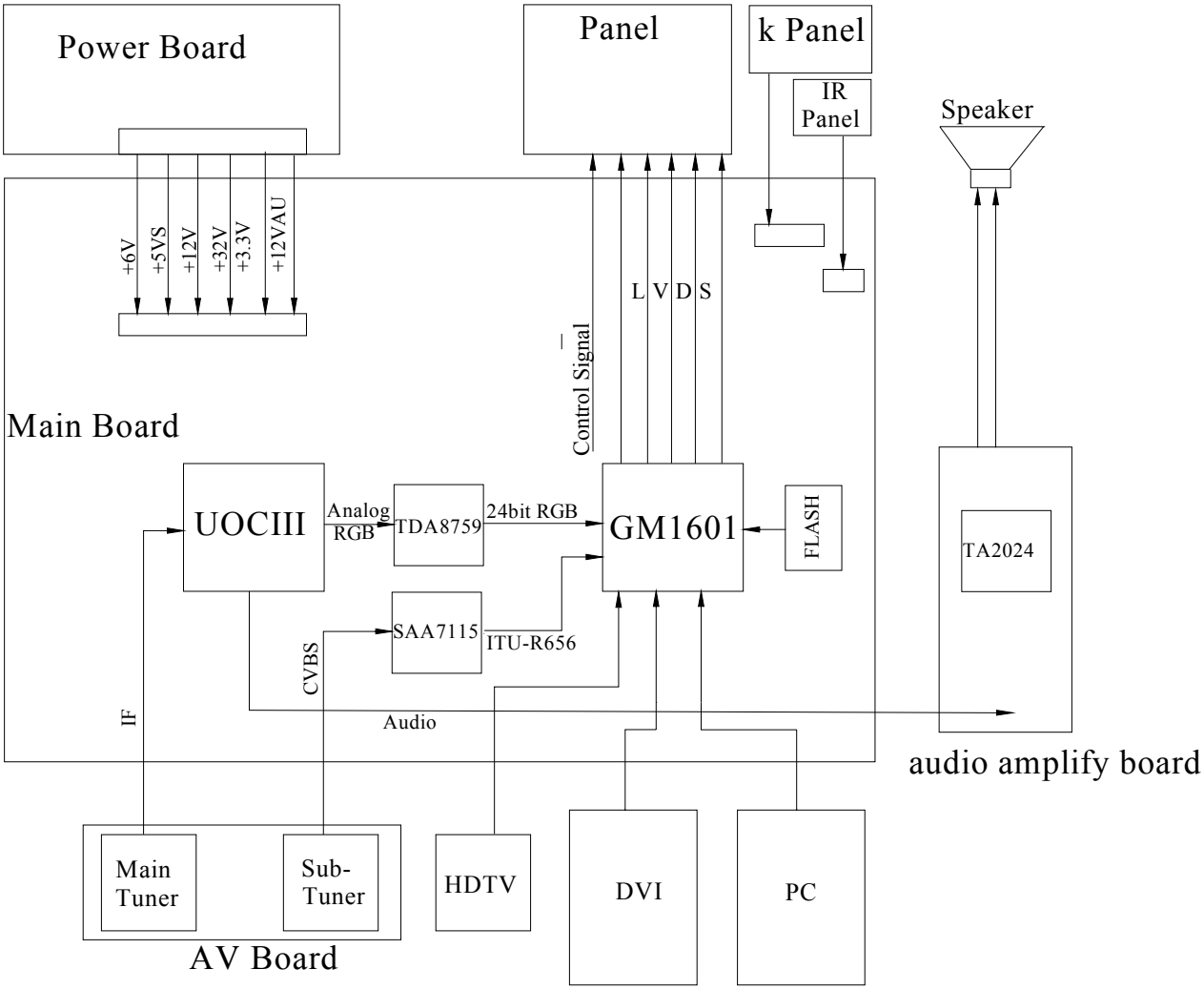


No.	Name
①	Front Cabinet
②	Filter Glass
③	PDP Panel Module
④	Shelve Bar
⑤	Down Cover Module etc.
⑥	Back Cabinet

Remarks: This drawing is for references only, please see the main assembly diagram and wire-connecting diagram for details.

3.2 Circuit block diagram:

PS08 chassis PDPD TV is mainly composed of regulator circuit、RF circuit、video processor circuit、Power Amplify circuit、Analog Video circuit、System Control circuit and Key Control circuit, block diagram of unit circuit is below:



3.3 PCB assembly introduction

It is mainly composed of AV Board、Remote Control Receiving board 、K Board 、power board、power amplifier board and Main Board. Herein introduct function of each PCB module:

Number	Parts	Description
1	Main Board assembly	It is the core of signal processing for PDP TV, which takes responsibility of transforming outer signal into the uniform digital signal identified by PDP display with control of System circuit. TV, AV and S-video signals input from AV Board are decoded by UOCIII to output RGB signal ,A/D converted by TDA8759,output 24bit RGB digital signal, then it is processed by GM1601/GM1501 to accomplish format convert, produce LVDS signal displayed on the screen. In addition, signals input from VGA、DVI would directly enter into GM1501 to process 、format convert and on screen display.
2	AV Board assembly	It is mainly composed of two tuners (main and sub tuners) 、earphone output and some peripheral processing circuit. The main tuner demodulates RF signal to IF signal, and the sub tuner produces CVBS signal, all signals are sent to the main board to do corresponding process after transfer .Earphone jack can connect earphone output directly, and output volume can be adjusted.

3	Remote Control Receiving assembly	It is composed of one indicator lamp, buzzer and one remote control receiving head, which enable Users operate the TV conveniently and know its current working status simply with a remote control box. Indicator lamp indicates unit on/off status and buzz prompts validity of key operation.
4	Built-in Power Board assembly	It can transform AC 220V into multiple DC power, including +12VAU(audio power amplifier)，+12V，+A6V，+D6V，+D3.3V，+34V and +5VS standby power supply .
5	K Board module	It consists of 7 inductive buttons by which users can operate the TV freely.
6	Power amplifier board assembly	Audio adopts two channel T-class digital audio power amplifier IC. Left and right channel output 2X5W.
7	Screen assembly	PDP panel is used to display image signal processed by main board.
8	Transfer board assembly(only used LG panel)	Transform each kind of DC voltage from panel(+9V、 +12V、24V) into each kind of DC voltage used by main board（+3.3、+D6V、A6V、+34V、+12V、+12VAU）.

Part Ⅱ:Introduction on main components functions of PT4216

1、PT4216 main components and function

NO.	NAME	TYPE	Function
AV board assembly			
1	UT921	TMI4-C22P2RW	Output sub-picture CVBS signal
2	UT920	TAD5-C2IP1RW	Output sound and video IF signal
Main board assembly			
3	U901	PIC16F505	Standby control CPU
4	U302，U303	24LC21A T/SN	EEPROM
5	U701	24LC32A T/SN	buffer
6	U306,U307,UA3	FSAV330QSCX	Select switch
7	K201	K7262N	SAW filter
8	K202	K9352N	SAW filter
9	U801	AM29LV800DT-70EC	Flash，save unit control program
10	U700	GM1501-BD	Video processor
11	U201	TDA15063H-N1B06557	Video and audio decoder
12	U402	SAA7115HL/V1	Sub-channel video decoder
13	U305	SM5302AS-G-ET	High definition signal filter
14	U400	TDA8759HV/8/C1	Video signal A/D converter
15	U5	TDA9178T/N1	Video signal picture quality improvement
16	U600	MT46V2M32LG-4	Frame buffer

2、PDP TV PT4216 main components function introduction:

2.1 Main tuner(TAD5-C2IP1RW)

Pin number	Pin definition	Pin function description
1	AGC	Auto gain control
2	UT	Not connect
3	ADD	Ground
4	SCL	IIC bus(clock)
5	SDA	IIC bus(data)
6	NC	Not connect
7	+5V	Power
8	NC	Not connect
9	30V	Form 0~30V tune voltage
10	NC	Not connect
11	IF	Output IF TV signal

2.2 Sub tuner(TMI4-C22P2RW):

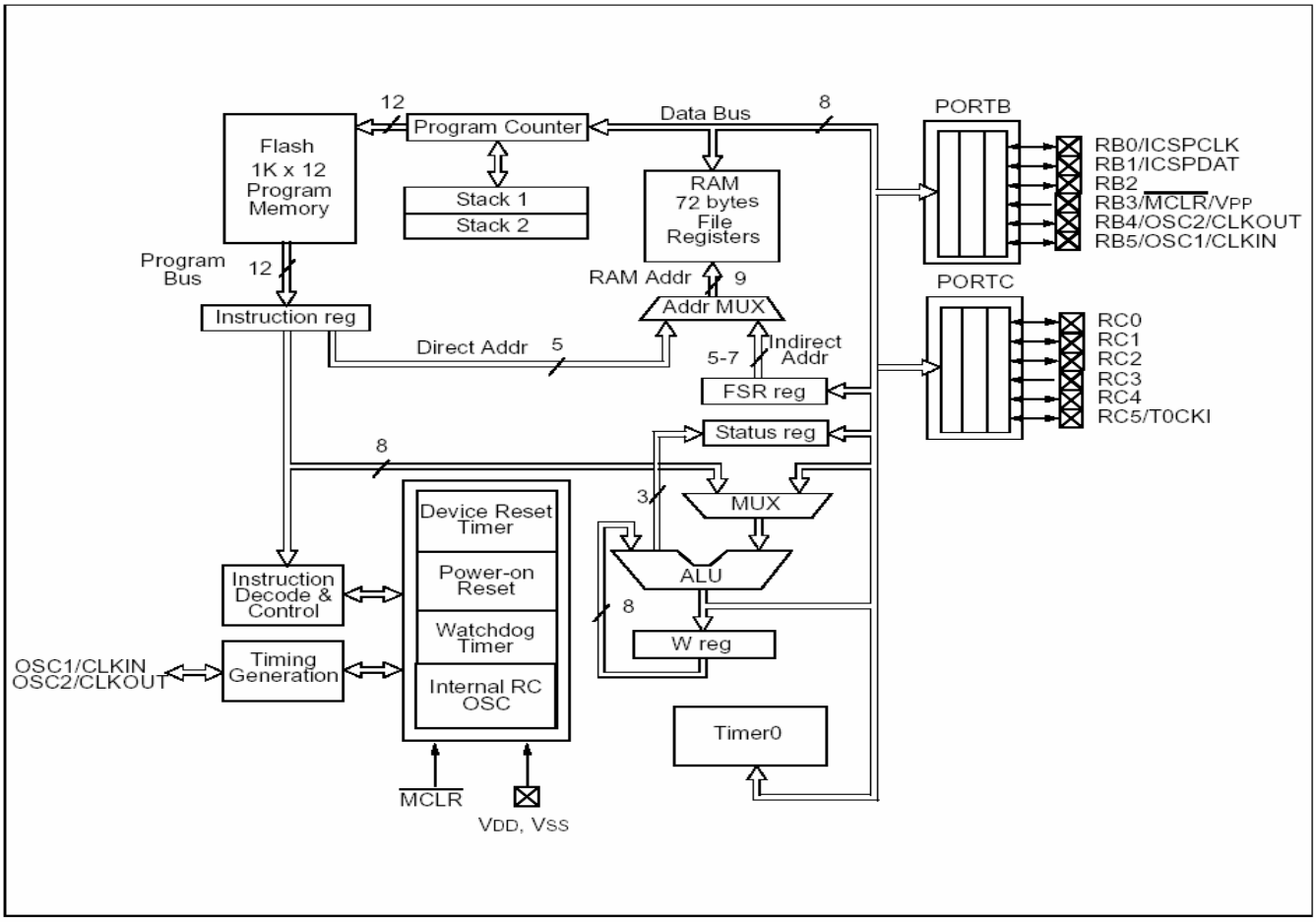
Pin number	Pin definition	Pin function description
1	AGC	Auto gain control
2	NC	Not connect
3	ADD	Ground
4	SCL	IIC bus(clock)
5	SDA	IIC bus(data)
6	NC	Not connect
7	+5V	Power
8	NC	Not connect
9	33V	Form 0~33V tune voltage
10	NC	Not connect
11	IF	IF signal output(not connect)

12	IF	IF signal output(not connect)
13	SW0	Band control
14	SW1	Band control
15	NC	Not connect
16	SIF	Not connect
17	AGC	Auto gain control
18	VEDIO	CVBS signal output
19	+5V	Power
20	AUDIO	Not connect

2.3、Standby control CPU（PIC16F505）

Pin number	Pin definition	Pin function description
1	VDD（+3.3V）	Power
2	RB5/OSC1/CLCKIN	NC
3	RB4/OSC2/CLCKOUT	LED1 KEYPAD STB output, standby indicator lamp control
4	RB3/MCLP/VPP	Input voltage (+5V)when programming or reset input(+5V)
5	RC5	I/O port: POWER OFF1 input, from GM1501 output, inform PIC16F505 to do off operation.
6	RC4	I/O port: ALARM input, turn on on time enable control.
7	RC3	I/O port: PDP-STB output, standby/on control
8	RC2	I/O port: POWER-STANDBY output,GM1501 to inform executing off operation by key button.
9	RC1	I/O port: IRIN remote instruction input
10	RC0	I/O port: POWERKEY input, connect to on/off key of k board directly.
11	RB2	I/O port: connect +3.3V
12	RB1/ICSPCLK	programming use
13	RB0/ICSPDAT	programming use
14	VSS	Ground

FIGURE 3-2: PIC16F505 BLOCK DIAGRAM



2.4 GM1501

GM1501 is a kind of dual channels image and video processing chip, which is mainly used for LCD displays and TV integrated products. With the resolution of WUXGA, it not only supports PIP technology, but also include all IC function of picture snap, process and display clock control. It integrates high speed AD converter, PLL, high reliability DVI receiver , X86 series microprocessor and LVDS converter inside. Its main e feature as below:

- High quality image zoom function
- Analog RGB signal input interface
- Intelligent input signal mode auto identification；
- Integrated high performance PLL output
- High-reliable self-adaptive DVI input interface;
- 4:4:4/4:2:2/CCR656/601 8/16/24bit digital video interface;；
- Embedded adjustment circuit for gain、contrast、brightness、color saturation、hue and skin color;
- technology of reducing EMI power consumption efficiently;
- small angle oblique ripple process;
- High quality video process technology;
- Programmable output format;
- Embedded LVDS transmitter;
- Advanced OSD;
- Embedded micro controller

Pin Description：

Pin	Name	Description

Analog signal input port		
L3	AVSYNC	ADC vertical synchronization signal input
L4	AHSYNC	ADC horizontal synchronization signal input
N2	VGA-SCL	VGA lock input
N1	VGA-SDA	VGA digital input
D1、D2	RED+、RED-	Red analog signal input
C3	SOG	Green pedestal synchronization signal
C1、C2	GREEN+、-	Green analog signal input
B1、B2	BLUE+、BLUE-	Blue analog signal input
A2,B3,E3,D3	ADC3.3	ADC3.3Vpower supply
A3，A4	ADC1.8	ADC1.8Vpower supply
A5，B4	ADC-DGND	ADC digital ground
C4，D4，E1，E2，E4	ADC-AGND	ADC analog ground
DVI import port		
N4	DVI-SCL	DDC interface , serial clock signal
N3	DVI-SDA	DDC interface ， serial data signal
A6，B6	RXC+，RXC-	DVI clock input signal
A8～A10 B8～B10	RX0+～RX2+ RX0-～RX2-	DVI input port
B11	REXT	External interrupt resistance
C6～C11	DVI-3.3	DVI 3.3V power supply
D6、D8～D10	DVI-1.8	DVI 1.8V power supply
A7,A11,B5,B7,C7,D7 D11	DVI-GND	DVI ground
Low bandwidth ADC port		
C13	LBADC-33	ADC3.3Vpower supply
A12，B12，C12	LBADC_IN1～ LBADC_IN3	ADC analog input channel
D12	LBADC_RETURN	Channel analog ground
D13	LBADC-GND	Power supply voltage analog ground
OCM bus port		
AA1~AA3,Y1~Y3, W1~W3,V1~V4, U1~U4,T1~T3	OCMADDR0～ OCMADDR19	Address input output port
AB1~AB3,AC1~AC3, AD1~AD4,AE1~AE3, AF1~AF3	OCMDATA0~ OCMDATA15	Data input output port
OCM port control signal		
R1，T4，P1，P2	ROM_CSn~ ROM_CS2n	chip selection signal
R2	OCM_REn	Read enable signal
R3	OCM_WEn	Write enable signal
L1 L2	OCM_INT2 OCM_INT1	Interrupt
M1	OCM_UDO	OCM data output
M2	OCM_UDI	OCM data input
D25	OCM_TIMER1	OCM timer input
Standard definition video control port		
D16	SVCLK	SV pixels clock input
C14	SVHSYNC	SV horizon synchronization signal input
B14	SVVSYNC	SV vertical synchronization signal input
A14	SVODD	Scan status input
A17	SVDV	SV data input
Standard definition video data port		
D14,D15,A15,A16, B15,B16,C15,C16	SVDATA7~ SVDATA0	SV ITU656 data input

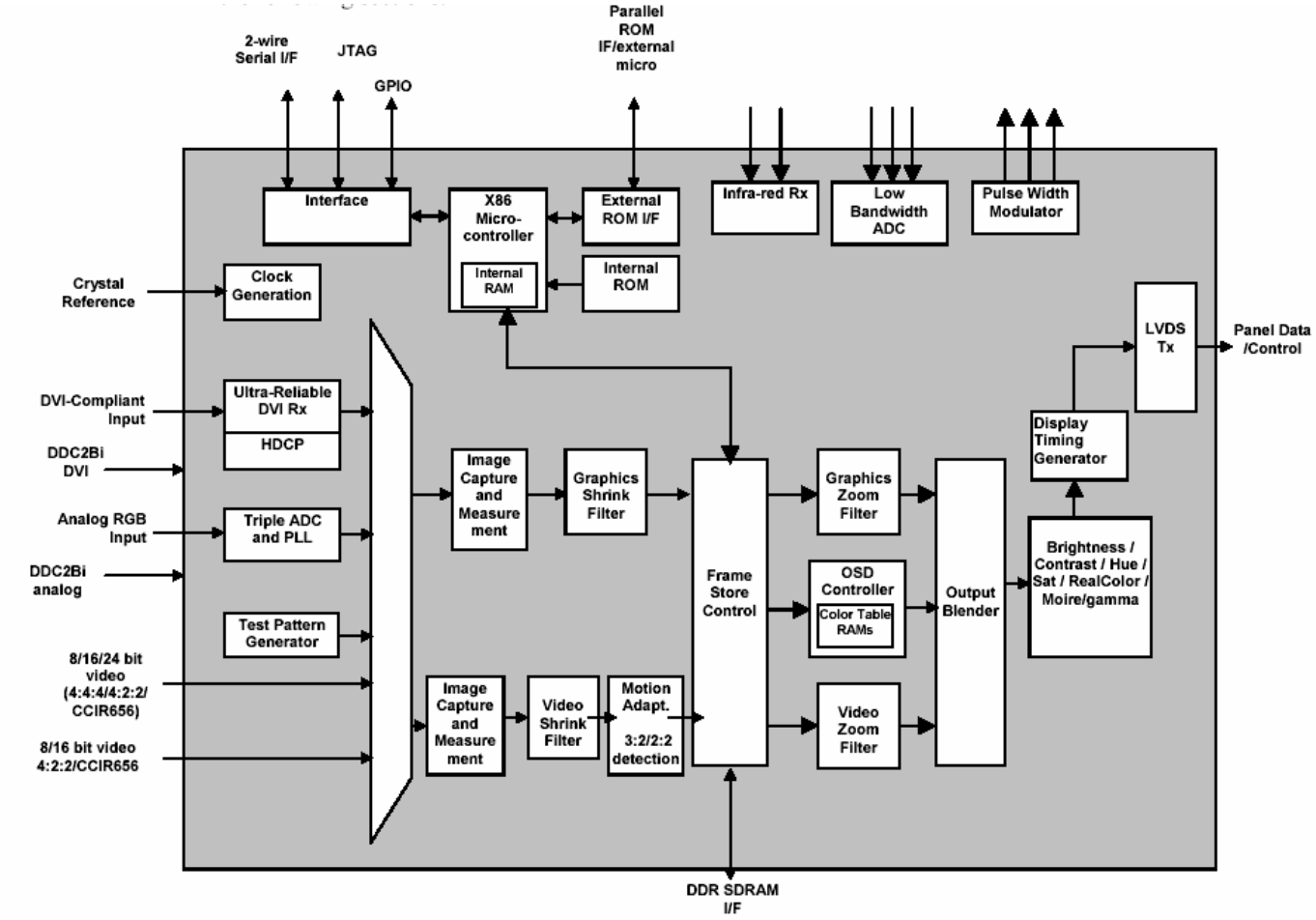
Video Control Port		
A20	VCLK	Video pixels clock signal
D19	VHS_CSYNC	Video horizonl synchronization signal input
C20	VVS	Video vertical synchronization signal input
B20	VODD	Scan status input
D20	VDV (VSOG)	Video data input
B17	VCLAMP	Video clamp enable output
A21,A22,A23,B21, B22,C21,C22,D21	VGRN7~ VGRN0	Green pedestal signal or Y signal input
C17,C18,C19,A18 A19,B18,B19,D18	VRED7~ VRED0	Red pedestal signal or V/Cr/Pr signal input
B23,B24,B25,A24 A25,C23,C24,D24	VBLU7~ VBLU0	Blue pedestal signal or U/Cb/Pb signal input
Screen Control Port		
A26	PPWR	Screen power control
B26	PBIAS	Screen bias control
D26，C25，C26	PWM2 ~PWM0	Pulse width modulation output
AC7	DCLK	Pixels clock output
AC16	OEXTR	Connect external LVDS bias resistance
LVDS Port		
AE14~AE16,AE19~ AE23,AF13~AF16 AF19~AF23,AF11	A0-~A3-, A0+~A3+ B0-~B3-, B0+~B3+	Low voltage difference data input
AD14,AD11,AE13 AE11,AC11,AF10	LVDS_SHIELD[5] ~ LVDS_SHIELD[0]	Low voltage difference protect output
AE12,AF12, AF20,AE20	AC+,AC-,BC+,BC-	Low voltage difference protect input
Screen Port Power Supply		
AD12,AD13,AC12	LVDSB_3.3	LVDS B channel power supply
AC13,AC14,AC15	LVDSB_GND	B channel ground
AC20,AC21,AC22	LVDSA_3.3	LVDS A channel power supply
AD19,AC19,AC20	LVDSA_GND	A channel ground
AE17	VDDD33_LVDS	Analog power supply
AD17	VSSD33_LVDS	Analog ground
Clock Composite and Power Supply		
G4	XTAL	Crystal oscillator interface
F2	VDDD33_PLL，	Digital power supply
H1	VDDD33_SDDS	
J1	VDDD33_DDDS	
G2	VSSD33_PLL	Digital ground
J4	VSSD33_SDDS	
K4	VSSD33_DDDS	
F4	VDDA33_RPLL	Analog power supply
G1	VDDA33_FPLL	
H3	VDDA33_SDDS	
J3	VDDA33_DDDS	
F3	VSSA33_RPLL	Analog ground
H4	VSSA33_FPLL	
H2	VSSA33_DDDS	
J2	VSSA33_DDDS	
G3	TCLK	Reference clock signal input
K2	ACS_RSET_HD	External resistance terminal
System Signal		

K1	RESETn	Reset signal
M3，M4	IR0，IR1	
P4	MSTR_SCL	Master clock output signal
P3	MSTR_SDA	Master data output/input signal
R4	EXTCLK	External clock input

Frame memory interface

U24,U23	FSCLKp,FSCLKn	Differential store clock output
V24,V25	FSRAS,FSCAS	Address output
V26	FSWE	Write enable terminal
W26	FSCKE	Read enable terminal
J24	FSVREF	Reference voltage input
K26	FSVREFVSS	Reference voltage ground
W25	FSVREF	Reference voltage input
W24	FSVREFVSS	Reference voltage ground
L26	FSDQS	Data filter
F24~F26,G23~G26 H24~H26,J25,J26, R24~R26,P24~P26 N23~N26,…….	FSDATA31~ FSDATA0	Data input output port
T24,T25,U25,U26	FSDQM3~ FSDQM0	Data output mark
Y26 Y25	FSBKSEL1， FSBKSEL0	Layer select address
AA24~AA26 AB24~AB26, AC24~AC26 AD24~AD26	FSADDR11~ FSADDR0	Row and column address output
E23, F23, H23, J23, L23,M23,P23, R23, T23,V23,W23,Y23, AA23,AB23,AC23	FS_2.5	2.5V power supply
K23	VDDA18_DLL	1.8V power supply
K25	VSSA18_DLL	Power supply ground
Digital power		
K10,K11,K16,K17, L11,L16,T11,T16, T17,U10,U11,U16,U17	CORE_1.8	1.8V power supply
D23, W4,Y4, AA4, AB4,AC4,AC6,D17, D22,AC8,AC10	IO_3.3	3.3V power supply
K12,K13,K14,K15, L10,L12,L13,L14, L15,L17,M10,M11, M12,M13。。。。。。	D_GND	Power ground
A1，AC，D5，AC17， K3，F1	NO_CONNECT	NC

GM1501internal block Diagram：

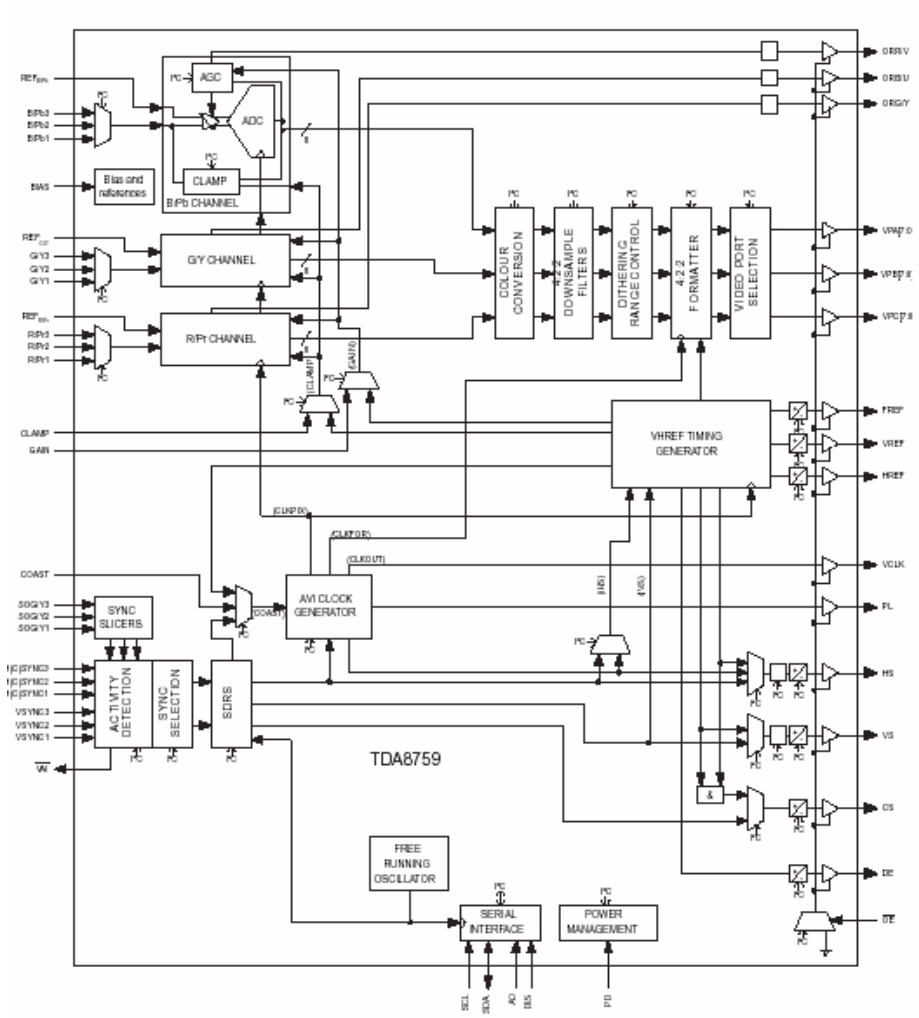


2.5． Brief Introduction of TDA8759：

TDA8759 is a triple 8-bit video converter interface. Sample rate is up to 81 Mbps .The IC can convert analog RGB signal into a 24bit RGB digital signal o, or converts analog YUV or YCbCr signal into a YUV or RGB digital. The IC supports resolutions from 480i and VGA to HDTV and XGA.

- Triple 8-bit Analog-to-Digital Converter (ADC)
- Three independent I2C selectable analog video sources
- Auto detect to interlace scan video signal
- 1.8Vand 3.3Vsupplies
- Low gain temperature shift
- Output format support RGB 4:4:4, YUV 4:4:4, YUV 4:2:2 ,CCIR 656 or YUV 4:2:2 ；
- I²C bus control
- Programmable clock phase correct circuit inside
- 100 MHz Amplifier bandwidth
- Integrated PLL distribution
- Power-Down mode

TDA8759 internal schematic Diagram：



Pin Description：

Pin	Name	Description
1	HREF	Horizon reference output
2	VCLK	Video clock output
3,13,21,29, 37,45,164	VDDO	Video port output supply voltage
4,14,22,30 38,46,165	OGND	Video port output ground
7，8，9，10， 15，16，17，18	VPA0~VPA7	Video port A
11,116,130,132	VDDC	Power supply port
12,117,159	CGND	Ground
23~28,31,32	VPB0~VPB7	Video port B
35,36,39~44	VPC0~VPC7	Video port C
47,53,57,58,55 60,66,70,71,75 81,83,85,86,	AGND	Analog ground
48,54,59,61,67 69,76,82,85,87,88	VDDA	Power supply port
49	REFB/Pb	Blue/blue-chrominance channel reference input signal
52,51,50	B/Pb1~ B/Pb3	Blue/blue-chrominance channel analog input
56	BIAS	Bias input
62	REFG/Y	Green/luminance reference input

65,64,63	G/Y1~G/Y3	Green/luminance analog input
74,73,72	SOG/Y1~SOG/Y3	Sync on green//luminance input
77	REFR/Pr	Red/red-chrominance channel reference input
80,79,78	R/Pr1~ R/Pr3	Red/red-chrominance channel analog input
89~92,97~101 112,121,122, 124,125,160~163	TST0~TST17	Reserved for test
93	PD	Power-down control input
94	OE	Output enable signal input
96	A0	I²C bus address control signal input
102	COAST	PLL control signal input
103	GAIN	Gain input
104	CLAMP	Clamp input
105~107	VSYNC1~VSYNC3	Vertical synchronization signal input
108~110	H(C)SYNC1~ H(C)SYNC3	Horizon (color)synchronization signal input
111	CKEXT	External clock input
113	TCLK	Reserved for test
114	DIS	I²C bus disable control signal input
118	SDA	I²C bus data input/output
119	SCL	I²C bus clock input
120,126,127,131 133,142,148,	IGND	Input digital ground
123,138,139,145 151,157	VDDI	Input digital supply voltage
166	PL	PLL disable signal output
167	DE	Data enable output
168	HS	Horizon synchronization signal input
169	VS	vertical synchronization signal input
170	CS	Color synchronization signal output
171	ORR/V	Red / chrominance ADC output
172	ORB/U	Blue /chrominance ADC output
173	ORG/Y	Green / chrominance ADC output
174	VAI	Video dynamic indication output
175	FREF	Scan signal output
17	VREF	Vertical reference input

2. 6、TA2024 general:

The TA2024 is a 10W/ch continuous average two-channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers. It has below feature:

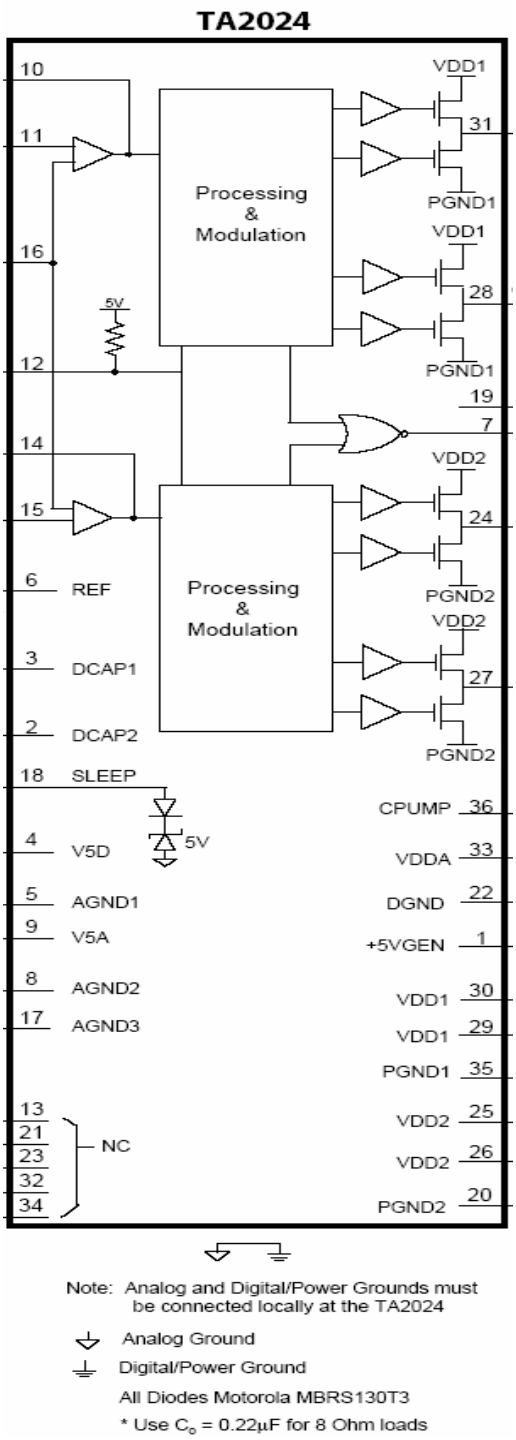
- Mute control
- Temperature protect circuit
- Low noise switch
- Power supply:12V

Pin Function Descriptions：

Pin(s)	Name	Function
2, 3	DCAP2, DCAP1	Charge pump switching pins
4, 9	V5D, V5A	Digital 5VDC, Analog 5VDC
5, 8, 17	AGND1, AGND2, AGND3	Analog Ground
6	REF	Internal reference voltage

7	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier
10，14	OAOUT1, OAOUT2	Input stage output pins.
11, 15	INV1, INV2	Single-ended inputs
12	MUTE	Mute control
16	BIASCAP	Input stage bias voltage
18	SLEEP	Sleep mode control
19	FAULT	A logic high output indicates thermal overload
20, 35	PGND2, PGND1	Power Grounds (high current)
22	DGND	Digital Ground
24, 27; 31, 28	OUTP2 & OUTM2; OUTP1 & OUTM1	Bridged outputs
25, 26, 29, 30	VDD2, VDD2 ， VDD1, VDD1	Supply pins for high current H-bridges, nominally 12VDC.
13, 21, 23, 32, 34	NC	Not connected
33	VDDA	Analog 12VDC
36	CPUMP	Charge pump output
1	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 4 and 9).

TA2024 Block Diagram：



2.7. Brief Introduction to SM5302AS ：

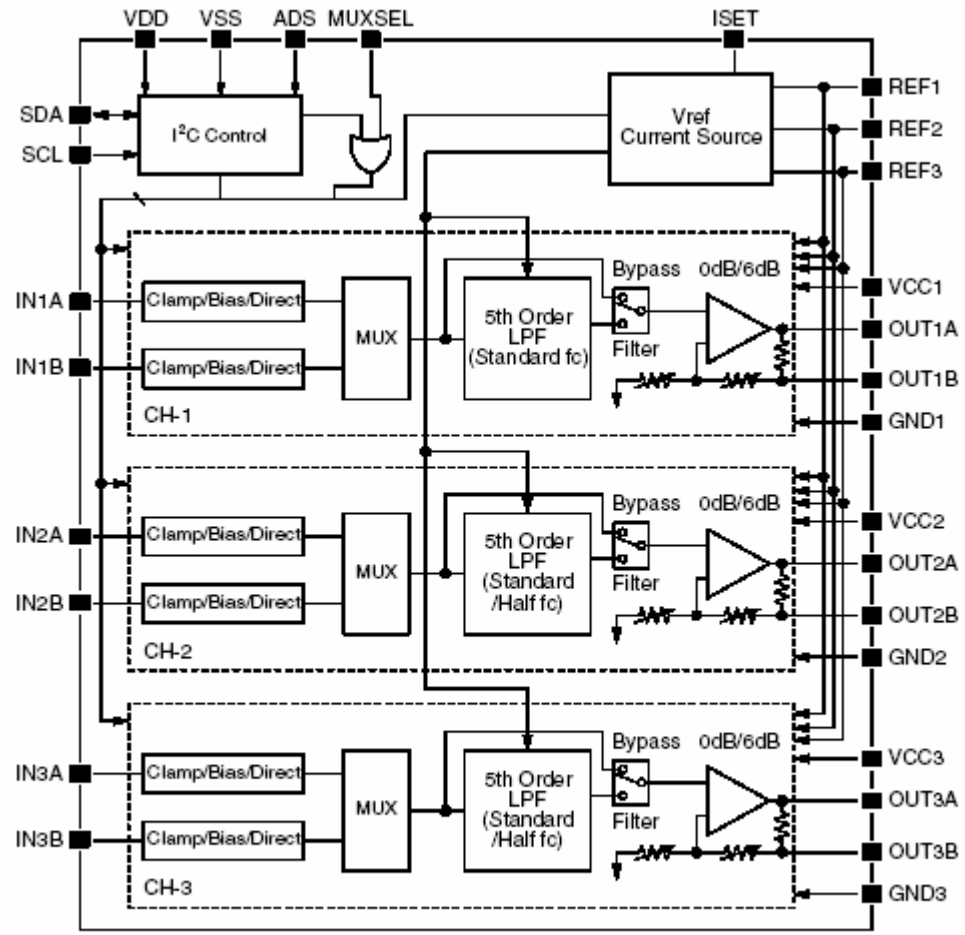
The SM5302AS is a 3-channel video buffer with built-in 5th -order low pass filter. The cutoff frequency, signal input type, and output gain switching can be controlled using a IIC control bus, and the IIC slave address can be set by ADS(3-state input) to allow a maximum of three devices to be used simultaneous.

FEATUES:

- supply voltage：analog:4.75V~5.25V; digital:3.0~5.5V
- 2-system input multiplexer function(switchable using IIC or MUXSEL input)
- Filter bypass mode function for display specifications up to SVGA resolution.
- Video input pins can be independently set to sync-tip clamp/bias/direct input.
- Output gain switching: 0/6dB
- Output sag compensation circuit built-in.
- Half fc mode switch function(CH-2,CH-3) suitable for digital component signals.

- IIC interface control: slave address:90h,92h or 94h(up to three devices can be used simultaneously,selected by ADS input); data transfer rate: fast mode(up to 400kbps)
- Cutoff frequency:4.8 to 43MHz variable

SM5302AS Internal Diagram：



Pin Description：

Pin	Name	Description
1	REF1	Internal reference voltage 1
2	VDD	Digital supply(3.0~5.5V).
3	SDA	IIC data signal input/output
4	SCL	IIC clock signal input
5	Vss	Digital ground
6	MUXSEL	Input multiplexer switch control
7	ADS	IIC slave address select(three state input)
8	IN1A	Video signal input 1(CH-1, input A)
9	IN1B	Video signal input 1(CH-1, input B)
10	ISET	Internal current-setting resistor(Riset) connection(1.8KΩ)
11	IN2A	Video signal input 1(CH-2, input A)
12	IN2B	Video signal input 1(CH-2, input B)
13	IN3A	Video signal input 1(CH-3, input A)
14	IN3B	Video signal input 1(CH-3, input B)

15	GND3	Analog ground(CH-3)
16	Out3B	Video signal output(CH-3,for sag compensation)
17	Out3A	Video signal output(CH-3)
18	VCC3	Analog supply(CH-3)(4.75 to 5.25V).
19	GND2	Analog ground(CH-2)
20	Out2B	Video signal output(CH-2,for sag compensation)
21	Out2A	Video signal output(CH-2)
22	VCC2	Analog supply(CH-2)(4.75 to 5.25V).
23	GND1	Analog ground(CH-1, Vref)
24	Out1B	Video signal output(CH-1,for sag compensation)
25	Out1A	Video signal output(CH-1)
26	VCC1	Analog supply(CH-1,Vref)(4.75 to 5.25V).
27	REF3	Internal reference voltage 3
28	REF2	Internal reference voltage 2

2.8. Brief Introduction to SAA7115：

The SAA7115 is a video capture device for various applications ranging from small screen products like e.g. digital set top boxes, personal video recording applications to big screen devices like e.g. LCD projectors due to it's improved comb filter performance and 10 bit video output capabilities.

●Six analog inputs, internal analog source selectors;

●Two improved 9 Bit CMOS analog-to-digital converter in differential CMOS style;

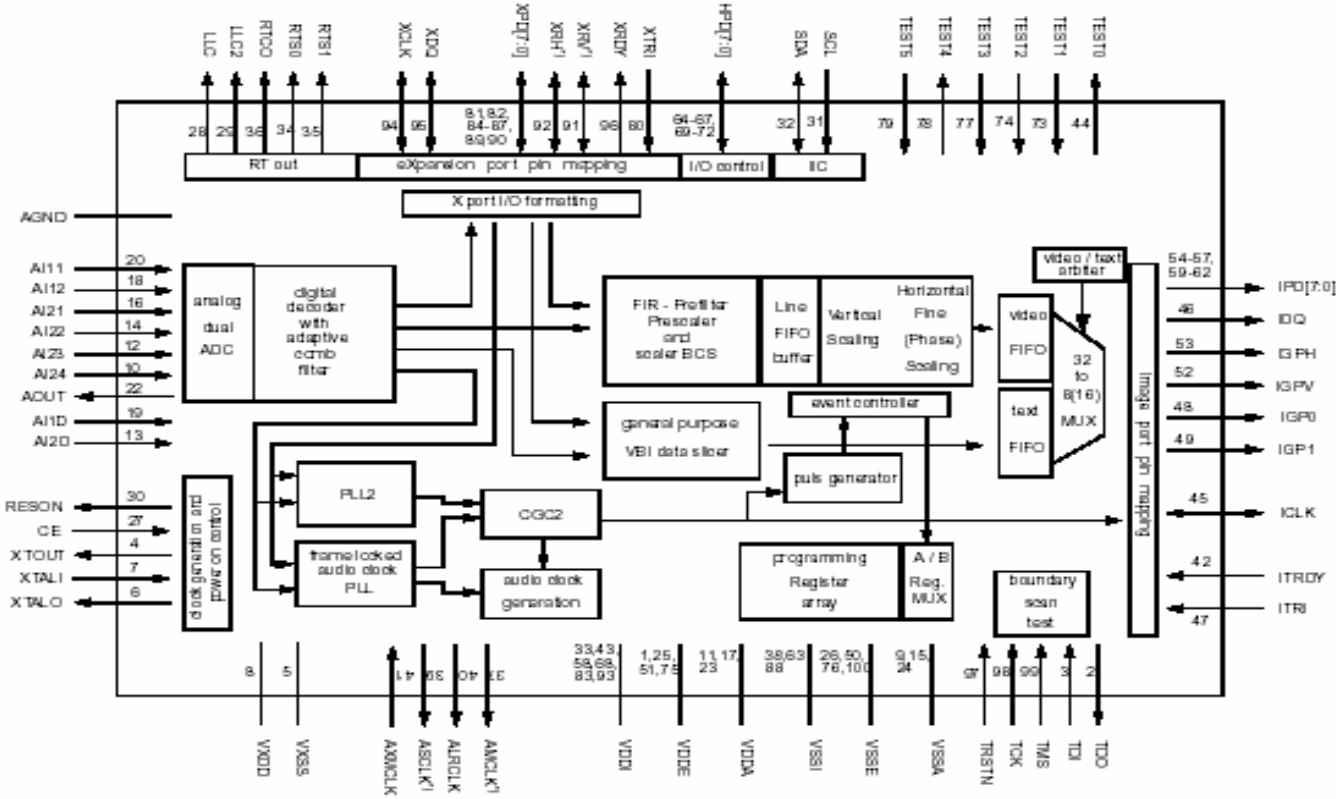
●Automatic Clamp Control (ACC) for CVBS, Y and C;

●Enhanced Horizontal and vertical Sync Detection;

●PAL delay line for correcting PAL phase errors;

●Automatic TV/VCR detection;

SAA7115 Internal Diagram：



Pin Function：

Pin	Name	Description
1,8,11,17,23,25,33	VDD	Supply voltage port

43,51,58,68,75,83 93		
2	TDO	Test Data Output for Boundary Scan Test (2)
3	TDI	Test Data Input for Boundary Scan Test (with internal pull-up)(2)
4	XTOUT	crystal oscillator output signal, auxiliary signal
6	XTALO	24.576 (32.11) MHz crystal oscillator output; not connected if XTALI is driven by an external single-ended oscillator.
7	XTALI	Input terminal for 24.576 (32.11) MHz crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal.
6	VXDD	Crystal oscillator power supply
10,12,14,16	AI21~AI24	Analog signal input
13	AI2D	differential input for ADC channel 2 (pins AI24, AI23, AI22, AI21)
19	AI1D	differential input for ADC channel 1 (pins AI12, AI11)
20	AI11	analog input 11
18	AI12	analog input 12
5,9,15,21,24,26,38 50,63,76,88,100	AGND VSS	ground
22	AOUT	Analog test output (do not connect)
27	CE	Chip Enable or RESET input (with internal pull up)
28	LLC	line-locked system clock output (27 MHz nominal), for backward compatibility, do not use for new applications
29	LLC2	line locked clock/2 output (13.5 MHz nominal) for backward compatibility, do not use for new applications
30	RESON	RESet Output Not signal
31	SCL	IIC serial clock line (with inactive output path)
32	SDA	IIC serial data line
34	RTS0	real time status or sync information, controlled by subaddr. “11h and 12h”
35	RTS1	RTS1 35 O real time status or sync information, controlled by subaddr. “11h and 12h”
36	RTCO	Real time control output
37	AMCLK	Audio master clock output
39	ASCLK	Audio serial clock output
40	ALRCLK	Audio lift/right clock output
41	AMXCLK	Audio master external clock input
42	ITRDY	Target ready input, image port(with internal pull up)
45	ICLK	clock output signal for image-port, LCLK of LPB image port mode, or optional asynchron. backend clock input
46	IDQ	output data qualifier for image port *(optional: gated clock output)*
47	ITRI	image-port output control signal, effects all I-port pins incl. ICLK, enable and active polarity is under software control (bits IPE in subaddr. “87”) output path used for **Testing**: scan output
48	IGP0	general purpose output signal 0; image-port (controlled by subaddr. “84”,”85”)
49	IGP1	general purpose output signal 1; image-port (controlled by subaddr. “84”,”85”), same functions as IGP0
52	IGPV	multi purpose vertical reference output signal; image-port (controlled by subaddr. “84”,”85”)
53	IGPH	multi purpose horizontal reference output signal; image-port (controlled by subaddr. “84”,”85”)
54~57,59~62	IPD0~IPD7	image port data output
64~67,69~72	HPD0~HPD7	Host port data I/O, carries UV chrominance information in 16 bit video I/O modes
80	XTRI	X-port output control signal, effects all X-port pins (XPD[7:0], XRH, XRV, XDQ and XCLK) enable and active polarity is under software control (bits XPE in subaddr. “83”)
81,82,84,85, 89,90,86,87	XPD0~XPD7	expansion-port data

91	XRV	vertical reference I/O expansion-port: In ten bit video output mode: this signal represents the video bit 0.
92	XRH	horizontal reference I/O expansion-port: In ten bit video output mode: this signal represents the video bit 1.
94	XCLK	clock I/O expansion port
95	XDQ	data qualifier I/O expansion port
96	XRDY	task flag or read signal from scaler, controlled by XRQT (subaddr. 83H)
97	TRSTN	Test Reset Not for Boundary Scan Test (with internal pull-up); for board design without Boundary Scan connect TRSTN to 'ground'(1)
98	TCK	Test Clock for Boundary Scan Test (with internal pull-up)(2)
99	TMS	Test Mode Select for Boundary Scan Test or Scan Test (with internal pull-up)(2)

2.9. Brief Introduction to UOCⅢ(TDA15063H):

The UOCIII series combines the functions of a Video Signal Processor (VSP) together with a FLASH embedded TEXT/Control/Graphics -Controller (TCG -Controller) and US Closed Caption decoder.

●DVB/VSB IF circuit for preprocessing of digital TV signals;

●Video switch with 3 external CVBS inputs and a CVBS output;

●Automatic Y/C signal detector;

●Adaptive digital (4H/2H) PAL/NTSC comb filter for optimum separation of the luminance and the chrominance signal

●Picture improvement features with peaking (with switchable center frequency, depeaking, variable positive/negative peak ratio, variable pre-/overshoot ratio and video dependent coring), dynamic skin tone control, gamma control and blue and black stretching. All features are available for CVBS, Y/C and RGB/YPBPR signals.

The mono intercarrier sound circuit has a selective FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted. In the stereo versions of UOCIII the use of this demodulator is optional for special applications.

Normally the FM demodulators of the stereo demodulator/decoder part are used (see below).

●The FM-PLL demodulator can be set to centre frequencies of 4.72/5.74 MHz so that a second sound channel can be demodulated. In such an application it is necessary that an external band-pass filter is inserted.

●The vision IF and mono intercarrier sound circuit can be used for the demodulation of FM radio signals. With an external FM tuner also signals with an IF frequency of 10.7MHz can be demodulated. For the QIP90 versions this is valid only for the "stereo" versions

●Built-in adaptable brightness delay circuit

●switchable brightness signal transmission rate

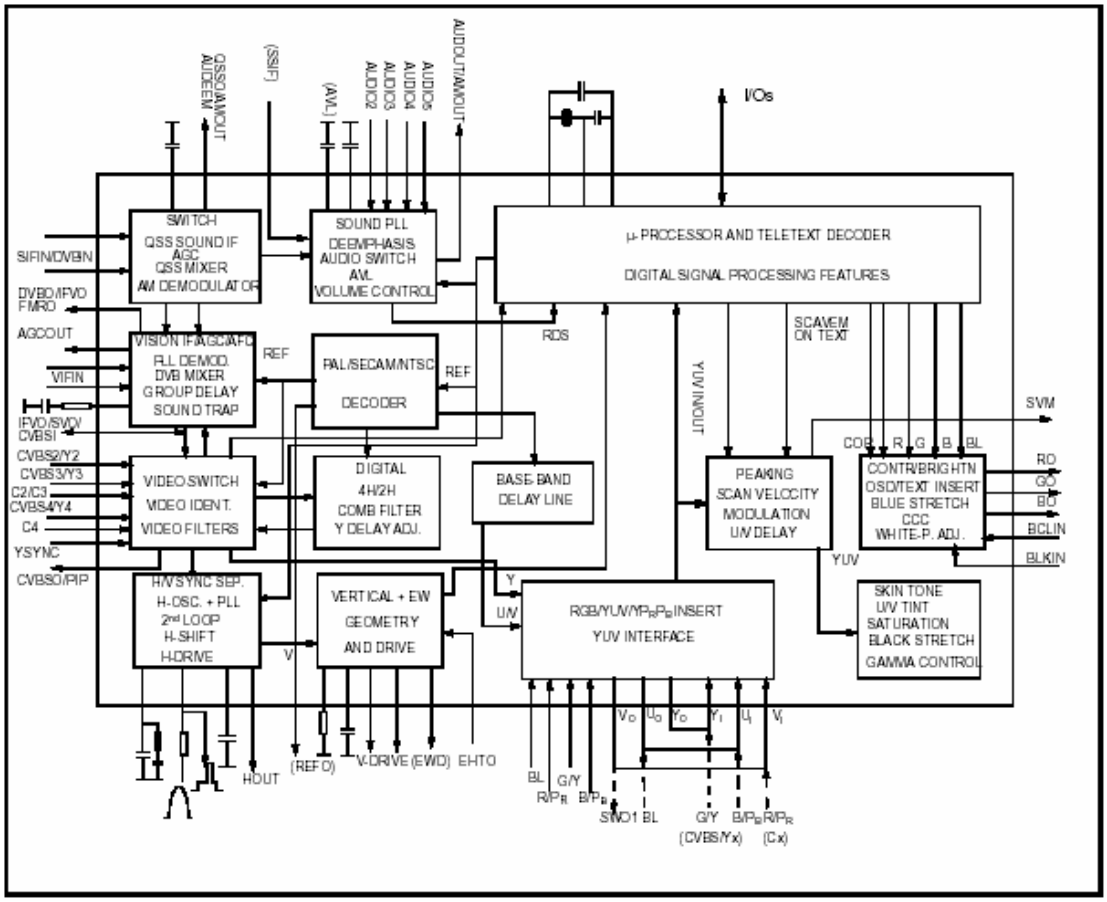
Pin Description:

Pin	Name	Description
1,2,12,18,28,40 68,81,89,92,95,101 121,125	VSS,GND	ground
3,4,45,69,82,88,90, 91,93,94,96,100, 110,117,118,124	VDD	Power supply
5	VREF_POS_LSL	SDAC input signal
6	VREF_NEG_LSL+HPL	
7	VREF_POS_LSR+HPR	
8	VREF_NEG_HPL+HPR	
9	VREF_POS_HPR	
10	XTALIN	Crystal oscillator input
11	XTALOUT	Crystal oscillator output
13	VGUARD/SWIO	V-guard input / I/O switch
14	DECDIG	decoupling digital supply
15	VP1	decoupling digital supply

16	PH2LF	phase-2 filter phase-1 filter
17	PH1LF	
19	SECPLL	SECAM PLL decoupling bandgap decoupling
20	DECBG	
21	EWD/AVL	East-West drive output or AVL capacitor
22	VDRB	vertical drive B output vertical drive A output
23	VDRA	
24	VIFIN1	IF input 1 IF input 2
25	VIFIN2	
27	IREF	reference current input
29	SIFIN1/DVBIN1	SIF input 1 / DVB input 1
30	SIFIN2/DVBIN2	
31	AGCOUT	tuner AGC output
32	EHTO	EHT / overvoltage protection input
33	AVL/SWO/SSIF/REFO/REFIN	Automatic Volume Levelling / switch output reference output / external reference signal DVB operation
34	AUDIOIN5L	audio-5 input (left signal) audio-5 input (right signal)
35	AUDIOIN5R	
36	AUDOUTSL	audio output for SCART/CINCH (left signal) audio output for SCART/CINCH (right signal)
37	AUDOUTSR	
38	DECSDEM	decoupling sound demodulator
39	QSSO/AMOUT/AUDEEM	QSS intercarrier output / AM output / deemphasis
41	PLLIF	PLL filter
42	SIFAGC/DVBAGC	AGC sound IF / internal-external AGC for DVB applications
43	DVBO/IFVO/FMRO	Digital Video Broadcast output / IF video output
44	DVBO/FMRO	
46	AGC2SIF	AGC capacitor second sound IF
47	VP2	2nd supply voltage TV processor (+5 V)
48	IFVO/SVO/CVBSI	video output / selected CVBS output / CVBS
49	AUDIOIN4L	audio-4 input (left signal) audio-4 input (right signal)
50	AUDIOIN4R	
51	CVBS4/Y4	CVBS/Y input
52	C4	chroma-4 input
53	AUDIOIN2L/SSIF	Audio input
54	AUDIOIN2R	
56	AUDIOIN3L	
57	AUDIOIN3R	
30	AUDOUTLSL	
61	AUDOUTLSR	
62	AUDOUTHPL	
63	AUDOUTHPR	
58	CVBS3/Y3	CVBS/Y input
59	C2/C3	chroma-2/3 input
55	CVBS2/Y2	CVBS/Y input
64	CVBSO/PIP	CVBS/PIP signal output
65	SVM	scan velocity modulation output
66	FBISO/CSY	flyback input/sandcastle output or composite H/V
67	HOUT	horizontal output

70	VIN (R/PRIN2/CX)	V-input for YUV interface
71	UIN (B/PBIN2)	U-input for YUV interface
72	YIN (G/YIN2/CVBS-YX)	Y-input for YUV interface
73	YSYNC	Y-input for sync separator
74	YOUT	Y-output (for YUV interface)
75	UOUT (INSSW2)	U-output for YUV interface
76	VOUT (SWO1)	V-output for YUV interface
77	INSSW3	3rd RGB / YP_BP_R insertion input
78	R/PRIN3	3rd R input / P_R input
79	G/YIN3	G input / Y input
80	B/PBIN3	3rd B input / P_B input
83	BCLIN	beam current limiter input
85	RO	Red output
86	GO	Green output
87	BO	Blue output
97	INT0/P0.5	external interrupt 0 or port 0.5 (4 mA current sinking direct drive of LEDs)
98,99,102~109 111~116,119,120 122,123,126~ 128	P0.0~ P0.4 P1.0~P1.7,P2.0~P2.5, P3.0~P3.3	Data port

UOCⅢ inside block diagram：



PartⅢ:Analysis on Signal Process Flow of PT4216 and key point test data

This chapter mainly introduces receiving and process of picture and sound signal of PDP TV and system control procedure, supply system of unit.

1. Picture signal process Flow

IF signal which is demodulated by main tuner is sent by AV board module into video decode chip UOCⅢ for decoding ,then switched with signal from AV/S jack by internal electric switch of UOCⅢ, then the output analog video signal is sent into analog-to-digital converter TDA8759HV/8/C1 for A/D transforming to produce R、G、B digital signals, format converted by GM1601/GM1501,then, GM1601/GM1501 transform the different input formats into the uniform up-screen signal format.

The signal demodulated by sub tuner is directly sent into sub-picture video decoder SAA7115HL/V1 for video decoding and A/D conversion，then sent into GM1601/GM1501 again to do format transforming, the output up-screen signal is used for sub-picture display.

The alternative PC、 HDTV(YPBPR) and DVI signals are sent directly into GM1601/GM1501 for processing to form uniform up-screen signal.

2 Sound process flow：

TV sound: RF signal is demodulated by main tuner and output SIF signal. SIF input to UOCⅢ to demodulate and wow process. Output audio signal to dual channel class-T digital audio power amplifier IC TA2024 on power amplifier board. At last is sent to speaker.

AV sound: audio signal from AV is sent to UOCⅢ for processing directly ,then be amplified by power amplifier IC TA2024 to drive speaker.

PC、DVI、YPbPr sound: Signal is processed by UOCⅢ on main board and amplified by TA2024 on power amplifier board after it is strobed by MC74LVX4052DR2.

3、System control process：

After connect the AC power input (we use 3 pins power jack，the GND pin must ground well).First of all ,standby power on power board works，signal main board obtains 5V-ST power supply，then 5V-ST power is regulated to 3.3V by U900 on main board. At this time, standby CPU PIC16F505 begin to work, and LED lamp indicates red. After user gives key or remote on instruction, the 7th pin of PIC16F505 sends PDP-STB high level signal to control relay T802 on power board to turn on, AC power on panel turns on. Each group DC power on power board is normal and output to main board. GM1501 on main board reset normally under A702 IC control, then finish system initialization. Meanwhile finish up-screen signal control. LED indicator turns green. It is proved system control normally.

3.1、When choice VGA mode by remote control box ，GM1501 controls TDA8759 enable by I^2C bus，let them work in low power consumption mode，which can save power and reduce interfere。At the moment GM1501 output Sel_HsVs signal to set PI5V330 in VGA input channel. If there is VGA signal input, directly into GM1501 to detect and process, output is transformed to signal suitable for PDP panel. If no VGA signal input, GM1501 can't detect horizon and vertical sync. Signal. PDP panel display PC icon at left upper corner of screen under GM1501 system control. Other area of panel display black screen. If no input after 60 sec, it hints to enter "save power mode".At the moment ，examines VGA signal ceaselessly，so it can be awaken automatically in VGA mode. It is said that when VGA signal inputs, it can work normally from standby state

3.2、When in TV / AV / YCbCr mode by remote control box，GM1501 controls UOC3 by I^2Cbus. When video signal inputs，PDP panel display normally；if no video signal input，under the control of GM1501，PDP panel displays blue background，if no signal after 15 mins，power off automatically and into standby state. It can not be awaken automatically。

3.3、When in DVI(digital RGB) mode by remote control box，GM1501 controls TDA8759 enable by I^2C bus，let them work in low power consumption mode. When DVI signal inputs, display video；if no DVI signal，GM1501 can't detect horizon and vertical sync. Signal. PDP panel display DVI icon at left upper corner of screen under GM1501 system control. Other area of panel display black screen. If no input after 60 sec, it hints to enter "save power

mode”.At the moment ，examines DVI signal ceaselessly，so it can be awaken automatically in DVI mode. It is said that when DVI signal inputs, it can work normally from standby state

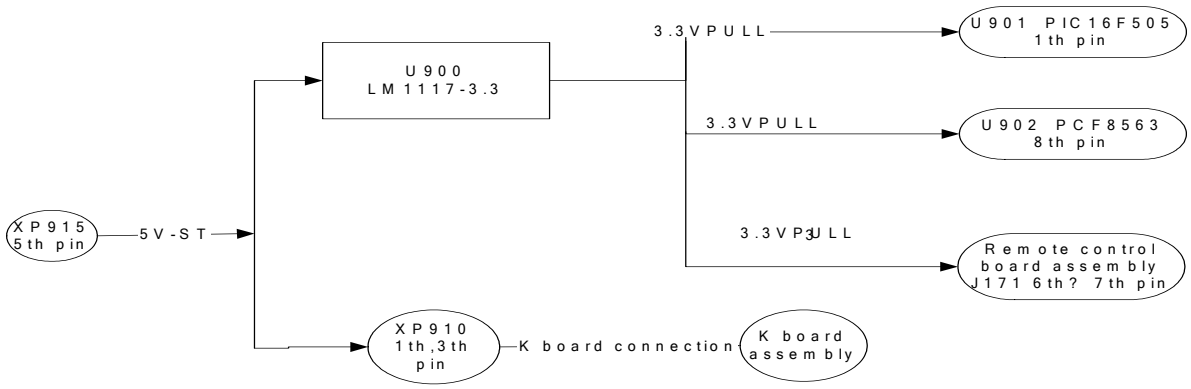
4、Power supply system：

Power board has seven ways voltage output all together. They are 34V， 12V， 12VAU，A6V，D6V，D3.3V and 5V. 34V regulated by IC upc574 is provided to tuner for tuning voltage. 12VAU is provided to audio power amplifier. A6V、D6V is changed 5V by LDO(example TA4805F),used by different circuit network. D3.3V is changed 2.5V and 1.8V by LDO(example LM1117,LM1084 etc.),used by different IC. 5V power supply is used by MCU（PIC16F505）,infrared receiver and k board assembly etc. when standby.

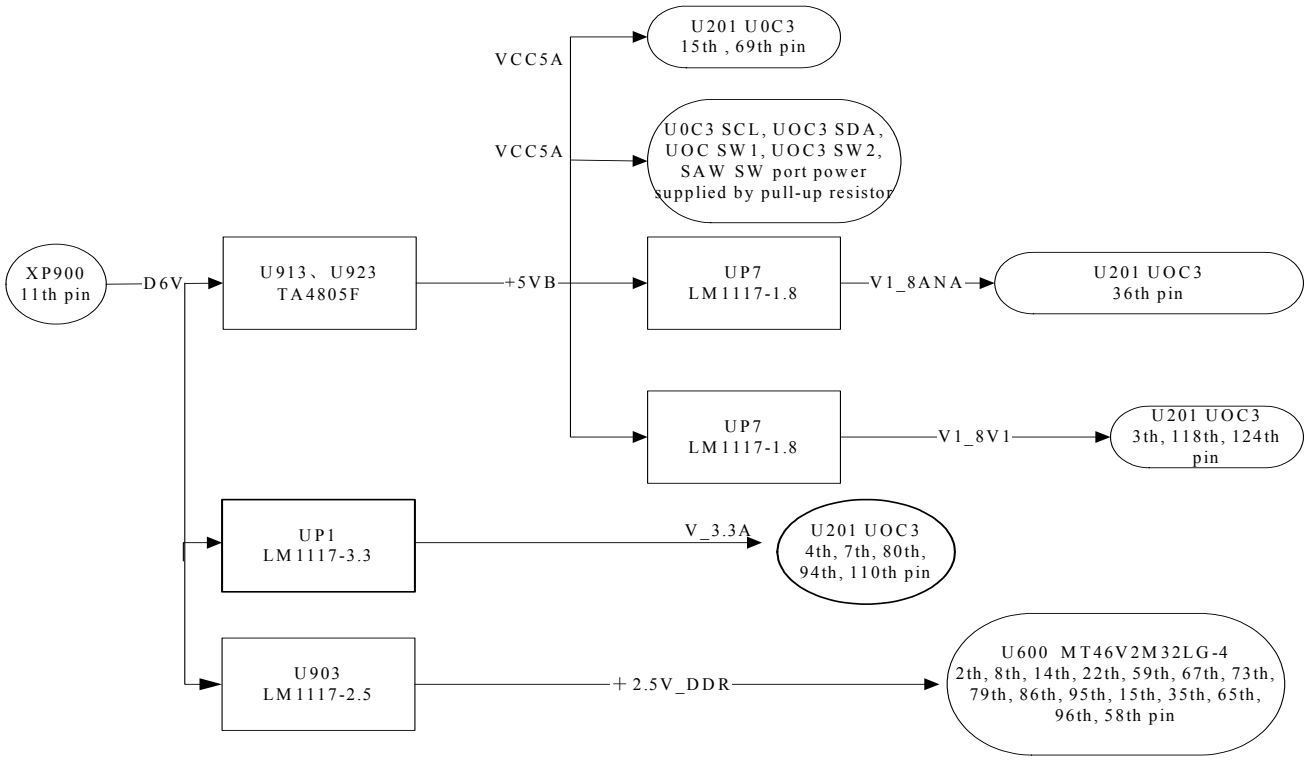
When standby, except above 5V supply, other powers are all off.

4.1 Main power form and power branch：

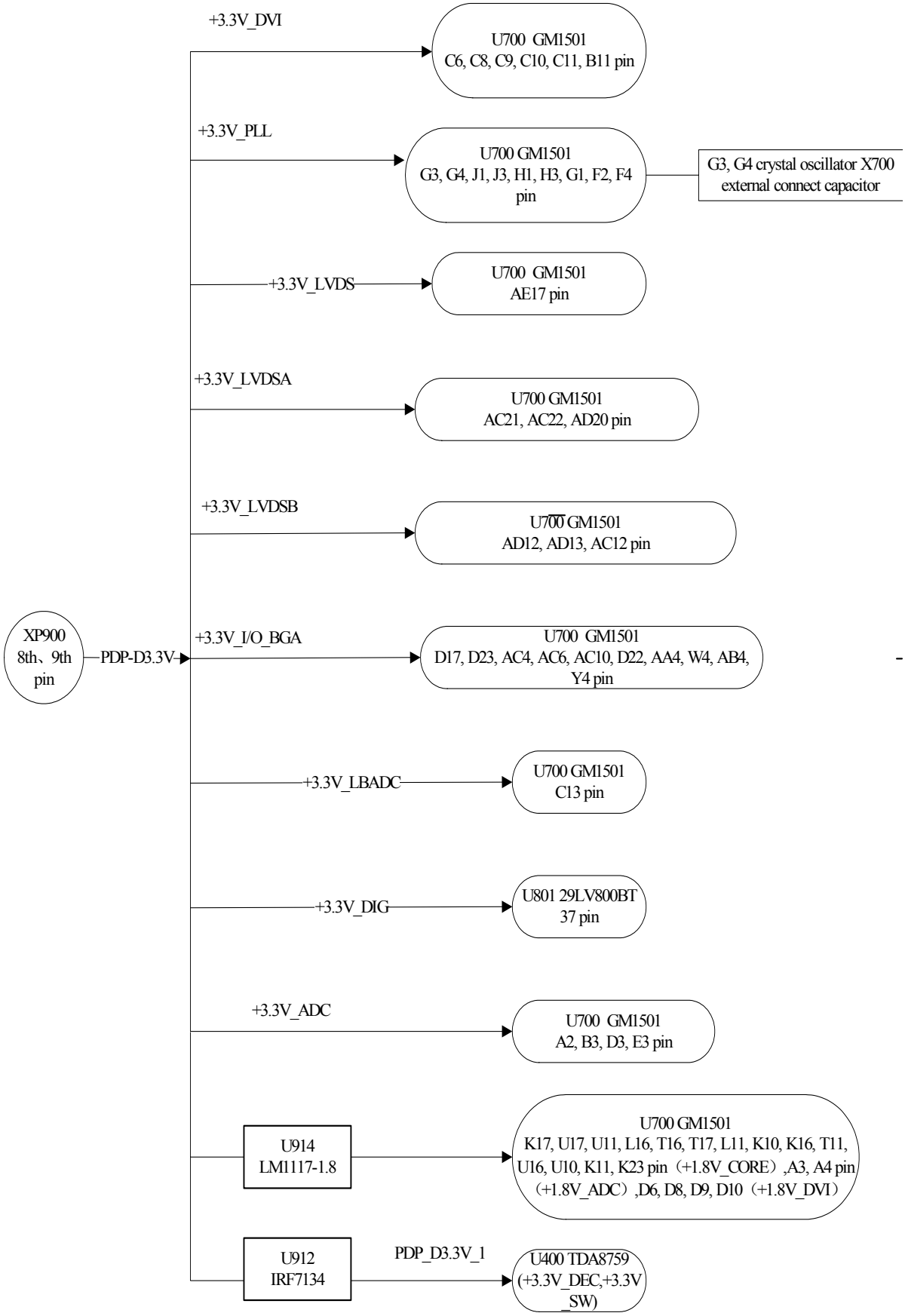
4.1.1、5V-ST power branch



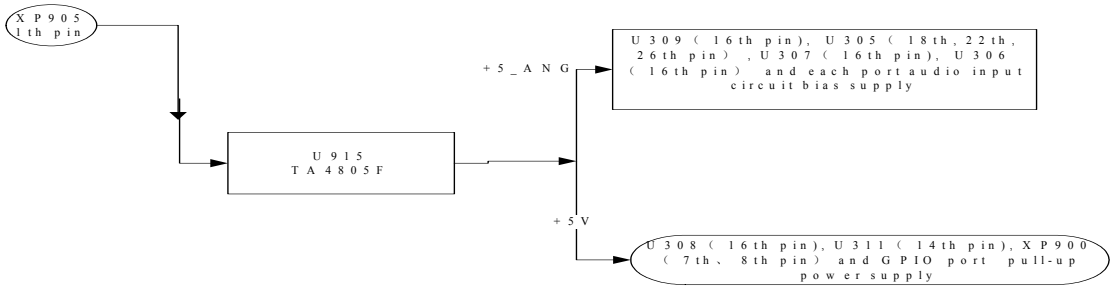
4.1.2、D6V power branch



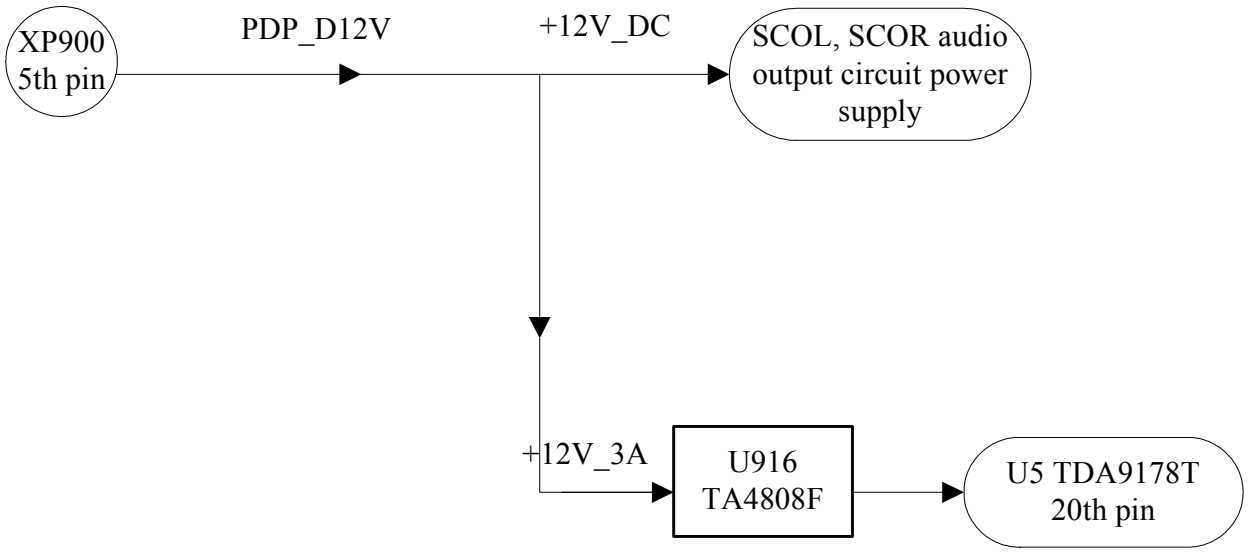
4.1.3、VDD(3.3V) power branch



4.1.4、A6V power branch



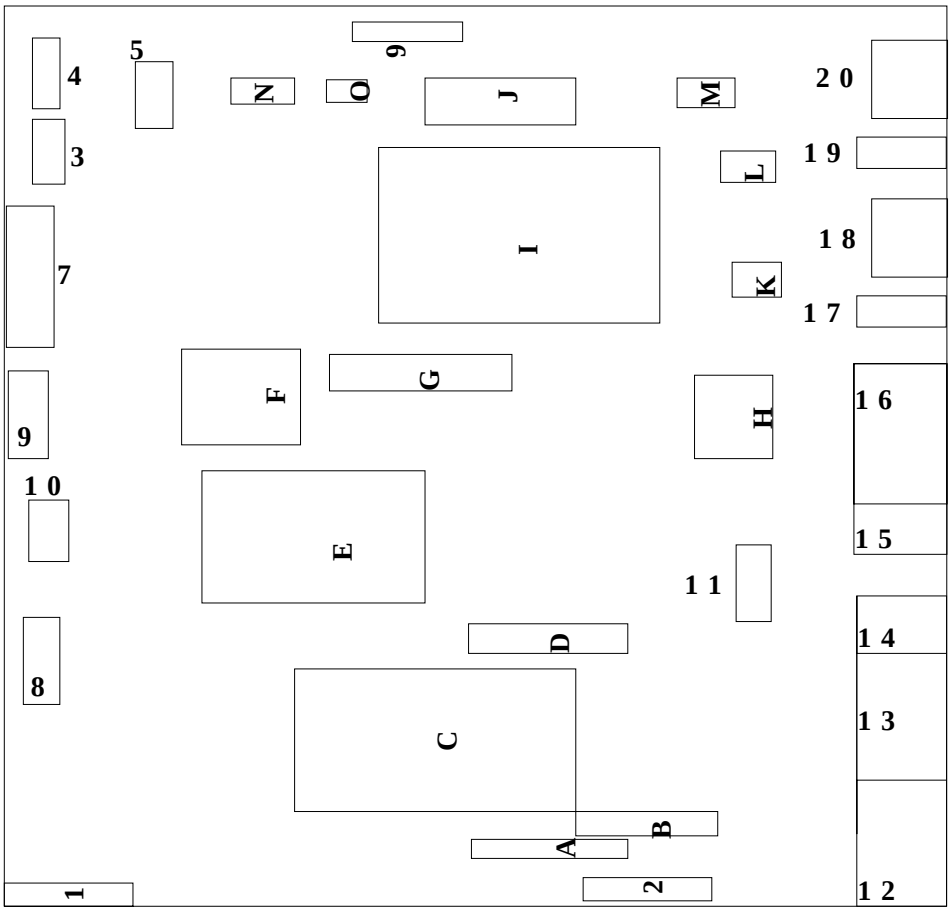
4.1.5、A12V power branch



4.2 The Pin Voltage of regulator on Main Board

position	type	PIN1(V)	PIN2(V)	PIN3(V)	PIN4(V)	PIN5(V)
UP7	LM1117-1.8V	0	1.8	5	1.8	
UP1	LM1117-3.3V	0	3.3	5	3.3	
U913	4805F	6	0	5		
U923	4805F	6	0	5		
U916	78M08	12	0	8		
U403	LM1117-1.8V	0	1.8	3.3	1.8	
U915	4805F	6	0	5	0	
U903	LM1117-2.5	0	2.5	5	2.5	
U914	LM1117-1.8V	0	1.8	3.3	1.8	
U900	LM1117-3.3V	0	3.3	5	3.3	

4.3 Main Components and Socket Locations and Definitions on main board module:



Socket definition

number	name	Connected object	Function description
6	XP915	Power board	Standby power and on/off control
11	XP907	Power amplified board	Left and right channel sound output
5	J171	Remote control board	
3	XP909	K board	
4	XP910	K board	
1	XP926	AV board	
2	XP927	AV board	
7	CN900	PDP pannel	LVDS cable to panel
10	XP936	PDP pannel	Timing control signal of power board of Panel
8	XP900	Power board	PDP-D6V，PDP-D3.3V，PDP-D12V input
9	XP905	Power board	PDP-A6V，PDP-A12V，PDP-12VAMP，PDP-VT33V input
12	XP922	AV output	
13	XP923	AV1 input	
14	XP935	AV2（S）input	
15	XP925	YPbPr audio input	
16	XP924	YPbPr high definition signal input	
17	AVP303	DVI audio input	
18	CN300	DVI input	
19	AVP300	VGA audio input	
20	CN301	VGA input	

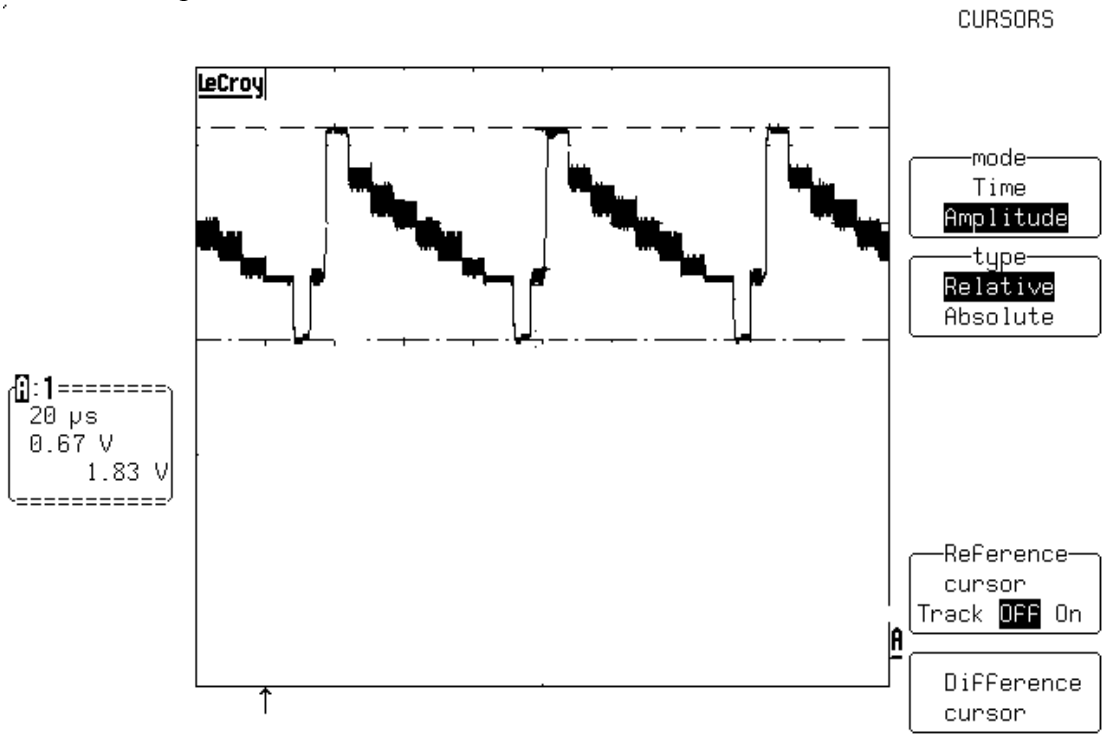
Main components description

number	**name**	type	**Function description**
C	U201	TDA15063H-N1B06557	Audio and video decoder
E	U400	TDA8759HV/8/C1	Video signal A/D converter
F	U402	SAA7115HL/V1	Sub channel video decoder

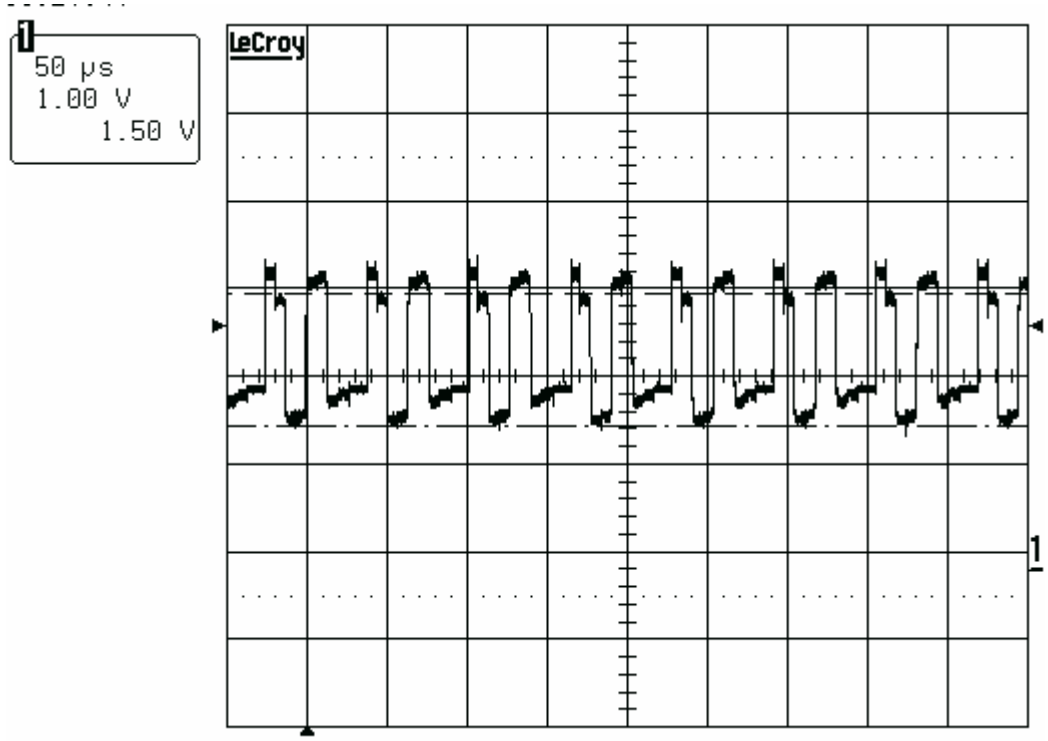
G	U600	MT46V2M32LG-4	Frame buffer
I	U700	GM1601/GM1501-BD	Video processor
H	U305	SM5302AS-G-ET	High definition signal filter
J	U801	AM29LV800DT-70EC	Flash，save TV control program
D	U5	TDA9178T/N1	Video signal picture quality improvement
B	K202	K9352N	SAW filter
A	K201	K7262N	SAW filter
N	U901	PIC16F505	Standby control CPU
O	U902	PCF8563	Real time clock counter
M	U306	FSAV330QSCX	Select switcher
L	U302	24LC21A T/SN	EEPROM
K	U303	24LC21A T/SN	EEPROM

5、Key point waveform

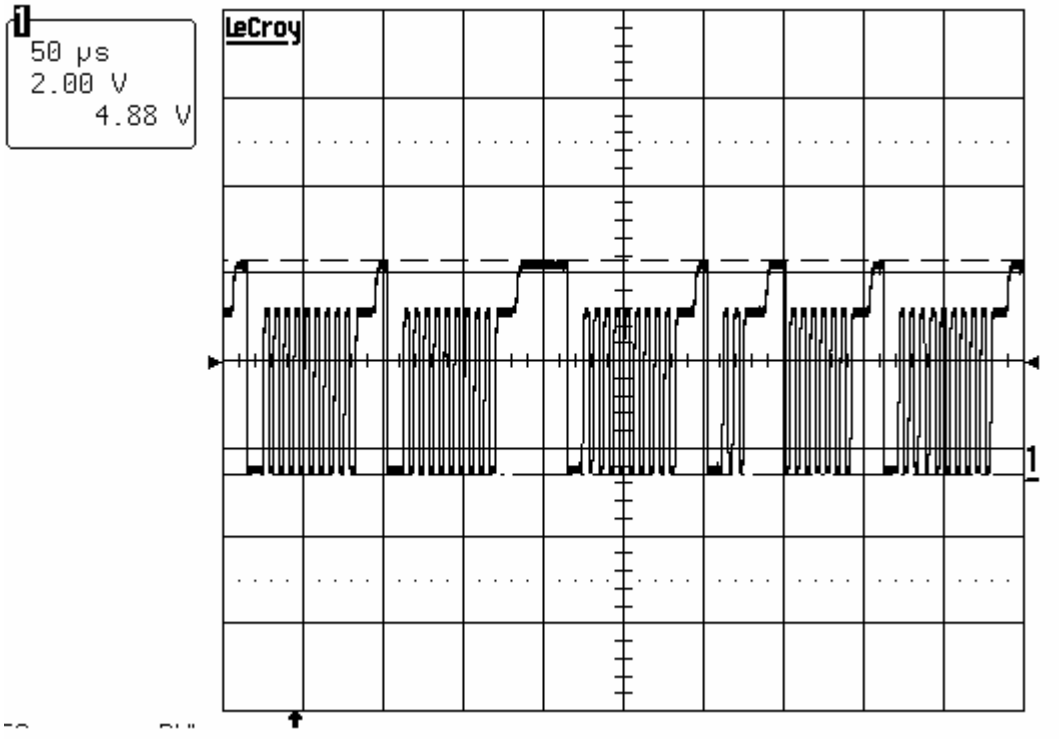
5.1 RF input full color stripe signal, waveform of the 18th pin of sub tuner UT921, the 8th pin of XP926 and the 10th pin of SAA7115 is like this:



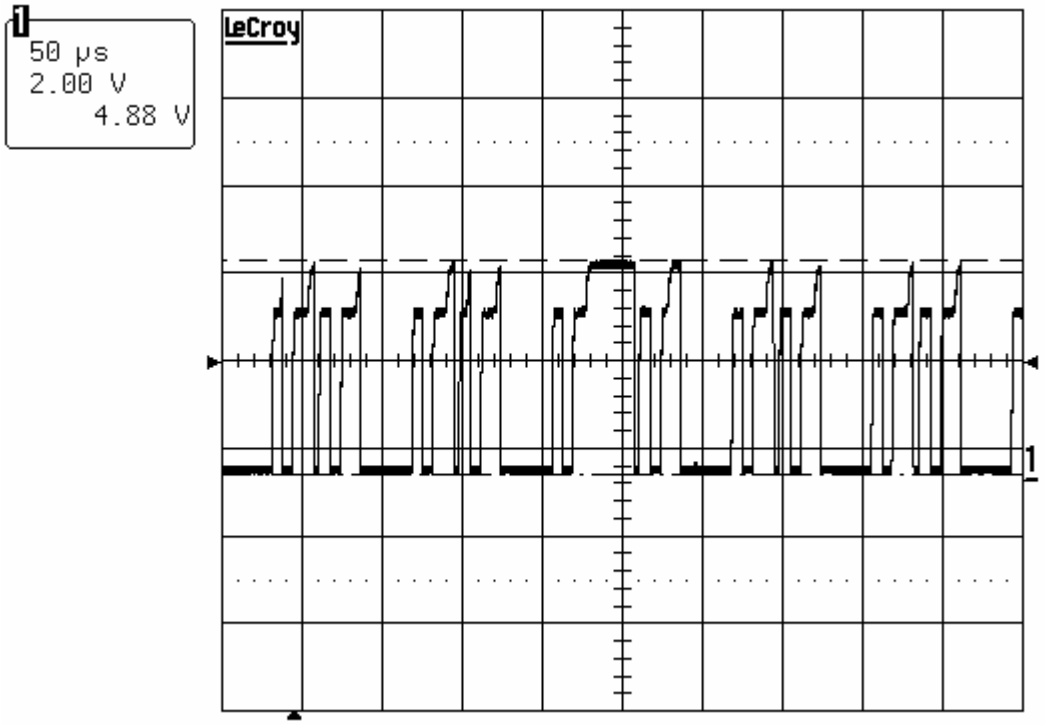
5.2 RF input full color stripe signal, the waveform of Pin85,Pin86,Pin87 of U201 output R,G,B signal ,the E pin of Q171,Q172,Q173 is like this:



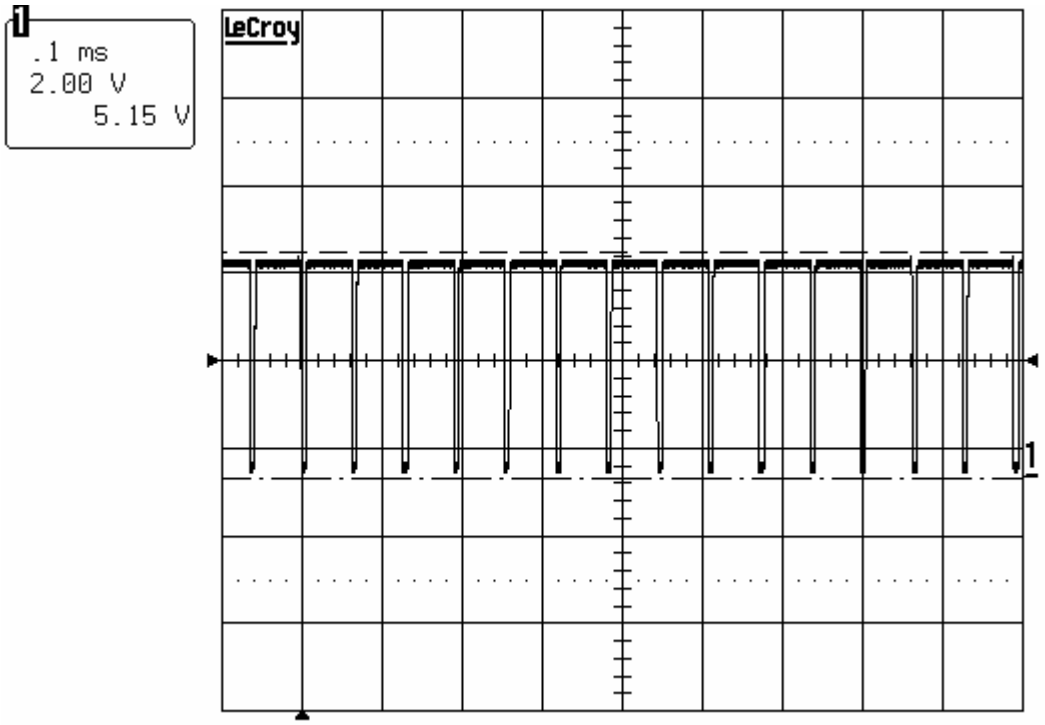
5.3、RF input full color stripe signal, the waveform of I²C bus clock signal UOCIII_SCL, the 98th pin of U201,the 11th pin of U5,the 4th pin of main tuner UT920, the 4th pin of sub tuner UT921,the 1th pin of XP926 is like this:



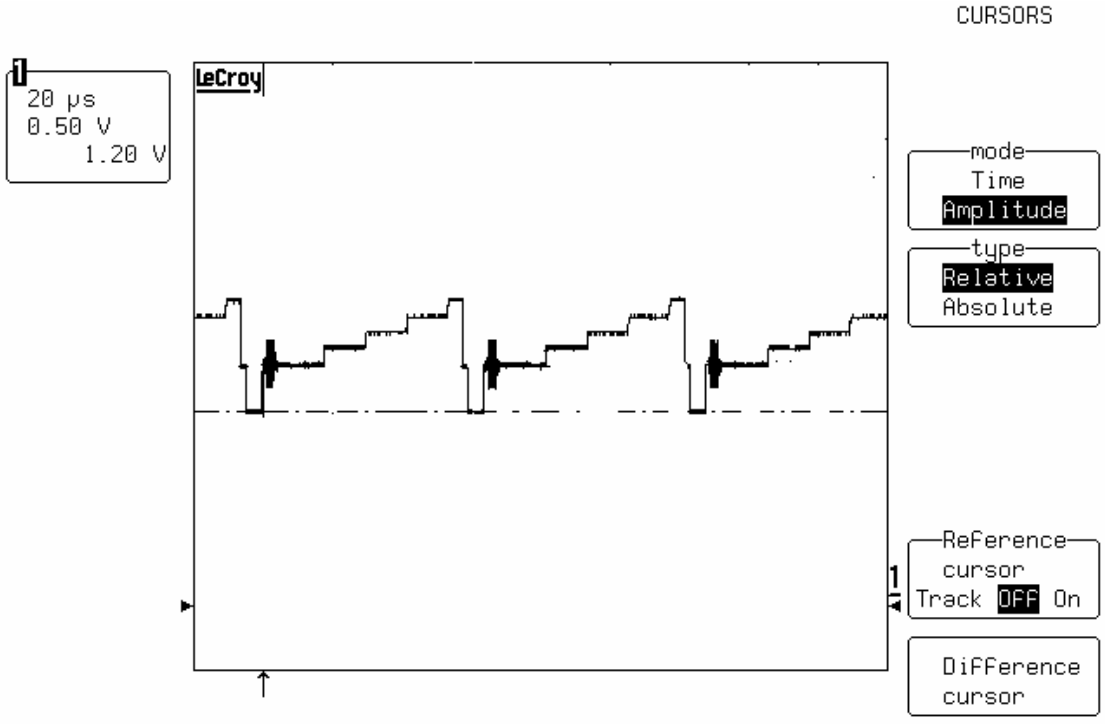
5.4、RF input full color stripe signal, the waveform of I²C bus clock signal UOCIII_SDA, the 99th pin of U201,the 14th pin of U5,the 5th pin of main tuner UT920, the 5th pin of sub tuner UT921,the 2th pin of XP926 is like this:



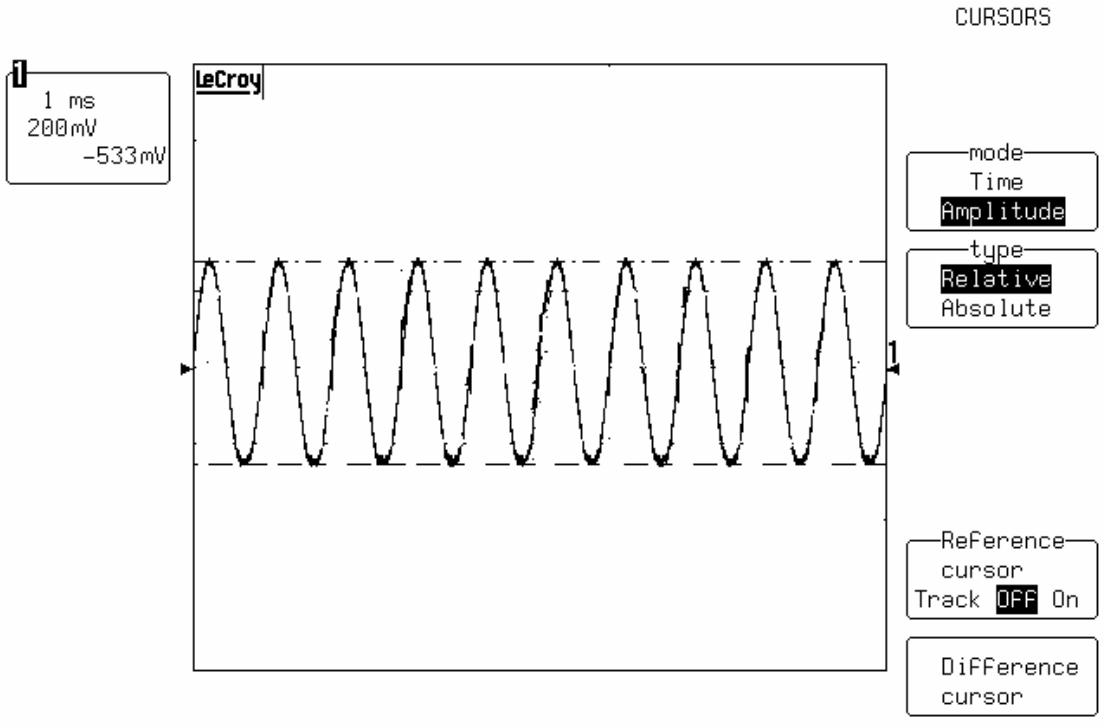
5.5、 RF input full color stripe signal, the waveform of UOC vertical sync signal, the 22th pin of U201,the 105th pin of U400 is like this:



5.6、RF input gray ladder signal, the waveform of the 18th pin of sub tuner UT921,the 8th pin of XP926，the 10th pin of SAA7115 is like this:

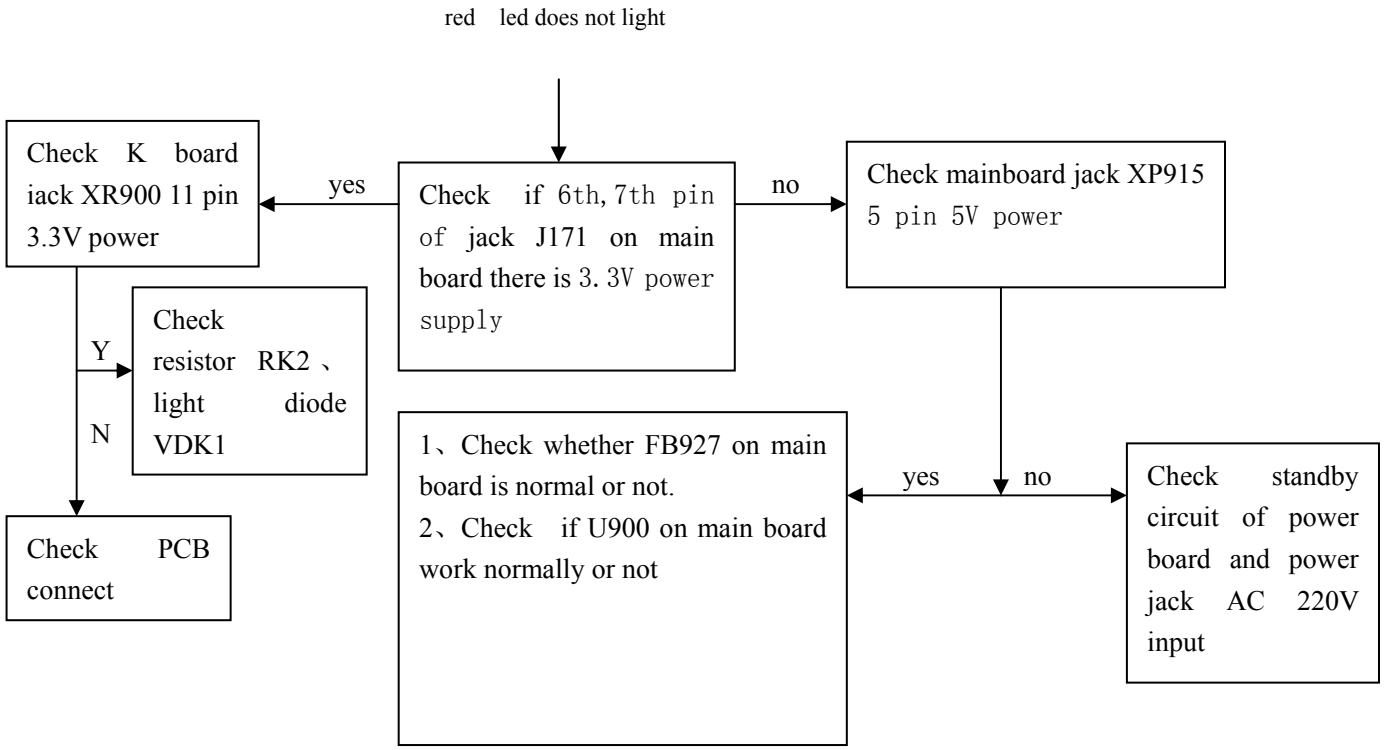


7、The 1KHz sound signal input, the waveform of the 60th 、61 th pin of U201, the 6th、8th pin of XP907 is like this:

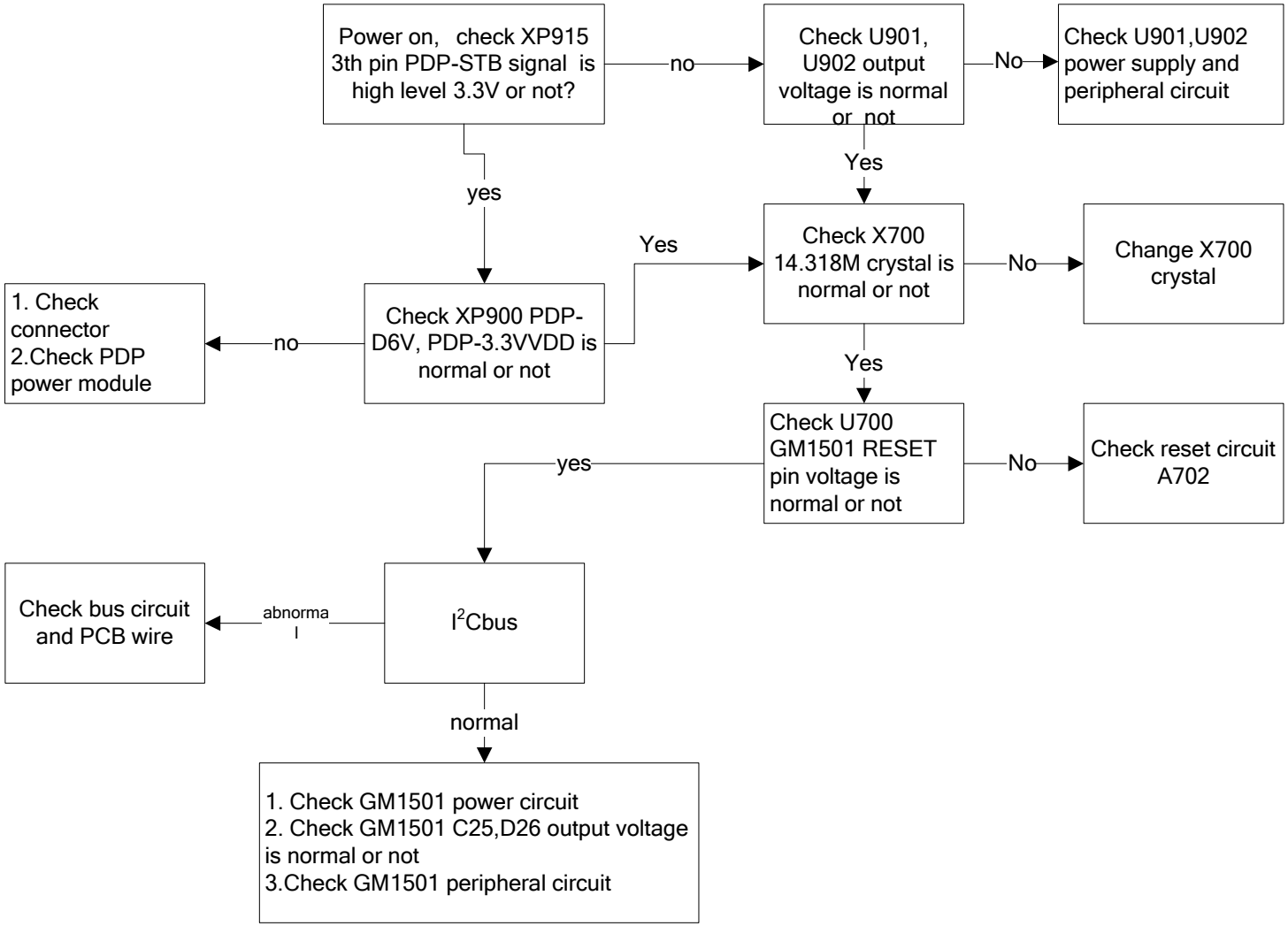


PartⅣ:Typical troubleshooting process flowchart of PT4216

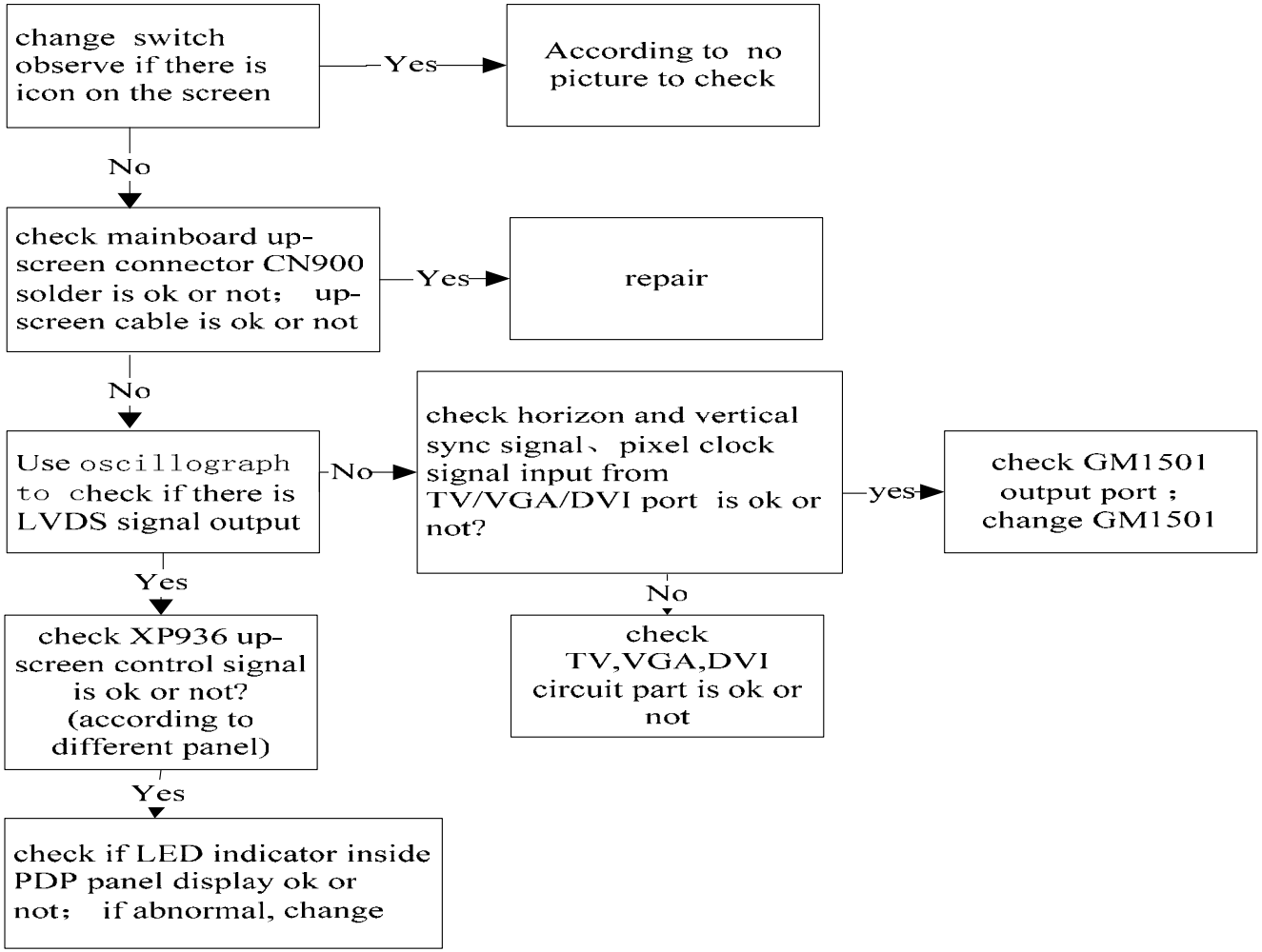
one、red　led does not light



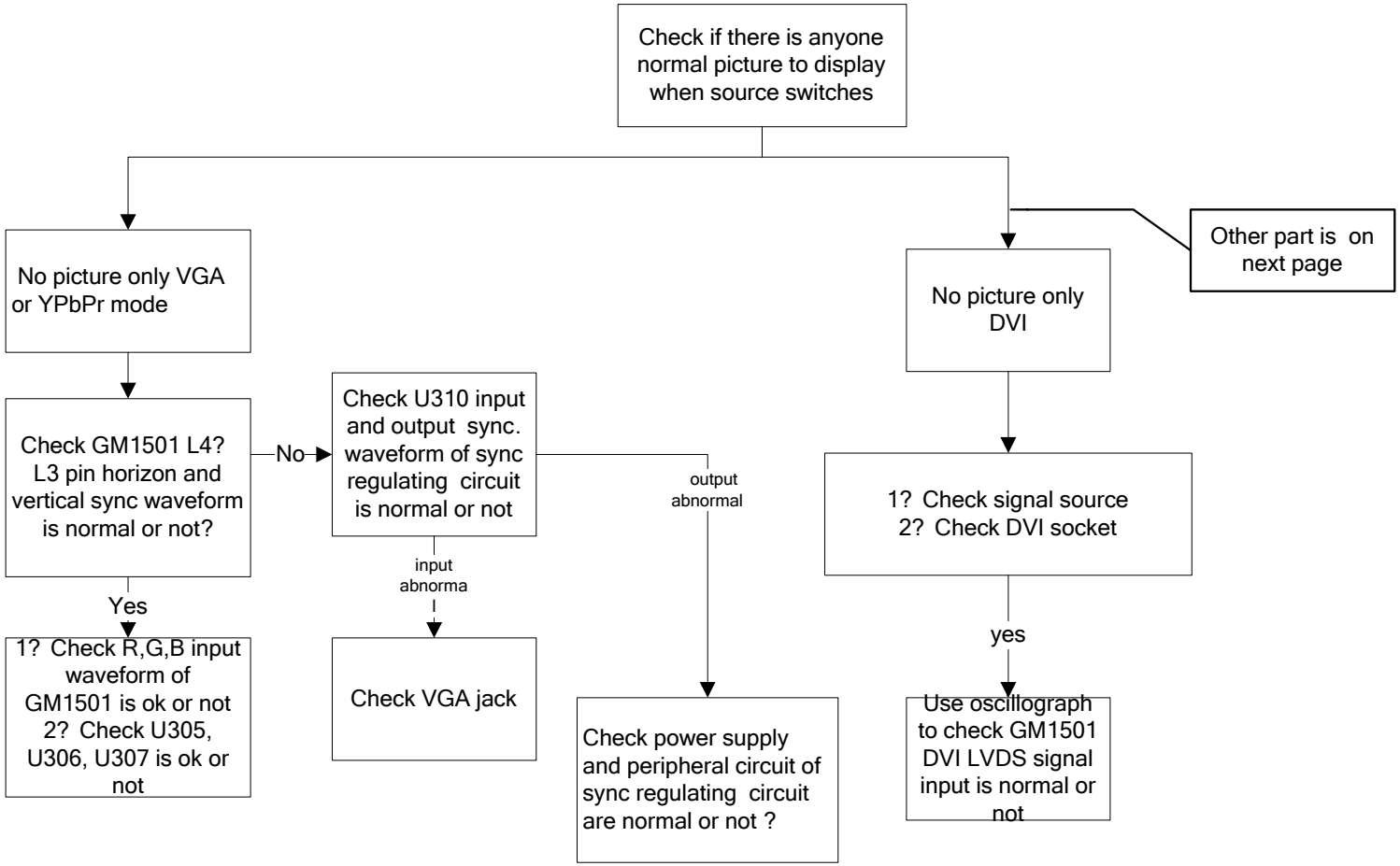
two、The red led lights，but doesn't turn to yellow after power on and black display

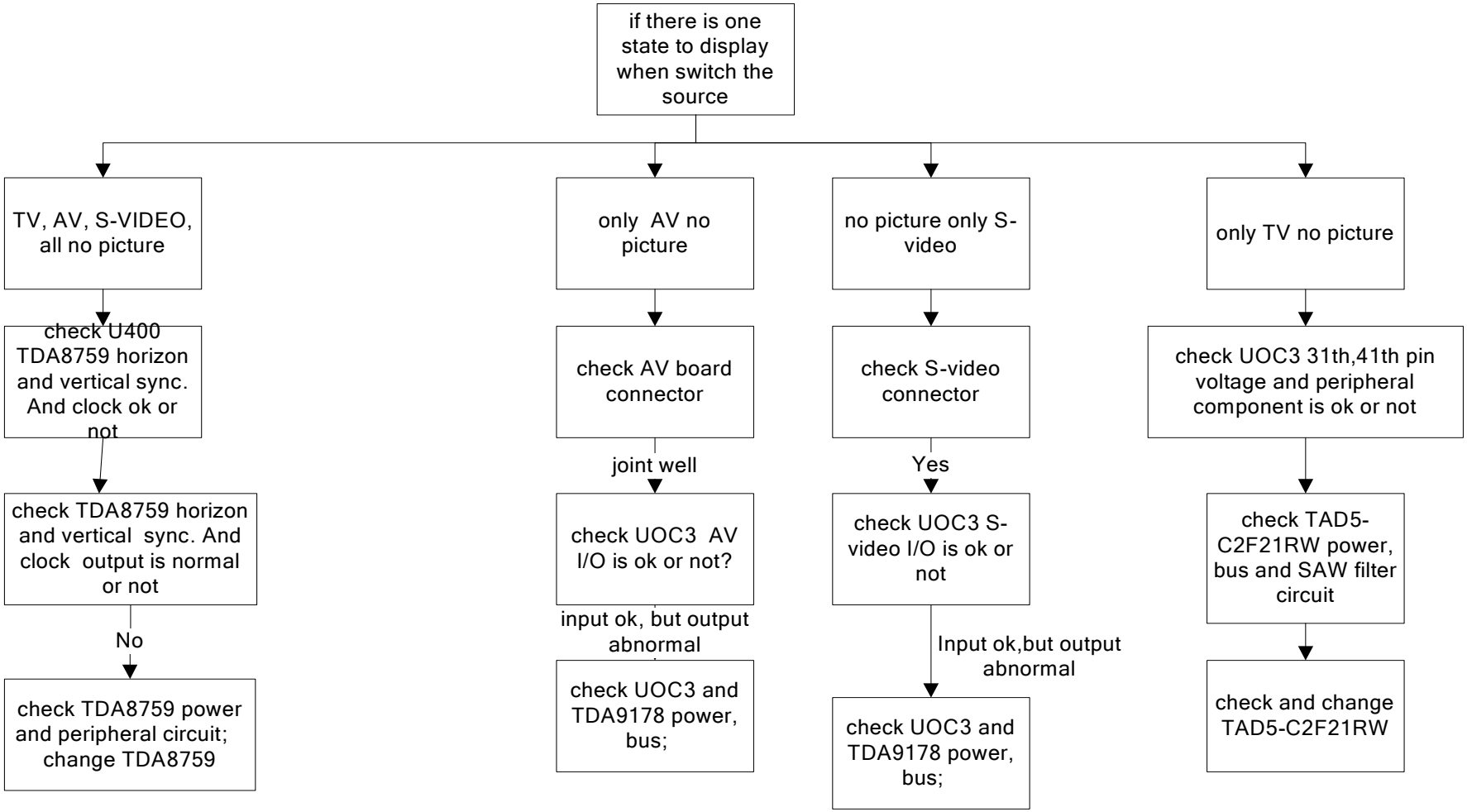


three、The red led lights，turns to green color after power on but display black screen

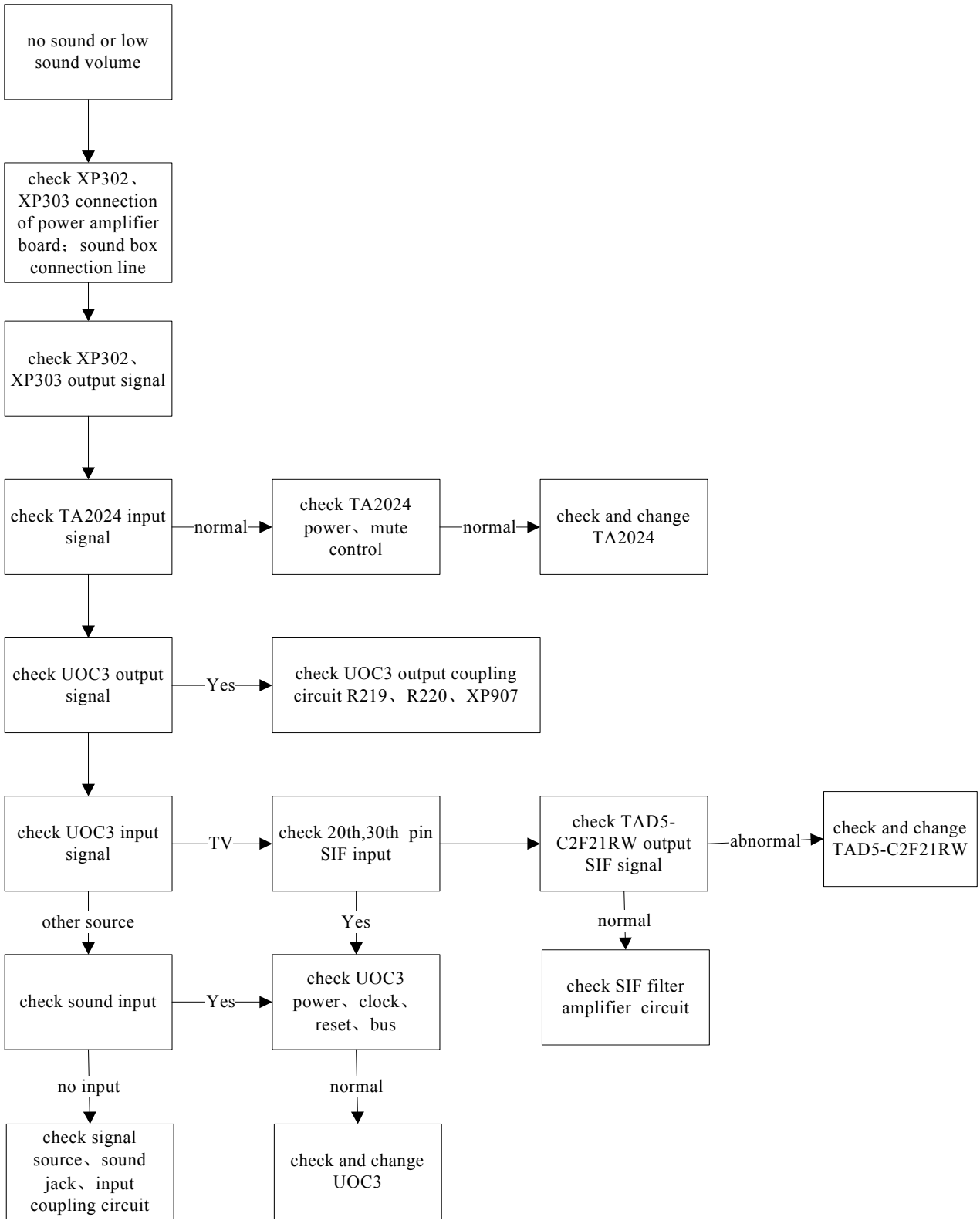


four、no picture：




if there is one state to display when switch the source
TV, AV, S-VIDEO, all no picture
check U400 TDA8759 horizon and vertical sync. And clock ok or not
check TDA8759 horizon and vertical sync. And clock output is normal or not
No
check TDA8759 power and peripheral circuit; change TDA8759
only AV no picture
check AV board connector
joint well
check UOC3 AV I/O is ok or not?
input ok, but output abnormal
check UOC3 and TDA9178 power, bus;
no picture only S-video
check S-video connector
Yes
check UOC3 S-video I/O is ok or not
Input ok,but output abnormal
check UOC3 and TDA9178 power, bus;
only TV no picture
check UOC3 31th,41th pin voltage and peripheral component is ok or not
check TAD5-C2F21RW power, bus and SAW filter circuit
check and change TAD5-C2F21RW

Five、no sound or low sound volume



Part Ⅴ: Spare part list

This list is only for reference, if change the parameters of those spare list ,we do not notice in advance. The exact type or specification is confirmed by newest information provided by corporation.

PT4216

number	**name**	Material number	**Assembly number**	**PCB number**
1、	Main board assembly(Panasonic M7 pannel)	8669000410J	JUJ6.690.041	*JUJ7.820.131*
2、	Main board assembly(Panasonic M8 pannel)	8669000413J	JUJ6.690.041-3	
3、	Main board assembly(LG pannel)	8669000414J	JUJ6.690.041-4	
4、	Main board assembly(Samsung V7 panel)	8669000415J	JUJ6.690.041-5	
5、	AV board assembly	8669300170J	JUJ6.693.017	JUJ7.820.174
6、	Inside power board assembly(Panasonic M8 pannel)	8669800040J	JUJ6.698.004	JUJ6.820.168
7、	Inside power board assembly(Panasonic M7 pannel)	8669800100J	JUJ6.698.010	JUJ7.820.203
8、	Inside power board assembly(LG pannel)	8669800090J	JUJ6.698.009	JUJ7.820.195
9、	Inside power board assembly(Samsung V7 panel)	8669800190J	JUJ6.698.019	JUJ7.820.226
10、	Power filter (Panasonic M7,M8 pannel)	57111381010	10SS1A-BG-Q（S）	
11、	Power filter(Samsung V7 panel)	50570070010	10SS1-CG-Q（S）	
12、	Power amplifier board assembly	8669100100J	JUJ6-691.010	**JUJ7.820.169**

13、	K board assembly	8669400270J	JUJ6.694.027	JUJ7.820.159
14、	Remote control board assembly	8669400280J	JUJ6.694.028	JUJ7.820.160
15、	Divide frequency board assembly	8669100120J	JUJ6.691.012	JUJ7.820.175
16、	Remote control emitter			
17、	PDP panel	69222500425	MD-42M7 N/S/R	
18、	PDP panel	69222500426	MD-42M8AS(N,R,S)	
19、	PDP panel	50890040010	42 V7 4013	
20、	PDP panel	50890040000	S42SD-YD07	
21、	PDP filter glass	31401040100	FG401PAA-01	
22、	PDP filter glass	31401051700	TKGA5170	
23、	PDP filter glass	31401051700	PAG42-01	
24、	PDP filter glass	31401042010	42P3-HI-3B	
25、	PDP filter glass	31070010100	SPC-S42-02	
26、	PDP filter glass	31070010110	SPC-L42-02	

PartⅥ:Factory mode setup and attention

1.Enter factory menu

(1) Enter child lock of main menu in TV mode, press “OK”, the password input box will appear;

(2) Use remote control to input the follows in order:7,red key,9,blue key, then you can enter factory mode menu. After entering factory mode menu, sign of the factory menu M will appear.

2.Factory menu and setup

(1) factory menu display is below:

M

Index: 1

HWUC_BRI 0x1F

The M denotes entering factory mode currently, the figures of index denotes the current adjustment index number, the HWUC_BRI denotes the name of current adjusting item, the 0X1F denotes the numerical value.

(1)Each adjusting item has only one unique index number ,the operator press the numeric key or press P+/P- directly.

(2) To Optional and adjustable items, the corresponding relation of index number and adjusting item is below:

(Index)	Item name	Item meanings	Operating key	remark
1	HWUC_BRI	UocIII subbrightness	V+/V-	adjust subbrightness
2	HWUC_SAT	UocIII saturation	V+/V-	adjust subsaturation
3	HWUC_CON	UocIII contrast	V+/V-	adjust subcontrast
4	HWUC_AGC	UocIII AGC	V+/V-	adjsut AGC
5	pipBrightness	7115 subbrightness	V+/V-	Open sub picture When adjusting it
6	PiVGAontrast	7115 contrast	V+/V-	Open sub picture When adjusting it
7	Balance	Sound balance	V+/V-	The adjusting value is 50, -50, 0
8	Volume	Sound Volume	V+/V-	Step is 10
9	Sound System	Sound System	V+/V-	DK/I/BG/M
10	Auto Search	Auto search	V+/ok	Source of Signal is TV
11	White Balance	White balance	V+/ok	
12	AutoColor	Auto color correct	V+/ok	Source of Signal VGA /YpbPr /TV
13	DVD	DVD preset	V+/V-	1 represent preset
14	BBE	BBE preset	V+/V-	1 represent preset
15	TruSurround	TruSurround preset	V+/V-	1 represent preset
16	SALESFOR	SALESFOR	V+/V-	Set sell country
17	Factory Out	initialization	V+/ok	factory set
18	GoldRatio	Golden ratio preset	V+/ok	

19	ClearEEProm	initialize EEPRom	V+/ok	Initialize the storage date
20	D Mode	Enter design mode	V+/ok	Can adjust all parameter of design mode
21	DPF	DPF preset	V+/V-	1 represent preset
22	BBE_CONT	BBE gain set	V+/V-	adjust BBE gain
23	BBE_PROC	BBE gain set	V+/V-	adjust BBE gain
24	Newcom	Newcom set	V+/V-	1 represent preset

Notice:

1、If no especial demand, please do not enter the 20th item(design mode);

2、When adjusting the 16th item , the storage data will be cleaned up, therefore, if not necessary , please do not adjust it, the items of index number 1,2,3,4,5,6 are not necessary to adjust.

3. The adjust method of factory menu

(1) Select the adjusting item

Operator can skip to the adjusting items by pressing the number key, also can select the adjusting item in the order of P+/P-. when pressing the number key, if the adjusting item is 1~9, input corresponding number keys and then press "OK", if the adjusting item is tens digit, input a tens digit number. For example, press number key 8 when adjusting the volume, you can see the color of index number to become green, then press "OK", the color of index number turns red, so you already selected corresponding volume adjusting item.

(2)Adjust method

Adjust it according to the operating key in above list. for one acting operation , press OK/V+. For example AutoColor, to some variable add/minus, example Volume, press V+/V- is ok.

(3)The description of white balance and AutoColor adjustment method

Index 11 corresponds to manual balance item , press "OK" or "V+", appear corresponding three variable, press "P+/P-" to select, press "V+/V-" to adjust, press menu key to exit.

The index number of AutoColor is 12, press "OK" or "V+" to do auto color correct, then the adjusted value will be displayed.

(4) BBE gain adjustment

Index number of BBE gain adjustment is 22 and 23, adjust it by pressing "V+/V-".

(5)You should press down the【display】 first before switching the program number in factory mode, press P+/P- to switch before the display content is disappeared;

(6)All menu functions are open in factory mode, if necessary you can use menu to check the items and effect test.

4. Factory debug item

（1）auto color correct（AutoColor）

You should finish auto color correct first before factory debug. Calibrate in TV、YPbPr and PC condition respectively.

① Required instrument

PC one suit

HD signal source one suit

②Debug (adjust in TV、YPbPr and PC condition respectively)

Set the channel in C-3 under TV mode, then do AutoColor.

Input full color stripe signal in YPBPR and do AutoColor.

Input window signal in PC, the window is white, surround is black signal. The result will appear on screen after AutoColor adjustment, make the adjustment results of Rgain、Ggain and Bgain close to 0×80 in TV condition, if the difference is too great, adjust the value of HWUC_CON (subsaturation),and adjust the AutoColor again.

(2)White balance, color temperature adjustment

①Required instrument

CHROMA 7120 color analyze instrument(or same function instrument, contain color coordinate - chroma conversion card) one suit

White balance adjusting implement(request the video output range 0-1V is adjustable,750hm load) one suit

②Prepare

A. connect all equipment, switch the condition of PDP TV to AV.

B. Set the picture quality of PDP TV in standard condition

C. Set the distance between light receiver of white balance to center place of PDP display screen is 15cm±3cm .

D. Make sure that the environmental brightness is below 2cd/m^2

③White balance, color temperature adjustment

Before adjusting it, put the first PDP TV in AV condition, and the image in standard condition, make white balance adjust implement output the white signal to AV terminal, adjust output level of balance adjust implement, make the brightness of the PDP TV is 200±20cd/m^2 (use CHROMA 7120 color analyze instrument to obtain the brightness value),then fix the video output level of white balance adjust implement(until all the PDP TV are adjusted).

Enter white balance adjusting item of factory mode, change R,G,B value(try best to adjust this 3 value biggest) .

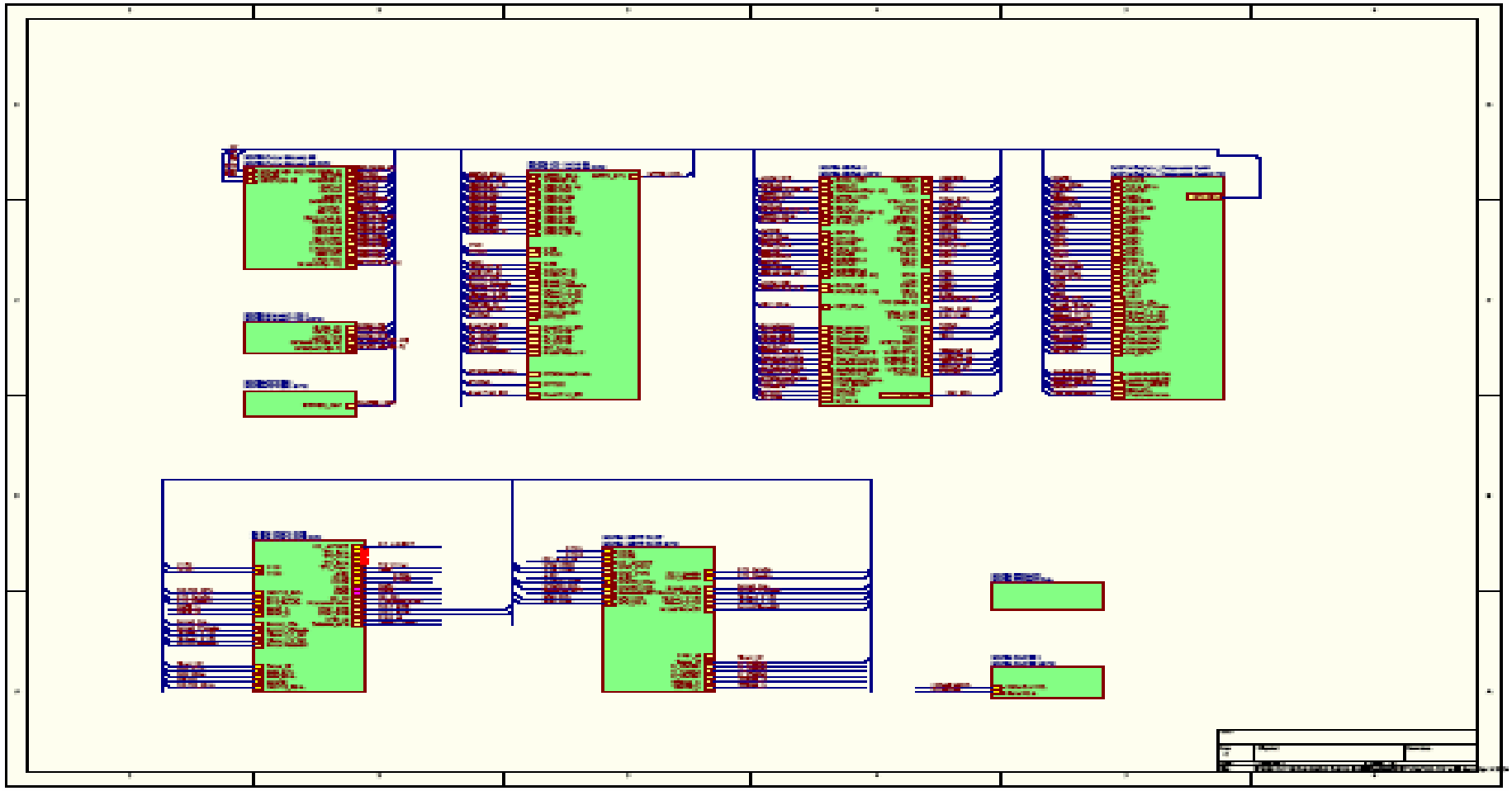
Make color temperature coordinate value like the value of above table(tolerance ±4%) :

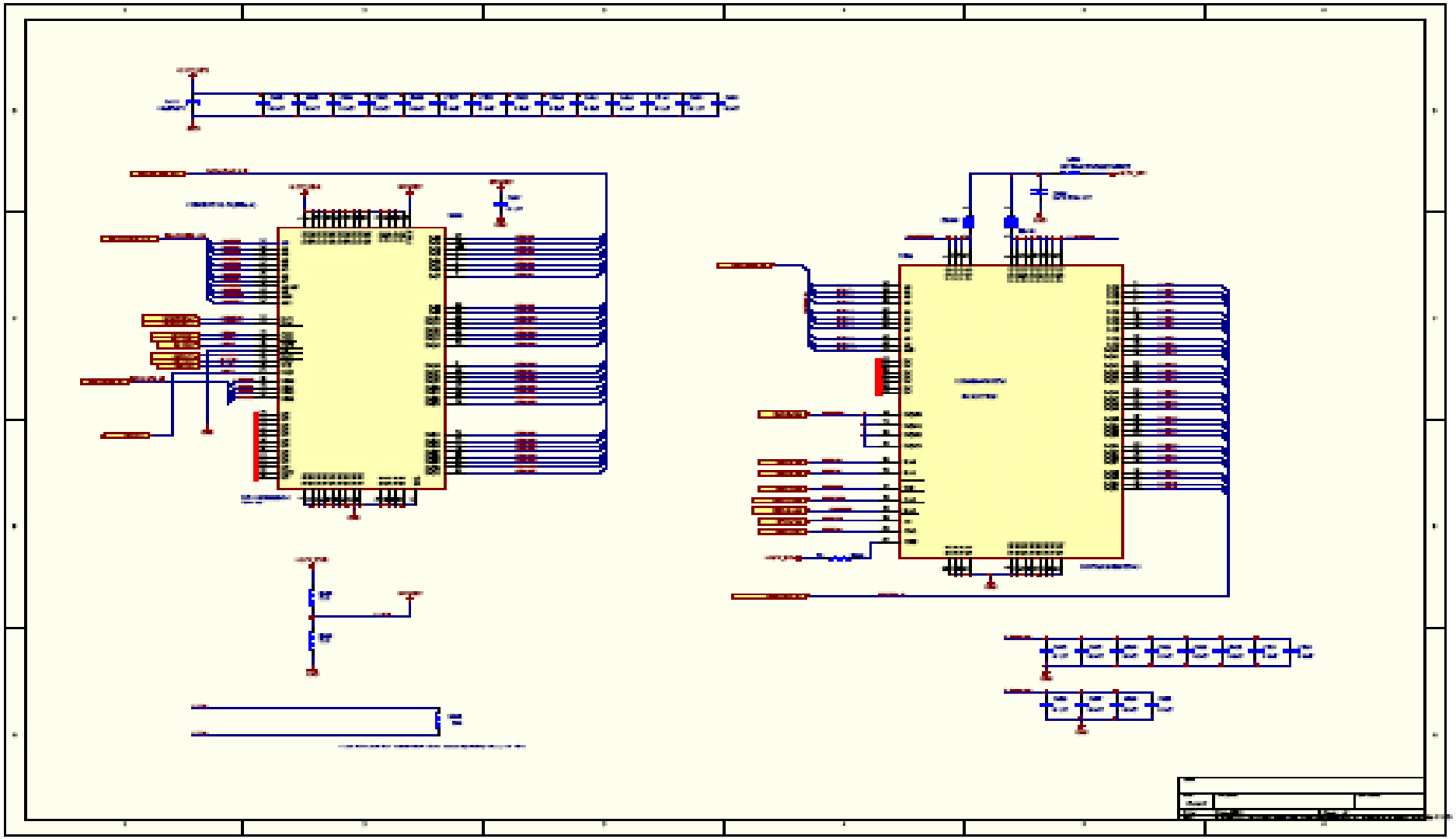
Z	X	Y
K12000	0.270	0.277

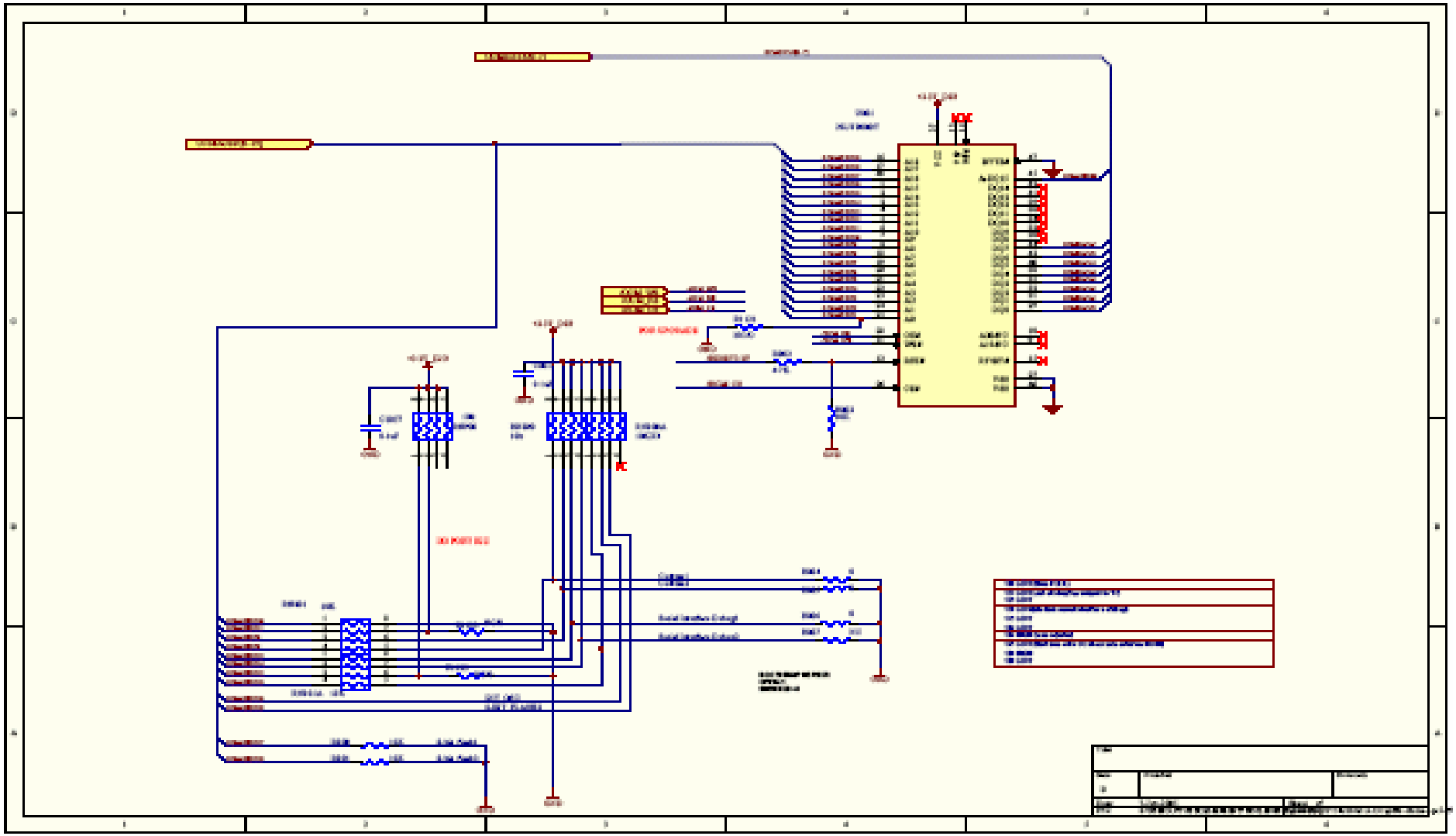
Attention：After the color temperature and color coordinate are satisfied with above request, you should judge if exist phenomenon of partial color, namely if the value of Δuv is 0 or not. Partial color phenomenon occur if Δuv is not 0 , adjust R,G,B value to 0 again, and make it satisfy color coordinate request.

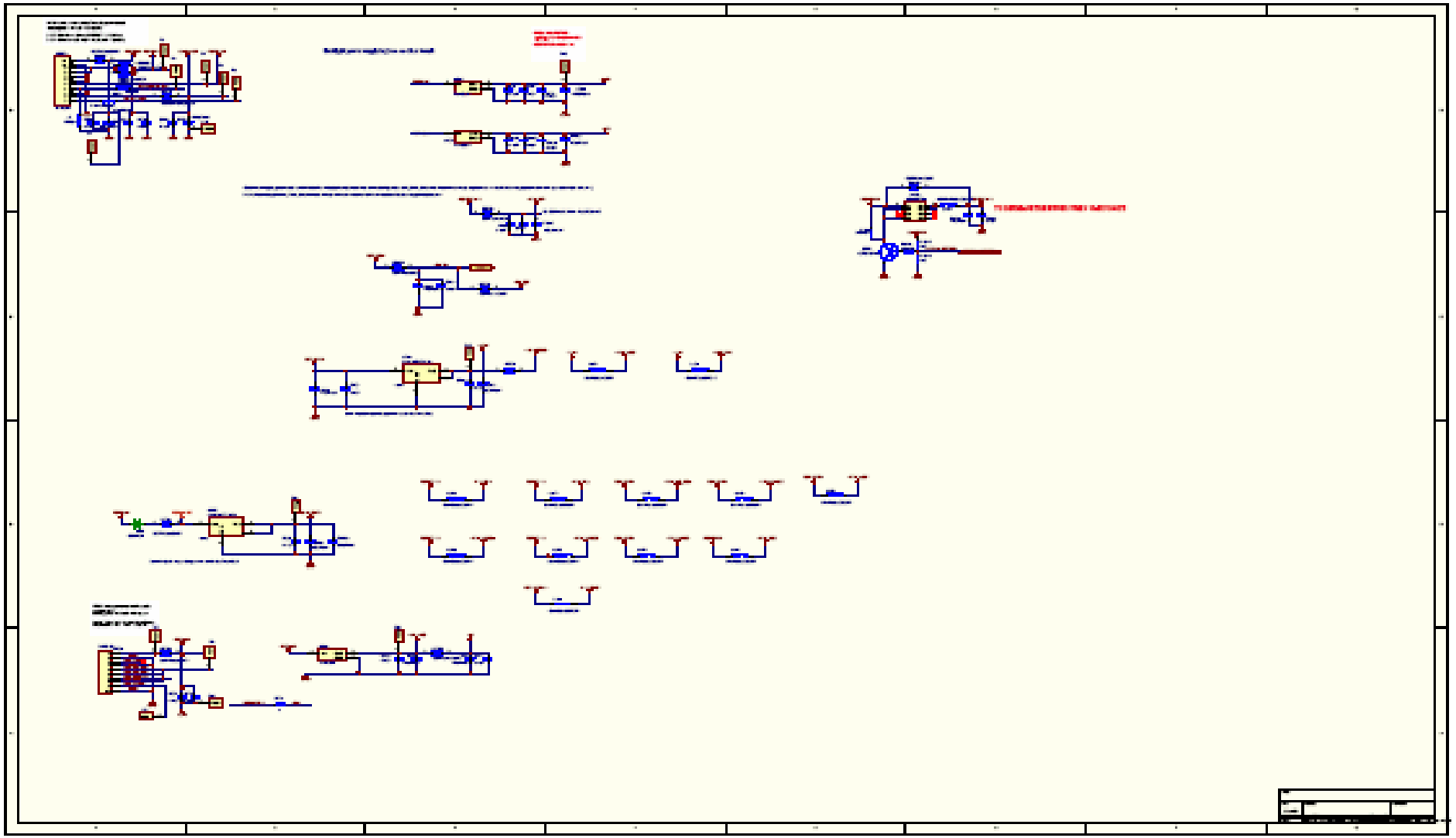
Annex 1、Circuit schematic diagram of PT4216

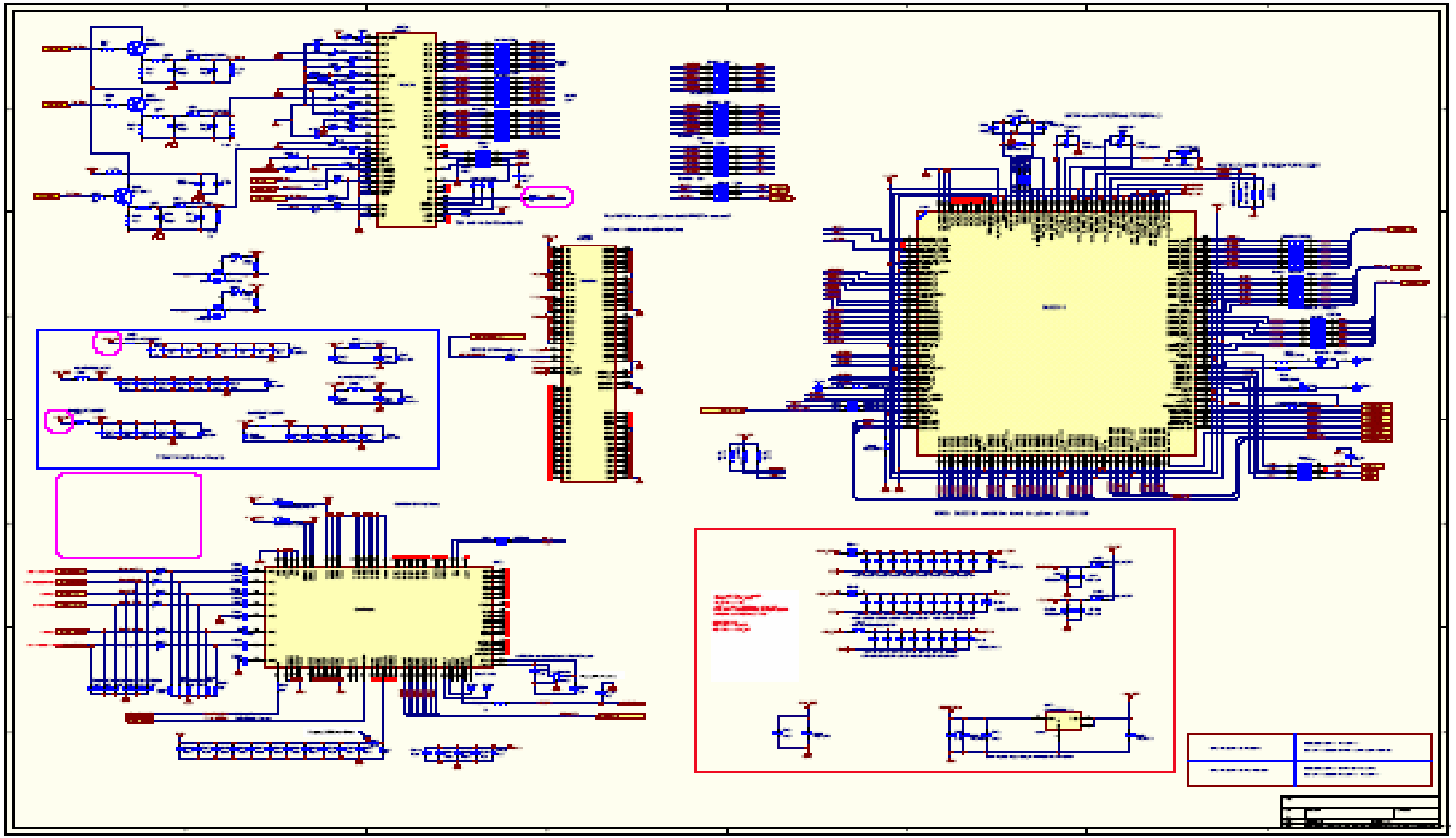
Main board

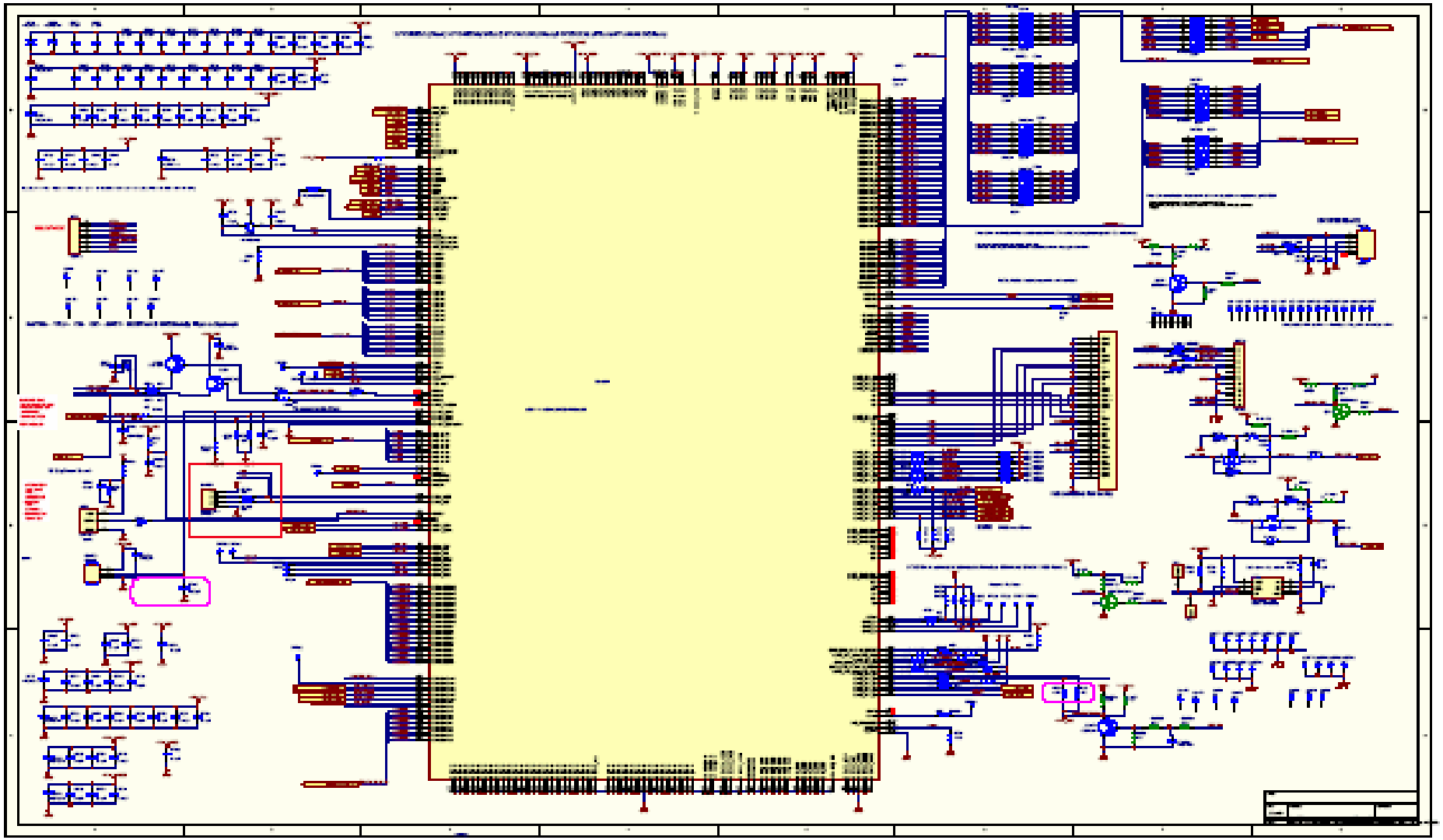


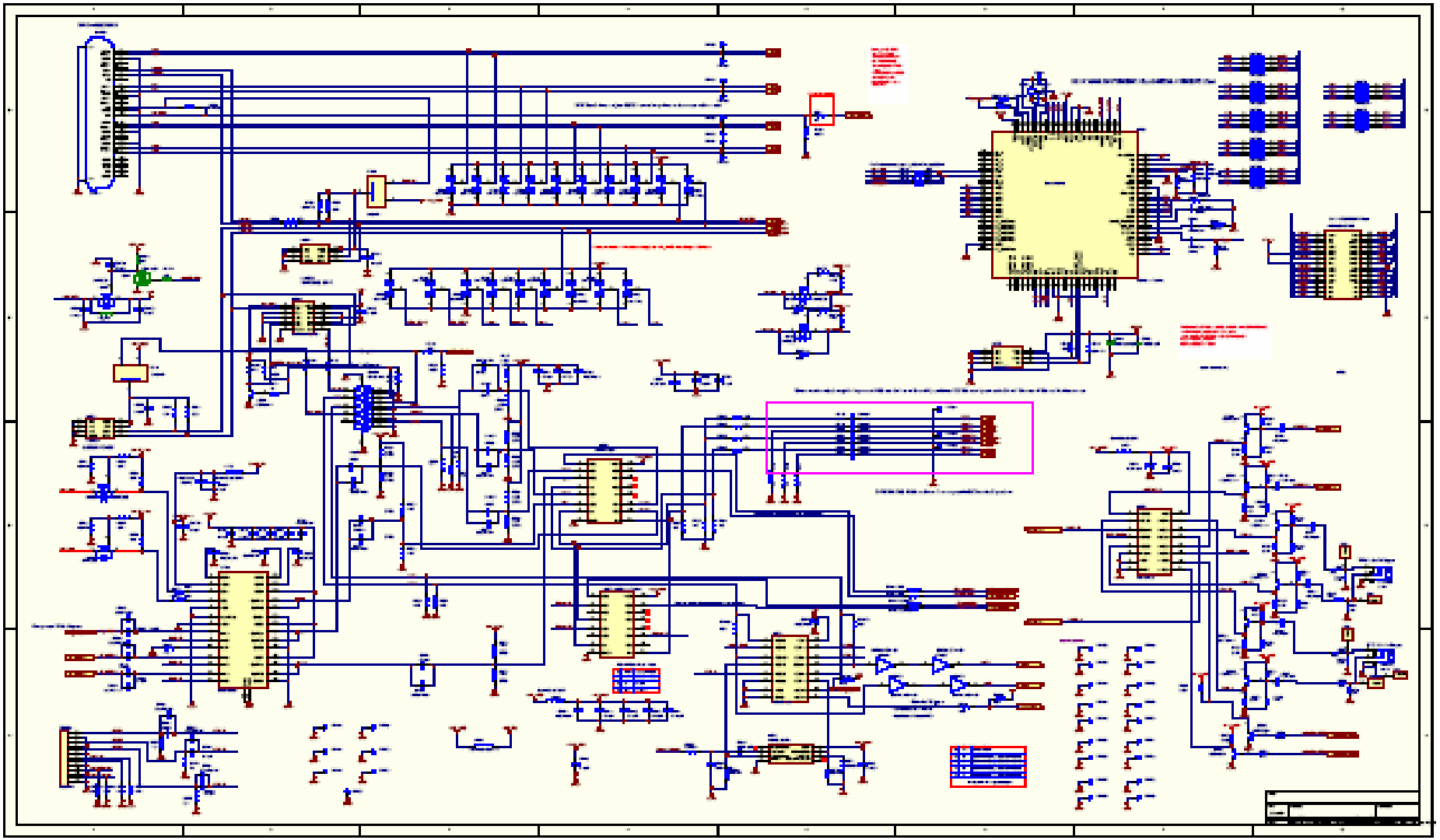


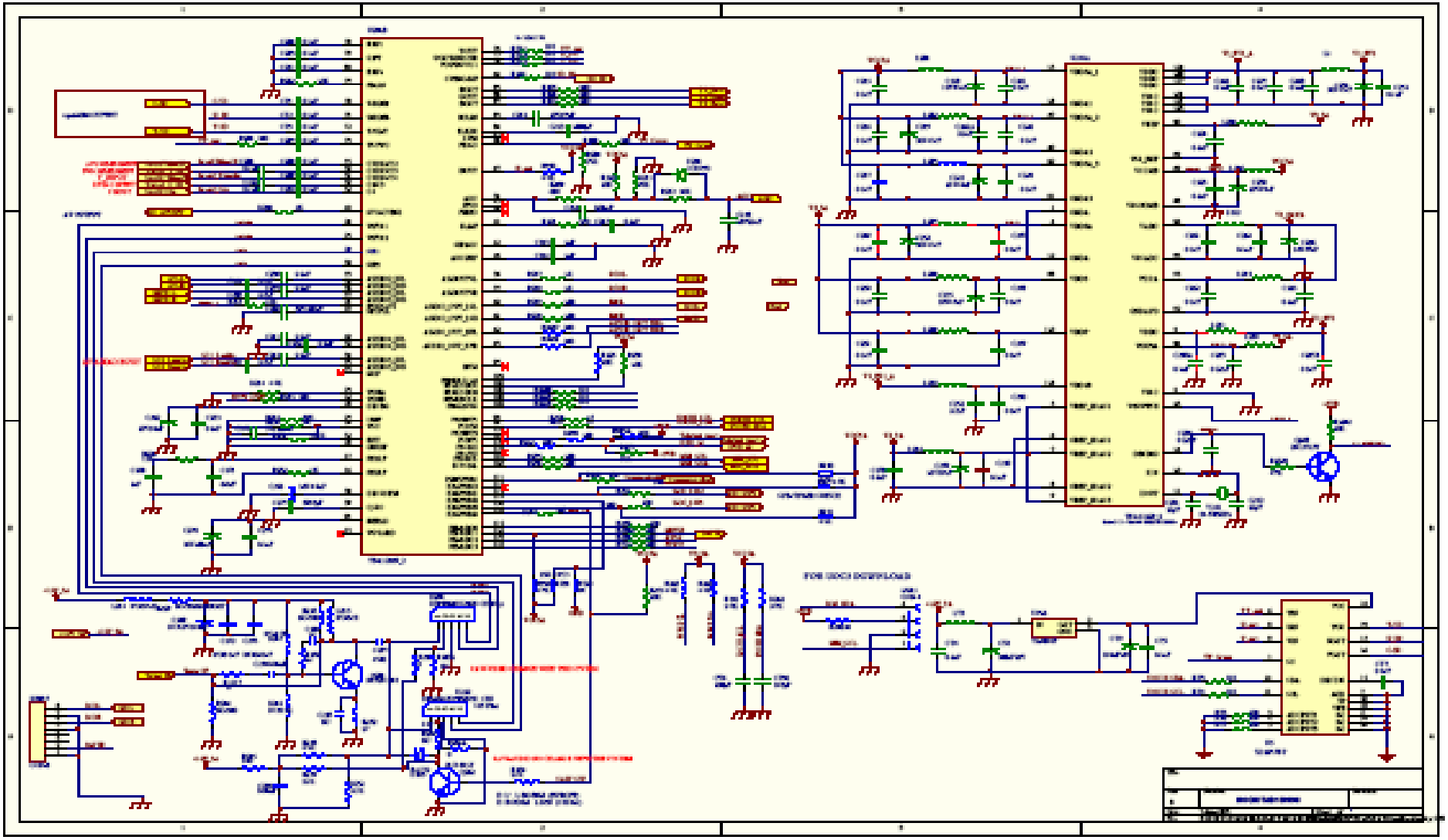


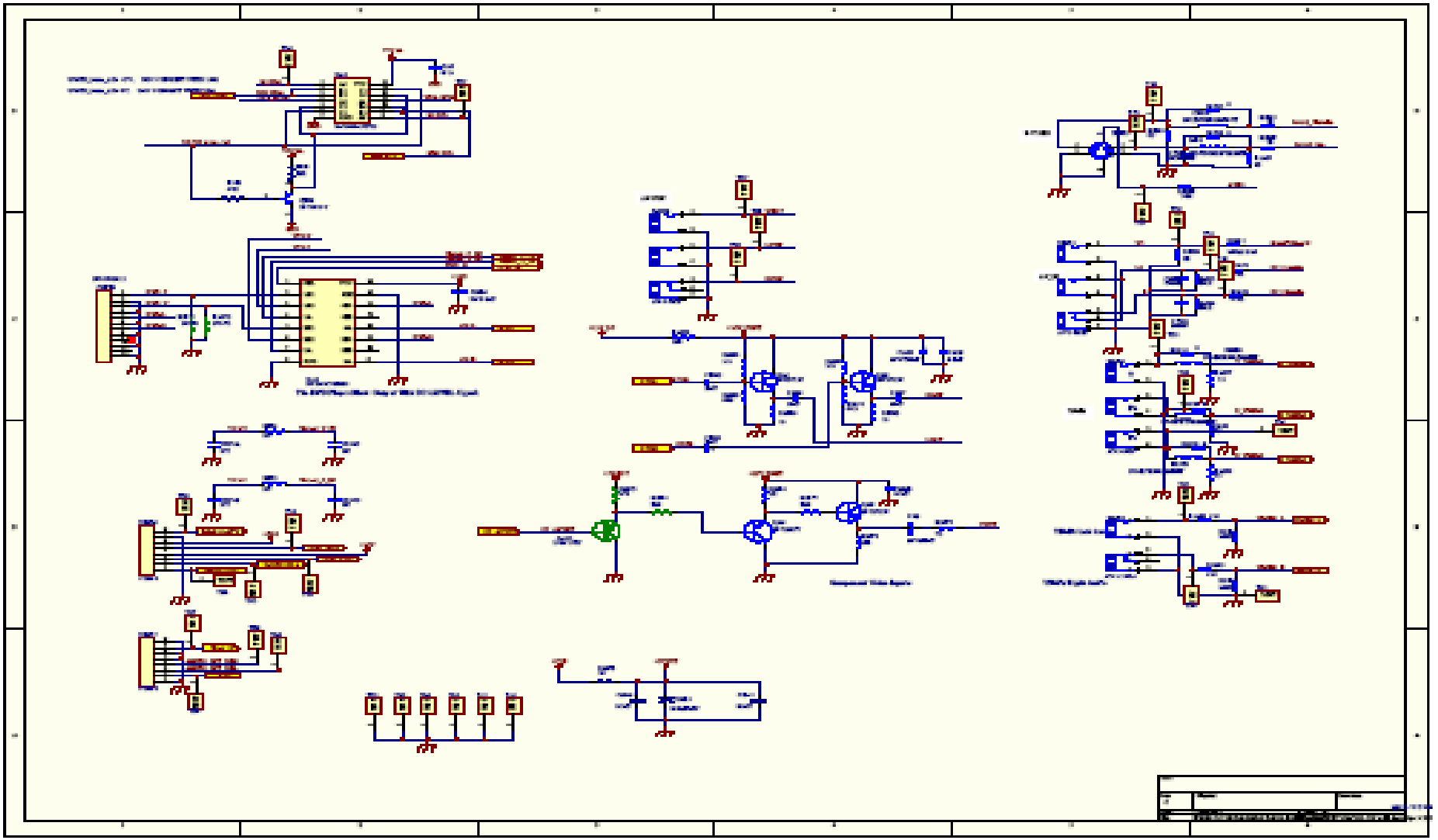


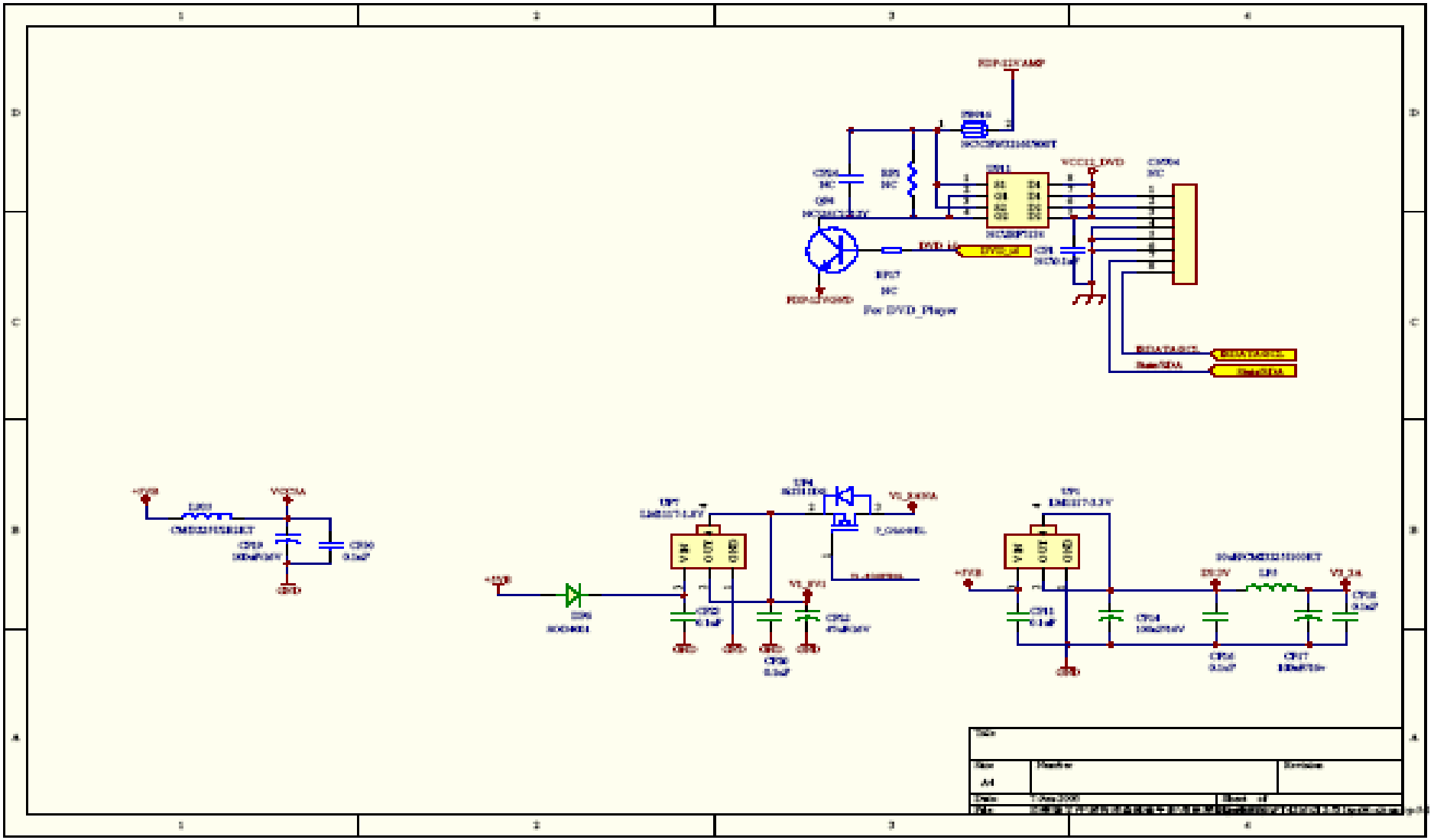


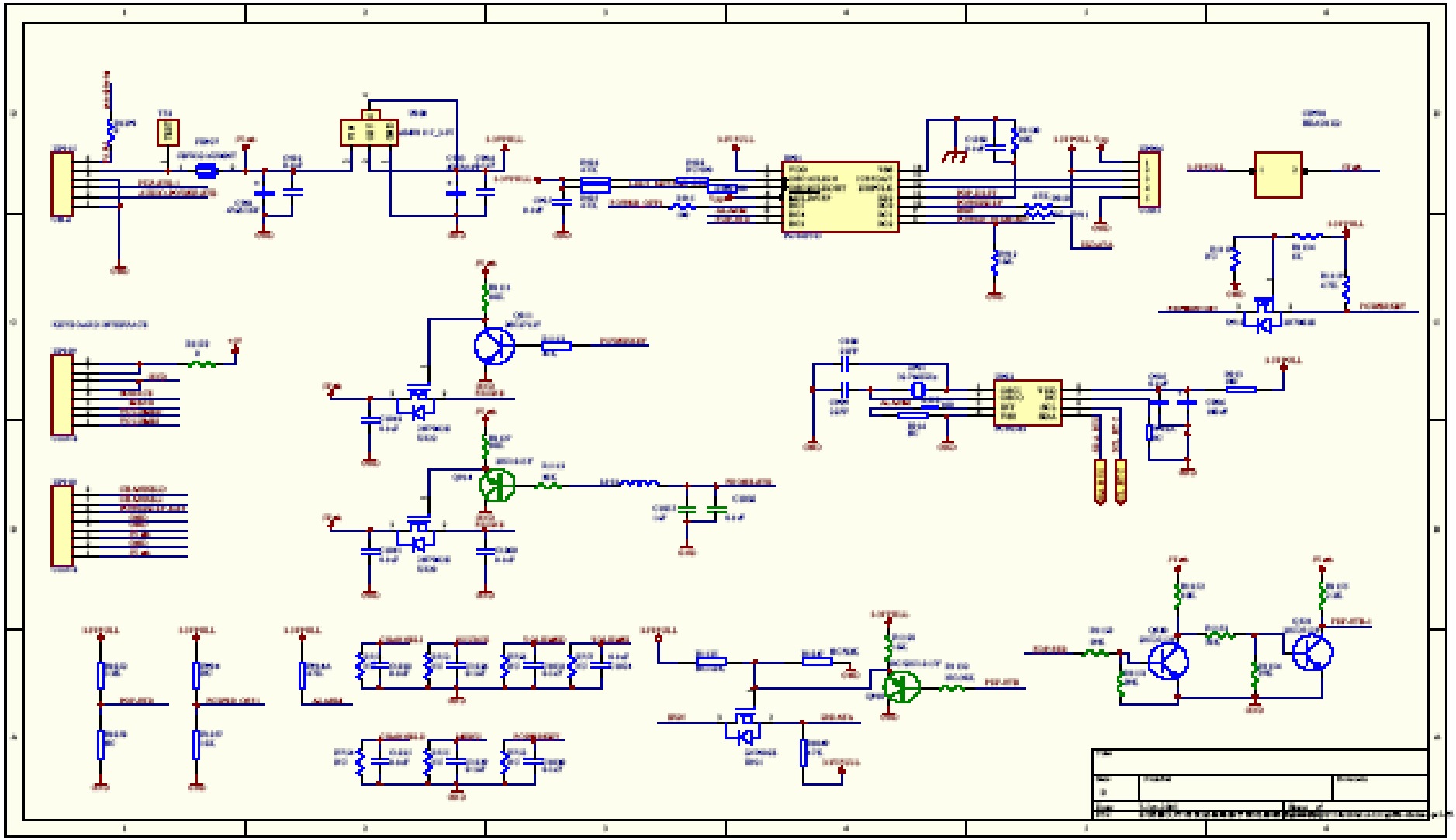




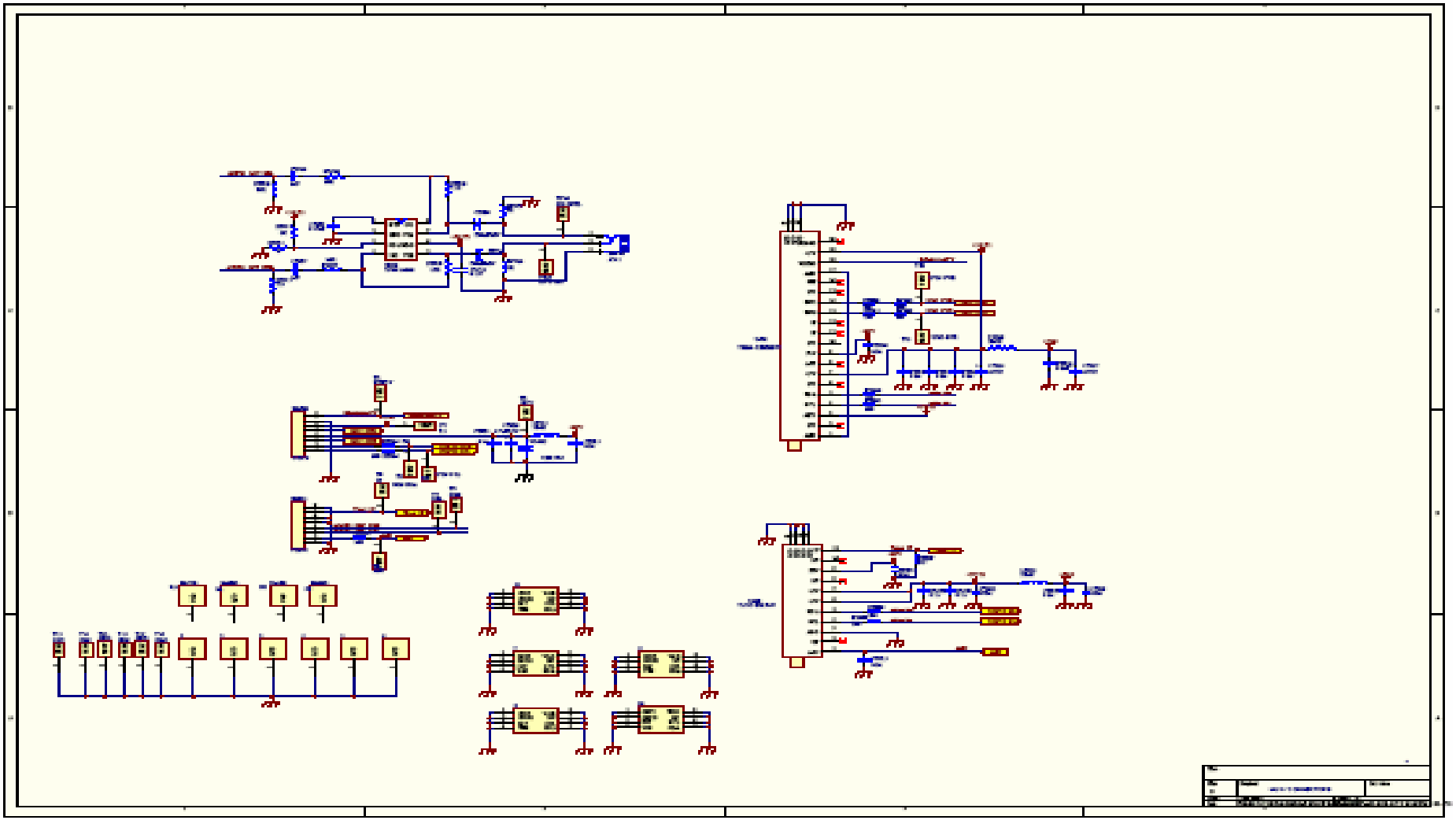




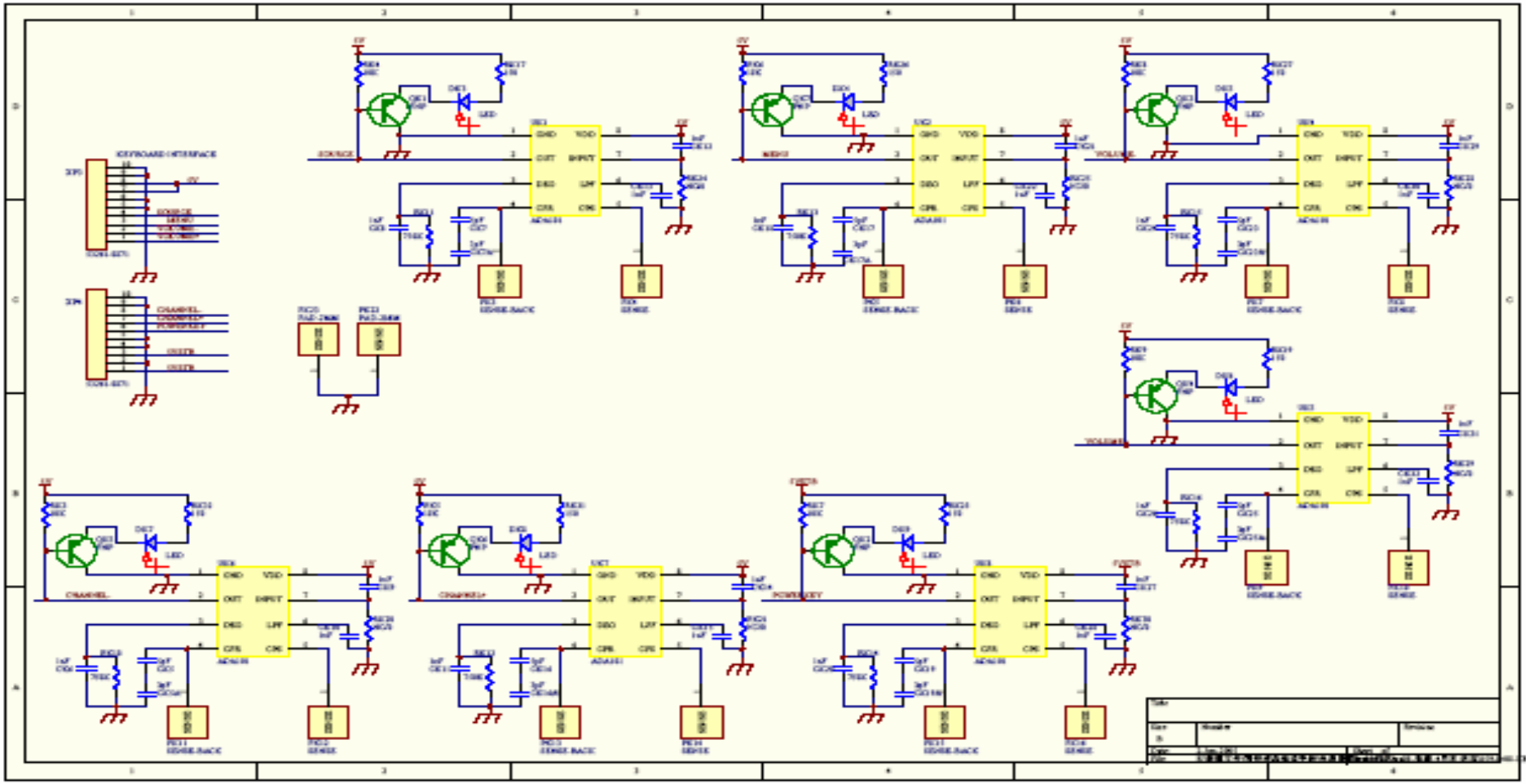

For DVD_Player



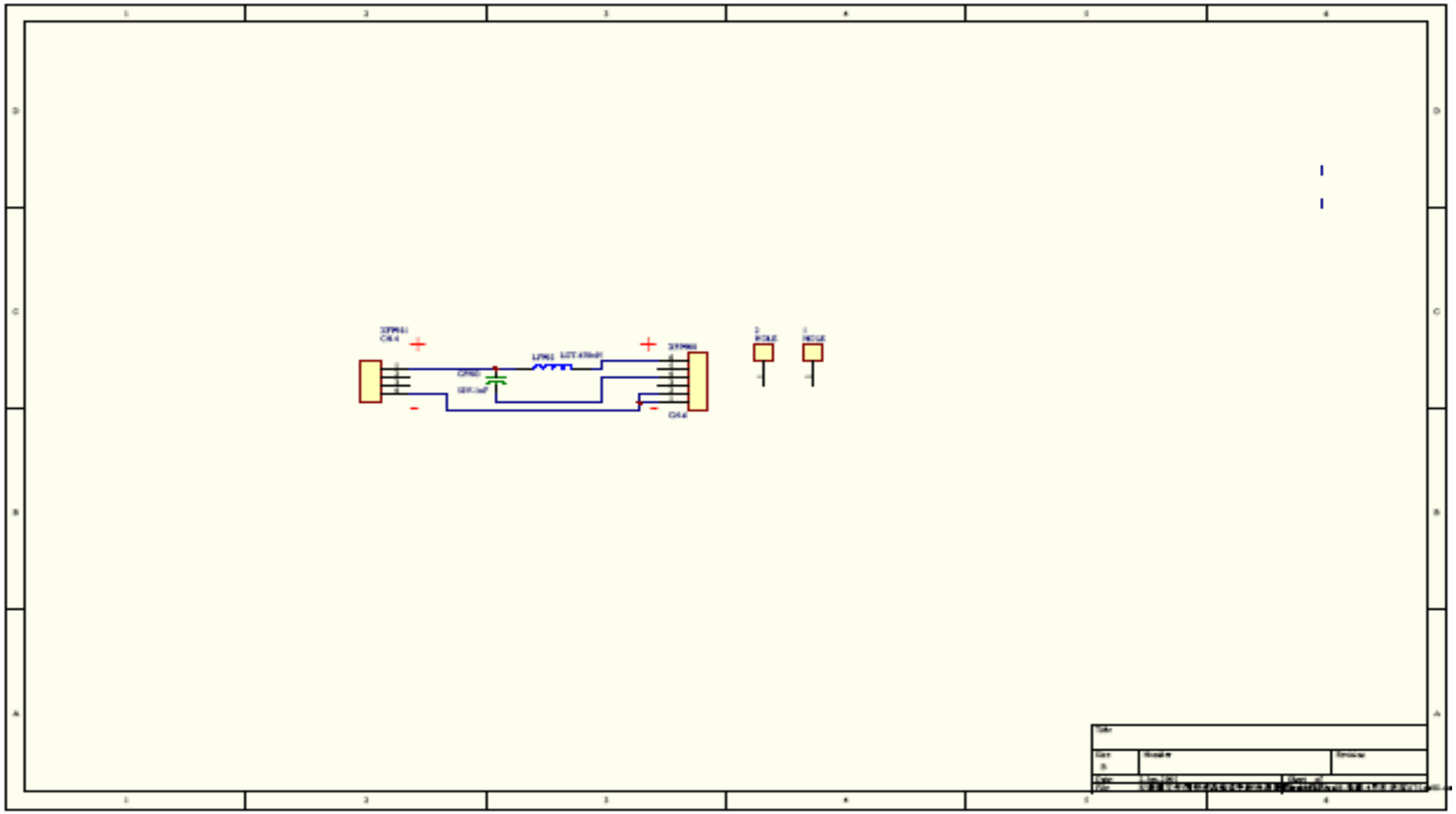
AV board



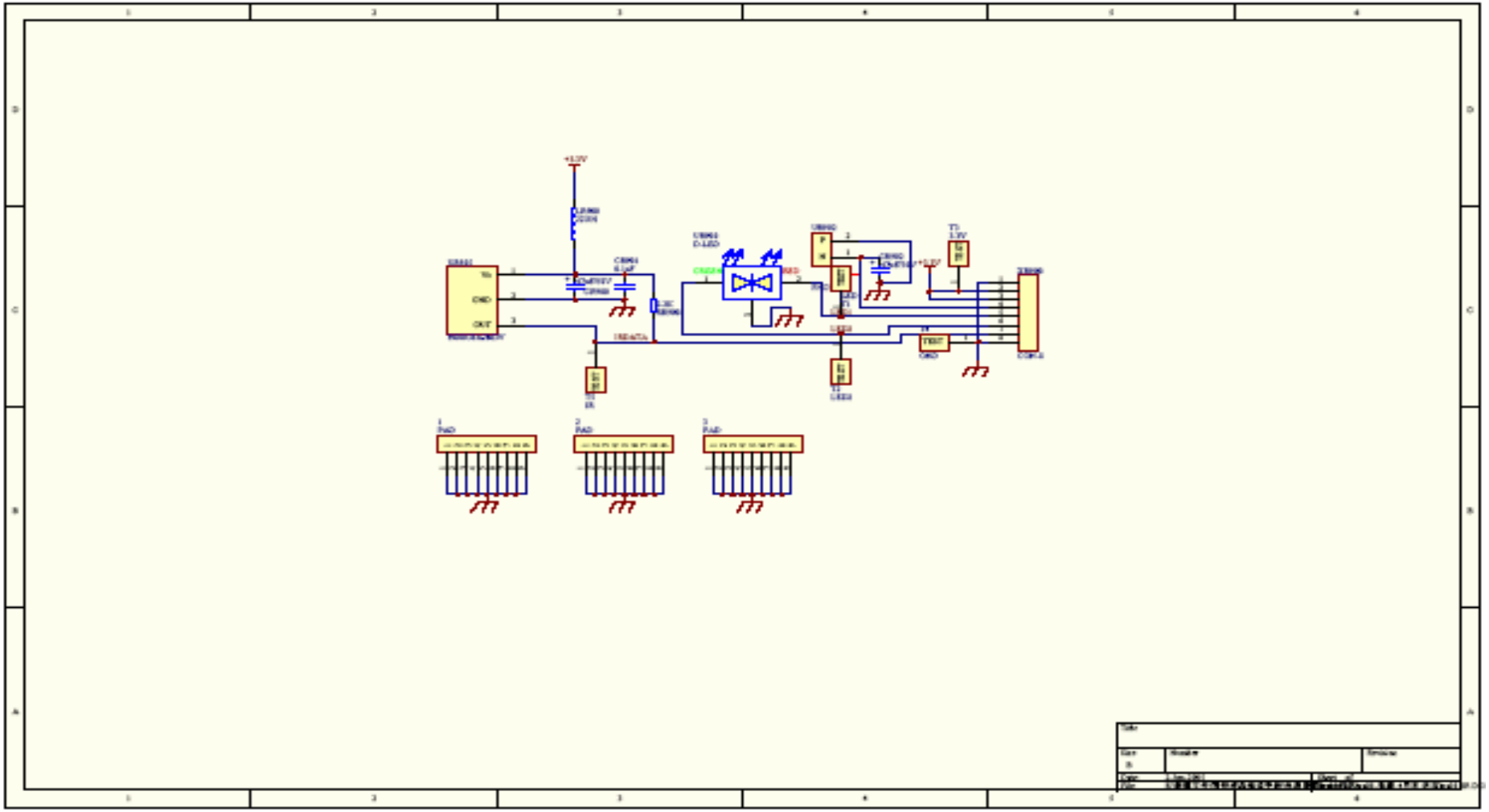
K board



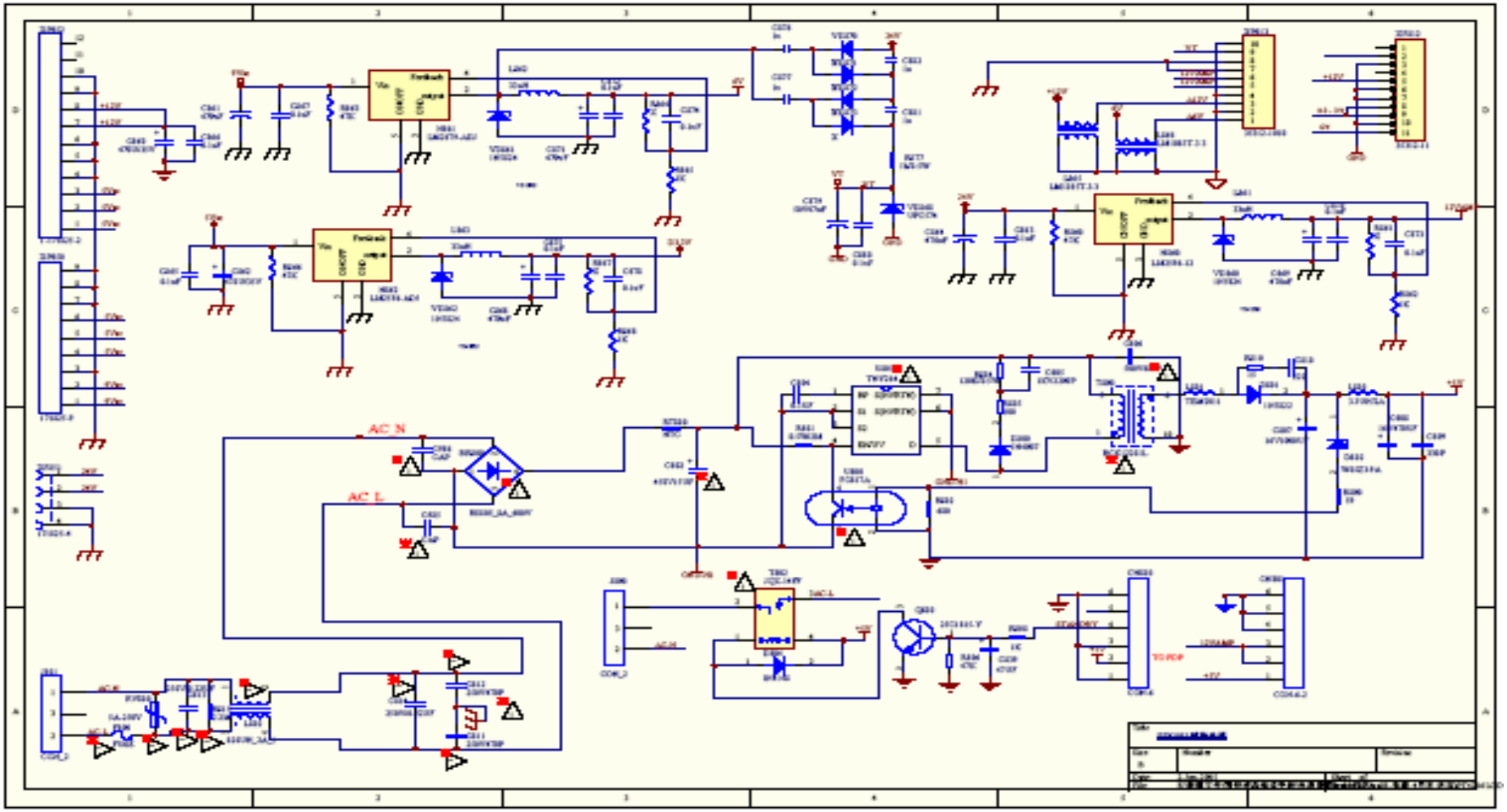
Divide frequency board



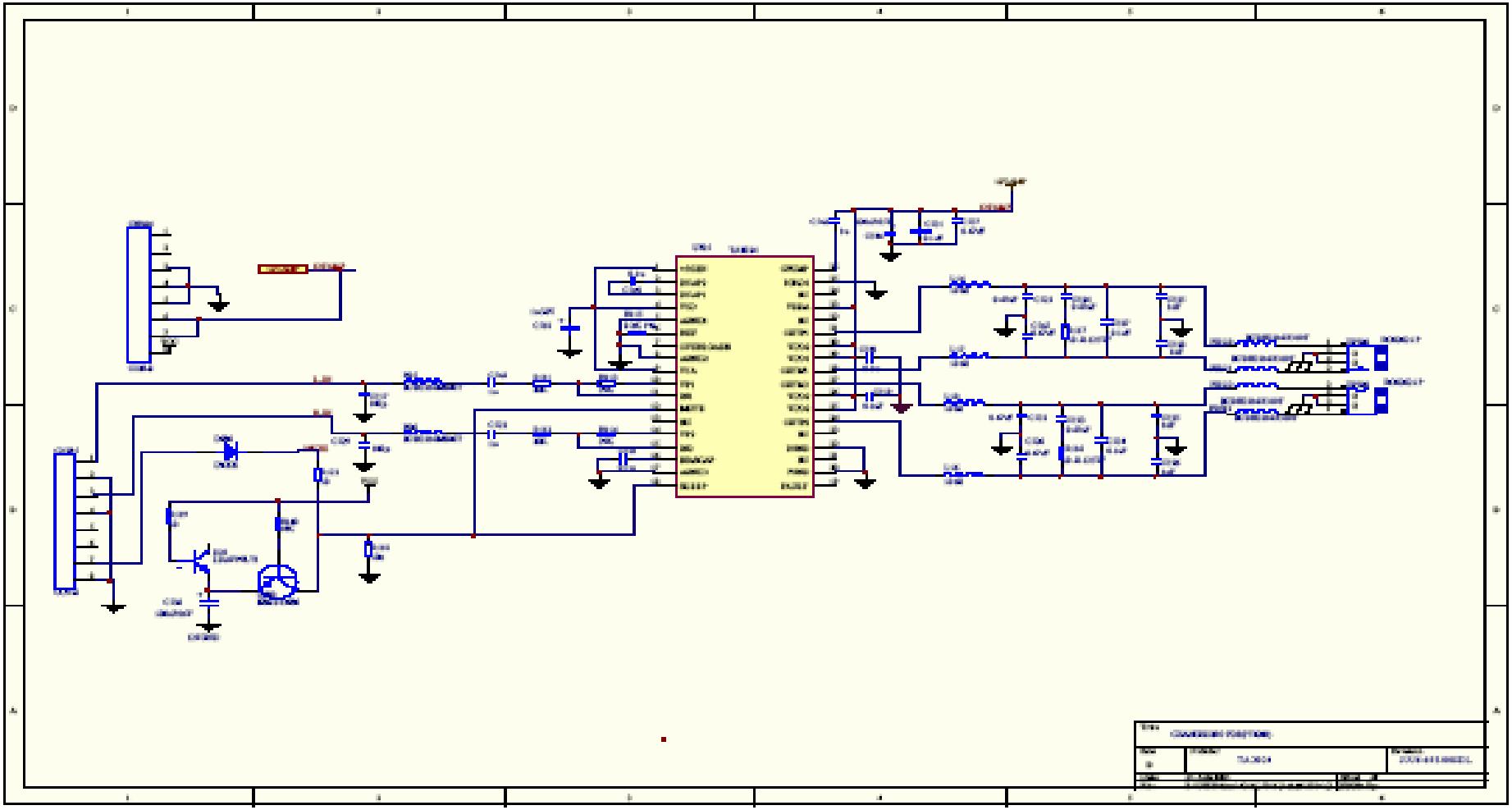
Remote control receiving board



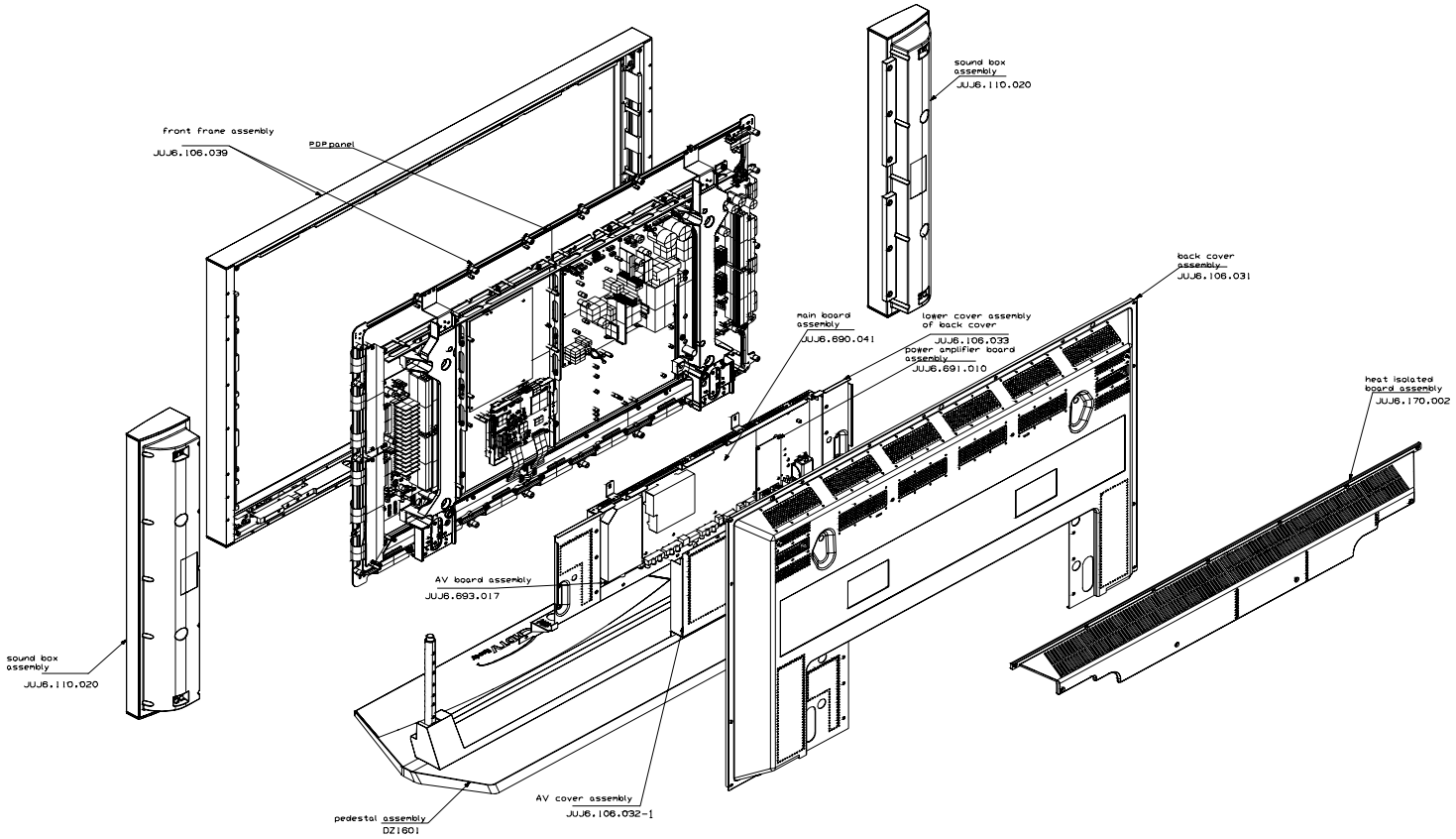
LG panel power board



PT4216 power amplifier board



Annex 2:Final assembly diagram of PT4216



Annex 3:Final wiring connection diagram of PT4216