

G320

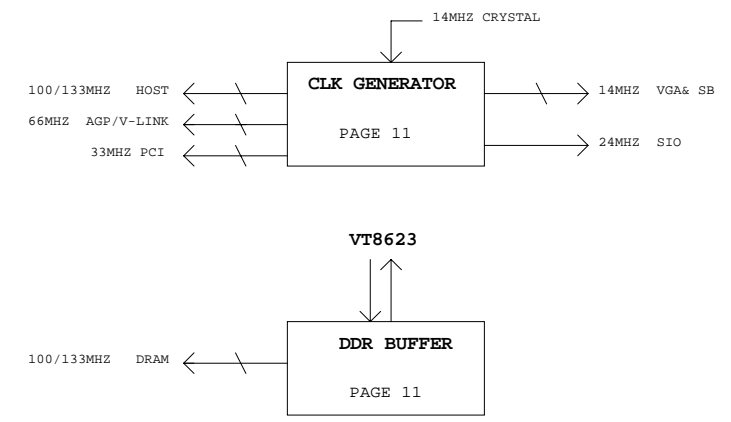
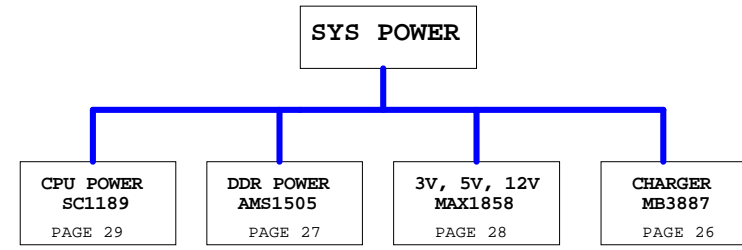
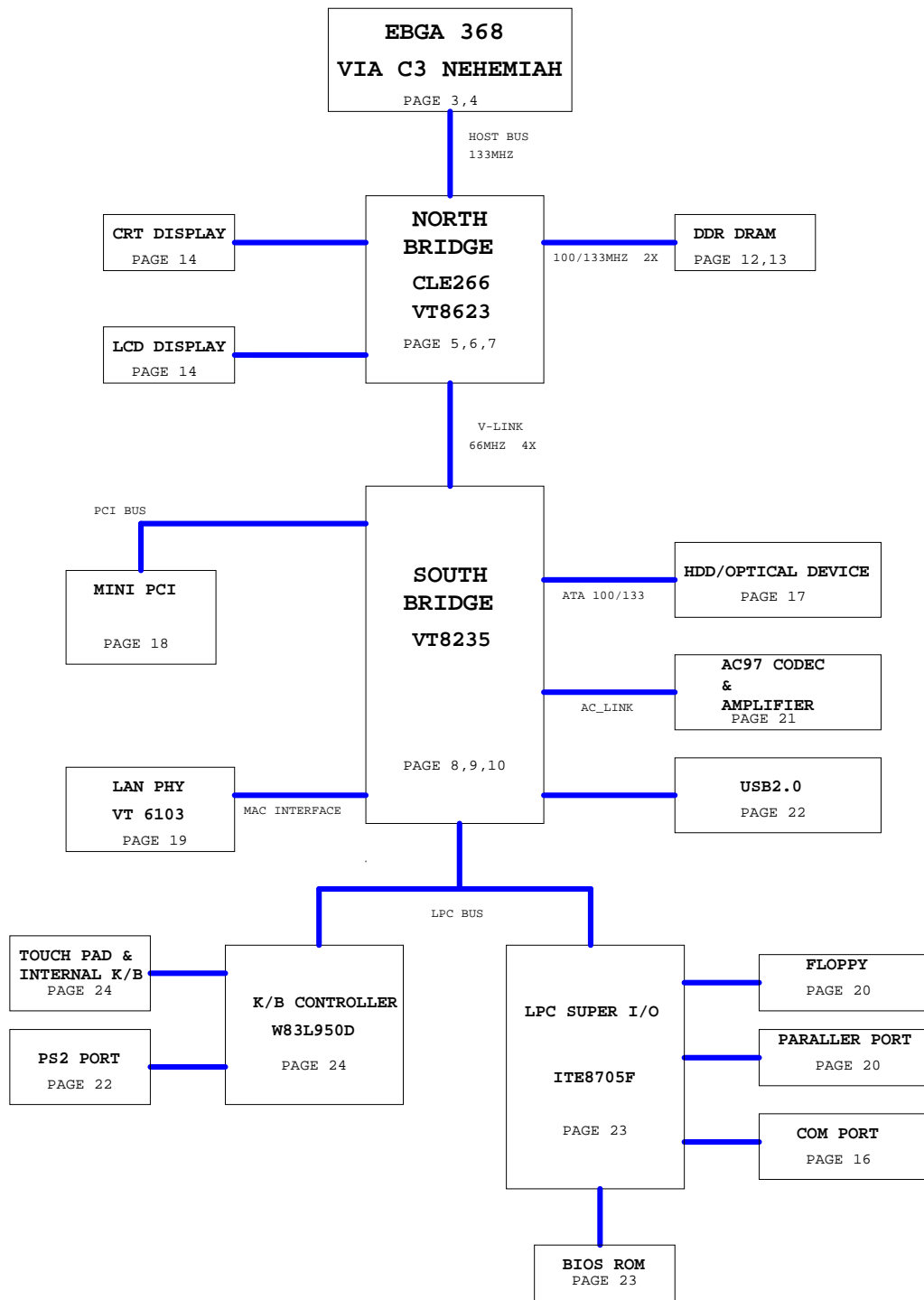
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15-F35-011000 V1.0
15-F35-012000 V2.0

ELITEGROUP COMPUTER SYSTEM CO., LTD.			
Title			
DESCRIPTION			
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VIA C3 PROCESSOR

4.5 HA[3..31] >> HA[3..31]
 4.5 HD[0..63] >> HD[0..63]

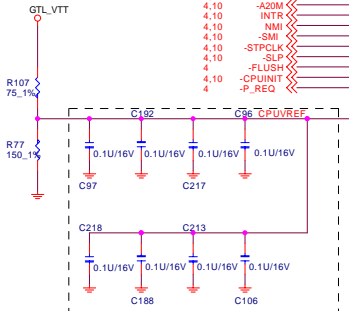
VIA C3 EPGA 376

- HA3 AD6
- HA4 AD9
- HA5 AD5
- HA6 AD7
- HA7 AE10
- HA8 AE8
- HA9 AE9
- HA10 AE3
- HA11 AE9
- HA12 AD4
- HA13 AE5
- HA14 AE10
- HA15 AE4
- HA16 AE6
- HA17 AD2
- HA18 U2
- HA19 AB3
- HA20 Y3
- HA21 AC1
- HA22 AB1
- HA23 Y2
- HA24 W3
- HA25 AC3
- HA26 T2
- HA27 V1
- HA28 AF2
- HA29 U1
- HA30 V2
- HA31 AA1

- 4.5 -ADS <<-ADS AE20
- 4.5 -DRDY <<-DRDY AD18
- 4.5 -DBSY <<-DBSY AD19
- 4.5 -HTRDY <<-HTRDY AE18
- 4.5 -HREQ0 <<-HREQ0 AD11
- 4.5 -HREQ1 <<-HREQ1 AE12
- 4.5 -HREQ2 <<-HREQ2 AE11
- 4.5 -HREQ3 <<-HREQ3 AD20
- 4.5 -BREQ0 <<-BREQ0 AD12
- 4.5 -BREQ1 <<-BREQ1 AD12
- 4.5 -BPR <<-BPR AF9
- 4.5 -BNR <<-BNR AF9
- 4.5 -HLOCK <<-HLOCK AE17
- 4.5 -HIT <<-HIT AD16
- 4.5 -DEFER <<-DEFER AE18
- 4.5 -RS0 <<-RS0 AD16
- 4.5 -RS1 <<-RS1 AD16
- 4.5 -RS2 <<-RS2 AE19
- 4.5 -CPURST <<-CPURST T3

For Longhaul stability issue
 C187 33p/50V

- 4.10 -FERR <<-FERR T24
- 4.10 -IGNNE <<-IGNNE W26
- 4.10 -A20M <<-A20M A20M
- 4.10 INTR <<-INTR H24
- 4.10 NMI <<-NMI A225
- 4.10 -SMI <<-STPCLK Y24
- 4.10 -STPCLK <<-SLP AD21
- 4.10 -FLUSH <<-FLUSH U25
- 4.10 -CPUNIT <<-CPUNIT AA26
- 4.10 -P_REQ <<-P_REQ U26



Use 0603 Packages and distribute within 500 mils of CPUVREF inputs (1 cap for every 1 input)

- D23 VREF0
- D18 VREF1
- G4 VREF2
- L4 VREF3
- R4 VREF4
- AA4 VREF5
- AC9 VREF6
- AC16 VREF7
- V28 VTT
- AE4 VTT
- AD8 VTT
- AD13 VTT
- AD22 VTT
- AA3 VTT
- U3 VTT
- T26 VTT
- P3 VTT
- G2 VTT
- C26 VTT
- E24 VTT
- C10 VTT
- C13 VTT
- C18 VTT
- C21 VTT

C3_EPGA376

AP1	W4	AP3	U24
AP7	W5	AP8	U1
AP11	W25	AP12	U22
AP15	W4	AP16	U23
AP19	W1	AP20	U26
AP23	L23	AP4	P3
AP26	L26	AP7	P4
AP1	U3	AP22	P24
AP2	U4	AP24	E1
AP5	U25	AP2	E8
AP25	W4	AD10	E13
AP26	W5	AD14	E23
AD3	W26	AD18	D2
AD17	U1	AD26	D4
AD24	U23	AC2	D5
AC5	U24	AC4	D8
AC7	P23	AC6	D9
AC8	P25	AC10	D12
AC12	E2	AC11	D13
AC13	E4	AC14	D17
AC16	E14	AC18	D20
AC17	E19	AC19	D21
AC20	E25	AC23	D24
AC21	D6	AC25	C1
AB2	D7	AB4	C9
AB8	D10	AB14	C17
AB13	D11	AB19	C25
AB23	D44	AB23	E3
AB25	D15	Y23	E16
Y1	D18	W2	E23
W4	D19	W5	E4
Y26	D22	V3	AT
W1	D25	W4	A11
W4	C3	U23	E15
W5	C14	U24	A19
W22	C26	T1	A24
W23	E2	R2	A25
W23	E5	R25	
W24	E22	P4	
U4	E25	P5	
N22	E2	N24	
N26	A1	N24	
R1	A8	M1	
P22	A12	L2	
P23	A16	E3	
P24	A20	K4	
K25	E26	K25	
W3	E26	K26	

BR4	BR3	BR2	BR1	BR0	RATIO
0	0	0	0	0	9.0x
0	0	0	0	1	3.0x
0	0	0	1	0	4.0x
0	0	0	1	1	10.0x
0	0	1	0	0	5.5x
0	0	1	0	1	3.5x
0	0	1	1	0	4.5x
0	0	1	1	1	9.5x
0	1	0	0	0	5.0x
0	1	0	0	1	7.0x
0	1	0	1	0	8.0x
0	1	0	1	1	6.0x
0	1	1	0	0	12.0x
0	1	1	0	1	7.5x
0	1	1	1	0	8.5x
0	1	1	1	1	6.5x
1	0	0	0	0	11.0x
1	0	0	1	0	12.0x
1	0	1	0	0	11.5x
1	0	1	0	1	12.5x
1	0	1	1	0	10.5x
1	0	1	1	1	14.0x
1	1	0	0	0	15.0x
1	1	0	1	0	16.0x
1	1	1	0	1	14.0x
1	1	1	1	0	15.5x
1	1	1	1	1	14.5x

CPU Default setting 1GHz (133X7.5)

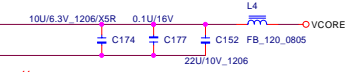


- D0 R3 HD0
- D1 N1 HD1
- D2 H2 HD2
- D3 P1 HD3
- D4 M2 HD4
- D5 M2 HD5
- D6 M2 HD6
- D7 D3 HD7
- D8 M3 HD8
- D9 H1 HD9
- D10 C3 HD10
- D11 K2 HD11
- D12 K2 HD12
- D13 H1 HD13
- D14 P2 HD14
- D15 H2 HD15
- D16 C4 HD16
- D17 J2 HD17
- D18 B1 HD18
- D19 E3 HD19
- D20 A3 HD20
- D21 B9 HD21
- D22 A2 HD22
- D23 D1 HD23
- D24 C5 HD24
- D25 B4 HD25
- D26 B12 HD26
- D27 C7 HD27
- D28 C7 HD28
- D29 C2 HD29
- D30 A6 HD30
- D31 A6 HD31
- D32 D3 HD32
- D33 C6 HD33
- D34 C8 HD34
- D35 B6 HD35
- D36 B10 HD36
- D37 A10 HD37
- D38 A9 HD38
- D39 C11 HD39
- D40 C15 HD40
- D41 A14 HD41
- D42 B13 HD42
- D43 B8 HD43
- D44 C12 HD44
- D45 B11 HD45
- D46 B20 HD46
- D47 B15 HD47
- D48 B18 HD48
- D49 A22 HD49
- D50 B14 HD50
- D51 B17 HD51
- D52 A21 HD52
- D53 A21 HD53
- D54 B18 HD54
- D55 A18 HD55
- D56 A23 HD56
- D57 C19 HD57
- D58 B11 HD58
- D59 A17 HD59
- D60 C23 HD60
- D61 B24 HD61
- D62 C22 HD62
- D63 C16 HD63



	BSEL1	BSEL0
66MHZ	0	0
100MHZ	0	1
133MHZ	1	1

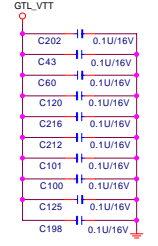
- BCLK M23 <<<CPUCLK 11
- BSEL0 AF24 <<-BSEL0
- PWRGOOD AE17 <<<PWRGD_CPU 25
- RSEL AE22 <<-BSEL1
- THERMDP AE21 <<<DTD+ 23
- THERMON AC24 <<<DTD- 23
- VID0 AC26 <<<CPUVID0 29
- VID1 AB24 <<<CPUVID1 29
- VID2 AA24 <<<CPUVID2 29
- VID3 AB26 <<<CPUVID3 29
- VID4 R24 <<<CPUVID4 29
- BR0 P26 BR0
- BR1 N26 BR1
- BR2 M26 BR2
- BR3 E26 BR3
- BR4 T23 VCORE PLL1
- PLL1 T23 VCORE PLL2
- PLL2
- CPICD0 M24 APICD0 <<<APICD0 4.10
- CPICD1 M24 APICD1 <<<APICD1 4.10
- CPICLK C20 <<<CPICLK 11
- NCHCTRL K24 NCHCTRL R286 <<<14.1%
- RTTCTRL J23 RTTCTRL R47 <<<SB_NC
- C26 DIVIDEN R49 <<<0_NC
- GT_L_VTT



- VTT E8 <<<GT_L_VTT
- E18 VTT
- J5 VTT
- J22 VTT
- U5 VTT
- V22 VTT
- AB6 VTT
- AB18 VTT

- CPICLK C80 <<<10P/50V_NC
- SMI C214 <<<56P_NC
- STPCLK C199 <<<56P_NC
- SLP C215 <<<56P_NC
- CPUNIT C223 <<<56P_NC
- INTR C99 <<<56P_NC
- FERR C195 <<<56P_NC
- IGNNE C200 <<<56P_NC
- A20M C197 <<<56P_NC

CPU VTT Decoupling Caps X 10 Pcs

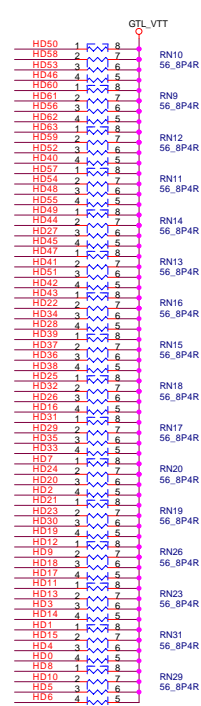
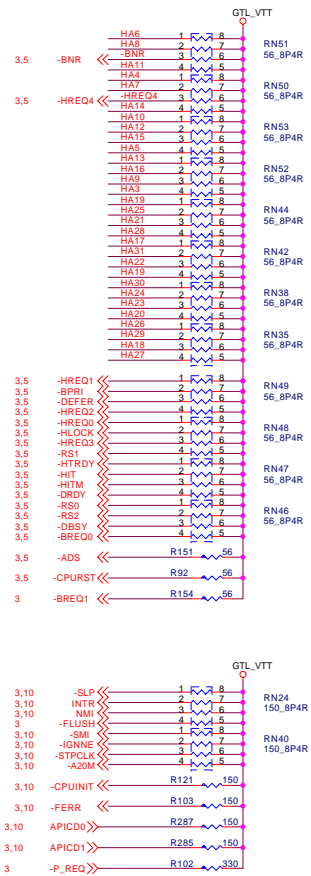


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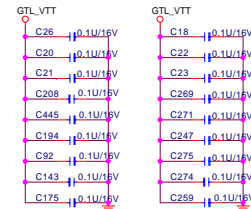
GTL+ PULL-UP RES NETWORK

The CLE266 add a feature for NB internal GTL pull-up, the internal pull-up strength is stronger than previous NB, so if enable the internal GTL pull-up can remove the CPU GTL pull-up R-PACK except -CPURST

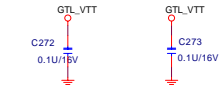


VTT Decoupling Cap. for GTL+ Pull-up R-PAK

(Place every decoupling capacitor for each R-pack.)



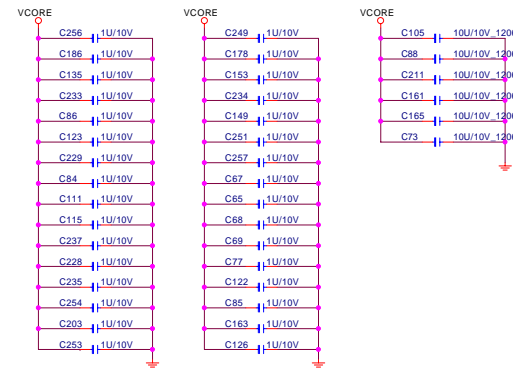
+1.5VCMOS Decoupling Cap. for Pull-up



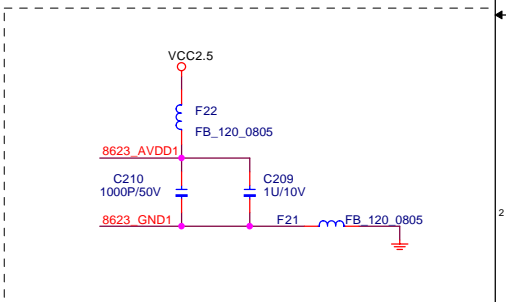
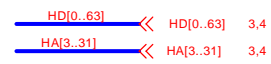
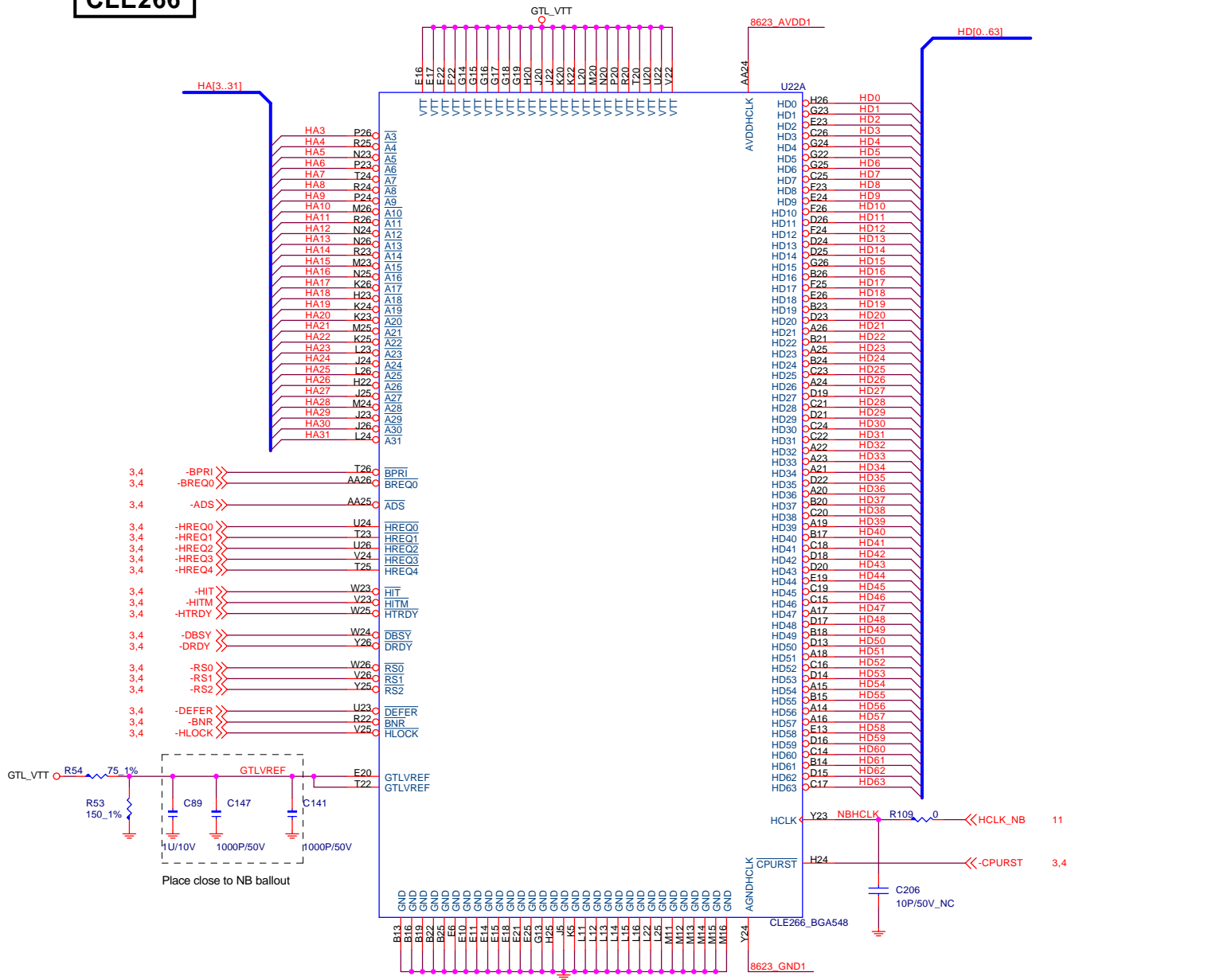
NOTE: CLOSE TO CPU CMOS I/O TERMINATION

CPU VCORE Decoupling Cap.

CPU VCORE Decoupling Caps: 10uF x 7, 1uF x 32

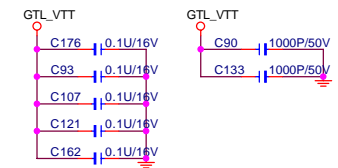


CLE266



NB Decoupling capacitors

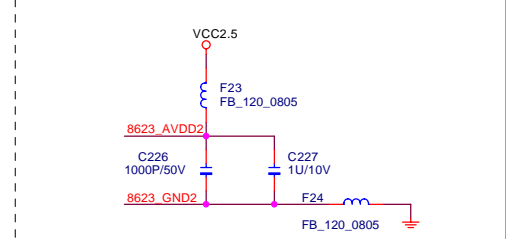
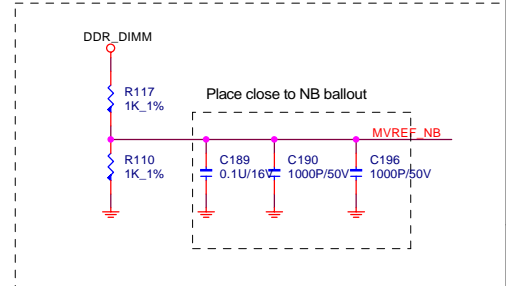
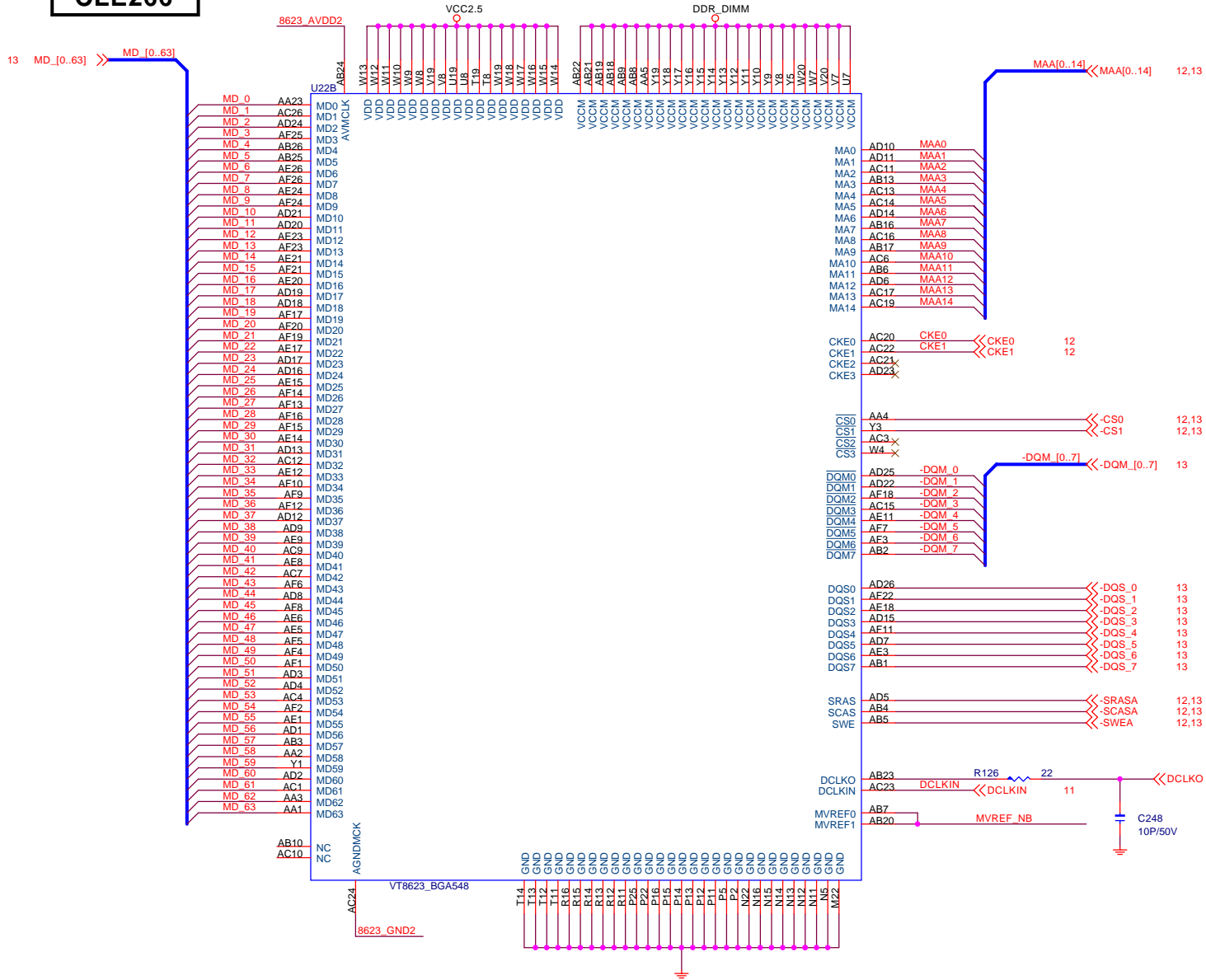
(CPU Interface: .1uF x 5, 1000pF x2)



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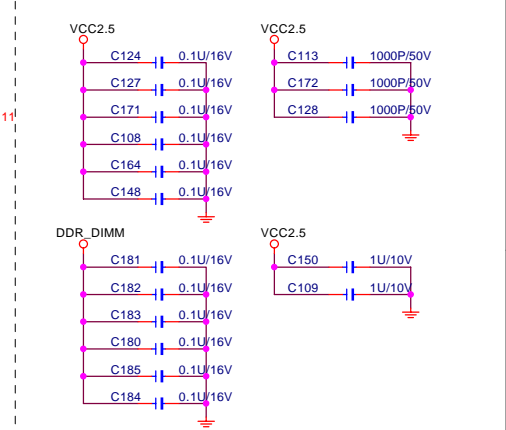
Title			NORTHBRIDGE (PART 1)		
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CLE266

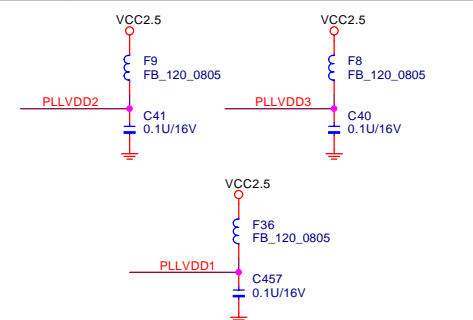
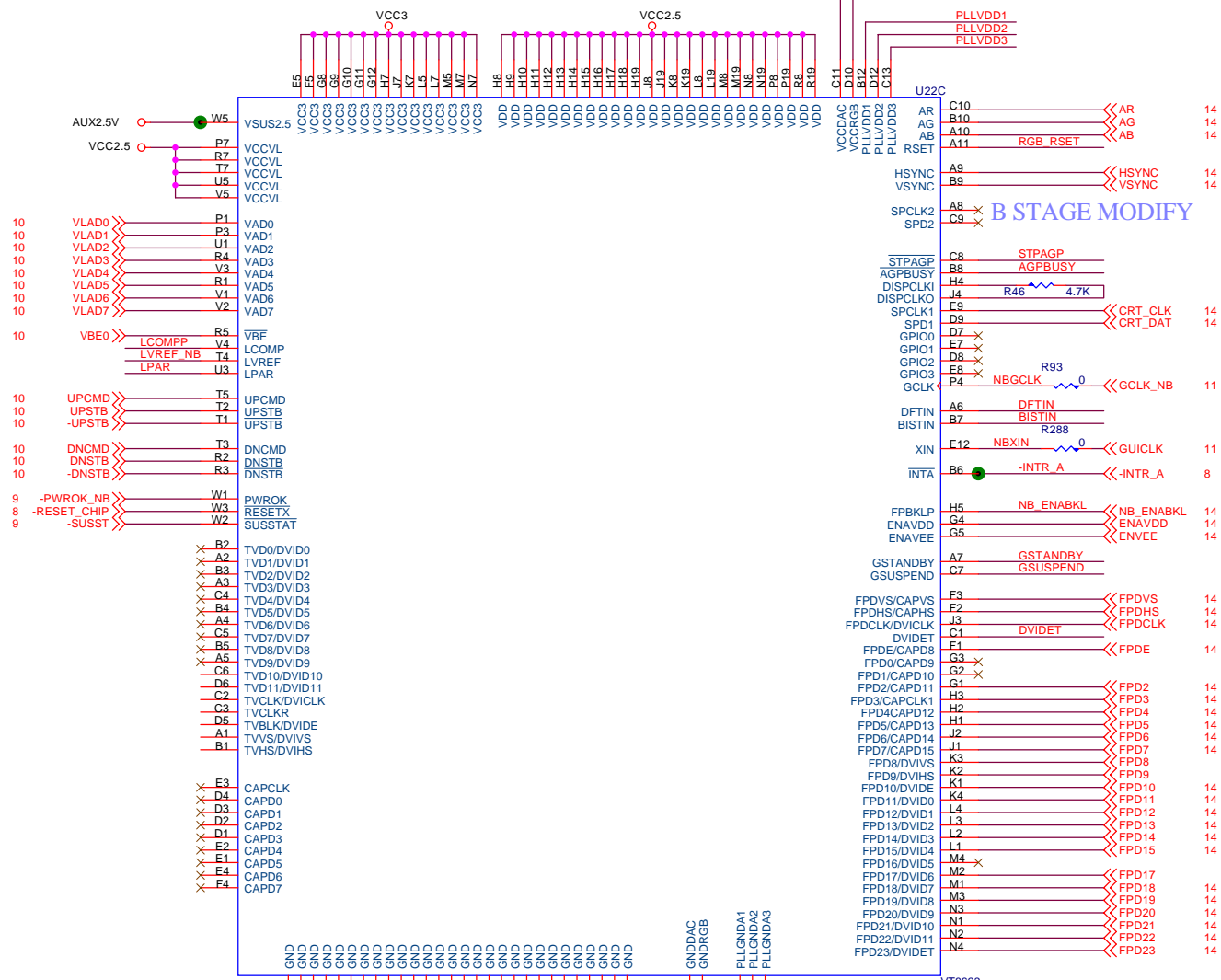


NB Decoupling capacitors

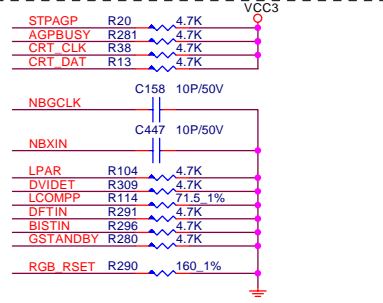
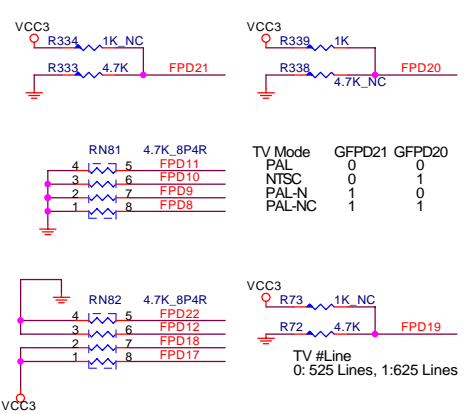
(Memory Interface: 1uF x 2, .1uF x 12, 1000pF x 6)



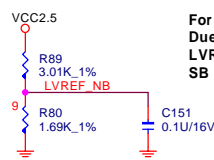
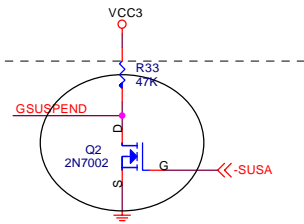
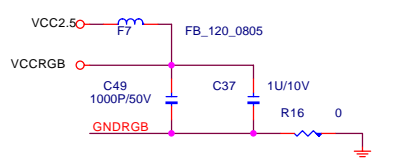
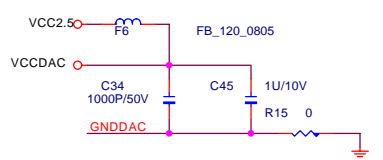
CLE266



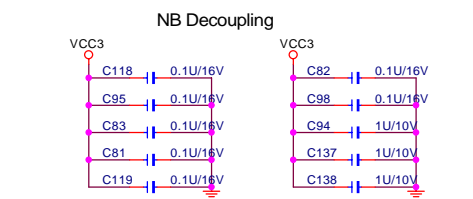
Panel Strapping Setting



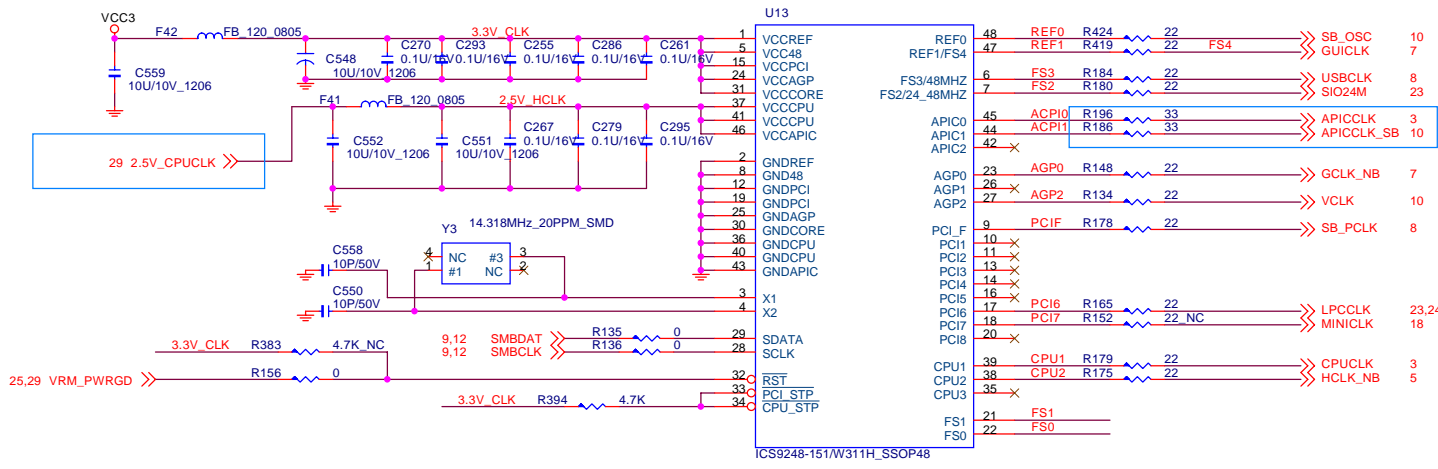
For VT8233: Connect NB to SB LPAR and do not need Pull-up.
 For VT8235: Do not connect the LPAR to SB, leave the NB LPAR for float, and pull-up the SB LPAR to +2.5V.



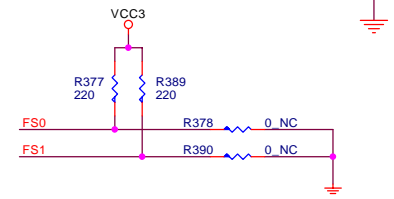
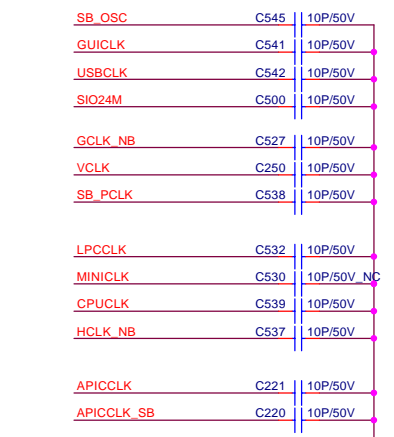
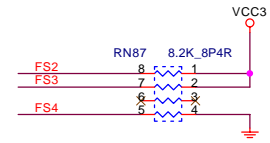
For LVREF_NB :
 Due to CLE266 is VLINK 4x so LVREF_NB should be 0.9V whenever SB is 8233 or 8235.



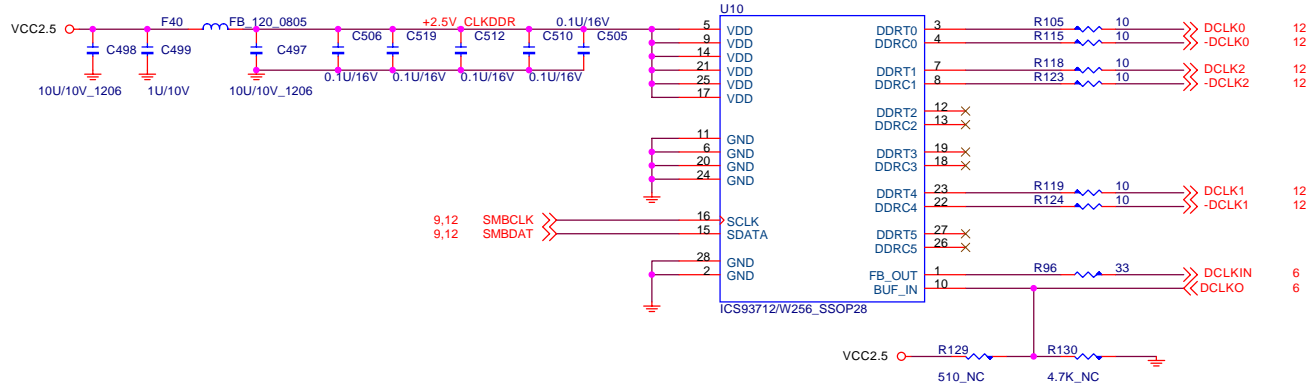
ICS9248-151



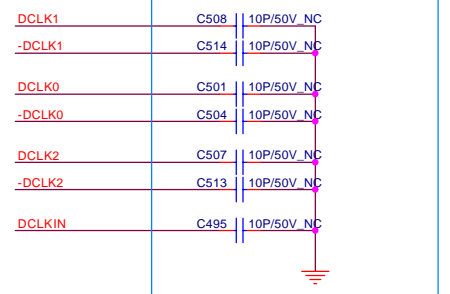
FS4	FS3	FS2	FS1	FS0	CPU	PCI
0	1	1	1	1	13	33
0	1	1	0	1	10	33
0	1	1	0	0	66	33



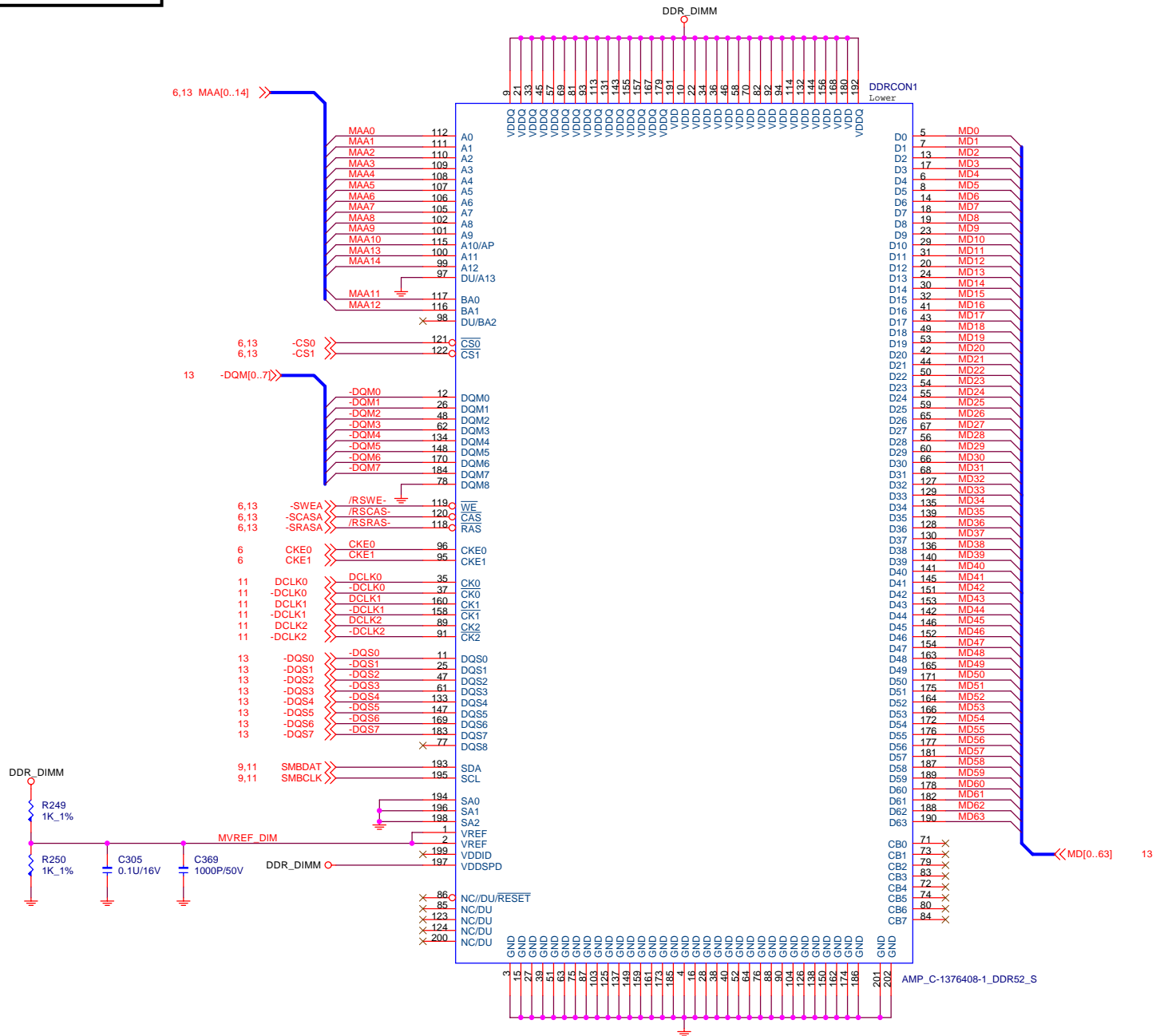
ICS93712

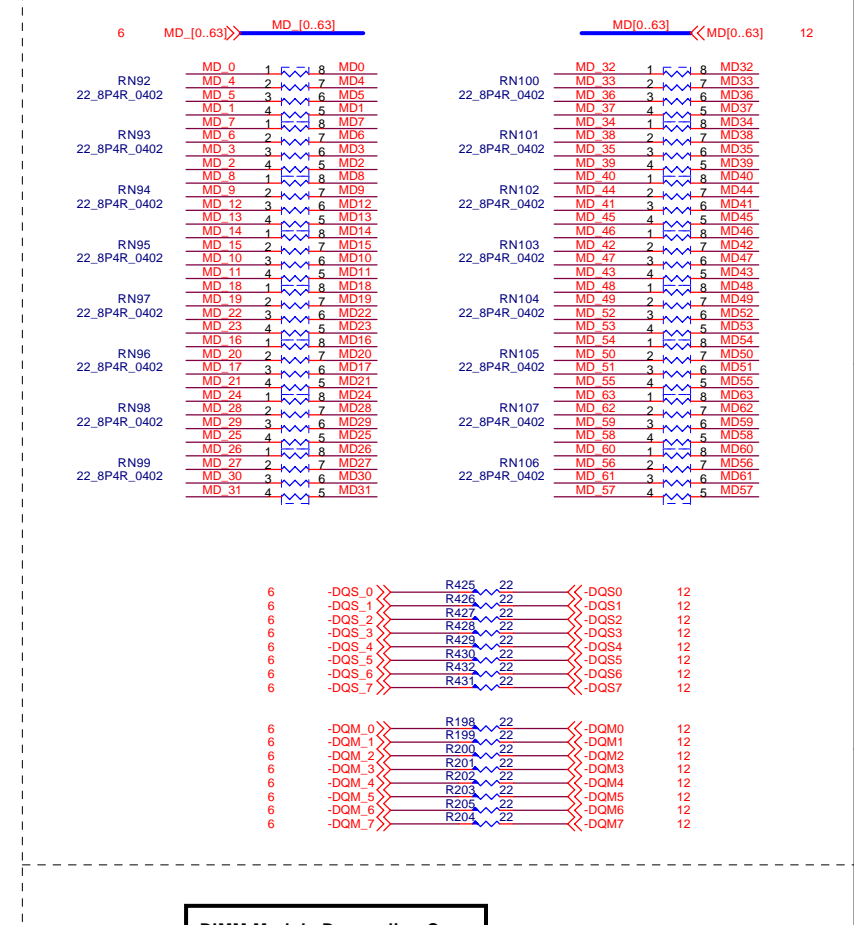
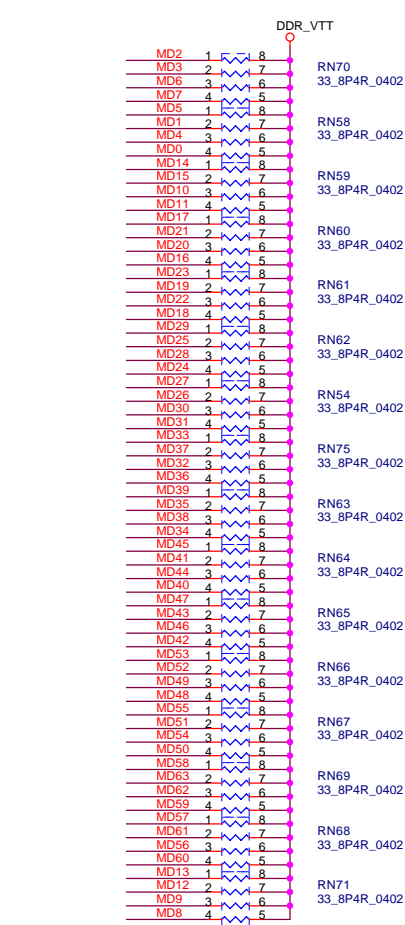
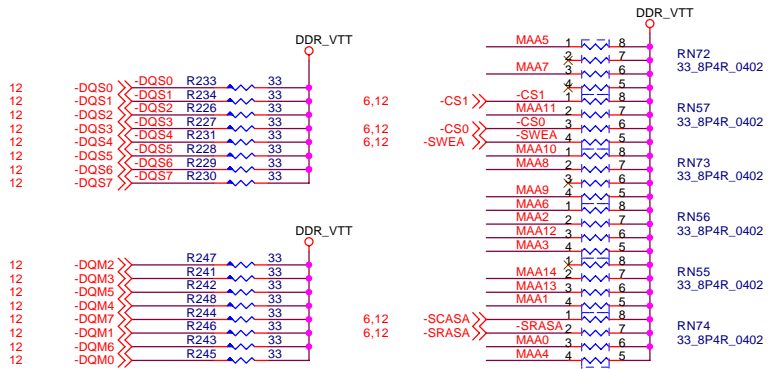


B STAGE MODIFY



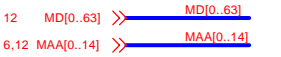
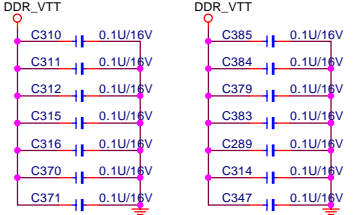
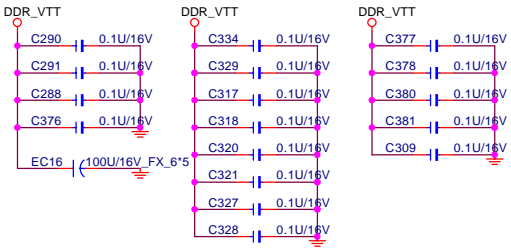
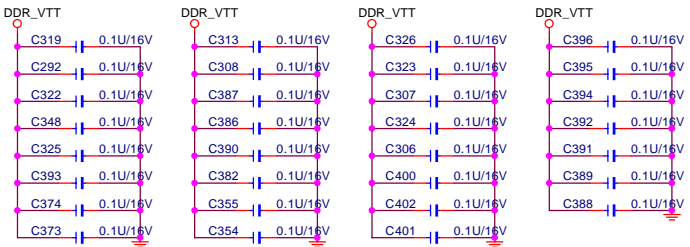
DIMM MODULE





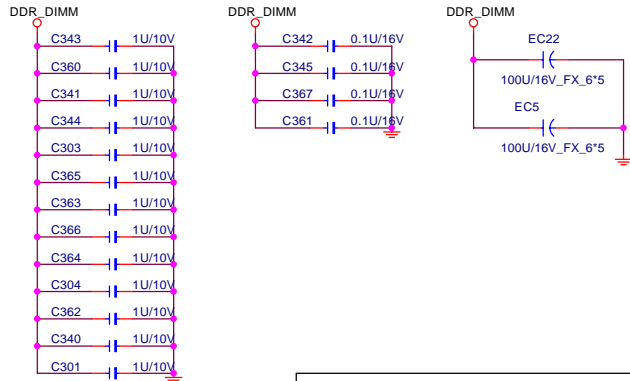
VTT_MEM Decoupling Caps

VTT_MEM Decoupling Caps: 1000uF x 1, .1uF x 62



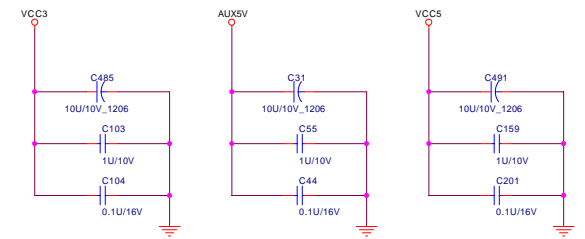
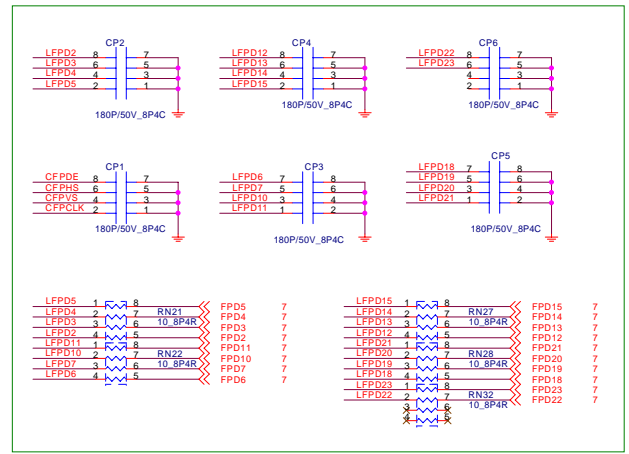
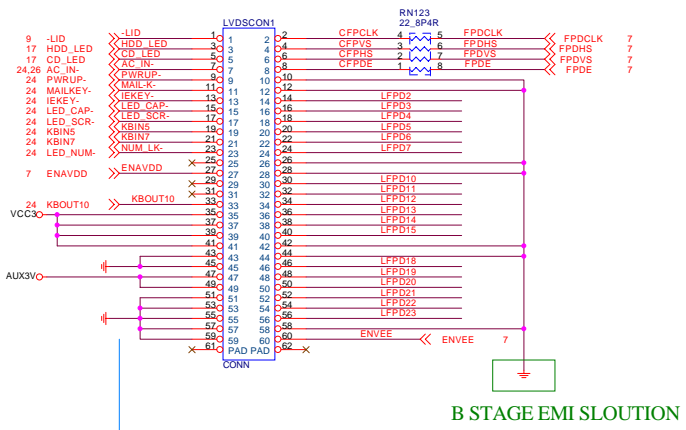
DIMM Module Decoupling Cap.

+2.5VDIMM Decoupling Caps: 1000uF x 3, 1uF x 13, .1uF x 4

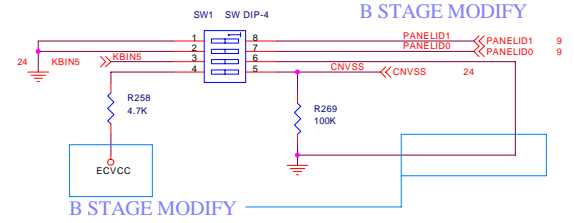
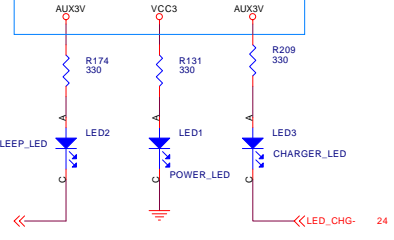


ELITGROUP COMPUTER SYSTEM CO., LTD.

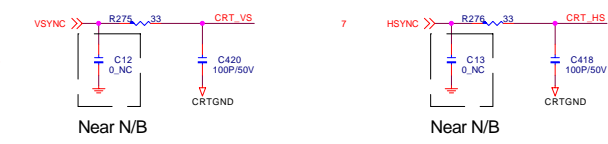
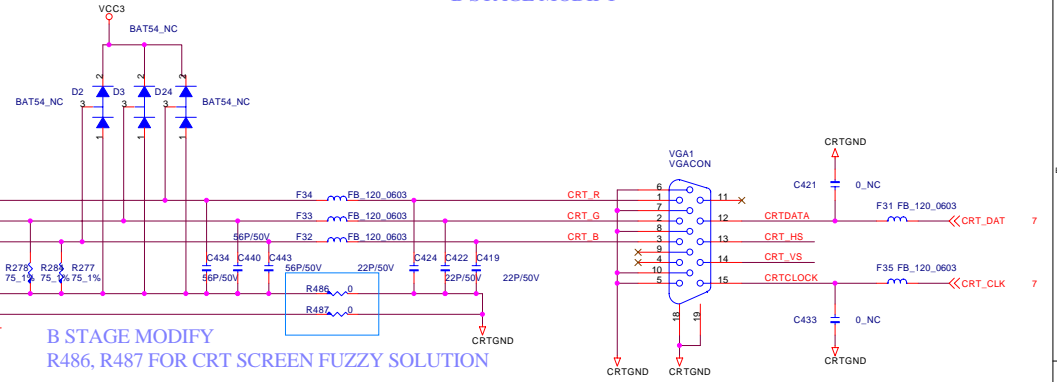
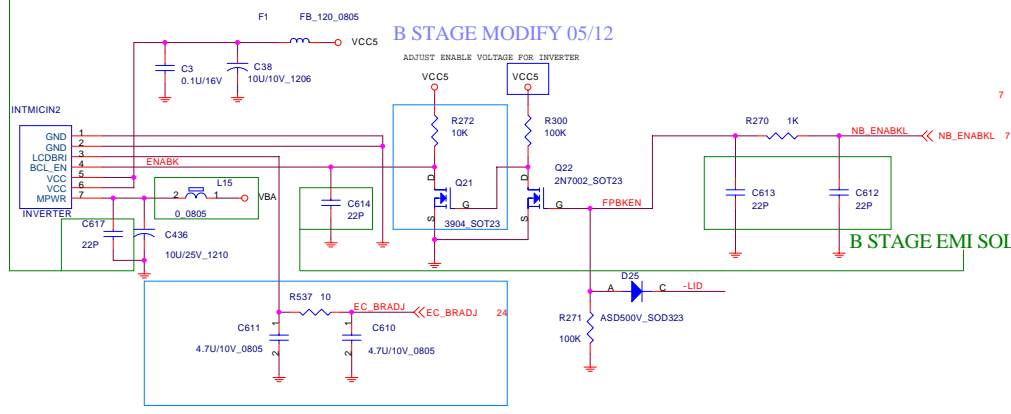
Title			DDR DAMPING RESISTORS		
Size	Document Number		G320-1-4-01		Rev
C					2.0
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B STAGE MODIFY

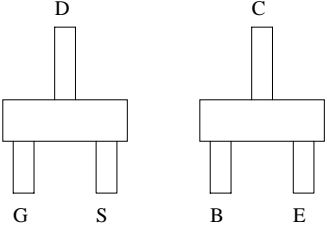
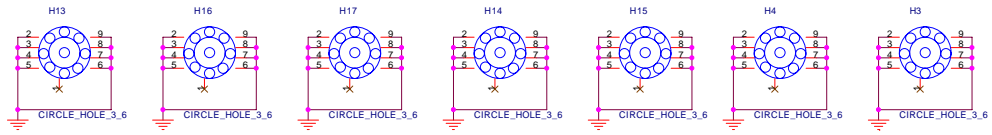


B STAGE EMI SOLUTION

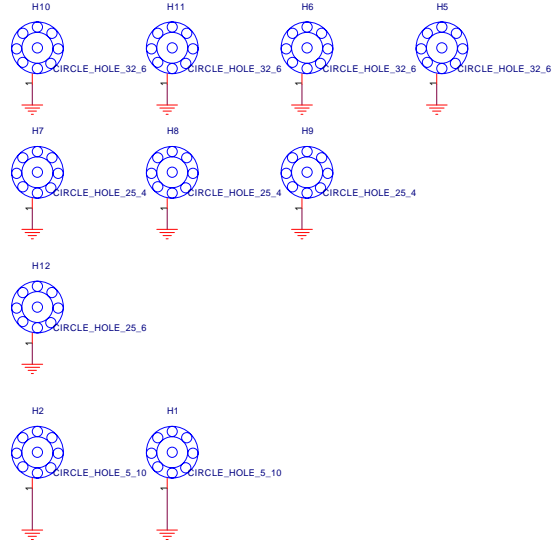


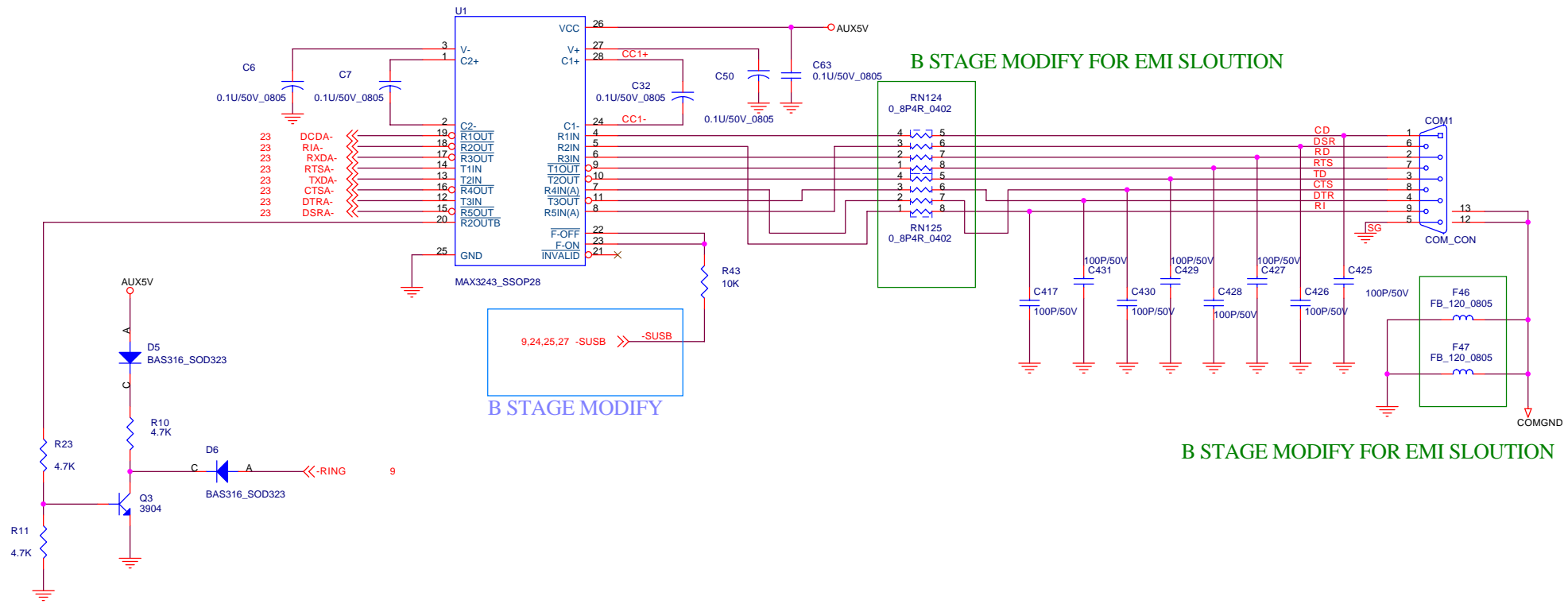
Title			LVDS CONNECTOR		
Size	Document Number			Rev	
C	G320-1-4-01			2.0	
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MOUNTING HOLE



CPU SIDE

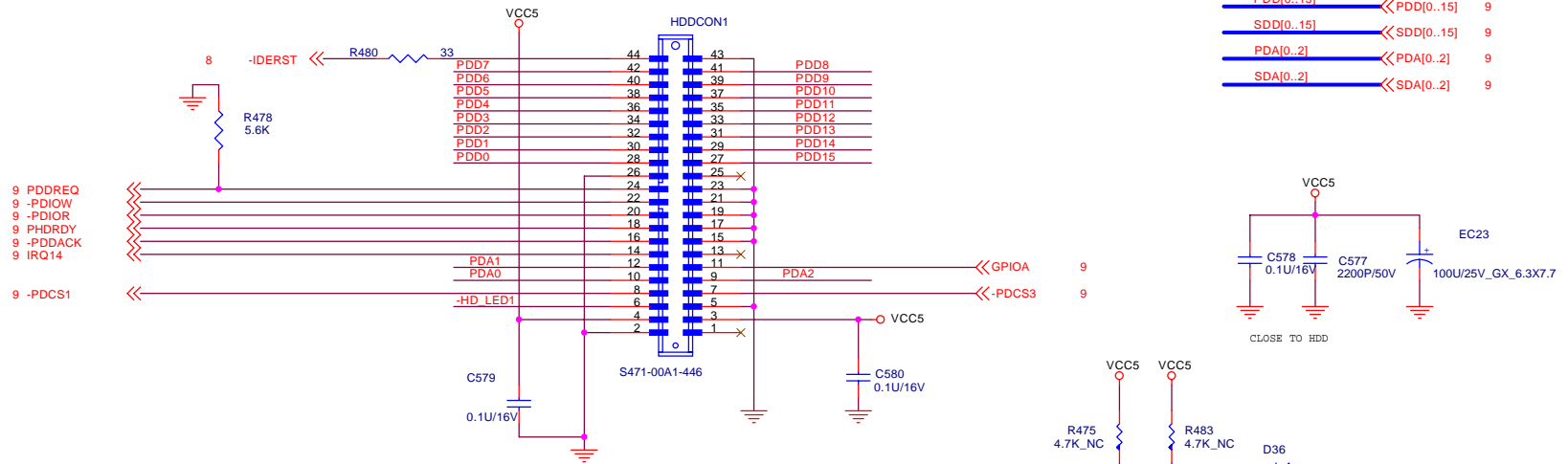




ELITEGROUP COMPUTER SYSTEM CO., LTD.		
Title	COM PORT	
Size	Document Number	Rev
C	G320-1-4-01	2.0
Date:	Thursday, July 24, 2003	Sheet 16 of 30

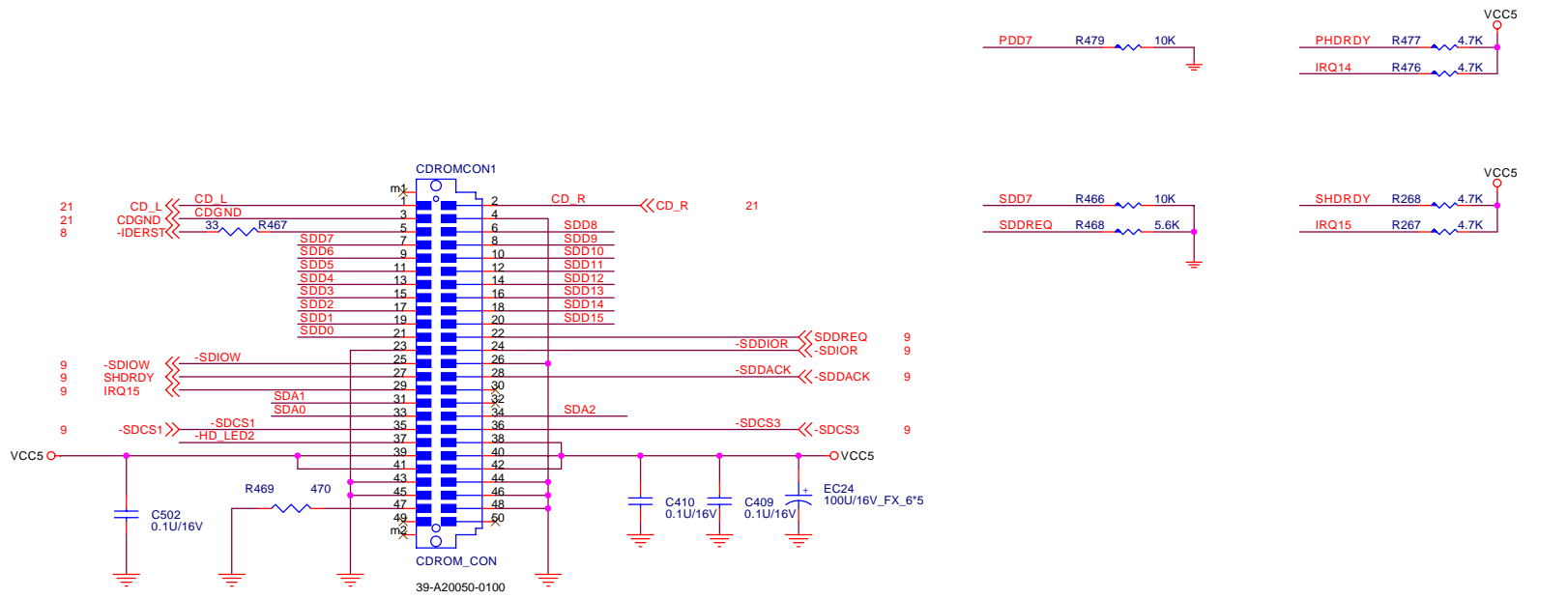
IDE Connector

PRIMARY



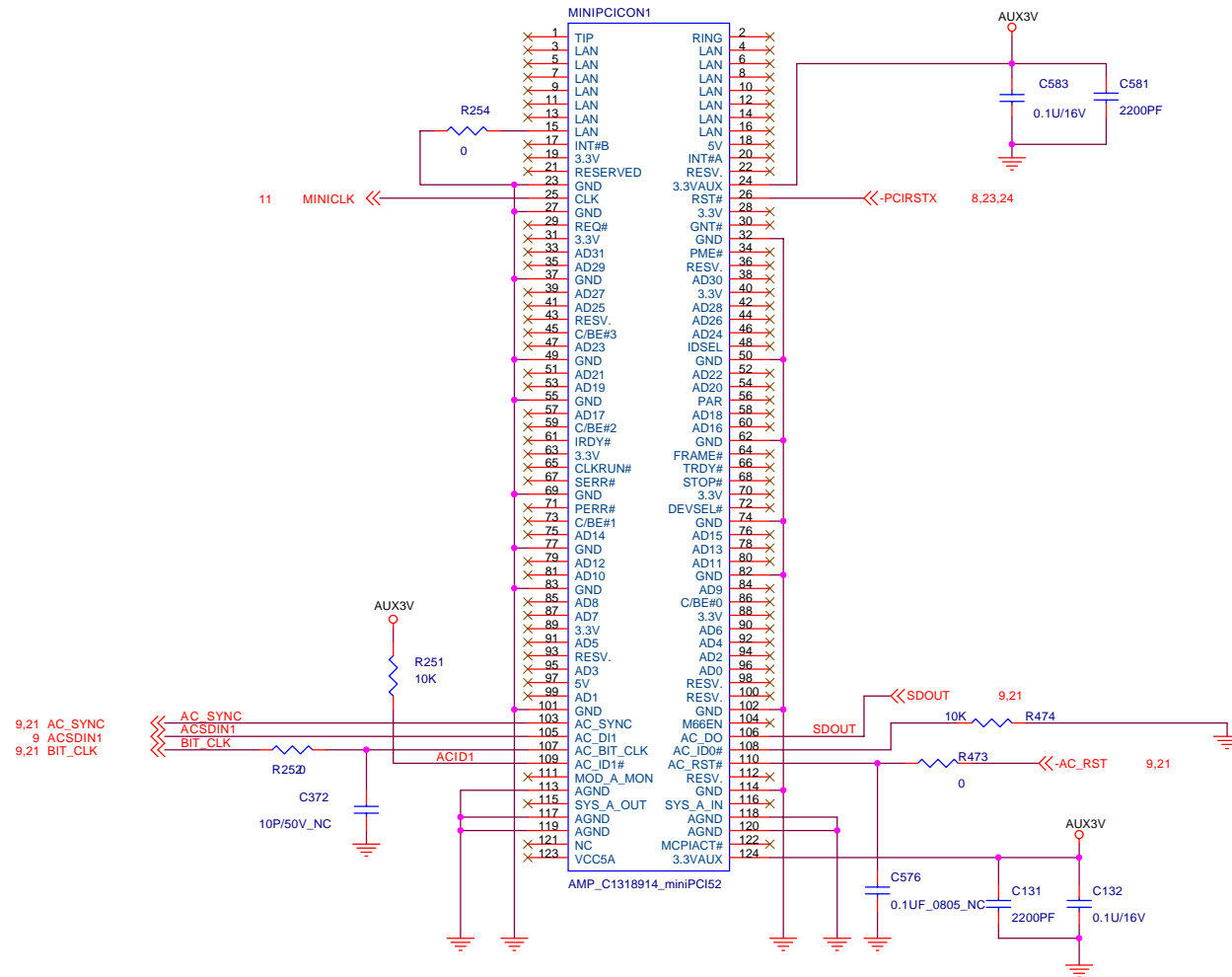
The HDD CON. footprint is not suitable, so we change the IDEbus to fit it. (pin1->pin?;pin2->pin?.....)And define the pin 1 on the "LEFT/RIGHT up" side.

SECONDARY



MINI PCI SLOT

B STAGE MODIFY ADD PCI BUS CONNECT TO MINIPCI SLOT



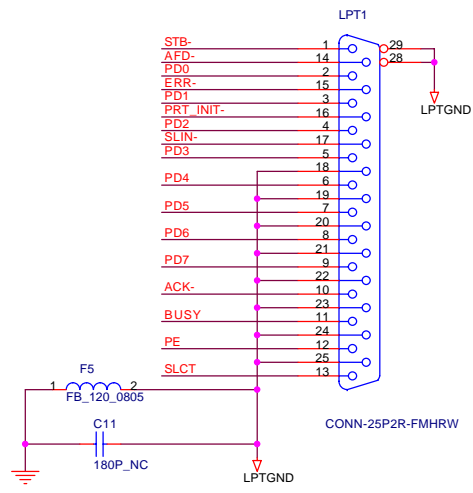
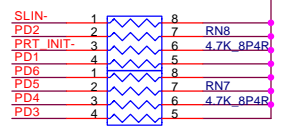
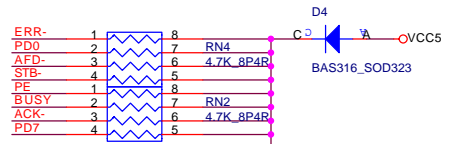
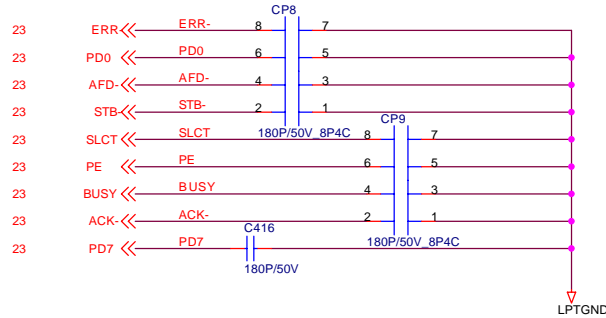
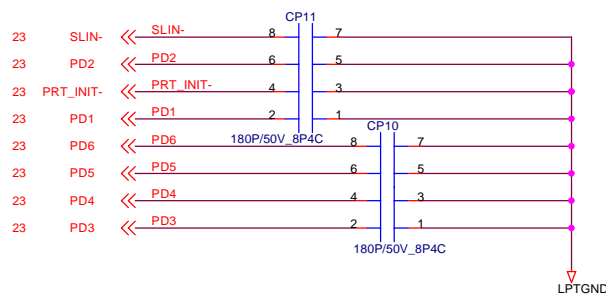
ELITEGROUP COMPUTER SYSTEM CO., LTD.

Title: MINIPCI SLOT

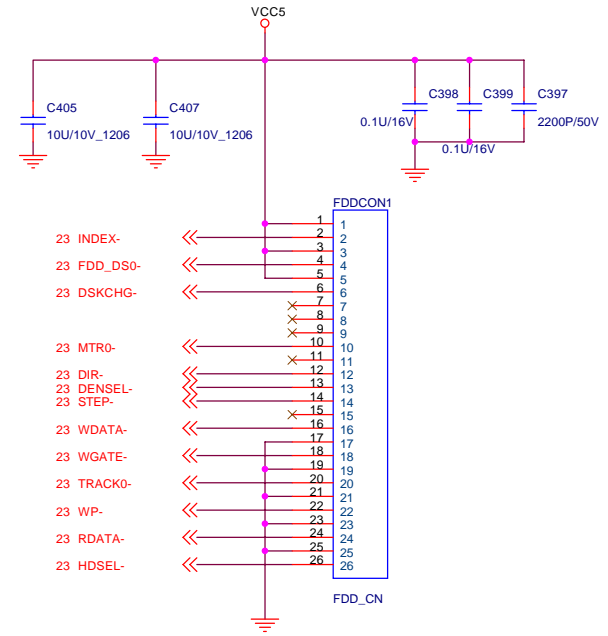
Size C Document Number G320-1-4-01 Rev 2.0

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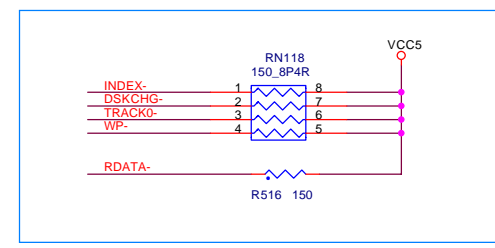
LPT



FLOPPY



B STAGE MODIFY

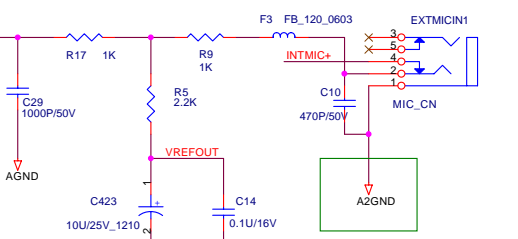
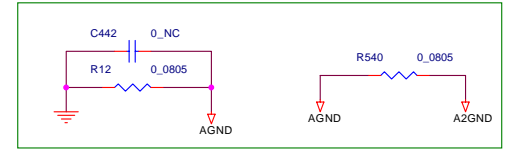


ELITGROUP COMPUTER SYSTEM CO., LTD.

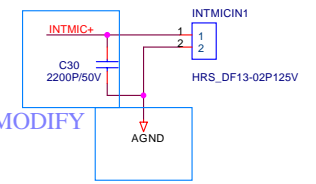
Title		LPT/FLOPPY	
Size	Document Number	G320-1-4-01	Rev 2.0
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VT1612A

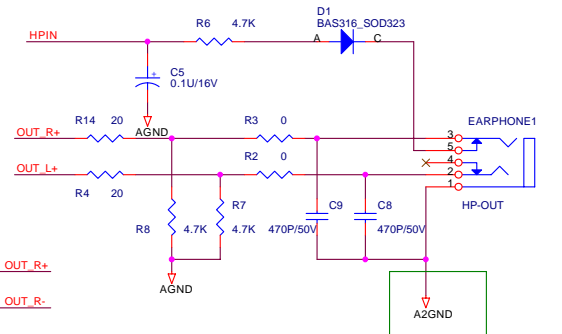
B STAGE EMI SLOUTION



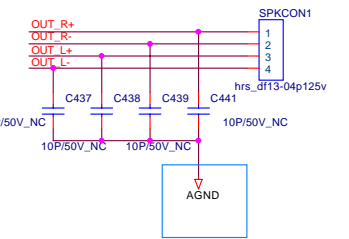
B STAGE EMI SLOUTION



B STAGE MODIFY

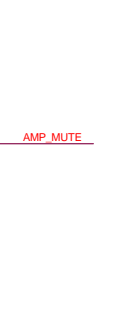
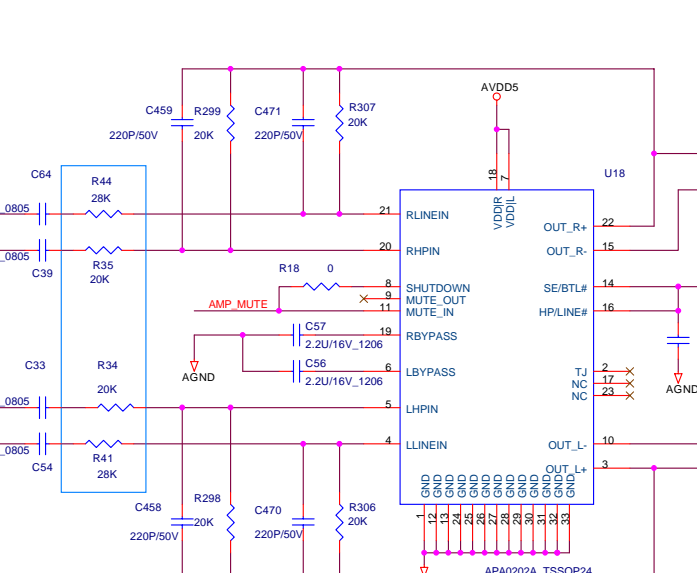
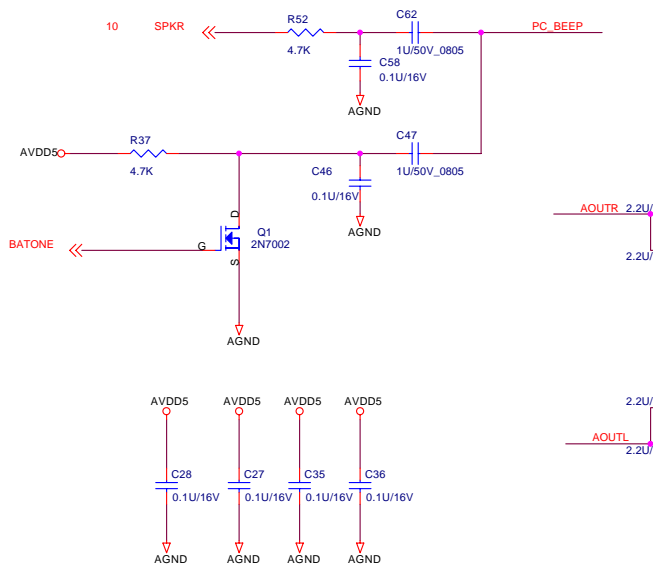
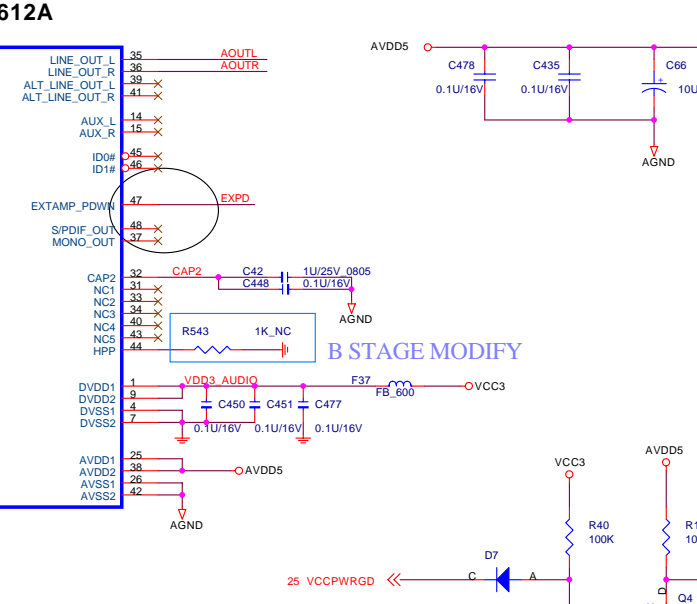
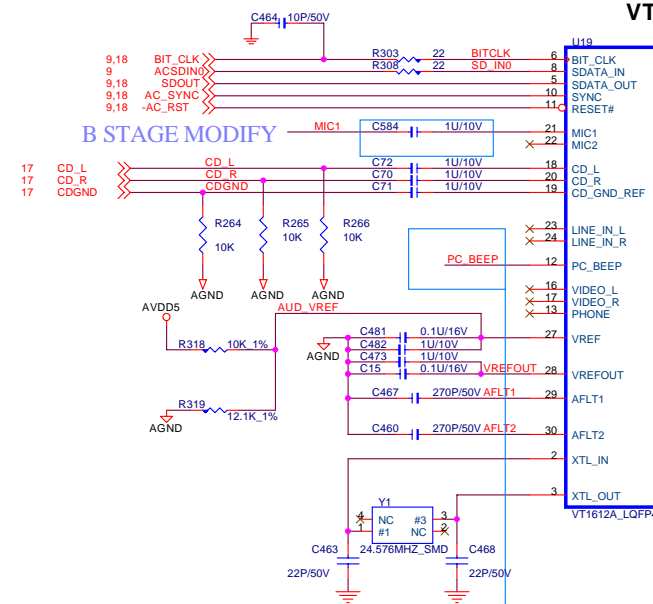


B STAGE EMI SLOUTION

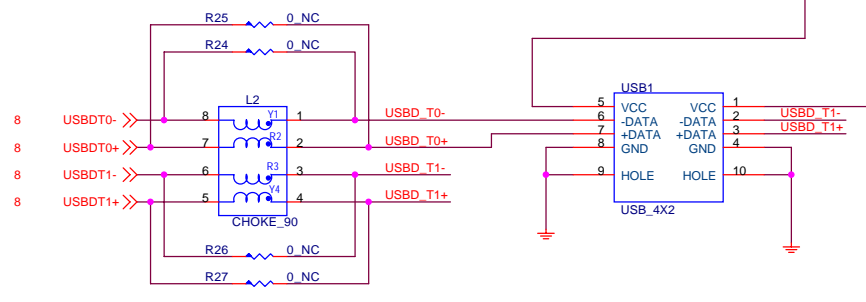
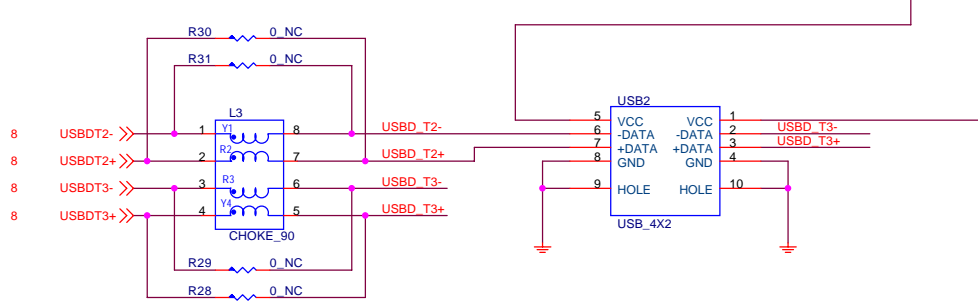
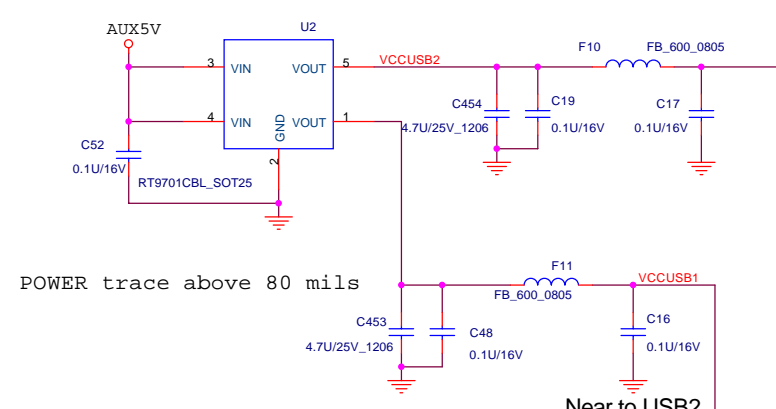
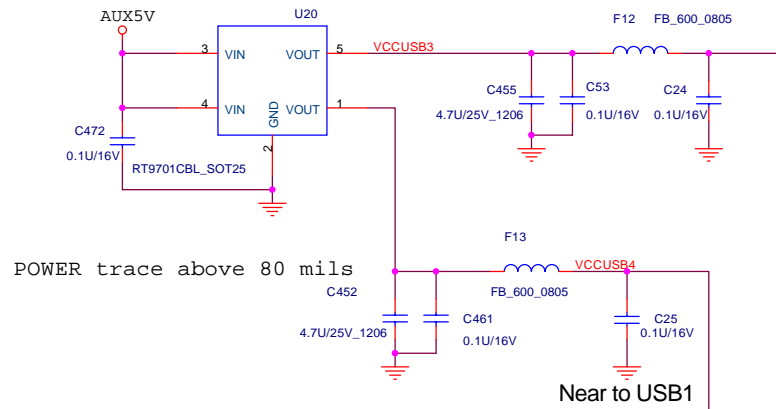


ELITEGROUP COMPUTER SYSTEM CO., LTD.

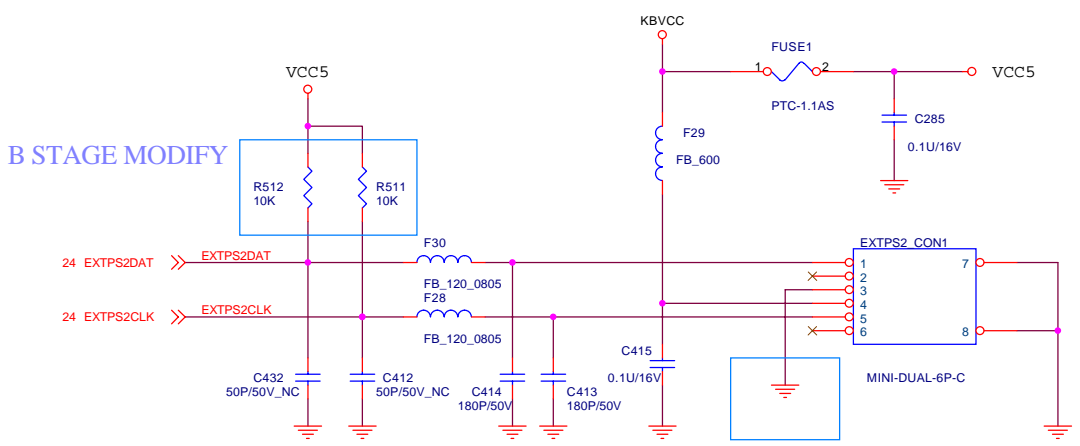
Title			AUDIO CODEC & AUDIO PORT		
Size	Document Number				Rev
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USB PORT



PS2 Connector



C480, C481 CLOSE TO EC (U17)

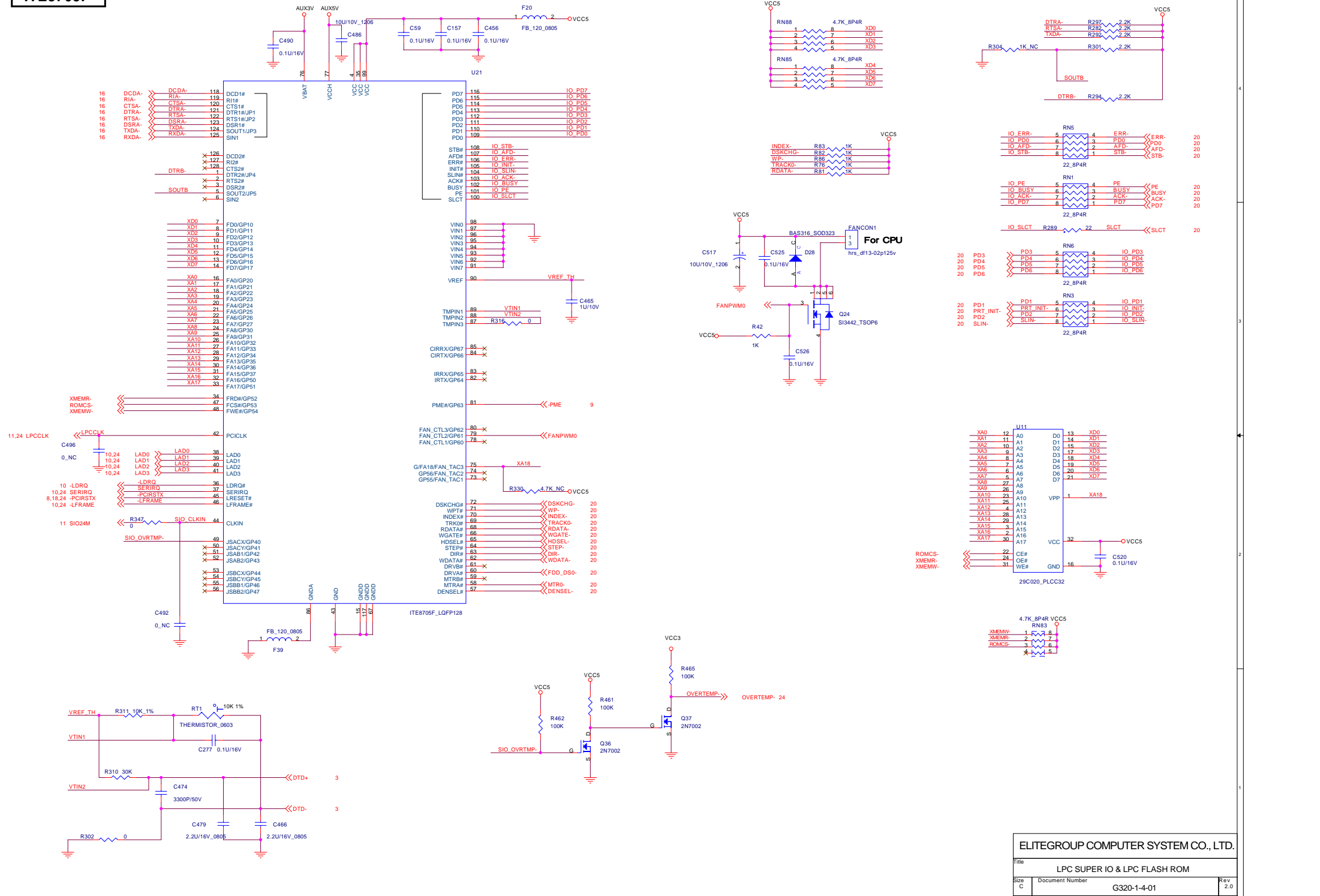
ELITGROUP COMPUTER SYSTEM CO., LTD.

Title: KB & USB CONNECTORS

Size C Document Number G320-1-4-01 Rev 2.0

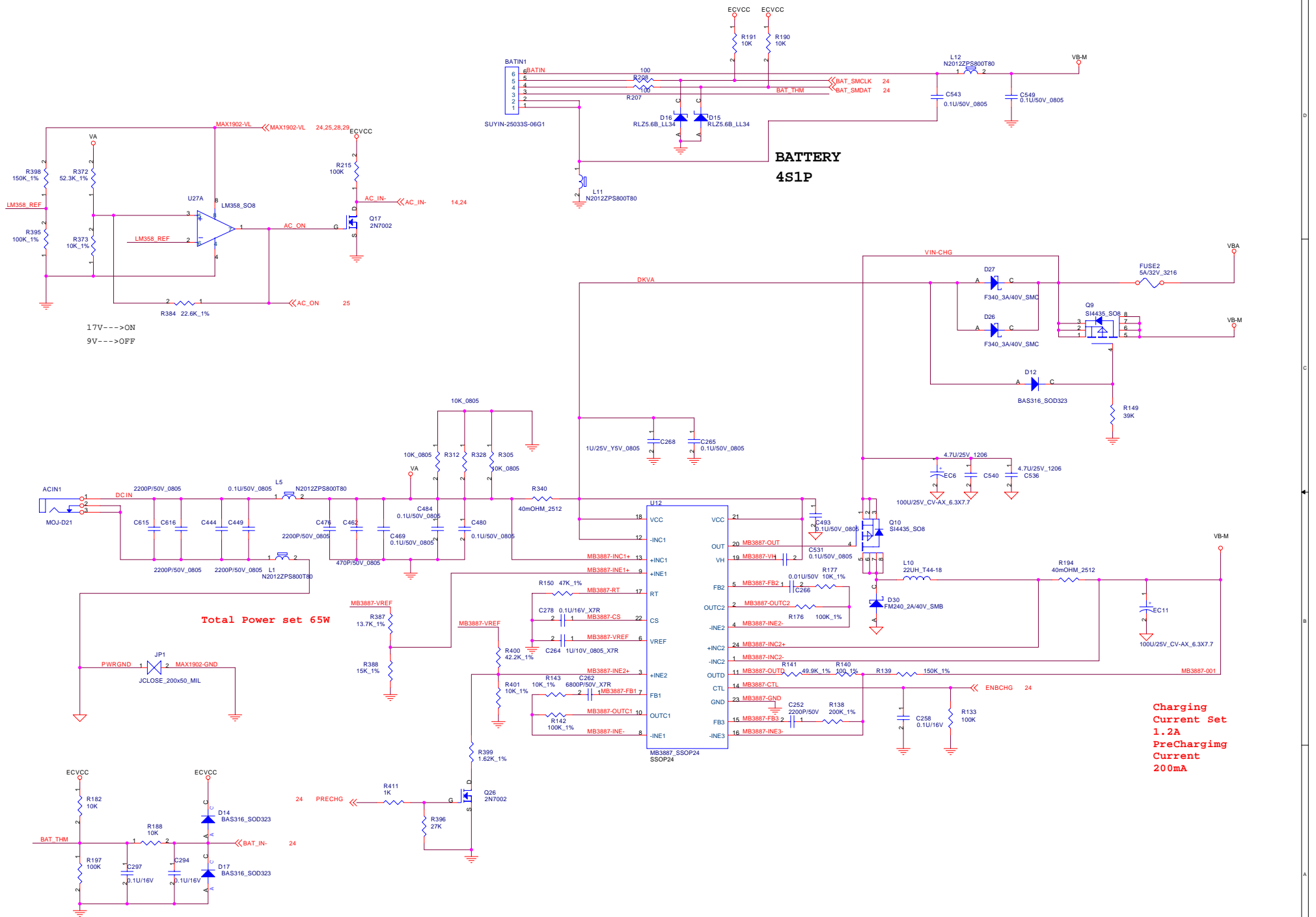
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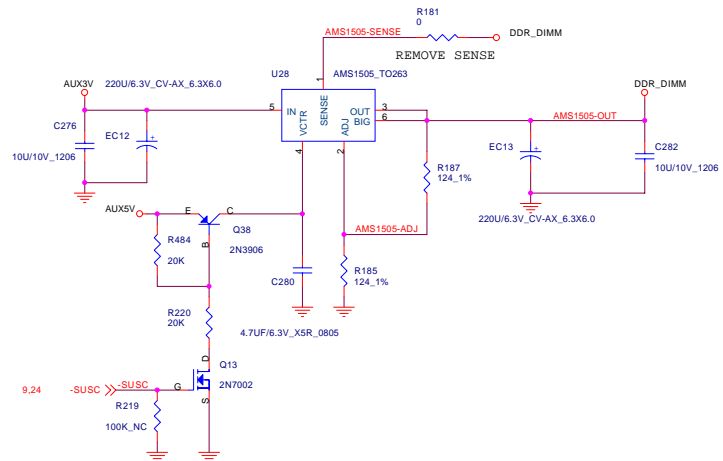
ITE8705F



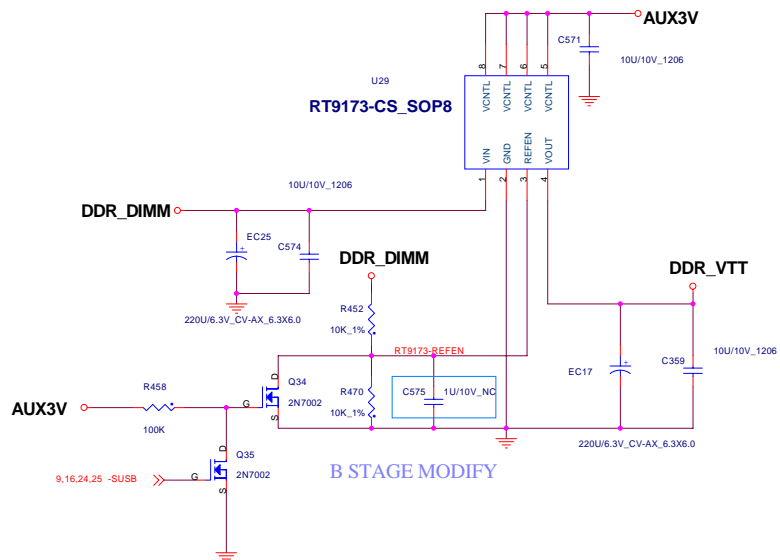
ELITEGROUP COMPUTER SYSTEM CO., LTD.

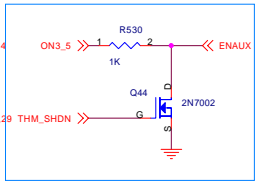
Title			
LPC SUPER IO & LPC FLASH ROM			
Size	Document Number	G320-1-4-01	Rev 2.0
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DDR_DIMM(2.5V) SUPPLY 3A FOR DDR





B STAGE MODIFY 05/13

THERMAL PROTECT OF H.W.

B STAGE MODIFY 05/08

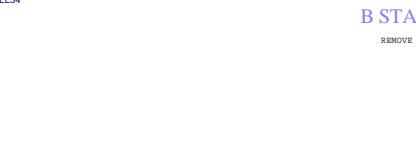
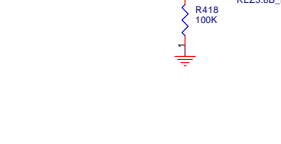
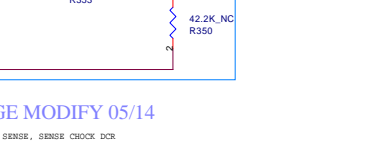
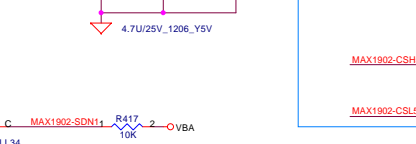
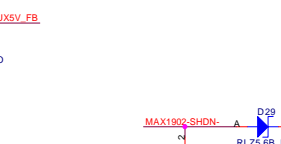
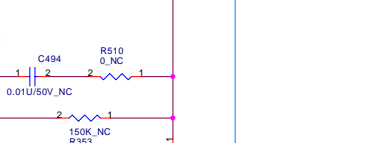
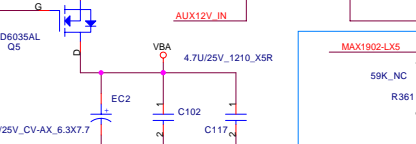
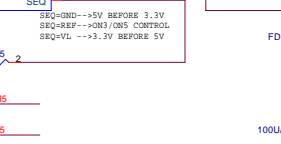
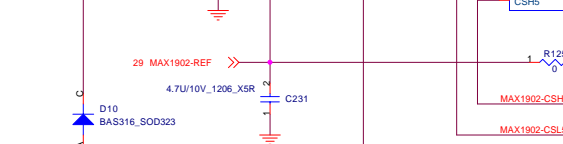
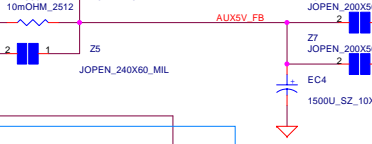
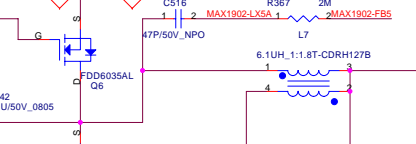
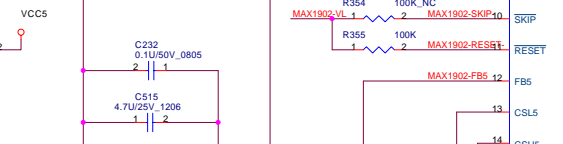
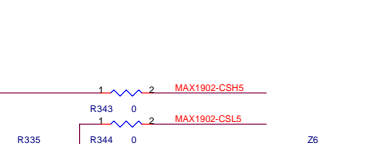
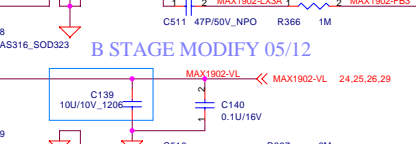
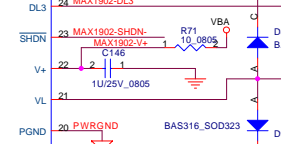
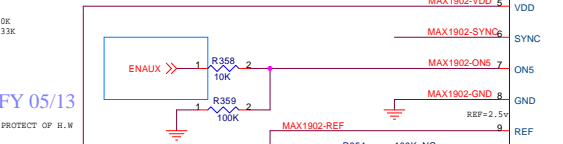
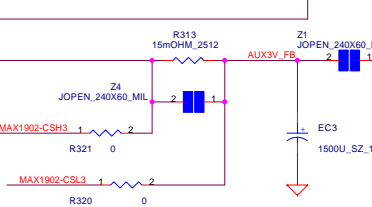
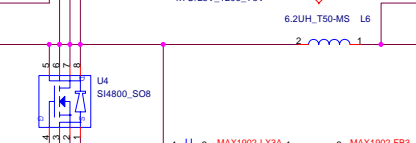
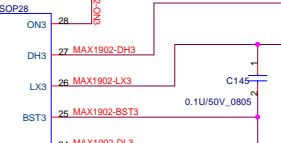
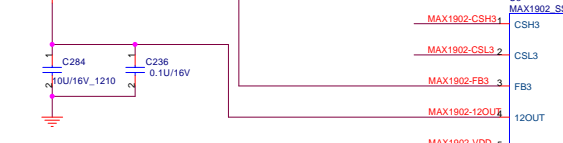
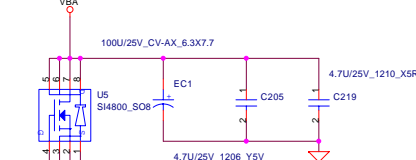
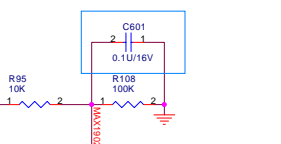
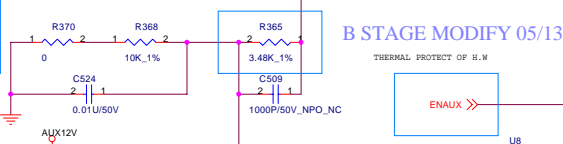
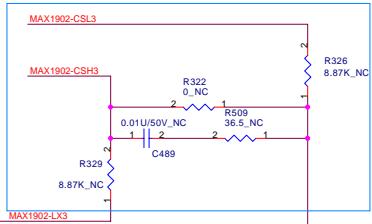
ADJUST AUX3V VOLTAGE

B STAGE MODIFY 05/02

DELAY AUX3.3V FOR CHIPSET BUG

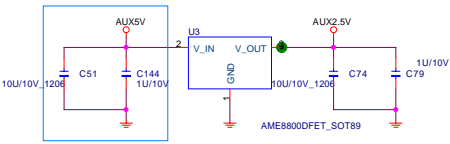
B STAGE MODIFY 05/14

REMOVE R SENSE, SENSE CHECK DCR



B STAGE MODIFY 05/02

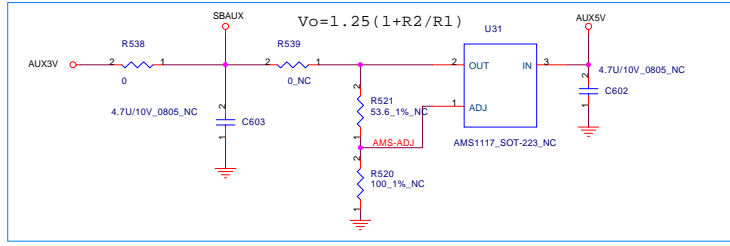
Chipset bug



FOR CHIPSET AUX 2.5V TIMING CONTROL

B STAGE MODIFY 05/08

SBAUX is adjustable for VIA chipset unstable issue



- 5 4 3 2 1
- 1. INITIAL KK0G726011000 V0.0 2003/03/21
 - 2. Project Name change from G726 to G320
 - 3. PP 15-F35-011000 V1.0 2003/05/28
 - 4. MP 15-F35-012000 V2.0 2003/07/02
- D C B A

Title		
HISTORY		
Size	Document Number	Rev
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