

# TTL ISOPLANAR MEMORY 93421/93421A

## 256 × 1 - BIT FULLY DECODED RANDOM ACCESS MEMORY

**DESCRIPTION** — The 93421 and 93421A are high-speed 256-bit TTL Random Access Memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three Chip Select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

- 3-STATE OUTPUT
- REPLACEMENT FOR 54/74S200 AND EQUIVALENT DEVICES
- ORGANIZATION — 256 WORDS X 1 BIT
- THREE HIGH-SPEED CHIP SELECT INPUTS
- TYPICAL READ ACCESS TIME
 

93421A	Commercial	30 ns
93421	Commercial	35 ns
93421	Military	35 ns
- ON CHIP DECODING
- POWER DISSIPATION — 1.8 mW/BIT
- POWER DISSIPATION DECREASES WITH TEMPERATURE
- INVERTED DATA OUTPUT

**PIN NAMES**

$\overline{CS}_1, \overline{CS}_2, \overline{CS}_3$   
 $A_0 - A_7$   
 $D_{IN}$   
 $\overline{D}_{OUT}$   
 $\overline{WE}$

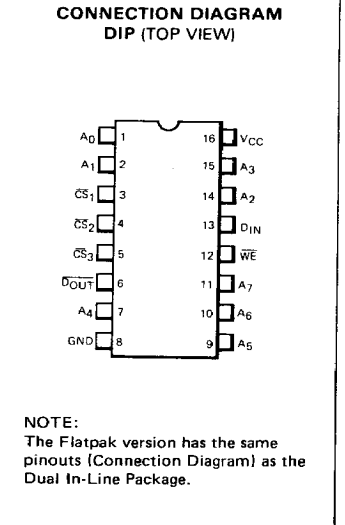
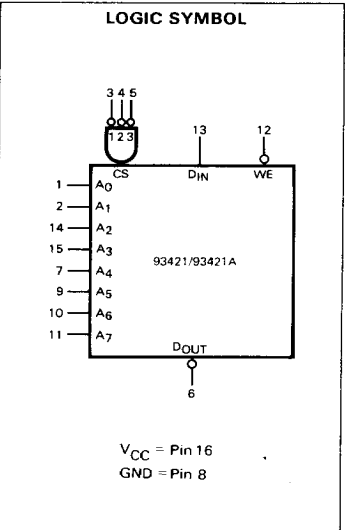
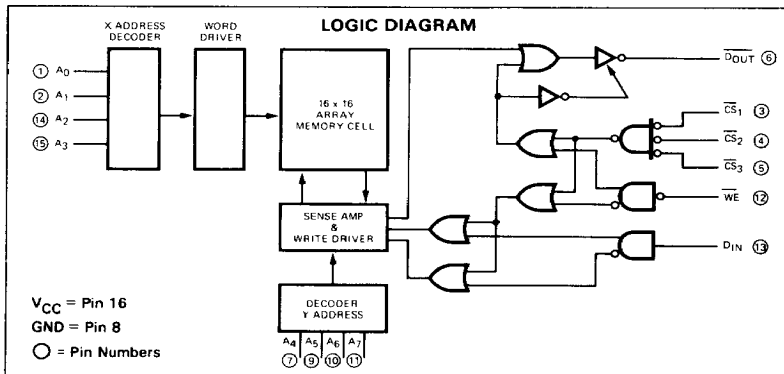
**LOADING**

(Notes a, b)

Chip Select Inputs	0.5 U.L.
Address Inputs	0.5 U.L.
Data Input	0.5 U.L.
Data Output	10 U.L.
Write Enable	0.5 U.L.

**NOTES:**

- a. 1 Unit Load (U.L.) = 40  $\mu$ A HIGH / 1.6 mA LOW
- b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at  $V_{OUT} = 0.45$  V, and will source a minimum of 10 mA at 2.4 V.



# FAIRCHILD ISOPLANAR TTL MEMORY • 93421/93421A

**FUNCTIONAL DESCRIPTION** — The 93421/93421A are fully decoded 256-bit Random Access Memories organized 256 words by one bit. Word selection is achieved by means of an 8-bit address,  $A_0$  through  $A_7$ .

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select,  $\overline{CS}$ , from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ( $\overline{WE}$ , pin 12). With  $\overline{WE}$  held LOW and the chip selected, the data at  $D_{IN}$  is written into the addressed location. To read,  $\overline{WE}$  is held HIGH and the chip selected. Data in the specified location is presented at  $\overline{D}_{OUT}$ .

The 3-state output provides drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

**TABLE I — TRUTH TABLE**

$\overline{CS}_1$		$\overline{CS}_2$		INPUTS			OUTPUT	MODE
				$\overline{CS}_3$	$\overline{WE}$	$D_{IN}$	$\overline{D}_{OUT}$	
H	X	X	X	X	X	HIGH Z	Not Selected	
X	H	X	X	X	X	HIGH Z	Not Selected	
X	X	H	X	X	X	HIGH Z	Not Selected	
L	L	L	L	L	L	HIGH Z	Write "0"	
L	L	L	L	H	H	HIGH Z	Write "1"	
L	L	L	H	X	X	$\overline{D}_{OUT}$	Read inverted data from addressed location	

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care (HIGH or LOW)  
 HIGH Z = High Impedance

**TABLE 2 — FUNCTION TABLE**

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	Stored Data
Not Selected	H	X	HIGH Z

**ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
$V_{CC}$ Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	-0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

\*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

\*\*Output Current Limit Required.

**GUARANTEED OPERATING RANGES**

PART NUMBER	SUPPLY VOLTAGE ( $V_{CC}$ )			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93421AXC, 93421XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93421XM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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## DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX		
V <sub>OL</sub>	Output LOW Voltage		0.3	0.45	V	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16 mA
V <sub>IH</sub>	Input HIGH Voltage	2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs
V <sub>IL</sub>	Input LOW Voltage		1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs
I <sub>IL</sub>	Input LOW Current		-530	-800	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0 V
I <sub>IH</sub>	Input HIGH Current		1.0	20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 4.5 V
I <sub>OFF</sub>	Output Current (HIGH Z)			50 -50	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.4 V V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.5 V
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.0	-1.5	V	V <sub>CC</sub> = MAX, I <sub>IN</sub> = -10 mA
I <sub>CC</sub>	Power Supply Current	93421XC	90	124	mA	V <sub>CC</sub> = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93421AXC	100	135		
		93421XM	90	117		
			100	143		
V <sub>OH</sub>	Output HIGH Voltage	93421XC,AXC	2.4		V	I <sub>OH</sub> = -10.3 mA
		93421XM	2.4		V	I <sub>OH</sub> = -5.2 mA
I <sub>OS</sub>	Output Current Short Circuit to Ground			-100	mA	V <sub>CC</sub> = MAX, Note 7

## AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

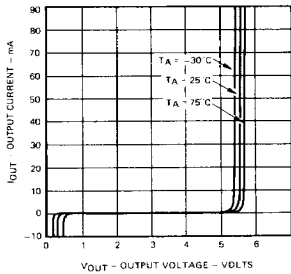
SYMBOL	CHARACTERISTIC	93421AXC			93421XC			93421XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t <sub>ACS</sub>	Chip Select Access Time		20	30		20	30		25	40	ns	See Test Circuit and Waveforms Note 5
t <sub>ZRCS</sub>	Chip Select to HIGH Z		20	30		20	30		20	40		
t <sub>AA</sub>	Address Access Time		30	40		35	50		35	60		
WRITE MODE	DELAY TIMES											
t <sub>ZWS</sub>	Write Disable to HIGH Z	10	20	35	10	20	35	10	20	45	ns	
t <sub>WR</sub>	Write Recovery Time		25	40		25	40		25	50		
	INPUT TIMING											
t <sub>W</sub>	Minimum Write Pulse Width	30	10		30	10		40	10		ns	See Test Circuit and Waveforms Note 6
t <sub>WSD</sub>	Data Set-Up Time Prior to Write	0	0		0	0		0	0			
t <sub>WHD</sub>	Data Hold Time After Write	5	0		5	0		5	0			
t <sub>WSA</sub>	Address Set-Up Time	0	0		0	0		0	0			
t <sub>WHA</sub>	Address Hold Time	5	0		5	0		5	0			
t <sub>WSCS</sub>	Chip Select Set-Up Time	0	0		0	0		0	0			
t <sub>WHCS</sub>	Chip Select Hold Time	5	0		5	0		5	0			
C <sub>I</sub>	Input Capacitance		2.5	3.5		2.5	3.5		2.5	3.5	pF	Measured with pulse technique
C <sub>O</sub>	Output Capacitance		5	7		5	7		5	7		

### NOTES:

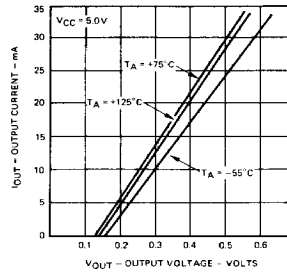
- Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
- Typical values are at V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = +25°C, and MAX loading.
- The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:  
 $\theta_{JA}$  (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.  
 $\theta_{JA}$  (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.  
 $\theta_{JC}$  (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
- The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
- t<sub>W</sub> measured at t<sub>WSA</sub> = MIN, t<sub>WHA</sub> measured at t<sub>W</sub> = MIN.
- Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTICS

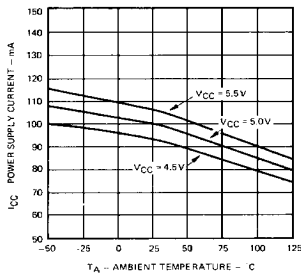
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



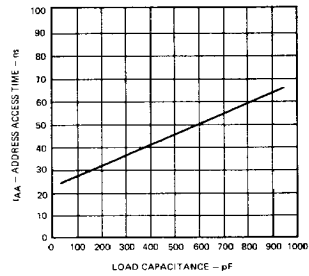
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



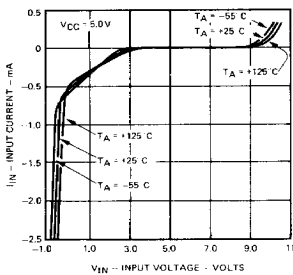
POWER SUPPLY CURRENT VERSUS TEMPERATURE



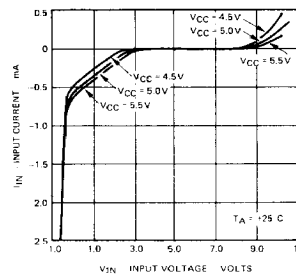
ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



AC Test Load and Waveforms same as 93L420, see page 7-93, 7-94 & 7-95.