Solutions for LCD TV Super IP Applications

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Abstract: Super inverters or high voltage inverters for LCD TVs continue to draw a tremendous amount of market attention due to their high efficiency and lower cost. This article conducts a circuit analysis and reviews the practical design considerations for Super IP converters in a 26 inch LCD TV application. It also explores transformer and circuit design in LCD TV applications.

1. Conventional Block vs. Super IP Block

In today's LCD TV inverter designs, designers are usually seeking solutions that offer high efficiency, but at minimal cost. With conventional topologies, it is difficult to improve the efficiency without increasing the cost. As a result, Super inverters or high voltage inverters have been offered as a viable solution since these products save the main output's rectification circuit. There are many different types of Super IP topologies, but this paper will focus on one of the topologies shown in Figure 1, which is suitable for a 26" 4 U-shaped lamps LCD TV.

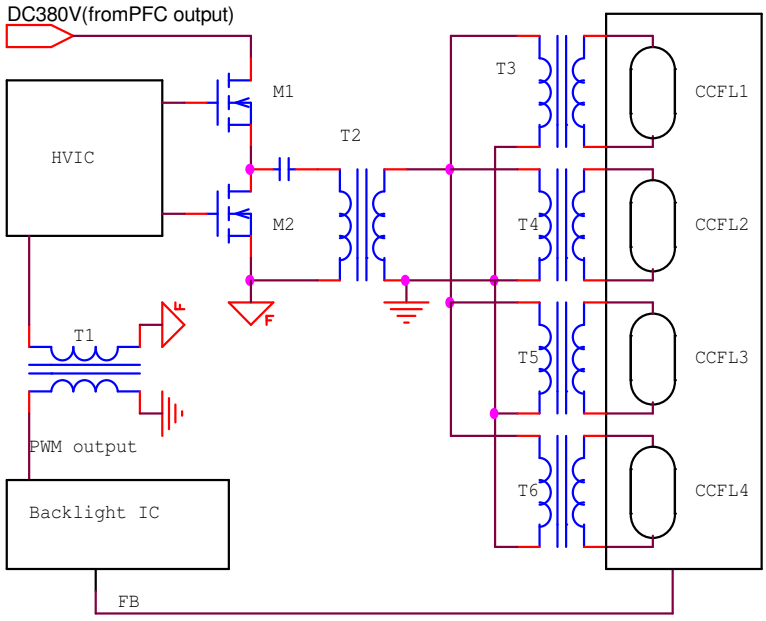

Figure 1. Super IP LCD TV Power Block

In the above Super IP block (Figure 1), the power stage and inverter stage have been combined into one stage to improve the total efficiency and save the cost. The half-bridge block supply directly comes from the primary side of PFC 380V output, and

T2 works as the primary side and secondary side isolation transformer. The resonant tank circuit, which is made of series cap, T2, T3, T4, T5 & T6 as well as CCFL, converts the square-wave voltage to a sinusoidal output to drive the CCFL.

2. Current Balance

Currently, U-shape lamps are commonly adopted by panel suppliers to reduce cost and power losses. However, for both terminals P1 and P2 of the U-shape lamp require operating in high voltage, it is very difficult to sense the lamp current, since you cannot directly measure the lamp's current by insert a sensing resistor in a series with a lamp. And it is also difficult to control the 4 U-shape lamps' current balance due to the difference of lamp impedance.

An inverter circuit consists of an inverter transformer, inside secondary side leakage inductance, lamp operation impedance and resonant caps as well as the lamp parasitic cap Clamp. Here, the lamp operation impedance is simplified as a resistor Rlamp. Figure 2 shows the lamps' current value with frequency variation.

It is interesting that the lamp current RMS value meets together at f_0 (resonant point) while the Rlamp in Figure3 is varied from 100K to 1Mohm. The f_0 (resonant point) is decided by the L3 and Clamp, C9 and C10. It means that we can easily get current balance if the operating frequency is close to f_0.

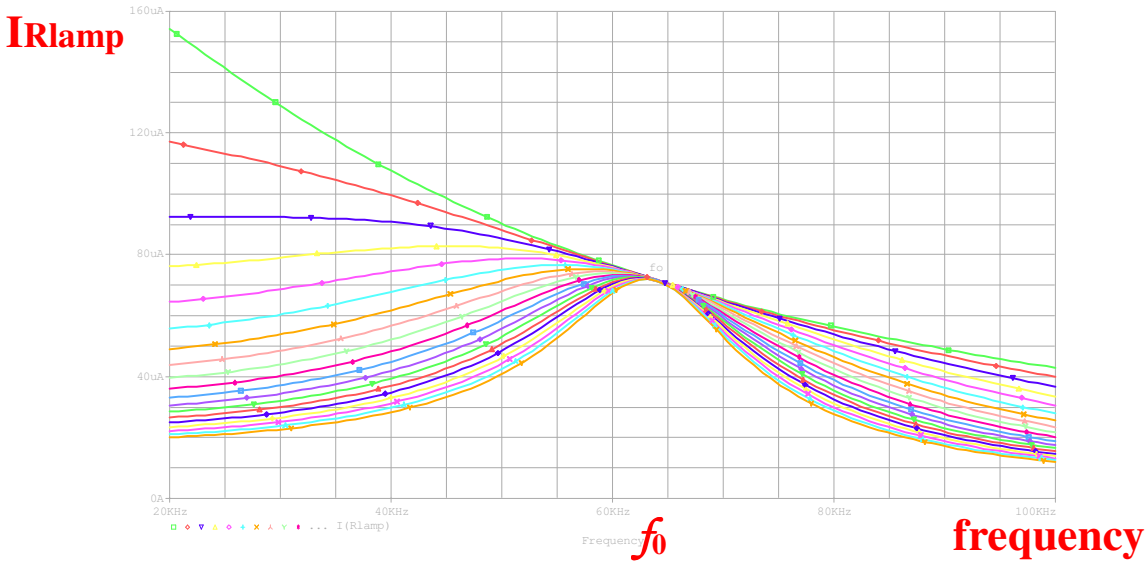

Figure 2. Lamp Current Vs Frequency, Rlamp

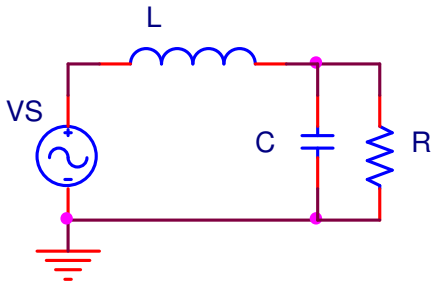

Figure 3. Simplied RCL tank circuit

The circuit in Figure 3 is a simplified inverter resonant circuit. It consists of inverter transformer leakage inductance L, and C which is made by lamp parasitic cap paralleled with outside caps, and Lamp equivalent resistor R. Then the lamp current transfer function I(R) is expressed as below.

$$I_R(\omega)=\frac{V_R(\omega)}{R}=\frac{VS(\omega)}{\omega L+\dfrac{R*\dfrac{1}{j\omega C}}{R+\dfrac{1}{j\omega C}}}*\frac{R*\dfrac{1}{j\omega C}}{R+\dfrac{1}{j\omega C}}*\frac{1}{R}=\frac{VS(\omega)}{R(1-\omega^2LC)+j\omega L} \qquad (2.1)$$

$$Q=\left|\frac{V_R(\omega)}{VS(\omega)}\right|_{\omega=\omega_0}=\left|\frac{\dfrac{R*\dfrac{1}{j\omega C}}{R+\dfrac{1}{j\omega C}}}{\omega L+\dfrac{R*\dfrac{1}{j\omega C}}{R+\dfrac{1}{j\omega C}}}\right|_{\omega=\omega 0}=\left|\frac{R}{R(1-\omega^2LC)+j\omega L}\right|_{\omega=\omega_0}=\frac{R}{\omega_0 L} \qquad (2.2)$$

$$\left|\frac{V_R(\omega)}{VS(\omega)}\right|=\left|\frac{R}{R(1-\omega^2LC)+j\omega L}\right|=\frac{1}{\sqrt{\left\{1-\left(\dfrac{\omega}{\omega_0}\right)^2\right\}^2+\dfrac{1}{Q^2}\left(\dfrac{\omega}{\omega_0}\right)^2}} \qquad (2.3)$$

If ω^2 LC=1, then the $I_R(\omega)=\dfrac{VS(\omega)}{j\omega L}$, which is not related with R lamp value, we can make constant current inverter. The Lamp current RMS value is decided by the Vs, the inverter transformer leakage inductance L and C value. And we also learn the current curve around $f_0=\dfrac{1}{2\pi\sqrt{LC}}$ is more closer , if the $Q=\dfrac{R}{\omega L}$ is more smaller.

3. A Half-Bridge MOSFET Switching Feature

Another issue is that the half-bridge MOSFETs' turn-on spike. Figure 4 is the simulation waveform with a small duty cycle. There is big current spike when high side MOSFET (S1) or low side MOSFET (S2) turn on. The turn on loss of S1 and S2 is very big and the efficiency is not good. Switching noise is also a big challenge since it can negatively impact the overall system reliability.

First, assuming the half-bridge load is inductive and the current waveform lags behind with Voltage waveform, D6 is the High side MOSFET S1 body diode, and D7 is the low side MOSFET S2 body diode.

t0->t1: Before t<t0 , S2 was turning on, and the transformer primary current IR65 was negative, at t=t0, S2 is turned off, causing the current IR65 to charge C46 and discharge C45, and the switching node Vs voltage are charging to 380V+0.7V@t1.

t1->t2: D6 starts to turn on, the transformer primary side current charge the 380VDC input power and the current reduce to 0@t2.

t2->t3: The D6 turns off, the resonant between C15,TX6 primary side inductance, R65 and C45/C46 start, the switching node Vs voltage reduces to negative voltage make D7 turn on first, then the Vs voltage become positive.

t3->t4: The dead time finish, the high side gate drive turns on the MOSFET. There is a large current spike conducted at MOSFET I_{DS}.

To reduce the current spike, we need to increase the V7 and V8 turns on duty to close to 50% to make the S1 and S2 ZVS. Then we can get square-wave voltage at the half-bridge switching node. On the other hand, we use Fairchild's FRFET to reduce the MOSFET body diode recovery during switching transition time to enhance the inverter ruggedness even in hard-switching conditions.

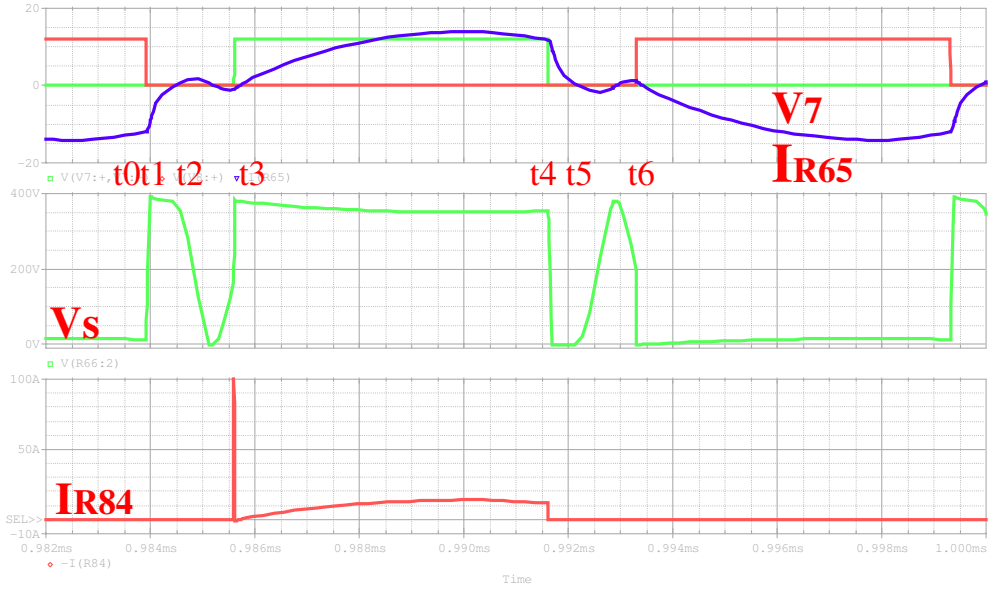

Figure 4. Operating Waveform

4. Fairchild Production Ready Board

Figure 5 is a Fairchild total solution for a 26” 4 U-shaped lamps LCD TV block diagram.

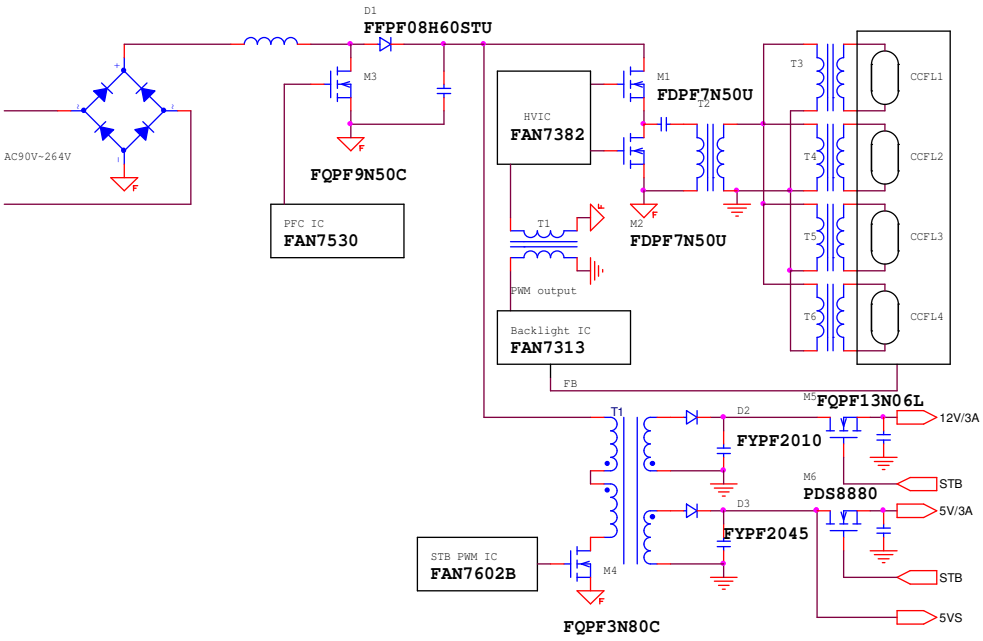

Figure 5.Super IP Fairchild Block Diagram

The specifications for this circuit were:
- Lamps typical operating voltage: 1920V_{RMS}
- Lamps typical operating current: 7.5mA_{RMS}
- Lamps starting voltage: 3180Vrms@ Ta = 0 ºC
- Lamps typical operating frequency: 56Khz
- Backlight typical power consumption: 54W
- Output 12V/3A for Audio Amp, 5V/3A for USB.
- Standby power<0.75W@AC240V, with 5V Standby /0.2A for MCU
- Open Lamp Protection, Lamp Short protection, Lamp over voltage protection
- Current balance :<+/-10%

The Backlight PWM IC FAN7313 was selected as it provided all the control functions, such as soft start, open lamp regulation, open lamp protection, over voltage protection, short circuit protection, UVLO, and synchronization circuit with an external signal for a series parallel resonant converter. At the same time, external component count is minimized and system cost is reduced by integration. It also supports analog and burst dimming modes of operation.

The FAN7313 provides all the control functions for a series parallel resonant converter as well as a pulse width modulation (PWM) controller to develop a supply voltage.

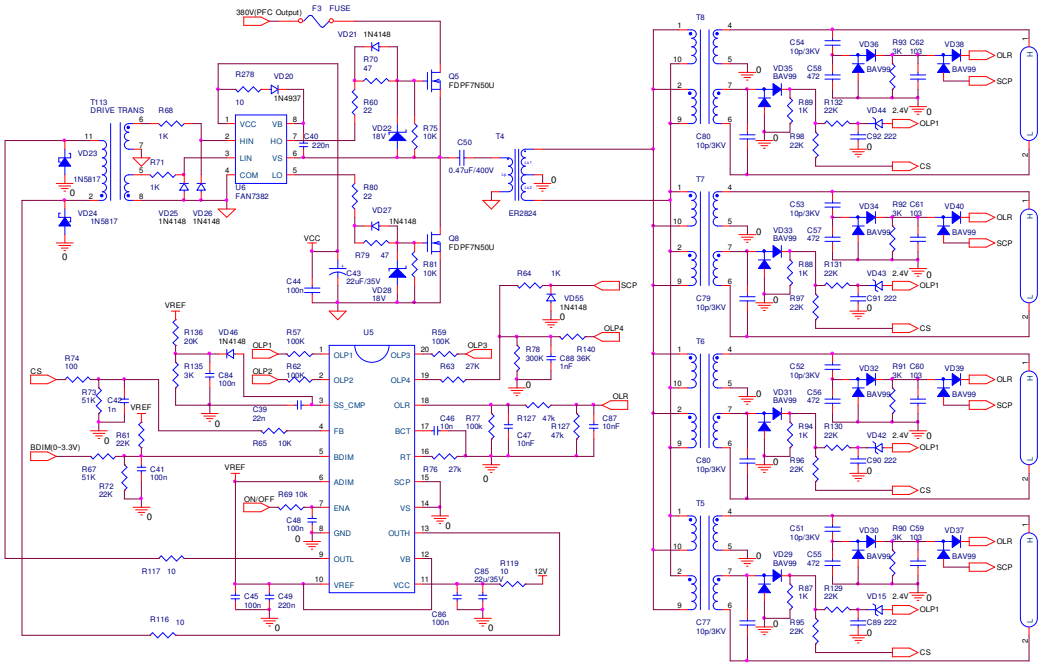

Figure 6. FAN7313 Backlight Super IP circuit

5. Design procedure

1) Set first stage Transformer T4 spec.

T4 isolates the primary side ground and secondary side ground, and convert 380V PFC high voltage to a middle square voltage +/-80V to drive secondary transformer. And T4 primary inductance should be large enough, so that the C50 and T4 primary resonant frequency are far smaller than the operating frequency 56K and the tank circuit will be inductive load for the half-bridge converter to achieve ZVS.

First, we choose C50=0.47uF/400V, set C50 and T4 primary inductance L resonant frequency to 7kHz, which is lower than the operating frequency 56khz. T4 primary inductance is

$$L = \frac{1}{(2\pi f)^2 C_{50}} = \frac{1}{(2 \cdot \pi \cdot 7\,kHz)^2 \cdot 0.47\,uf} = 1.1\,mH$$

Choose T4 primary inductance = 1mH, and EER28L core, with $A_e = 82\ mm^2$, The T4 primary minimum turns is

$$N_{p\min} = \frac{V_{in} \cdot \Delta t_{\max}}{\Delta B \cdot A_e} = \frac{190\ V \cdot 8.9\,us}{0.35\,T \cdot 82\ mm^2} = 58.9$$

We choose Np=60turns, T4 primary secondary turns is

$$N_s = \frac{N_p \cdot V_s}{V_p} = \frac{60 \cdot 80\,V}{190\ V} = 25.2$$

We choose Ns=26turns, so secondary output voltage is

$$V_s = \frac{N_s \cdot V_p}{N_p} = \frac{26 \cdot 190\ V}{60} = 82.3V$$

2) Set Second stage Transformer T5 spec.

T5, T6, T7, T8 are same transformers to convert the square voltage to square-wave voltage and then to a sinusoidal output to drive the CCFL.

First, we set the secondary resonant circuit frequency f_0=65kHz,Q=1, from (2.2), the leakage inductance is

$$L_l = \frac{R}{\omega_0 Q} = \frac{256k}{2 \cdot \pi \cdot 65kHz \cdot 1} = 0.627H$$

we chose L_l=0.6H, and EEL17 core, with $A_e = 22\ mm^2$, T5 primary minimum turns is

$$N_{p\min} = \frac{V_{in} \cdot \Delta t_{\max}}{\Delta B \cdot A_e} = \frac{82.3V \cdot 8.9us}{0.2T \cdot 22\ mm^2} = 166.4$$

Transfer the T5 input square-waveform to sinusoidal wave, the fundamental sinusoidal wave RMS Voltage is

$$V_{rms} = \frac{\sqrt{2}}{\pi} V_{in} \sin D\pi = \frac{\sqrt{2}}{\pi} \cdot 164.6V \cdot \sin \frac{\pi}{2} = 74.1V$$

From (2.3), the transformer turn ratio is

$$n \geq \frac{V_{lamp} \cdot \sqrt{\left\{1 - \left(\frac{\omega}{\omega_0}\right)^2\right\}^2 + \frac{1}{Q^2}\left(\frac{\omega}{\omega_0}\right)^2}}{V_{rms}} = \frac{1920V \cdot \sqrt{\left\{1 - \left(\frac{56kHz}{65kHz}\right)^2\right\}^2 + \left(\frac{56kHz}{65kHz}\right)^2}}{74.1V}$$

=23.29

Regarding minimum primary turns, minimum turns ratio and leakage inductance, we can then determine primary turns, turns ratio and the gap of core to get the required leakage inductance. For this application, the number of primary turns is 178Ts and that of the secondary turns is 4200Ts whereas the Turns ratio is 23.6.

3) Determine The Required Output Capacitance C51, C77

Assume a parasitic capacitance per U shape lamp is 5pF. Each parasitic capacitance is effectively in paralleled with the output capacitors. Then the output capacitor C51 is

$$C_{51} = 2 \cdot (C_p - C_{para}) = 2 \cdot (\frac{Q}{\omega_0 R_{Lamp}} - 5pF) = 2 \cdot (\frac{1}{2 \cdot \pi \cdot 65kHz \cdot 256k} - 5pF) = 10pF$$

we choose C51 & C77=10pF.

Summary
With the consumer demand for highly efficient and cost-effective LCD TVs, high voltage inverters need to provide efficiency at a minimal cost. This article explored an innovative solution that combines the power stage and inverter stage without a conventional DC-DC block after the PFC block. By using this advanced topology, LCD TV system efficiency and reliability were dramatically increased, while overall system cost was reduced.

REFERENCES

[1] Jason Choi, *Application Note "AN6017 LCD Backlight Inverter Drive IC（FAN7314）"*.Korea, Fairchild Semiconductor 2006.
[2] Datasheet FAN7313, Fairchild Semiconductor 2006.