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FAN7382

Half-Bridge Gate Driver (SOURCING/SINKING : 350mA/650mA)

Features

- Floating Cannel Designed For Bootstrap Operation To +600V.
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability For Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative VS Swing To -9V For Signal Propagation @ VCC=VBS=15V
- VCC & VBS Supply Range From 10V To 20V
- UVLO Functions For Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50nsec
- Output In-phase With Input

Description

The FAN7382 is a monolithic half-bridge gate driver IC for driving MOSFETs and IGBTs, which operate up to +600V. Fairchild's high voltage process and common-mode noise canceling technique give stable operation of high-side driver under high dv/dt noise circumstances. Advanced level shift circuit allows high-side gate driver operation up to VS=-9.8 V(typ.) for VBS=15V. The input logic level is compatible with standard TTL series logic gates. UVLO circuits for both channels prevent malfunction when VCC and VBS are lower than the specified threshold voltage. Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for the applications such as fluorescent lamp ballast, PDP scan driver, motor control, etc.

Typical Applications

- PDP Scan Driver
- Fluorescent Lamp Ballast

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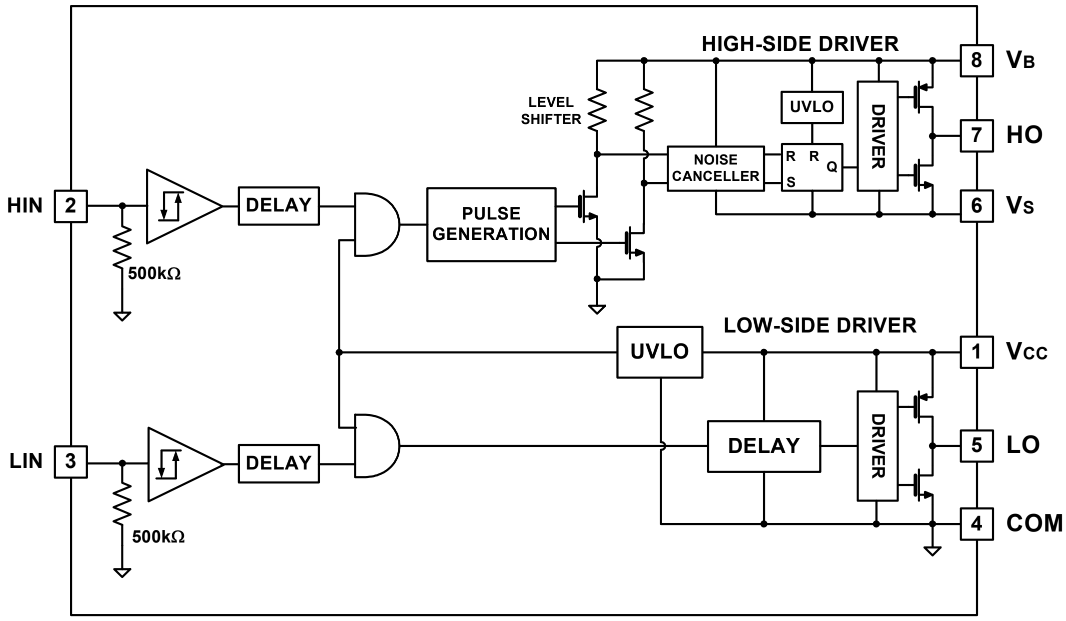
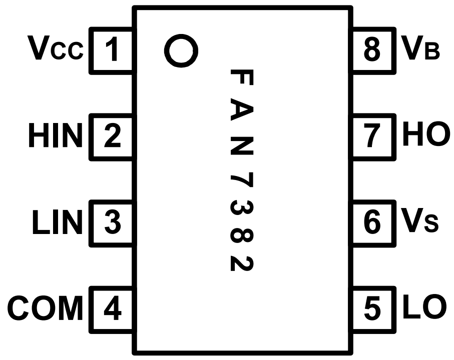
Internal Block Diagram



Rev. 0.0.3

Pin Assignments



Pin Descriptions

Pin No	Symbol	I/O	Decription
1	VCC		Low Side Supply Voltage
2	HIN		Logic Input for High Side Gate Driver Output
3	LIN		Logic Input for Low Side Gate Driver Output
4	COM		Logic Ground and Low Side Driver Return
5	LO		Low Side Driver Output
6	VS		High Voltage Floating Supply Return
7	HO		High Side Driver Output
8	VB		High Side Floating Supply

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
High side offset Voltage	V_S	V_{BS}-25	-	V_{BS}+0.3	V
High side floating supply voltage	V_B	-0.3		625	
High side floating output voltage HO	V_{HO}	V_S-0.3		V_B+0.3	
Low side and logic fixed supply voltage	V_{CC}	-0.3		25	
Low side output voltage LO	V_{LO}	-0.3		V_{CC}+0.3	
Logic input voltage(HIN, LIN)	V_{IN}	-0.3		V_{CC}+0.3	
Logic Ground	Com	V_{CC}-25		V_{CC}+0.3	
Allowable offset voltage SLEW RATE	dVs/dt			50	V/ns
Power Dissipation	P_D			0.625	W
Thermal resistance, junction to ambient	Rthja			200	°C/W
Junction Temperature	T_J			150	°C
Storage Temperature	T_S			150	°C

Note : Absolute maximum ratings indicate sustained limits beyound which damage to the device may occur. All voltage parameters are absolute voltage referenced to COM, all currents are defined positive into any lead.

Recommended Operating Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
High side floating supply voltage	V_B	V_S+10	-	V_S+20	V
High side floating supply offset voltage	V_S	6-V_{CC}		600	
High side(HO) output voltage	V_{HO}	V_S		V_B	
Low side(LO) output voltage	V_{LO}	COM		V_{CC}	
Logic input voltage(HIN, LIN)	V_{IN}	COM		V_{CC}	
Low side supply voltage	V_{CC}	10		20	
Ambient Temperature	T_A	-40		125	°C

ESD Level

Parameter	PIns	Conditions	Level	Unit
Human Body Model(HBM)	VCC,COM,HIN,LIN,LO	R=1.5kΩ, C=100pF	±2,000	V
	VB,HO,VS		±1,500	
Machine Model(MM)	VCC,COM,HIN,LIN, VB,HO,VS	C=200pF	±300	
	LO		±200	
Charged Device Model(CDM)	All Pins		±500	

Static Electrical Characteristics

(V_{BIAS}(V_{CC}, V_{BS})=15.0V, T_A = 25°C, unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and V_S is applicable to HO and LO.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCC and VBS supply undervoltage positive going threshold	V_{CCUV+} V_{BSUV+}		8.2	9.2	10.0	V
VCC and VBS supply undervoltage negative going threshold	V_{CCUV-} V_{BSUV-}		7.6	8.7	9.6	
VCC supply undervoltage lockout hysteresis	V_{CCUVH} V_{BSUVH}		-	0.6	-	
Offset supply leakage current	I_{LK}	V_B=V_S=600V	-	-	50	uA
Quiescent VBS supply current	I_{QBS}	V_{IN}=0V or 5V	-	45	120	
Quiescent VCC supply current	I_{QCC}	V_{IN}=0V or 5V	-	70	180	
Operating VBS supply current	I_{PBS}	f_{in}=20kHz,rms value	-	-	600	uA
Operating VCC supply current	I_{PCC}	f_{in}=20kHz,rms value	-	-	600	
Logic "1" input voltage	V_{IH}		2.9	-	-	V
Logic "0" input voltage	V_{IL}		-	-	0.8	
High level output voltage, VBIAS-VO	V_{OH}	I_O=20mA	-	-	1.0	
Low level output voltage, VO	V_{OL}		-	-	0.6	
Logic "1" input bias current	I_{IN+}	V_{IN}=5V	-	10	20	uA
Logic "0" input bias current	I_{IN-}	V_{IN}=0V	-	1.0	2.0	
Output high short circuit pulse current	I_{O+}	V_O=0V PW<10us	250	350	-	mA
Output low short circuit pulsed current	I_{O-}	V_O=V_B, PW<10us	500	650	-	
Allowable negative VS pin voltage for HIN signal propagation to HO	VS		-	-9.8	-7	V

Dynamic Electrical Characteristics

(V_{BIAS}(V_{CC}, V_{BS})=15.0V, V_S=COM, C_L=1000pF and T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	t_{on}	V_S=0V	100	170	300	ns
Turn-off propatation delay	t_{off}	V_S=0V or 600V	100	200	300	
Turn-on rise time	t_r		20	60	140	
Turn-off fall time	t_f		-	30	80	
Delay matching, HS & LS turn-on/off	MT		-	-	50	

Typical Characteristics

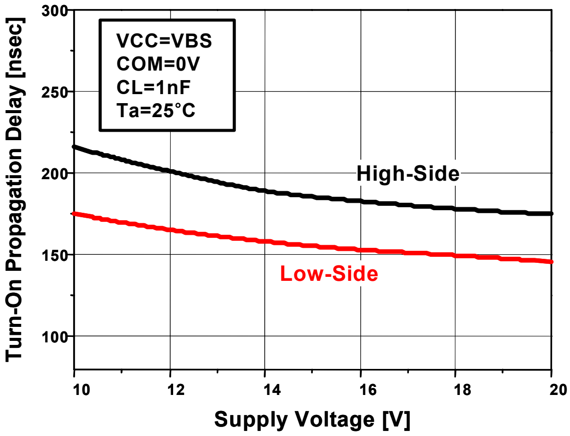


Fig. 1 Turn-On Propagation Delay vs. Supply Voltage

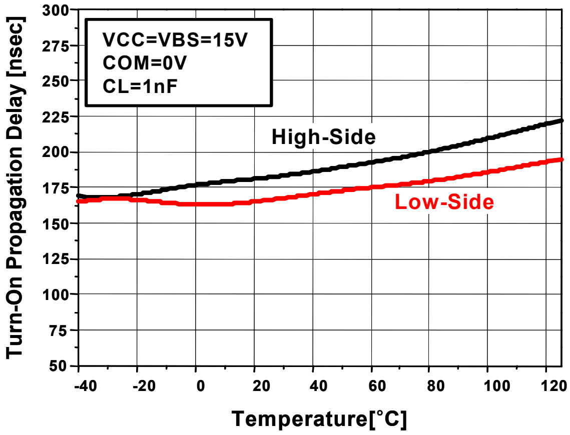


Fig. 2 Turn-On Propagation Delay vs. Temperature

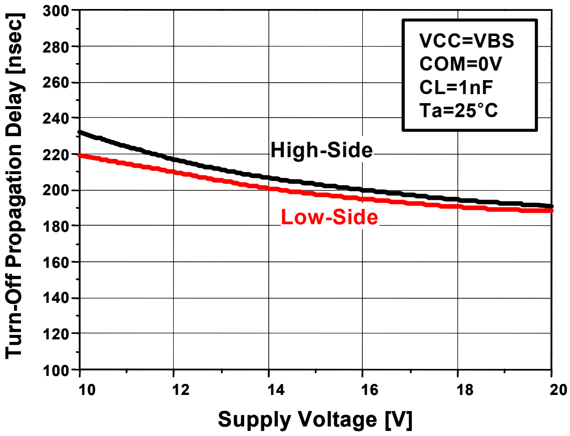


Fig. 3 Turn-Off Propagation Delay vs. Supply Voltage

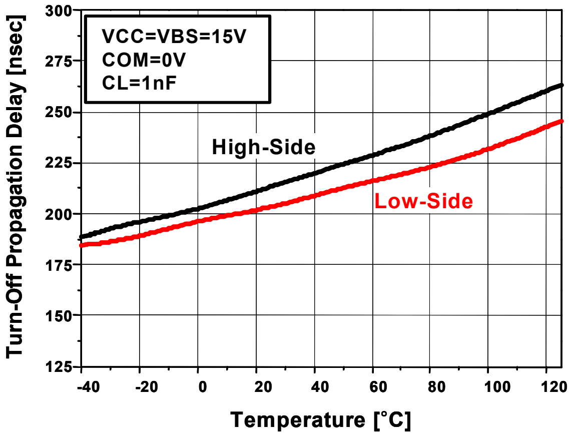


Fig. 4 Turn-Off Propagation Delay vs. Temperature

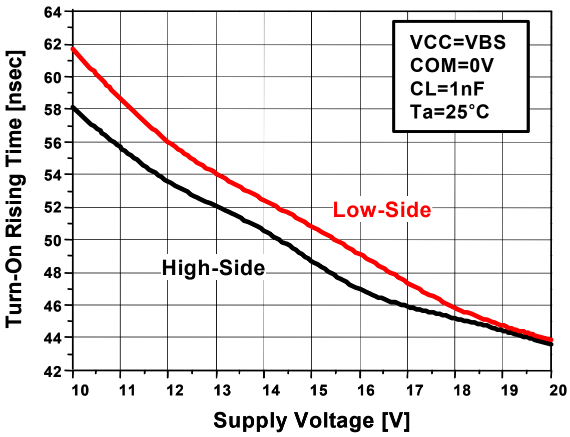


Fig. 5 Turn-On Rising Time vs. Supply Voltage

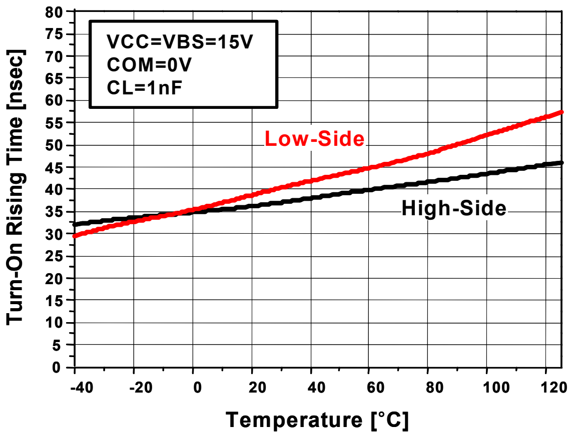


Fig. 6 Turn-On Rising Time vs. Temperature

Typical Characteristics(cont')

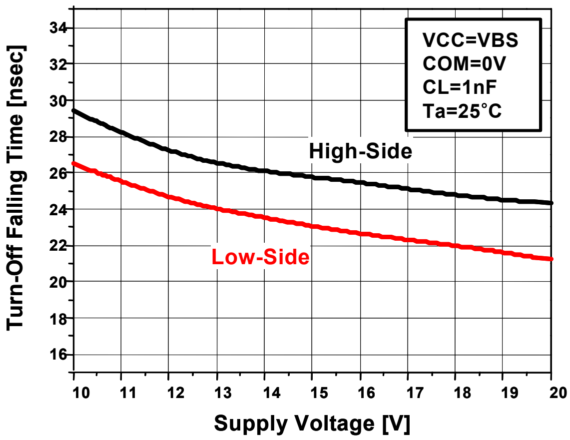


Fig. 7 Turn-Off Falling Time vs. Supply Voltage

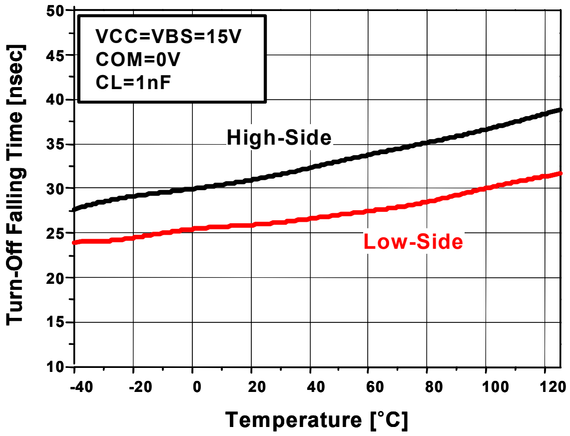


Fig. 8 Turn-Off Falling Time vs. Temperature

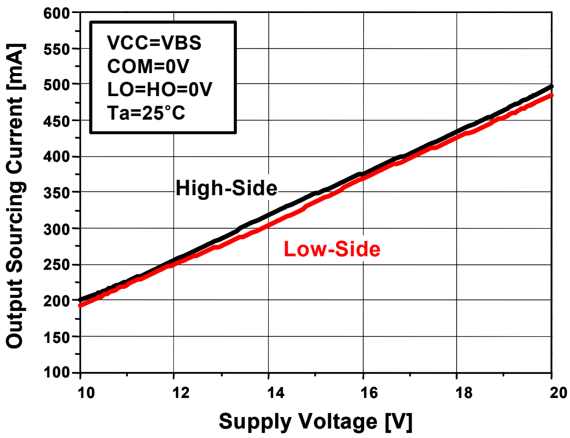


Fig. 9 Output Sourcing Current vs. Supply Voltage

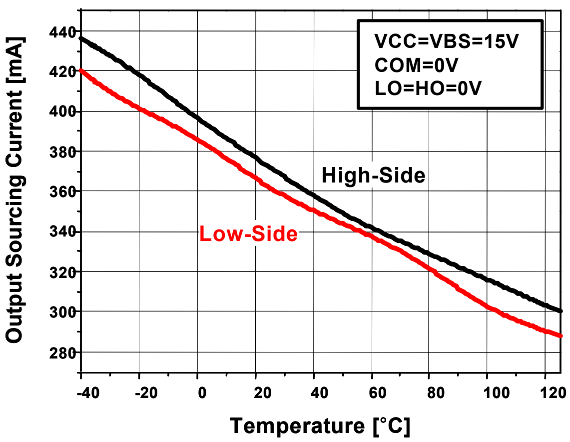


Fig. 10 Output Sourcing Current vs. Temperature

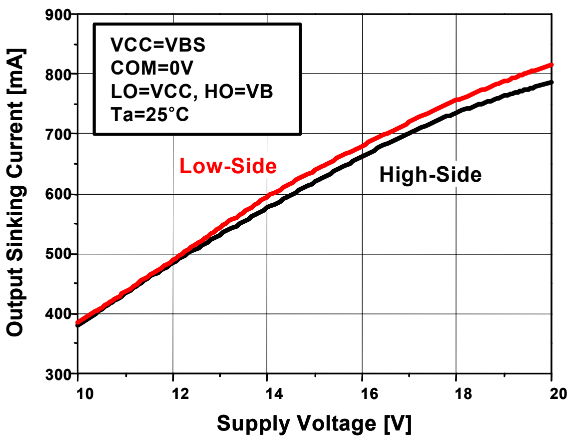


Fig. 11 Output Sinking Current vs. Supply Voltage

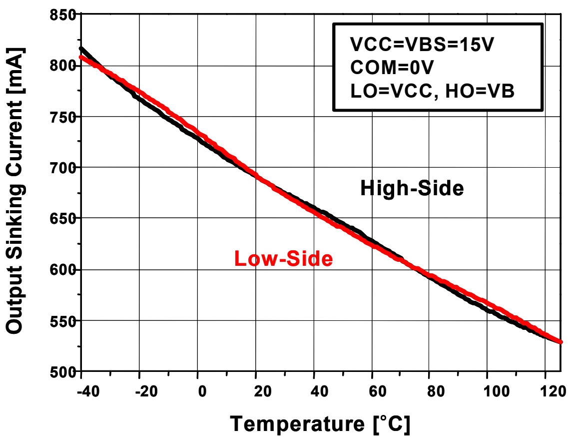


Fig. 12 Output Sinking Current vs. Temperature

Typical Characteristics

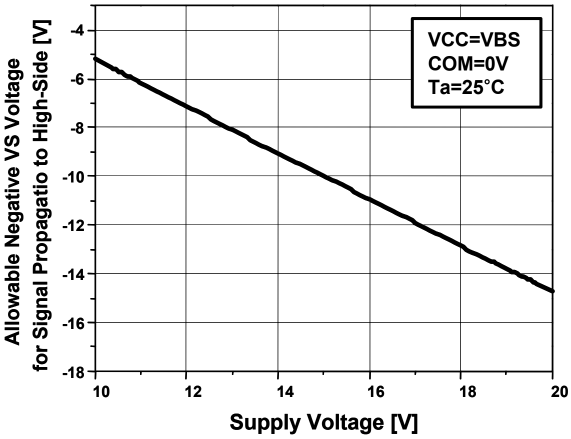


Fig. 13 Allowable Negative VS Voltage
for Signal Propagation to High Side vs. Supply Voltage

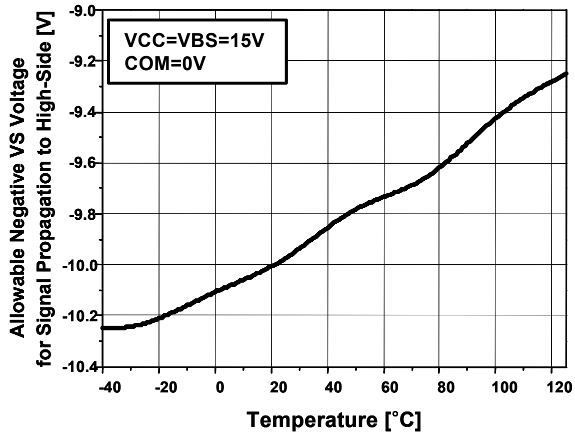


Fig. 14 Allowable Negative VS Voltage
for Signal Propagation to High Side vs. Temperature

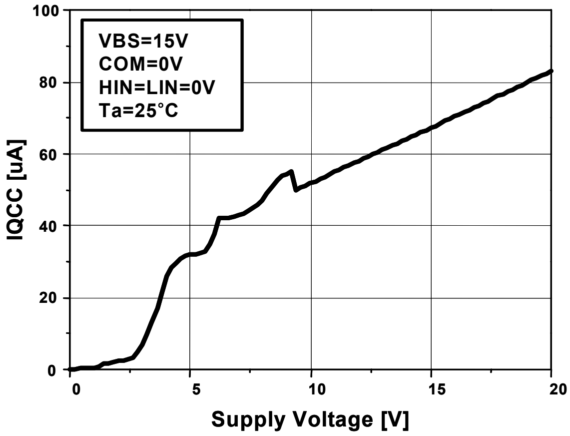


Fig. 15 I_{QCC} vs. Supply Voltage

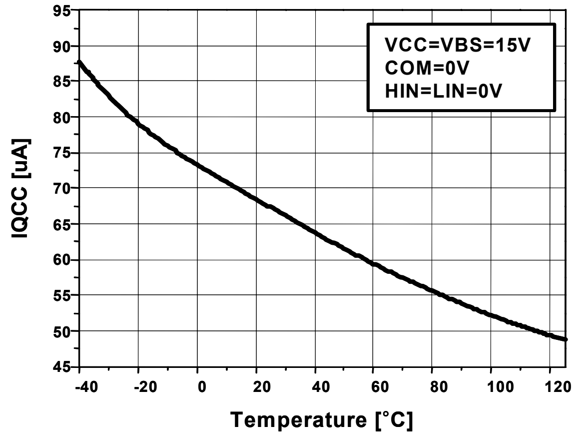


Fig. 16 I_{QCC} vs. Temperature

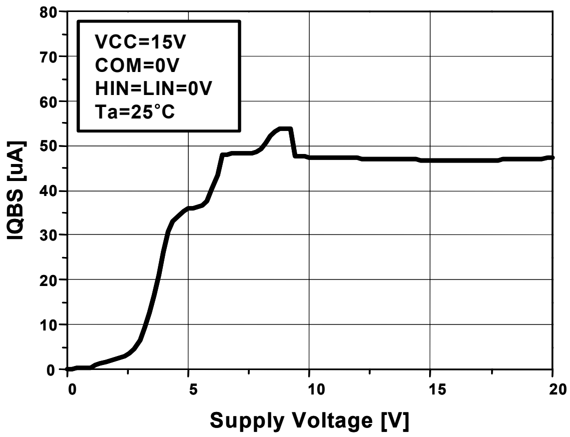


Fig. 17 I_{QBS} vs. Supply Voltage

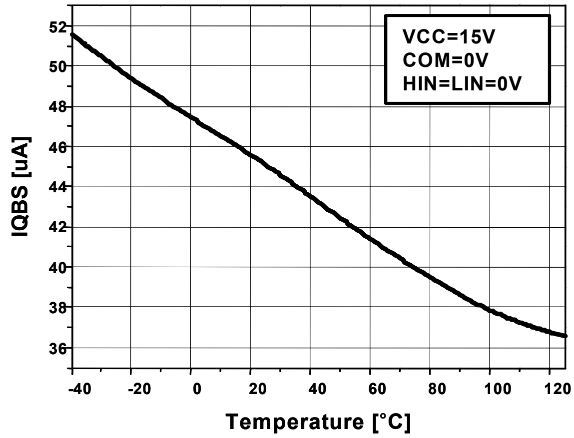


Fig. 18 I_{QBS} vs. Temperature

Typical Characteristics

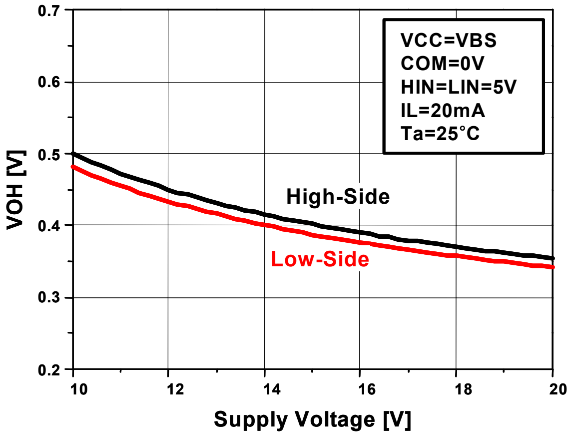


Fig. 19 High Level Output Voltage vs. Supply Voltage

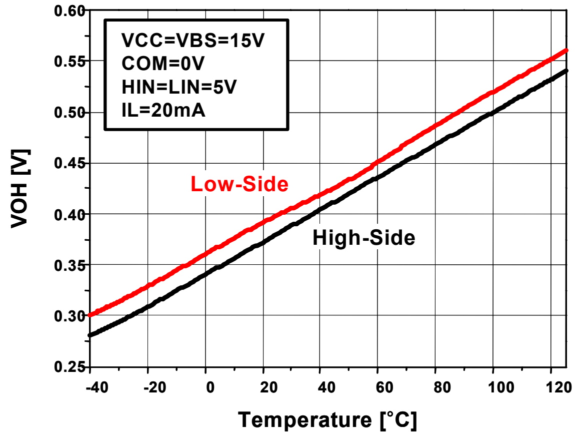


Fig. 20 High Level Output Voltage vs. Temperature

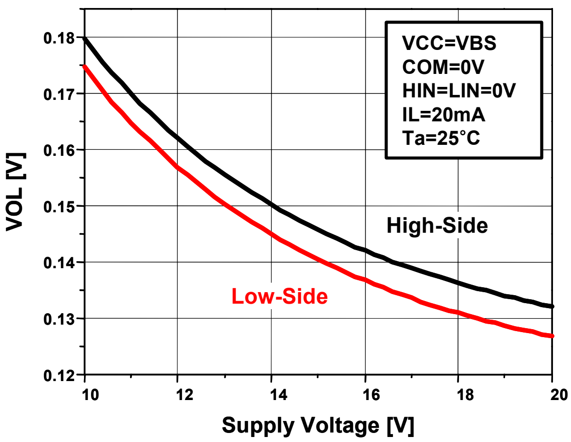


Fig. 21 Low Level Output Voltage vs. Supply Voltage

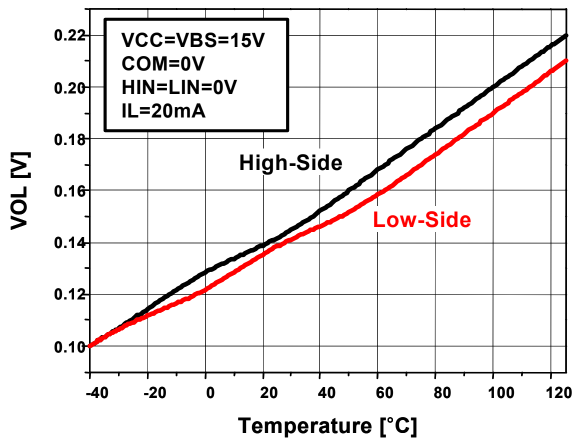


Fig. 22 Low Level Output Voltage vs. Temperature

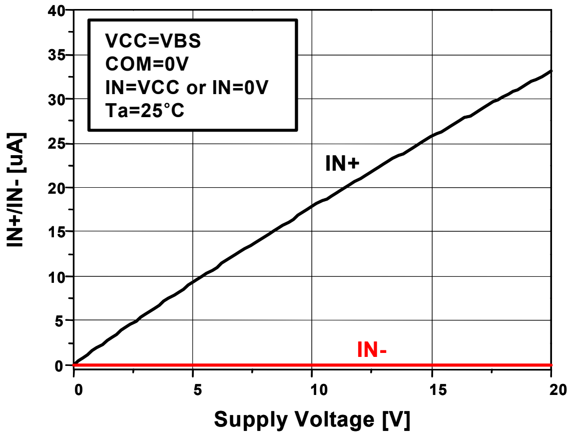


Fig. 23 Input Bias Current vs. Supply Voltage

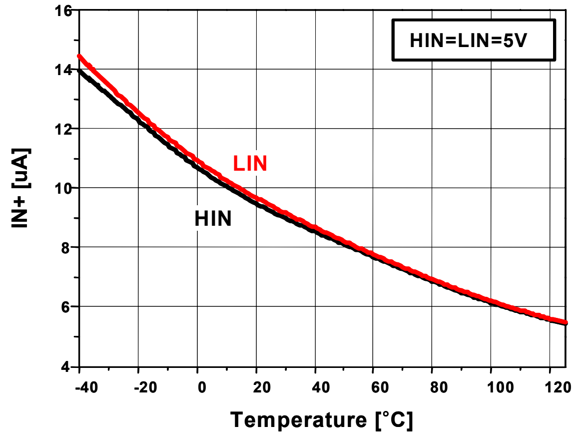


Fig. 24 Input Bias Current vs. Temperature

Typical Characteristics

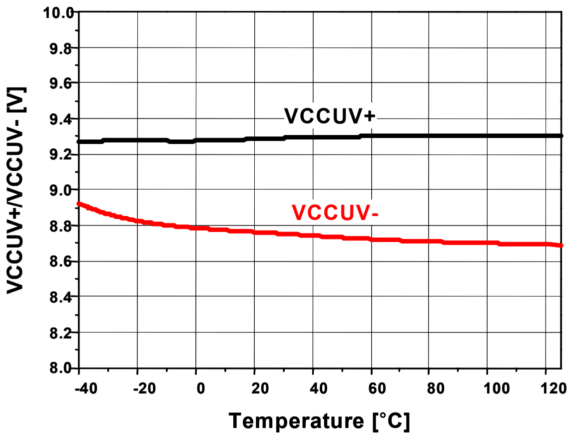


Fig. 25 VCC UVLO Threshold Voltage vs. Temperature

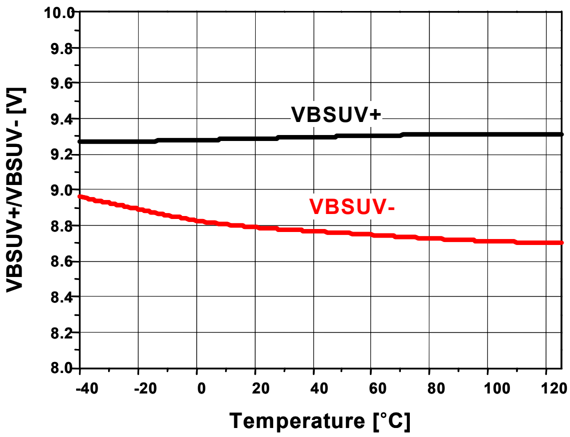


Fig. 26 VBS UVLO Threshold Voltage vs. Temperature

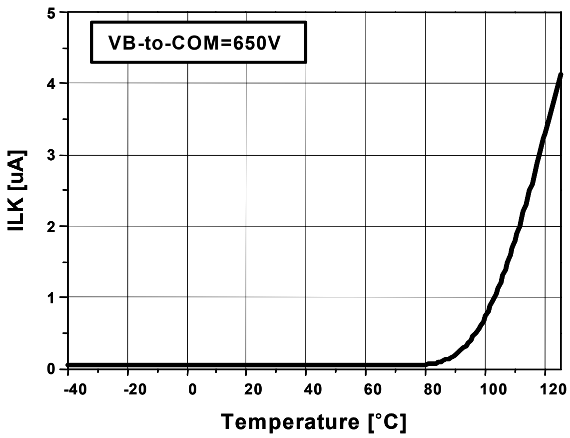


Fig. 27 VB to COM Leakage Current vs. Temperature

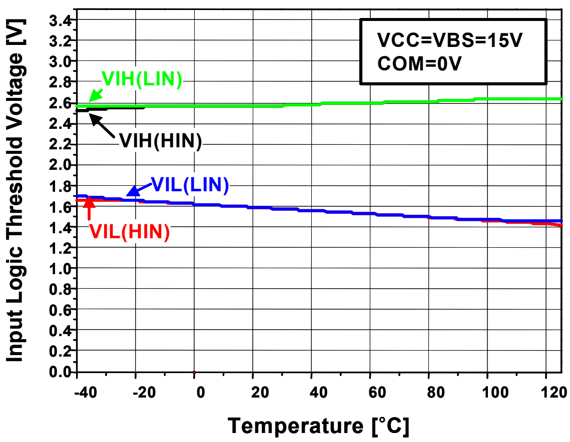


Fig. 28 Input Logic Threshold vs. Temperature

Typical Characteristics

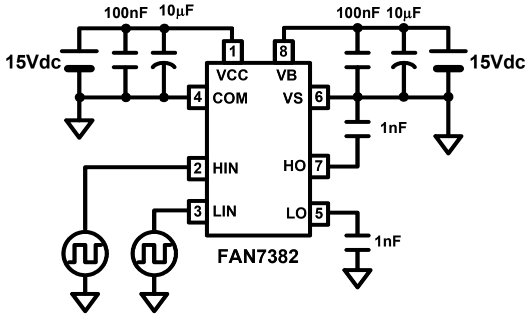


Fig. 29 Switching Time Test Circuit

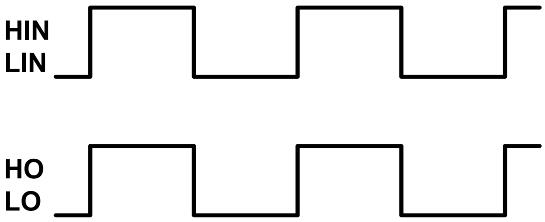


Fig. 30 Input / Output Timing Diagram

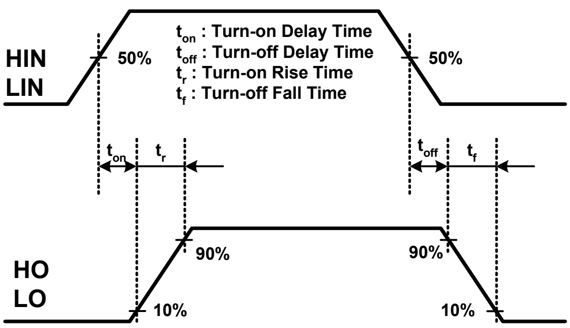


Fig. 31 Switching Time Waveform Definitions

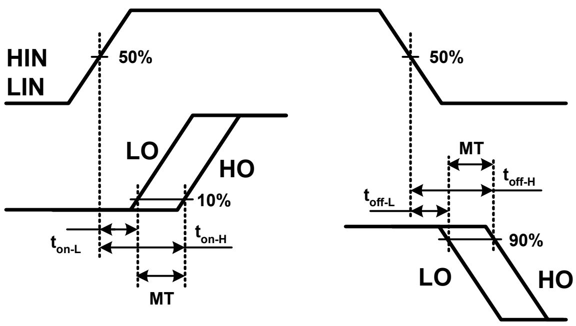
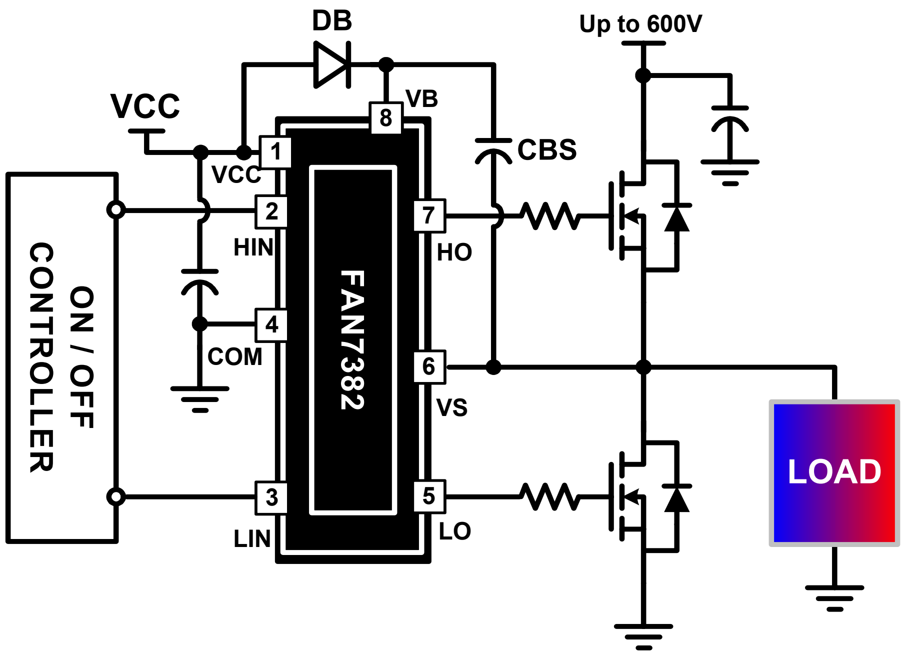


Fig. 32 Delay Matching Waveform Definition

Typical Application Circuit



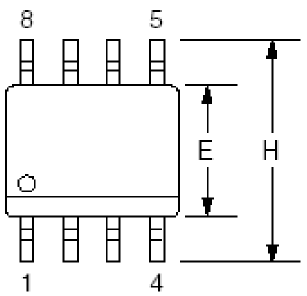
Mechanical Dimensions

Package

Dimensions in millimeters

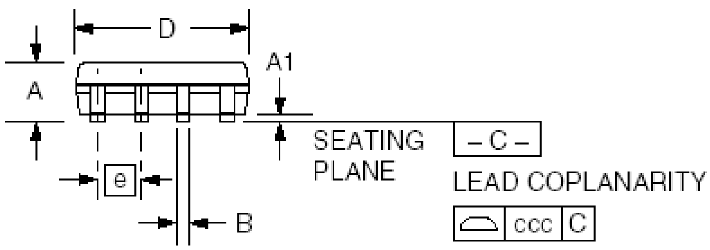
8-SOP

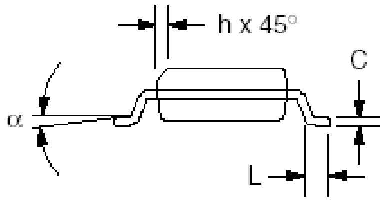
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	



Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





Ordering Information

Device	Package	Operating Temperature	Packing
FAN7382M	8SOIC	-40°C ~ +125°C	Tube
FAN7382MX			Tape & Reel

2/24/05 0.0m 001
Stock#DSxxxxxxxx