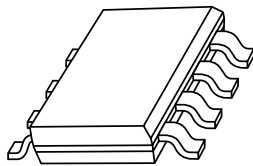


DATA SHEET



PHC2300

Complementary enhancement
mode MOS transistors

Product specification
Supersedes data of 1997 Oct 24

2002 Jul 09

Complementary enhancement mode MOS transistors

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FEATURES

- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Universal line interface in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s ₁	source 1
2	g ₁	gate 1
3	s ₂	source 2
4	g ₂	gate 2
5	d ₂	drain 2
6	d ₂	drain 2
7	d ₁	drain 1
8	d ₁	drain 1

CAUTION

The device is supplied in an antistatic package.
The gate-source input must be protected against static discharge during transport or handling.

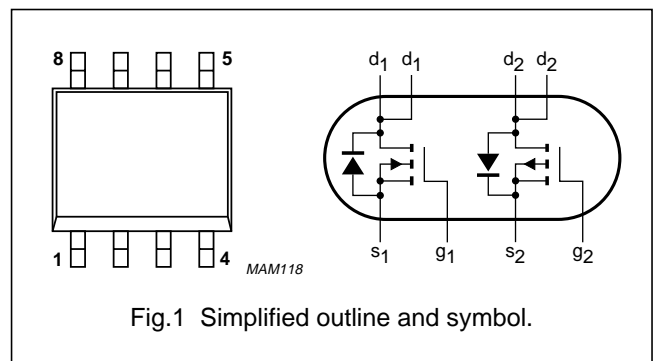


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V _{DS}	drain-source voltage (DC) N-channel P-channel		–	300 –300	V V
V _{GS}	gate-source voltage (DC)		–	±20	V
V _{GSth}	gate-source threshold voltage N-channel P-channel	V _{DS} = V _{GS} ; I _D = 1 mA V _{DS} = V _{GS} ; I _D = –1 mA	0.8 –0.8	2 –2	V V
I _D	drain current (DC) N-channel P-channel	T _s = 80 °C	– –	340 –235	mA mA
R _{DSon}	drain-source on-state resistance N-channel P-channel	V _{GS} = 10 V; I _D = 170 mA V _{GS} = –10 V; I _D = –115 mA	– –	6 17	Ω Ω
P _{tot}	total power dissipation	T _s = 80 °C	–	1.6	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

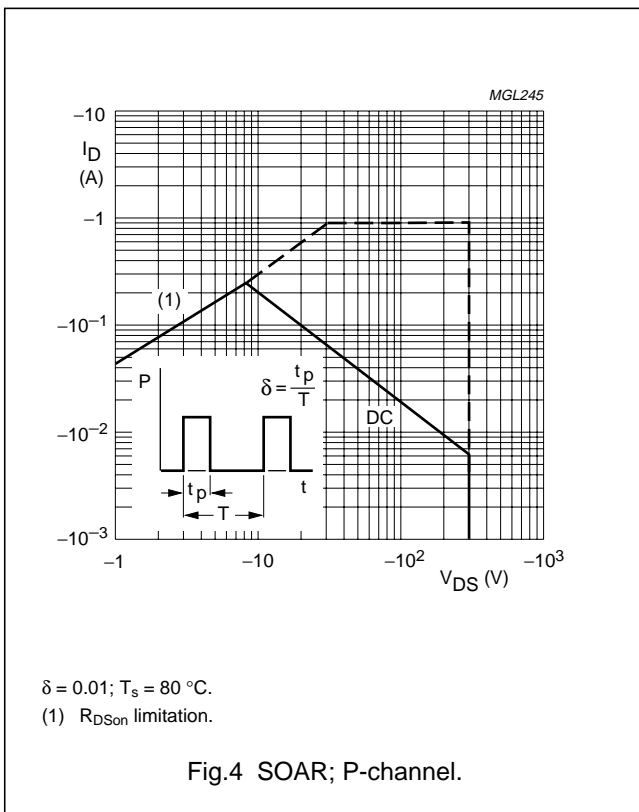
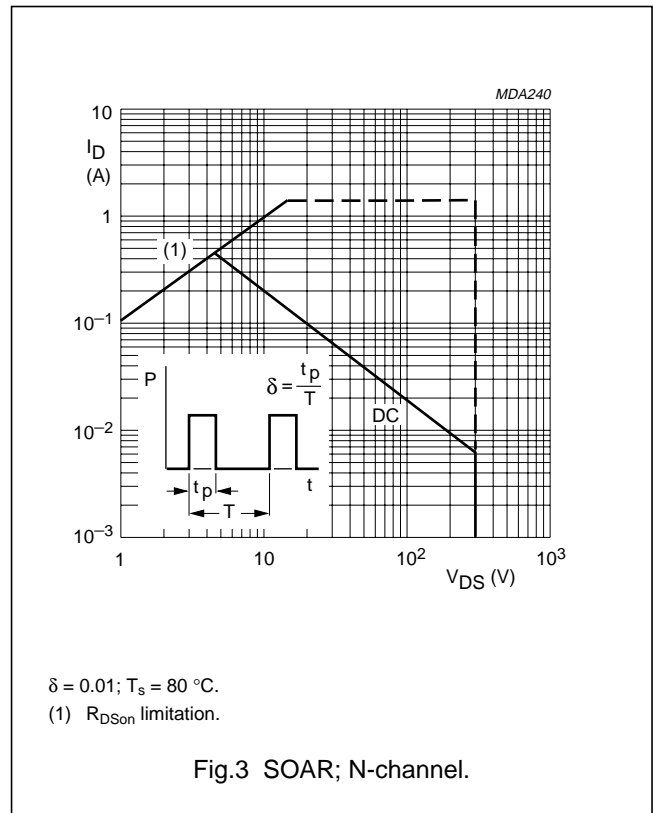
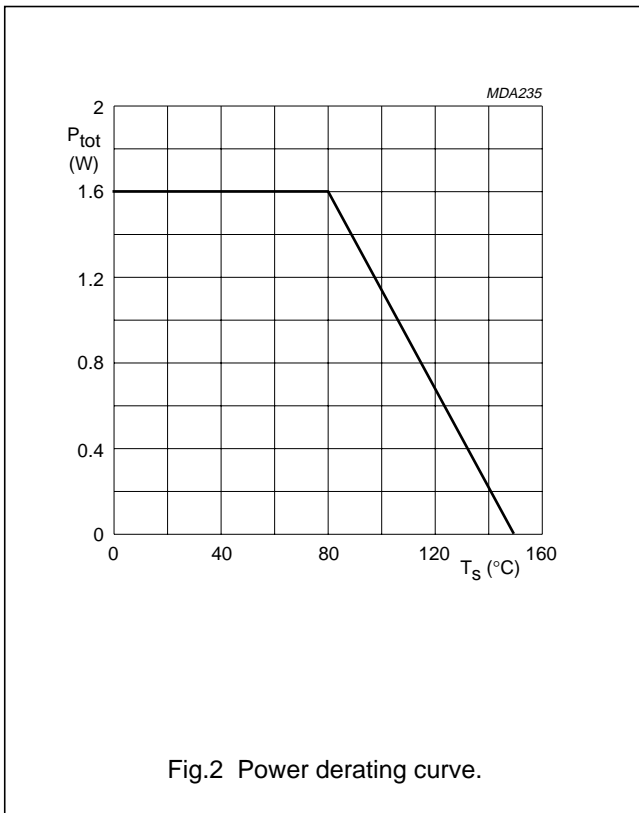
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V _{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V _{GS}	gate-source voltage (DC)		–	±20	V
I _D	drain current (DC)	T _s = 80 °C; note 1			
	N-channel		–	340	mA
	P-channel		–	–235	mA
I _{DM}	peak drain current	note 2			
	N-channel		–	1.4	A
	P-channel		–	–0.9	A
P _{tot}	total power dissipation	T _s = 80 °C; note 3	–	1.6	W
		T _{amb} = 25 °C; note 4	–	1.8	W
		T _{amb} = 25 °C; note 5	–	0.9	W
		T _{amb} = 25 °C; note 6	–	1.2	W
T _{stg}	storage temperature		–55	+150	°C
T _j	operating junction temperature		–55	+150	°C

Notes

1. T_s is the temperature at the soldering point of the drain leads.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor (both devices may thus be loaded up to 1.6 W at the same time).
4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an R_{th a-tp} (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an R_{th a-tp} (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an R_{th a-tp} (ambient to tie-point) of 90 K/W.

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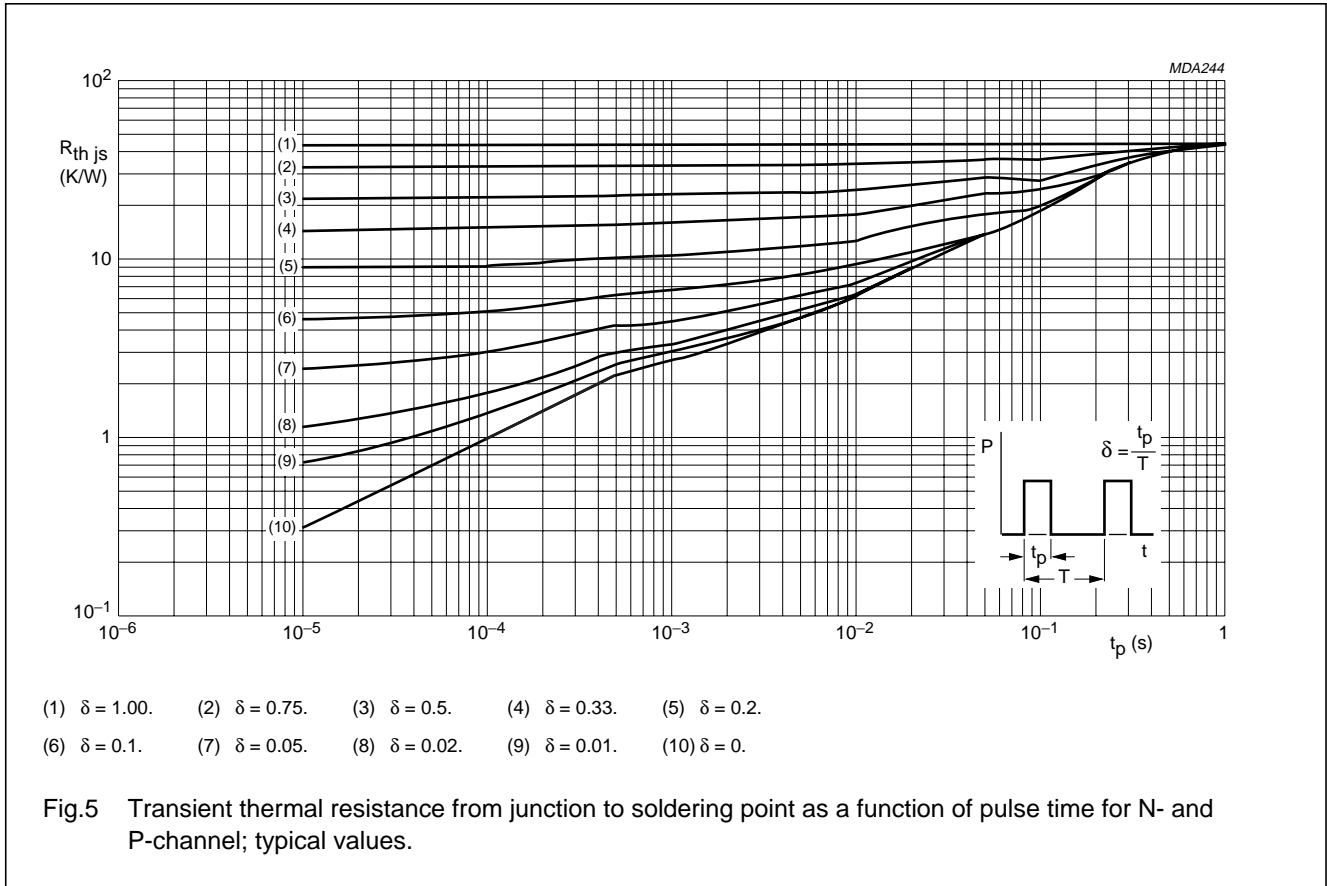


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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	43	K/W



CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	$V_{GS} = 0; I_D = 10\ \mu\text{A}$	300	–	–	V
	P-channel	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-300	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	$V_{GS} = V_{DS}; I_D = 1\ \text{mA}$	0.8	–	2	V
	P-channel	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-0.8	–	-2	V
I_{DSS}	drain-source leakage current					
	N-channel	$V_{GS} = 0; V_{DS} = 240\ \text{V}$	–	–	100	nA
	P-channel	$V_{GS} = 0; V_{DS} = -240\ \text{V}$	–	–	-100	nA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GSS}	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$				
	N-channel		–	–	± 100	nA
	P-channel		–	–	± 100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	$V_{GS} = 10 \text{ V}; I_D = 170 \text{ mA}$	–	–	6	Ω
	P-channel	$V_{GS} = -10 \text{ V}; I_D = -115 \text{ mA}$	–	–	17	Ω
C_{iss}	input capacitance					
	N-channel	$V_{GS} = 0; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	–	102	–	pF
	P-channel	$V_{GS} = 0; V_{DS} = -50 \text{ V}; f = 1 \text{ MHz}$	–	45	–	pF
C_{oss}	output capacitance					
	N-channel	$V_{GS} = 0; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	–	15	–	pF
	P-channel	$V_{GS} = 0; V_{DS} = -50 \text{ V}; f = 1 \text{ MHz}$	–	15	–	pF
C_{rss}	reverse transfer capacitance					
	N-channel	$V_{GS} = 0; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	–	7.3	–	pF
	P-channel	$V_{GS} = 0; V_{DS} = -50 \text{ V}; f = 1 \text{ MHz}$	–	3	–	pF
Q_G	total gate charge					
	N-channel	$V_{GS} = 10 \text{ V}; V_{DS} = 50 \text{ V}; I_D = 170 \text{ mA}$	–	6240	–	pC
	P-channel	$V_{GS} = -10 \text{ V}; V_{DS} = -50 \text{ V}; I_D = -115 \text{ mA}$	–	2137	–	pC
Q_{GS}	gate-source charge					
	N-channel	$V_{GS} = 10 \text{ V}; V_{DS} = 50 \text{ V}; I_D = 170 \text{ mA}$	–	226	–	pC
	P-channel	$V_{GS} = -10 \text{ V}; V_{DS} = -50 \text{ V}; I_D = -115 \text{ mA}$	–	68	–	pC
Q_{GD}	gate-drain charge					
	N-channel	$V_{GS} = 10 \text{ V}; V_{DS} = 50 \text{ V}; I_D = 170 \text{ mA}$	–	1385	–	pC
	P-channel	$V_{GS} = -10 \text{ V}; V_{DS} = -50 \text{ V}; I_D = -115 \text{ mA}$	–	674	–	pC
Switching times						
t_{on}	turn-on time					
	N-channel	$V_{GS} = 0 \text{ to } 10 \text{ V}; V_{DD} = 50 \text{ V}; I_D = 170 \text{ mA}$	–	7	12	ns
	P-channel	$V_{GS} = 0 \text{ to } -10 \text{ V}; V_{DD} = -50 \text{ V}; I_D = -115 \text{ mA}$	–	4	10	ns
t_{off}	turn-off time					
	N-channel	$V_{GS} = 10 \text{ to } 0 \text{ V}; V_{DD} = 50 \text{ V}; I_D = 170 \text{ mA}$	–	53	65	ns
	P-channel	$V_{GS} = -10 \text{ to } 0 \text{ V}; V_{DD} = -50 \text{ V}; I_D = -115 \text{ mA}$	–	25	35	ns

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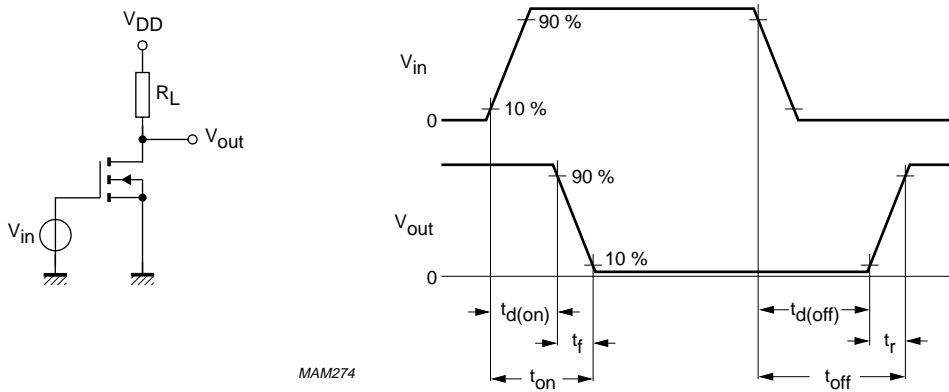


Fig.6 Switching times test circuit with input and output waveforms; N-channel.

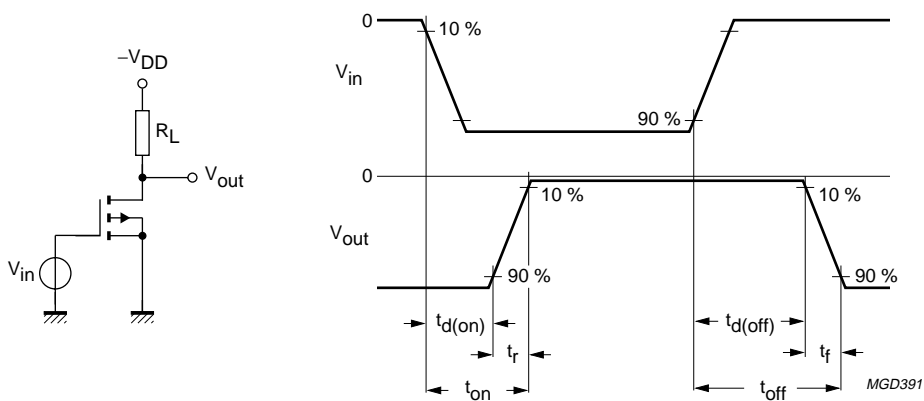
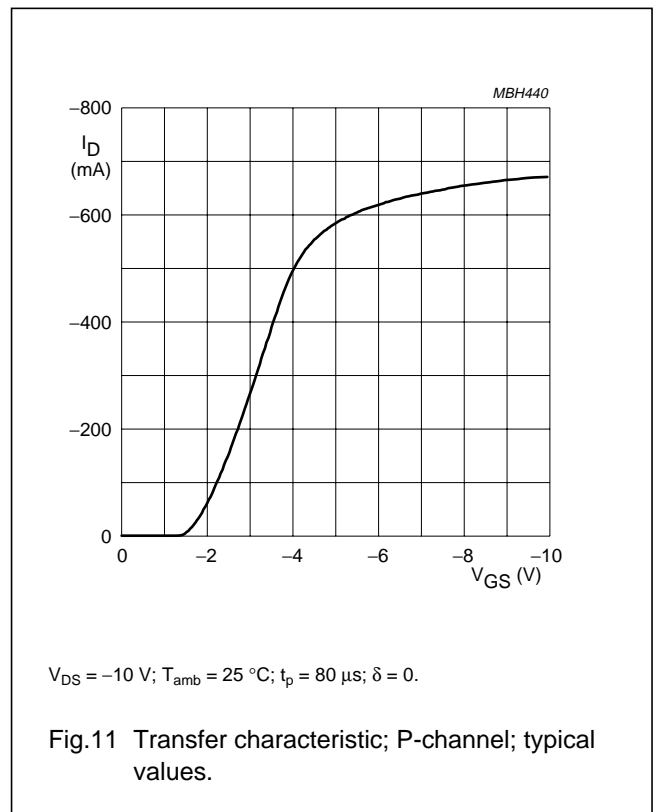
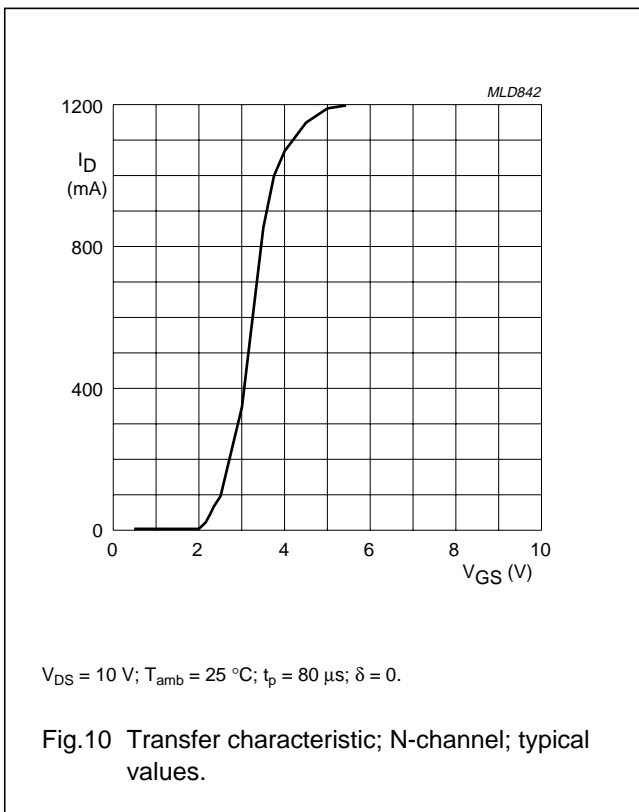
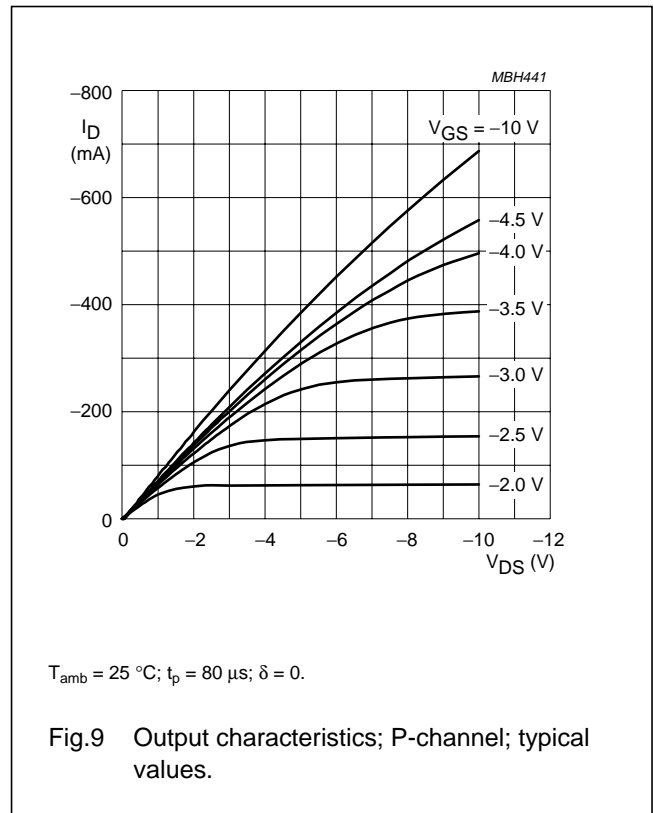
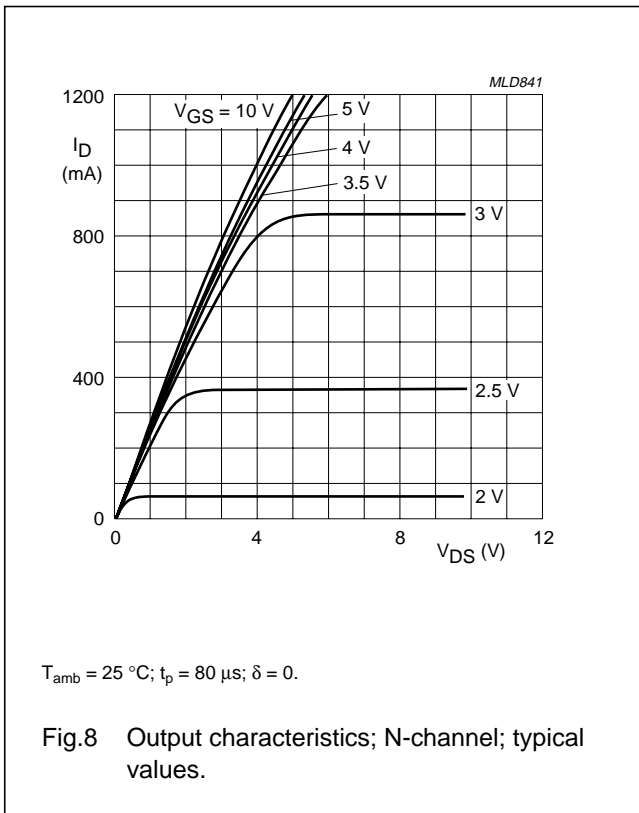


Fig.7 Switching times test circuit with input and output waveforms; P-channel.

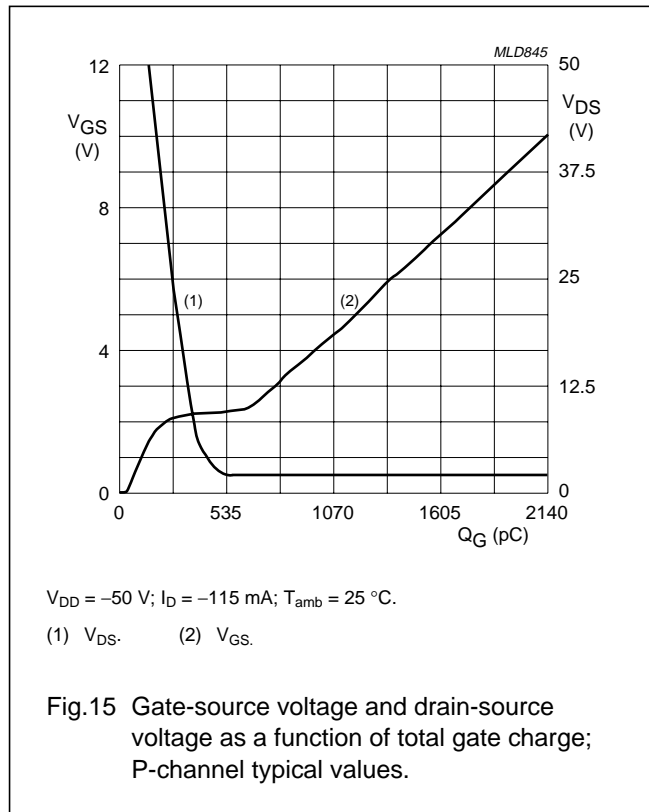
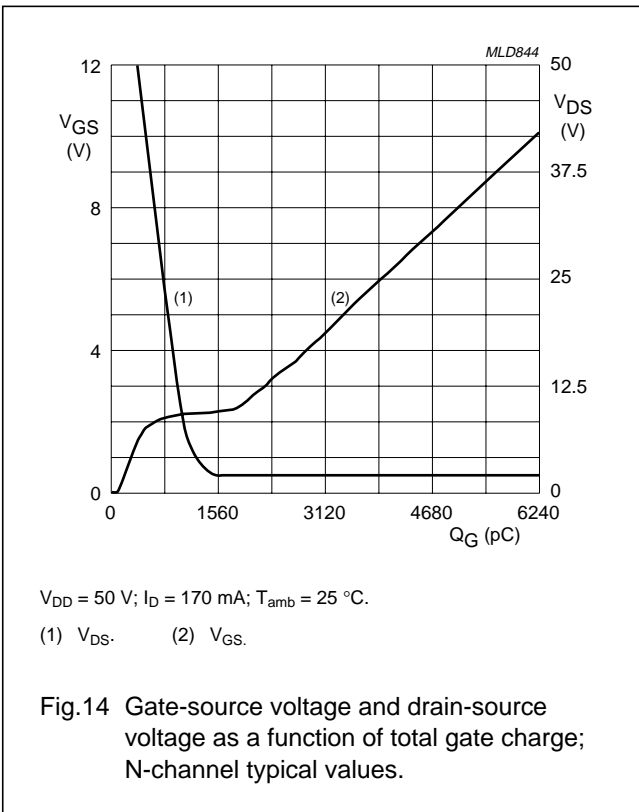
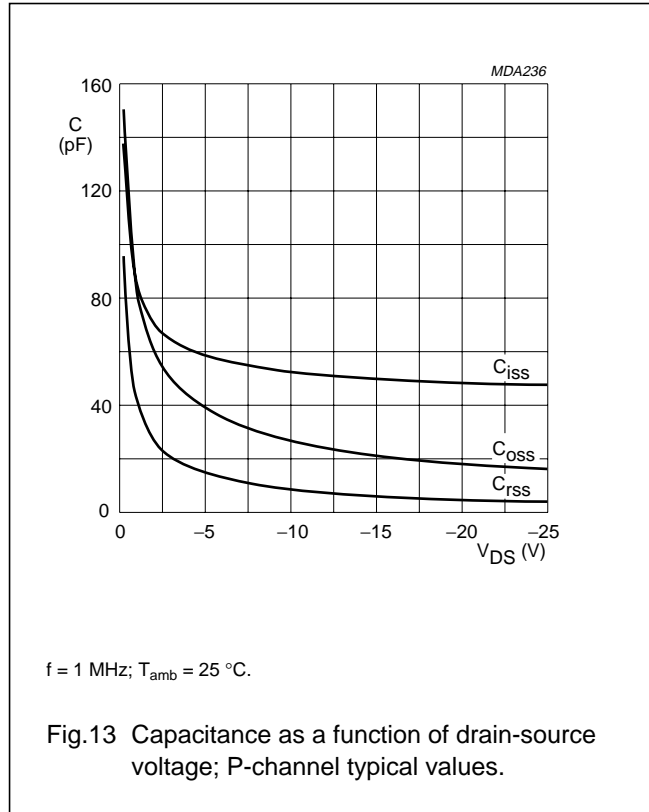
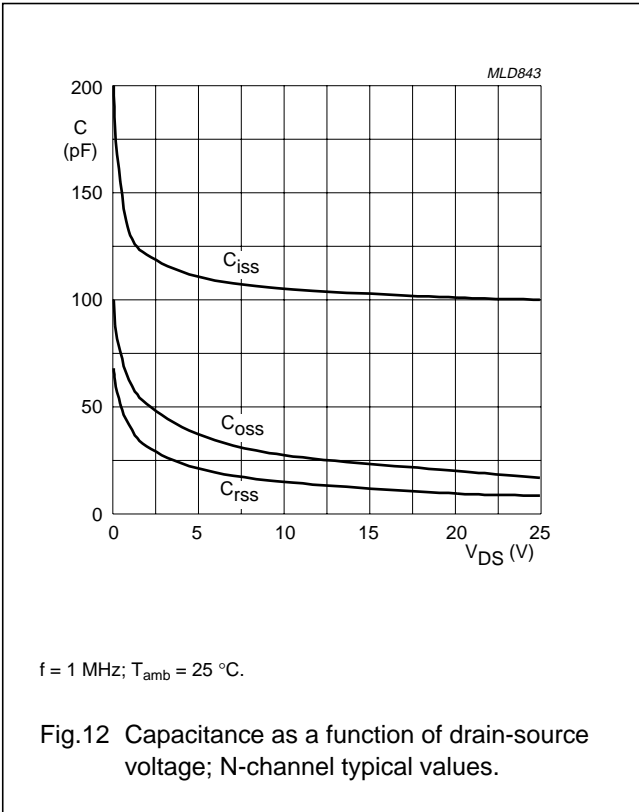
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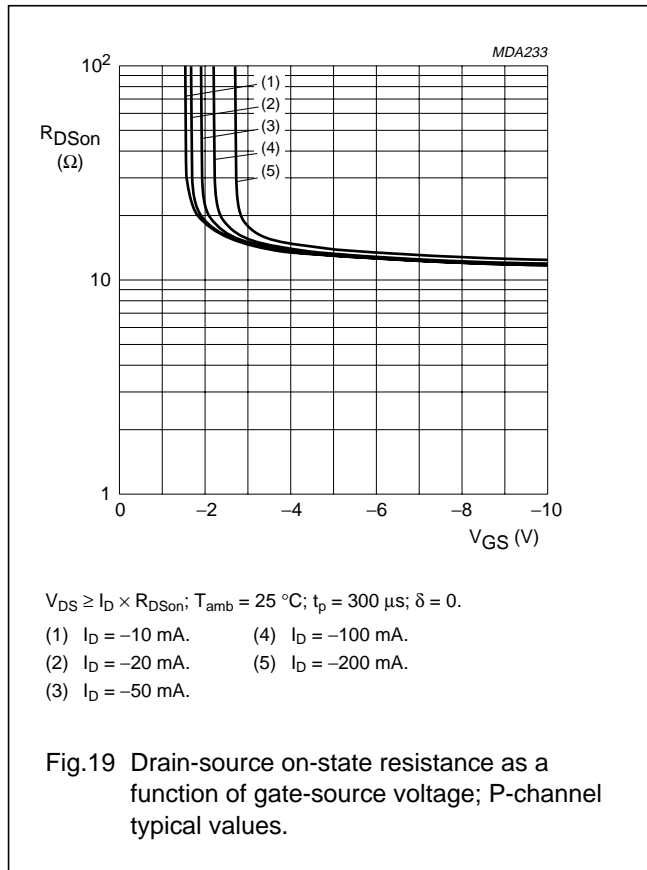
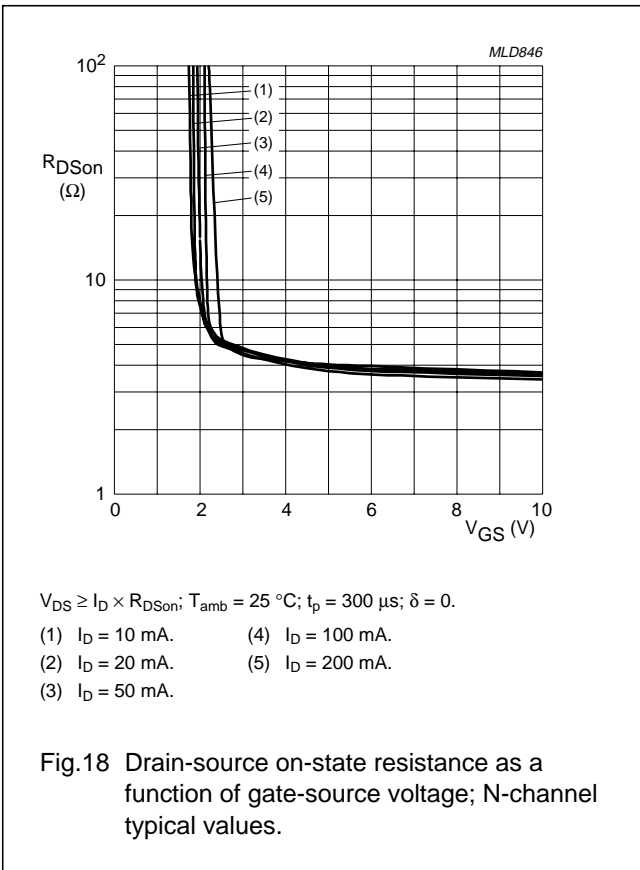
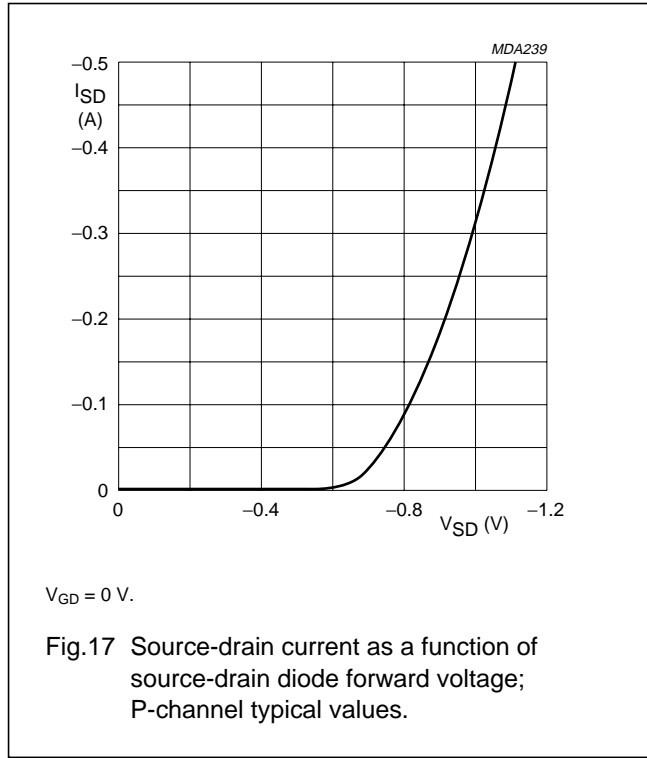
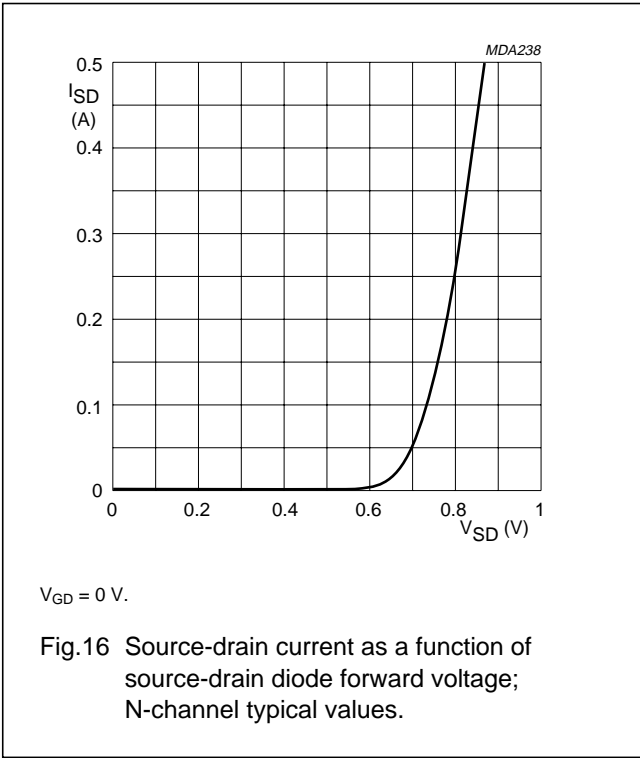
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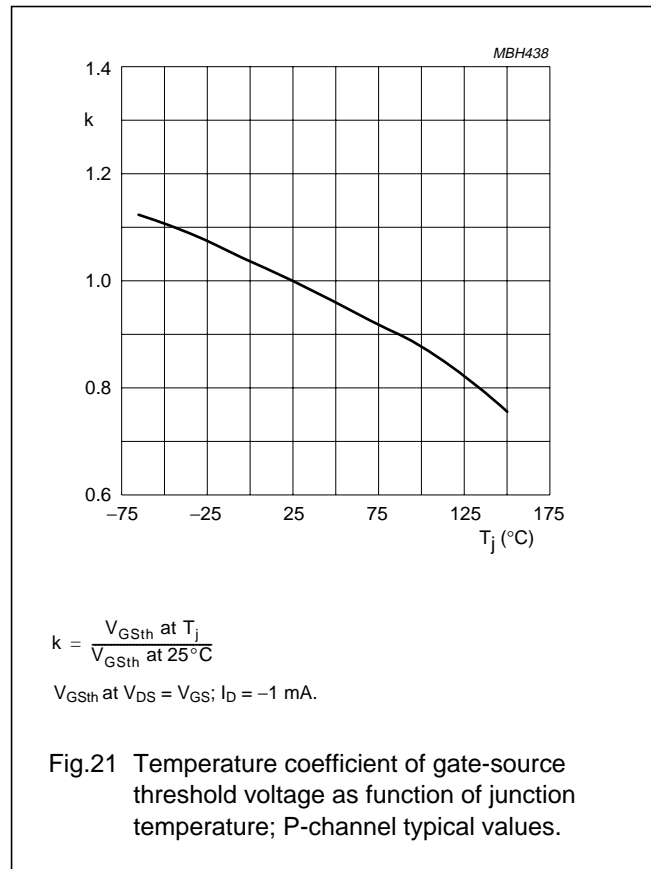
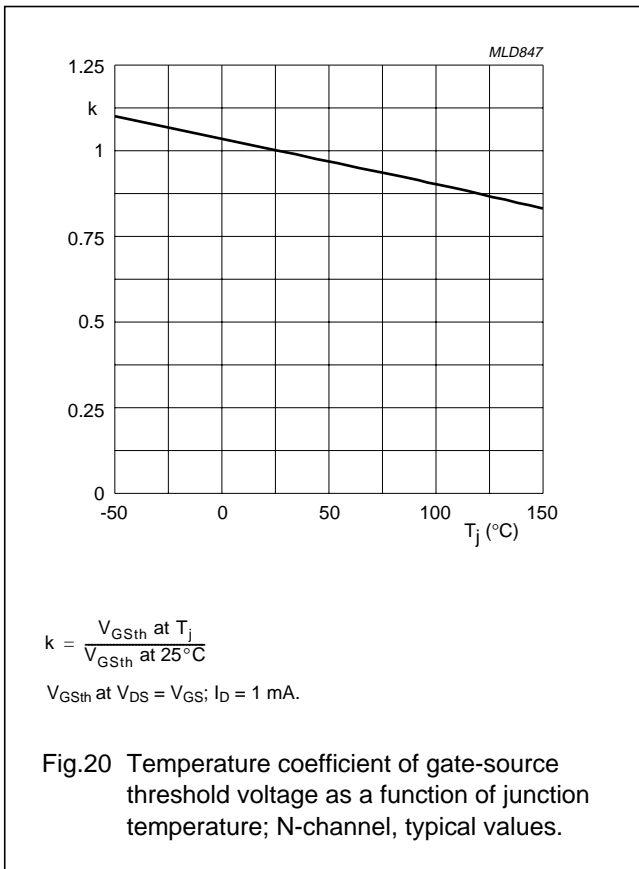
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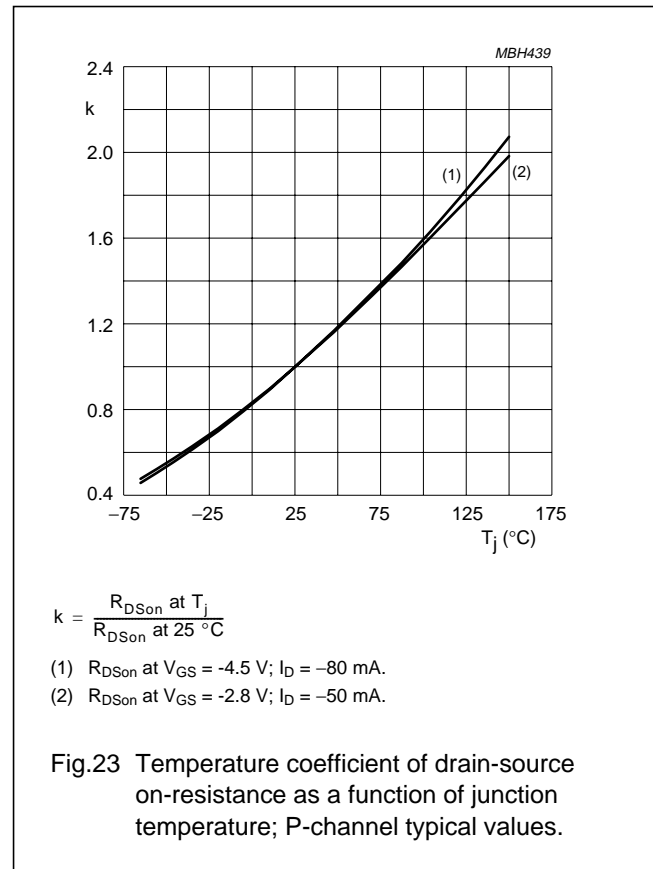
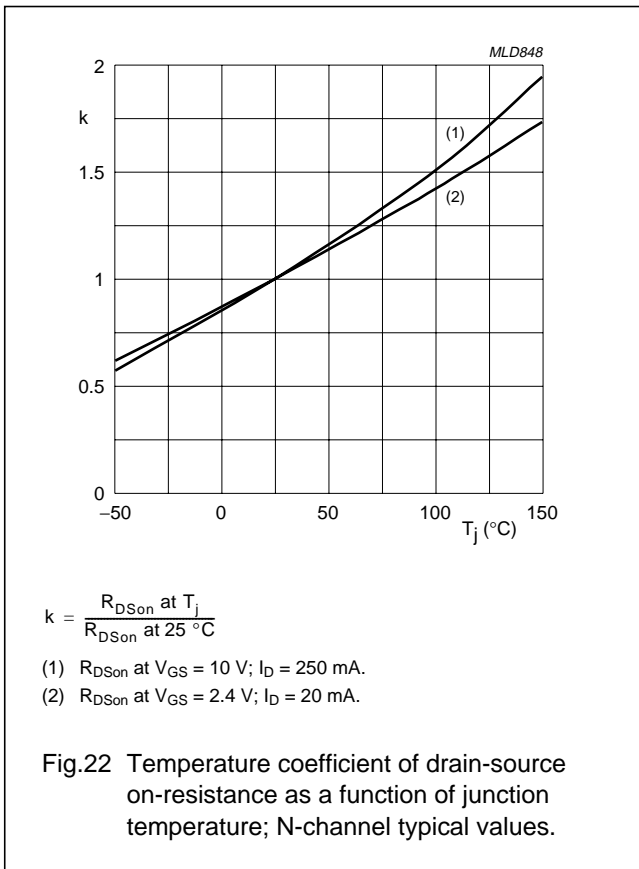
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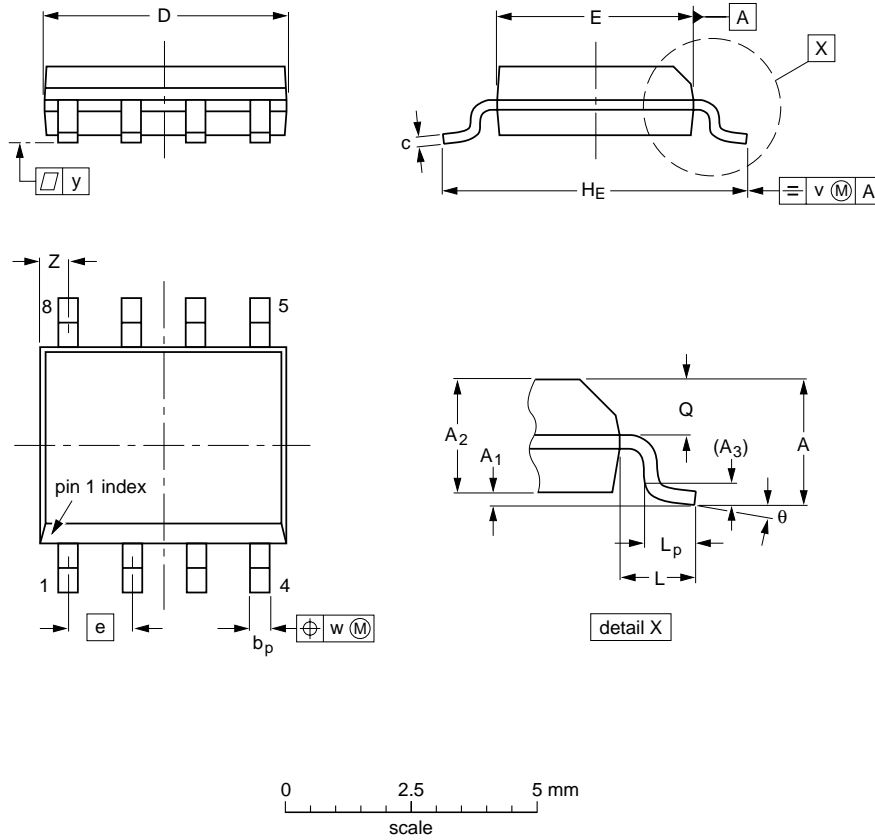
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PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT96-1	076E03	MS-012			97-05-22 99-12-27

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