FAIRCHILD SEMICONDUCTOR™

August 2000

QFET™

FQS4900

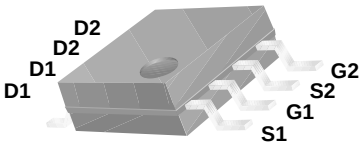
Dual N & P-Channel, Logic Level MOSFET

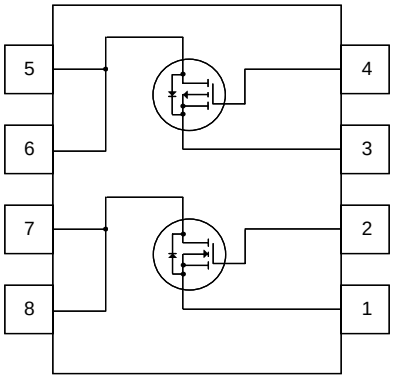
General Description

These dual N and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. This device is well suited for high interface in telephone sets.

Features

- N-Channel 1.3A, 60V, $R_{DS(on)}$ = 0.55 Ω @ V_{GS} = 10 V
  $R_{DS(on)}$ = 0.65 Ω @ V_{GS} = 5 V
  P-Channel -0.3A, -300V, $R_{DS(on)}$ = 15.5 Ω @ V_{GS} = -10 V
  $R_{DS(on)}$ = 16 Ω @ V_{GS} =- 5 V
- Low gate charge (typical N-Channel 1.6 nC)
  (typical P-Channel 3.6 nC)
- Fast switching
- Improved dv/dt capability





Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		60	-300	V
I_D	Drain Current - Continuous (T_A = 25°C)		1.3	-0.3	A
	- Continuous (T_A = 70°C)		0.82	-0.19	A
I_{DM}	Drain Curent - Pulsed	(Note 1)	5.2	-1.2	A
V_{GSS}	Gate-Source Voltage		± 20		V
dv/dt	Peak Diode Recovery dv/dt	(Note 2)	7.0	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)		2.0		W
	(T_A = 70°C)		1.3		W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W