# Chassis Professional 8000
Circuit description

# Power supply

Consists of two completely separate sections:

- **Stand-by power supply**
- **Main power supply**

**Stand-by power supply**

This is an SMPS (**S**witch **M**ode **P**ower **S**upply) operating at about 50 kHz with primary side control and stabilisation performed by the integrated circuit VIPer20A (ICP10), which provides exclusively the voltages required by the appliance in stand-by mode.
In these conditions the main power supply is completely deactivated, which allows for an exceptionally low overall consumption (< 1 W), far lower than even the most stringent standards.
The transformer TRP2 performs the dual function of isolating the appliance from the mains power supply and generating on the secondary winding the supply voltage + 5 Vsb which powers the IR receiver (IRH1), the microcontroller (ICR1), the NVM memory (ICR3), the reset circuit (ICR6) and the EPROM (ICR2) containing the software. A duplicator circuit is used to obtain a voltage of about 20 V used for turning off the electromagnetic mains switch (optional).

**Main power supply**

This is an SMPS (**S**witch **M**ode **P**ower **S**upply) operating at about 45 kHz with secondary side control and stabilisation performed by the integrated circuit TEA2262 (ICP1).
The transformer TRP1 performs the dual function of isolating the appliance from the mains power supply and generating the correct supply voltages on the various secondary windings.
In stand-by the TRIAC DP2 does not conduct, so the circuit (including the PTC powering the degaussing coil) is completely disconnected from the power supply and therefore has no power consumption.
When it is turned on by means of the photo-coupler ICP3, the TRIAC DP2 is made to conduct and the rectified and smoothed mains voltage across CP14, via winding 5/2 of transformer TRP1, is present on the collector of TP1, which does not conduct because ICP1 is not yet powered.
Simultaneously CP16 is charged from mains via RP3. As soon as the voltage across it reaches a value of about 10 V, the integrated circuit begins to operate and generates on pin 14 the driving pulses for making transistor TP1 conduct.
Current therefore begins to flow in the primary winding 5/2 of the transformer and across the winding 1/7 there are formed pulses which are rectified by DP4 and smoothed by CP16 and ensure a complete power supply of ICP1.
At the same time currents are also induced in the secondary windings; after being rectified and smoothed these currents generate the various power supply voltages.
A voltage taken from across CP37 by way of the voltage divider made up of RP35/RP29/RP23/RP33/PP1 is applied to the base of TP4 and causes a proportional current to flow in the photodiode contained in the optocoupler ICP2.

This value is transferred via the photo-coupler emitter to the input (pin 6 of ICP1) of a comparator which regulates the duration of the base drive pulses of transistor TP1.
This controls the time for which current is allowed to flow in the primary winding (and therefore regulates the energy fed into the transformer) and gives extremely precise stabilisation of the voltages available on the transformer's secondary windings.
The circuit made up of CP24/CP25/LP10/DP6 controls the current harmonics towards the mains power supply and may be present or absent depending on applicable regulations.

This solution activates automatic demagnetisation of the CRT every time the appliance is turned on, not just from the switch but also from stand-by. This solves the problem of possible purity degradation if the appliance (as often happens) is not turned off regularly from the mains switch.

**Protection**

To protect against supply voltage variations, the integrated circuit ICP1 interrupts generation of driving pulses to pin 14 if the voltage at pin 16 is higher than about 15.5 V.
Furthermore the current that flows in the transistor TP1 is read across RP9 and is applied to pin 3 via RP5/RP14; if it exceeds the maximum permitted value, the driving pulses to pin 14 are interrupted.
This protects the transistor TP1 and safeguards against short-circuits in the transformer's secondary windings.

## Microcontroller

A latest-generation device with 16-bit architecture (ICR1 - M30612SFP) is used, supported by an EPROM (**E**lectrically **P**rogrammable **R**ead **O**nly **M**emory) that contains all the appliance software.
The various functions are controlled either by changing the logic state (L or H) of some pins on the microcontroller or by way of a two-wire digital bus (pins 27/28) designated IIC-bus (**I**nter **I**ntegrated **C**ircuit Bus).
An additional IIC-bus (pins 91/92) is devoted exclusively to dialoguing with the NVM memory (**N**on **V**olatile **M**emory) (ICR3) to provide maximum protection against data corruption.
Connected to pins 32/33/34 there is also a special high-speed M3-L bus dedicated exclusively to dialoguing with ICR5 (SDA5273-2P) for managing teletext and graphic OSDs (**O**n **S**creen **D**isplays).
The signal from the IR receiver is applied to pin 7 of the microcontroller, which begins its activity when the supply voltage is present and the reset cycle (active L) at pin 12 has been completed.
For this reason if the system shows abnormal behaviour it is important to turn the power switch off and back on again to generate a reset pulse allowing the program to be reinitialised.

When the reset pulse has terminated, the microcontroller waits until the control signals from IR are present at pin 7 or those from the local control are present at pin 97.
Execution of the entire program is timed by the clock signal generated by the 10 MHz crystal and applied to pins 13/15.
A valid command for exiting standby generates a level L at output pin 100, thereby enabling powering up of all the circuits as described in the power supply section.
The microcontroller first verifies that the power supply has come on correctly by checking that pin 18 (START) is at level H, then all the possible peripherals are interrogated via the IIC-Bus to recognise the configuration of the appliance and thereby structure the program.
All data regarding the operating parameters required for correct setting of all the functions (tuning, analogue values, geometries, option bytes, etc.) are subsequently called up from the memory ICR3.
The various functions are carried out and commands given primarily via the digital buses.
The functions of the remaining microcontroller pins are described below:

**Pin 1 -** Output (LPW) which goes to level L during the main power supply start-up to activate initial operation of the horizontal deflection stage.

**Pins 3/4 -** DAC (**D**igital to **A**nalog **C**onverter) outputs for headphone volume and balance control.

**Pin 19 –** Input connected to vertical flyback pulse used for managing communication timing with 100 Hz processor.

**Pin 20 –** Output which goes to level H to activate audio power amplifier muting.

**Pin 21 –** Output for controlling satellite antenna system switching.

**Pins 24/25 –** Inputs for automatically recognising the configuration of the 100 Hz conversion system.

**Pin 26 –** Input for automatically recognising correspondence of deflection hardware used.

**Pin 30 –** Input for automatically recognising the presence of the Comb filter.

**Pins 35/36/37 –** Outputs reserved for future use.

**Pin 38** – Output for controlling loudspeaker configuration in Dolby Pro Logic mode.

**Pin 89** – Input used for controlling VGA input enabling.

**Pin 93 –** Output for controlling illumination of local control LED.

**Pin 94 –** Output for controlling activation of electromagnetic switch (if present).

**Pin 95 –** Input connected internally to an ADC (**A**nalog to **D**igital **C**onverter) to measure the value of the tuner's AGC voltage.

**Pin 97 –** Input connected internally to an ADC (**A**nalog to **D**igital **C**onverter) to measure the value of the voltage generated by the local control keys and hence discriminating the control.

Note that the software also identifies the configuration of the appliance by way of an option code contained in the memory ICR3. This option code must therefore be checked and if necessary adjusted if ICR3 is replaced. The correct value for each model is marked on the label on the back of each item after the words “option code”. It can be set by entering service mode (follow the necessary safety procedures).
In this mode it is also possible to make all the adjustments for the various calibrations under the control of a specific program contained in the microcontroller, which also verifies automatically whether NVM data initialisation operations are required.

## **NVM memory** (ICR3)

This is an EEPROM (**E**lectrically **E**rasable **P**rogrammable **R**ead **O**nly **M**emory) NVM (**N**on **V**olatile **M**emory) with a 16K bit capacity and an IIC-bus interface.
The microcontroller writes and reads all the variable data relevant to operation in the memory.
In addition to user option data (tuning, analogue levels, etc.), memory ICR3 also contains data regarding the settings of many of the appliance’s functions, such as geometries, option bytes, white level adjustment, etc.
**If the memory is replaced, these settings must be restored through the appropriate service procedures**.
However, the program contains special check routines so the appliance can be turned on when the memory is not programmed or even not present, thereby simplifying the service procedures.

## Video signal processing / deflection

The various items of information in the video signal are processed by the integrated circuits TDA9321H (ICC2), TDA9332H (ICC1) and SAA4977H (ICY1).

- **TDA9321H**

## Video

The IF signal from the tuner whose band is limited by the surface wave filter FCC5 is routed to pins 2/3, which are connected to the input of the video demodulator (synchronous PLL type with active carrier regeneration). This assures ultralinear demodulation, an excellent demodulation figure, a low harmonic content and an excellent impulsive response.
The only residual adjustment that must be carried out on the video demodulation circuits is tuning of coil LC9 of the VCO oscillator and setting the working point of the tuner AGC, which is controlled by way of pin 62. Both the adjustments are performed fully automatically by the software in service mode.
The baseband video signal is available with an amplitude of 2 Vpp at pin 10 and is applied via the audio carrier suppression filter FCC3 to pin 12, which represents the input of the group delay correction circuit controlled by software.
After this treatment the signal is available at pin 13 with an amplitude of 2 Vpp.
From here it is sent both to the SCART 1 output and to one of the video selector inputs (pin 14) after being taken to the level of 1 Vpp.
Further video inputs are available at pins 16 (AV1), 18 (SAT), 20 (AV2) and 23 (FRONT). S-VHS sources whose chrominance signals are connected to pins 21 and 24 can also be connected to the AV2 and FRONT inputs respectively.
The video signal of the selected source is taken from pin 26 to power the teletext decoder.
In order to send the selected signal to the screen, it is routed internally through a band-pass filter to remove the chrominance signal and a trap to eliminate the colour subcarrier from the luminance signal.
In the case of SVHS sources these circuits are bypassed.
Switched capacitance circuits are also included for creating luminance delay lines.
The chrominance signal is demodulated in accordance with the PAL/SECAM/NTSC standard identified automatically and with the aid of integrated delay lines. The carrier reconstruction oscillators are connected to their respective crystals via pins 54 and 57.
**Original spare parts must be used for these components as all the functions of the integrated circuit take their frequencies as reference**.
After the treatments described above, the luminance signal Y50 and the colour difference signals U50, V50 are available on pins 49, 50 and 51 respectively.
There are also two video outputs which can be freely connected to any of the inputs and are used for the SCART2 output (pin 34) and for the PIP module (pin 32).
Pins 25, 26, 27, 28, 29 and 30 are used for connection to an optional comb-filter. The SCART1 RGB input is connected to pins 40, 41, 42 and 43 and the PIP source Y/U/V signals to pin 36, 37, 38, 39.
Pins 19 and 22 are outputs which can be placed in an H or L level under the control of the software and are used respectively for L/L' switching of the audio filter FCC4 and for switching of the video signal output on SCART1 by means of the transistors TW3, TW4, TW5, TW6, TW7 and TW8.

## Audio

The IF signal from the tuner whose band is limited by the surface wave filter FCC4 is routed to pins 63/64, which are connected to the mixer consisting of a multiplier which

converts the IF signal to the intercarrier frequency. This frequency is available at pin 5 after a high-pass filter which eliminates the video content.
The is also an AM audio demodulator whose output is also connected to pin 5.

**Deflection**

The horizontal and vertical synchronising signals are extracted from the screen video signal.
The horizontal synchronising pulse HA is available at pin 60, the vertical synchronising pulse VA at pin 61 and the sandcastle pulse at pin 59.

- **SAA4977H (1fH / 2fH converter)**

The signals Y50, U50, V50 coming from ICC2 are connected to input pins 26, 28 and 30, while the horizontal HA and vertical VA synchronising signals are connected to pins 22 and 20 respectively.
To double the field frequency (100 Hz) it is necessary to write the same original field twice on the screen.
For this purpose, the incoming video signals are first digitalised by sampling them at 8 bits and then transferred to a memory (ICY4), from which they are read at double speed. Digital to analog reconversion is then performed and the double-frequency analog signals are available at pins 79, 76 and 74. The circuits formed by TY1/TY2, TY3/TY4 and TY5/TY6 adapt the levels for the ICC1 inputs.
It is also necessary to generate the HD/VD synchronising pulses at double frequency and synchronous to those of the original HA/VA signal.
This is done with the help of the PLL circuit made up of ICY2 and ICY3.
All checks and signals needed for the various functions and for memory management are inside ICY1, which also contains a microcontroller and resident software to carry out the various activities. The transistors TY8/TY9 form the reset circuit for this microcontroller.
The integrated circuit ICY9 switches the synchronising signals between the internal source (pins 2 and 5) and the VGA input (pins 3 and 6). Switching is controlled by pin 3 of ICY1.
The integrated circuit ICY5 (if present) increases the definition by acting on the signal's transient fronts.

- **TDA9332H**

**Video**

Signals Y100, U100 and V100 from the 100Hz conversion module are connected to pins 26, 27 and 28.
The RGB signals for performing saturation, contrast and brightness controls are restored by way of the matrix circuits. The signals for driving the video final amplifiers are therefore available on output pins 40, 41 and 42.
Pin 44 is the input for the measurement pulses for adjusting the cut-off, which uses an automatic system for alignment at both low and high current, thereby optimising the

performance of the tube. Adjustment of voltage Vg2 is fully automated in service mode by a special software procedure.
Pin 43 is the control input for automatic limitation of the tube current.
Pins 35, 36, 37 and 38 are the inputs of the RGB signals for the OSD and teletext, while pins 30, 31, 32 and 33 are the RGB inputs of the VGA source. These inputs require sources with a horizontal frequency of 32 kHz.

**Deflection**

The entire management of the deflection controls refers to the 12 MHz oscillator FCC1 connected to pins 20/21.
When turned on, the transistor TC3 is made to conduct by pin 1 of microcontroller ICR1, thereby powering pin 22. This activates the output of horizontal driving pulses from pin 8 at a frequency of about 50 kHz. This starts the horizontal deflection stage, whose consumption permits stabilisation of the power supply.
When the power supply voltage on pins 17/39 reaches 8V, the horizontal driving output progressively switches to its rated frequency (32 kHz) and the steady-state operating mode is reached. The software now disconnects the power supply voltage from pin 22.
The transistor TC4 is normally inhibited because its base, via RC34, is connected to earth by the jumper JF1 situated on the power supply/deflection circuit and this level L is also carried to pin 26 of the microcontroller. This also allows the correct operating frequency of ICC1 (H = 32 kHz; L = 15 kHz) to be provided via pin 12, which also depends on the deflection hardware used.
The horizontal HD and vertical VD synchronising pulses are applied to input pin 24 and 23 respectively.
Pin 13 is the input of the horizontal flyback pulse and pin 4 is the input for dimensional stabilisation of the image as the tube current varies.
Pin 9 is used as input to protect the tube, blancking it out in the event of a fault in the vertical deflection circuits.
Pins 1 and 2 are the symmetrical outputs for vertical driving and pin 3 is the output for E/W correction control.
All the adjustments are performed in service mode by a special support software program.

## Video final amplifiers

The RGB signals available at pins 40/41/42 on ICC1 (TDA9332H) must be amplified and inverted in order to reach the level required for driving the CRT.
The integrated circuit TDA6108 (ICV1) is used for this purpose.
The final amplifier inputs are connected to pins 1/2/3 and the outputs (pins 7/8/19) are connected directly to the CRT's cathodes via the protection resistors RV5/RV7/RV10.
A copy of the currents flowing in the CRT's cathodes are available at pin 5 and this information is sent to the video processor TDA9332H for automatic cut-off control circuit operation.

Transistors TV1 and TV4 form a circuit which serves to eliminate CRT spot formation when the appliance is turned off.
During operation the heater's supply pulses, which are rectified and filtered by DV6 and CV6, keep TV1 saturated and hence inhibit TV4.
The capacitor CV19 is therefore able to charge up at the voltage of +200V by way of RV19 and DV10. Grids 1 (G1) of the tube remain at ground potential since DV10 is conducting.
As soon as the appliance is turned off, the final line stage stops providing the heater's power supply pulses; TV1 is inhibited and TV4 is saturated by the +200V voltage still present and applied at its base via RV18.
The collector of TV4 grounds the positive armature of CV19. As a result, grids 1 of the CRT are polarised with the negative 200V voltage present on its negative armature since the diode DV10 is now polarised the other way round.
This way the CRT is completely inhibited for the time it takes CV19 to discharge, thus preventing spot formation.

The RGB signals, decoupled by means of the transistors TV7/TV8/TV9, are added together and transferred to the power stage made up of TV5 and TV6 by means of the circuit made up of TV2 and TV3. The coupling capacitor CV13 together with the power stage input impedance forms a differentiator circuit which generates pulses of suitable polarity upon each signal transition. This drives a special deflection coil on the CRT which modulates the deflection velocity (**B**eam **V**elocity **M**odulation), thereby significantly improving image definition.

## Horizontal deflection

The output line transistor is driven by the transformer TRL1 whose primary winding is driven by the transistor TL1, connected to the horizontal drive output of ICC1 via the emitter-follower TC5.
The horizontal deflection stage is carried out in a conventional manner with the deflection transistor TL2, the diode (DL4/DL5) EW modulation circuit and pin-cushion distortion correction (CL8/LL6). The correction signal EW is injected into the central point of the diodes via LG2.
The capacitive divider formed by CL11/CL12 is used for picking up the horizontal flyback pulse to be applied to pin 13 of ICC1, limiting its maximum value to 8V by means of the diode DL11.

## Vertical deflection – EW correction

These functions are performed by the integrated circuit TDA8351 (ICF1). This is a power amplifier with a bridge output that allows the vertical deflection coils to be connected directly to pins 4 and 7. The resistances RF9/RF10, which provide pin 9 with the necessary feedback signal, are placed in series.
The differential input circuit (pins 1/2) is driven by the voltage formed across RF3/RF4 for the symmetrical driving currents provided by ICC1.
Pin 8 is an output which switches to the value H at vertical flyback. This signal is connected to pin 9 of ICC1 and is used to protect the CRT in the event of failure of the vertical deflection circuits.
Two separate supply voltages are used for the deflection part (pin 3) and for generating the flyback pulse (pin 6), thereby achieving a high value of efficiency.
The power stage for EW correction consists of transistor TG1 which is driven directly by ICC1 and whose collector is connected to the injection coil LG2 by means of RG4.

# Audio signal processing

The various audio functions are treated by the circuits TDA9870/5A (ICS1), SAA7710T (ICS4), TDA7467D (ICS5), TDA2616 (ICS2/ICS6), TDA7053AT (ICS3).

- **TDA 9870A / TDA 9875A**

The integrated circuits have the same basic functions: the version TDA9875A additionally contains a complete NICAM digital audio decoder.
The audio IF signal from pin 5 of ICC2 is applied to input pin 12. The AM audio signal (in the case of L/L' standard) is also extracted by way of the transistor TS1 and the low-pass filter formed by RS34 and CS13 and is taken to input pin 29. A second IF input (pin 10) is used for the audio signal of the satellite receiver (if present).
All audio functions (demodulation, stereo/NICAM decoding, input/output switching, volume/tone control, effects) for BG/DK/I/LL' standards are contained in the integrated circuit and are totally selected and controlled via software.
The audio inputs from the SCART 1 and SCART 2 sockets are connected to pins 33/34 and 36/37 respectively, while the audio input from the front RCA sockets (optional) is connected to pins 31/32.

Pins 47/48 and 51/52 are the outputs towards the SCART 1 and SCART 2 sockets respectively.
Pins 62/63 are the constant level outputs for the LINE OUT sockets, fed by the transistors TW11 and TW13; pins 60/61 are the outputs for the loudspeaker power amplifiers (ICS2).
Pins 22/23/25/26/27 are the inputs/outputs of the I2S digital bus used for communications with ICS4 (present only in Dolby Pro Logic appliances).

- **SAA 7710T**

This is present only in appliances equipped with Dolby Pro Logic decoding and also provides the function of a 5-band audio equaliser.
Signal treatment is fully digital and data transfer to and from ICS1 is performed via the bus I2S which is connected to pins 22/23/24/28/29.
A specific software program is responsible for complete management of all functions, including a special spatial sound (Incredible Sound) which offers effects similar to Pro Logic decoding without the need to install rear loudspeakers.

- **TDA 7467D**

ICS5 can be used as an alternative to the Dolby Pro Logic decoder ICS4. This creates special spatial sound effects while using solely the loudspeakers contained in the appliance.
The input signal to be processed is connected to the pins 2/3 and the outputs are connected to pins 1/28. It is fully managed by software.

- **TDA 2616**

This is a double Hi-Fi audio power amplifier in accordance with DIN45500.
ICS2 is always present, whereas ICS6 is used solely in Dolby Pro Logic appliances to amplify the central and rear channels.
The input signals are connected to pins 1/9 and the outputs to pins 4/6.
Pin 2 mutes the amplifiers and is controlled via the transistor TW9.
The transistors TW12 and TW14 activate MUTE during power supply transients.
The right and left channel signals are also added together and sent, via the transistor TW10, to the woofer box amplifier (present in some models only).

- **TDA 7053AT**

This is a double amplifier used to power the headphone socket.
The inputs are connected to pins 4/6 and the outputs to pins 9/16. The reproduced signal is the same as that of the loudspeakers and its volume and balance can be controlled by way of pins 2/8 connected to the output pins 3/4 of microcontroller ICR1.

## Woofer amplifier

This is present in some models only and is used to power the woofer loudspeaker box.
The integrated circuit LM358N (ICB1A/B) constitutes a two-stage low-pass filter in cascade and serves to eliminate all frequencies higher than about 300 Hz from the audio signal spectrum.
Power amplification is performed by the integrated circuit TDA2616 (ICB2) connected in a bridge configuration, which directly powers the box loudspeaker.
The circuit made up of the transistor TB2 and the relay RLB1 is used solely in Dolby Pro Logic appliances to adapt the internal loudspeaker connections according to the installation configuration chosen by the user from the OSD menu.
Switching is managed by pin 38 of the microcontroller, which directly drives the base of TB2.

## VGA interface

This option (present only on some models) allows the appliance to be used as a computer monitor at the following VGA resolutions only:

| pixel | horizontal | vertical |
|---|---|---|
| 640x480 | 31.5 kHz | 60 Hz |
| 640x350 | 31.5 kHz | 70 Hz |
| 640x400 | 31.5 kHz | 70 Hz |

The PC's graphic interface must be set for these resolutions.
The RGB video signals are sent directly to the input pins 30/31/32 of ICC1 while the synchronising signals from pins 13 and 14 of CNM1 are applied to the integrated circuit ICM1 (Quad.2-input exclusive-OR) which provides positive pulses to output pins 3/6 whatever the input polarity. This way the appliance is automatically adapted to any type of PC.
The presence of horizontal and vertical synchronising pulses is checked by means of ICM2, whose output pins 6 and 10 are at level H only if the horizontal and vertical synchronising pulses respectively are present.
Only in this case can pin 2 of CNM3 (VGA ENABLE) go to level H.
The integrated circuit ICM3 is used to check that the frequency of the horizontal synchronising pulses is lower than the maximum value set by PM1 to prevent an incorrect PC resolution setting damaging the television's horizontal deflection stages.
**Potentiometer PM1 is factory-set. It requires special equipment for adjustment and its setting must not be altered.**

If the value of the horizontal frequency is not correct, pin 10 of ICM3 is kept at level L and consequently the communication line with the microcontroller (VGA ENABLE) goes to about 2.5 V. This information is used to generate a specific error message.
The integrated circuit ICM4 switches between VGA and front RCA audio sources and the transistors TM1/TM2/TM3/TM4 adapt the VGA audio level to that inside the TV set.