

# DATA SHEET

## **BSN304; BSN304A** N-channel enhancement mode vertical D-MOS transistors

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistors

## BSN304; BSN304A

### FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

### DESCRIPTION

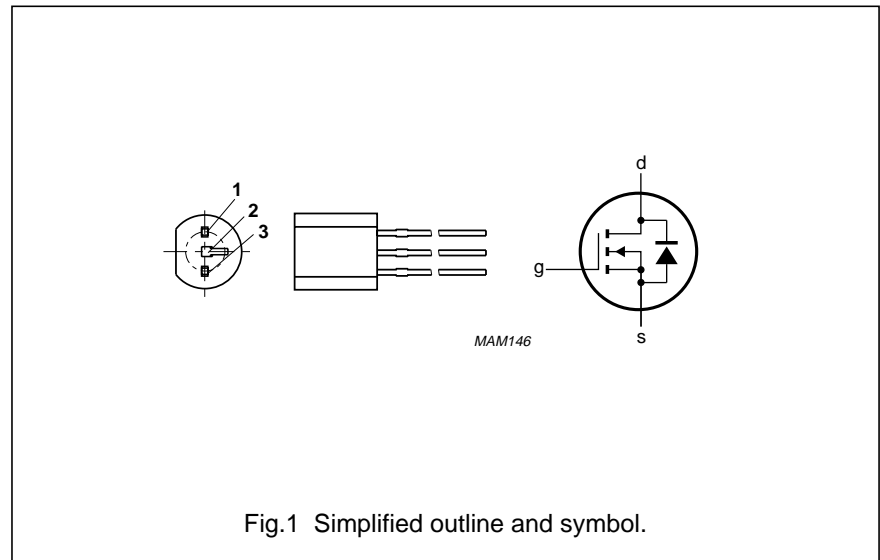
N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

### PINNING - TO-92 variant

PIN	DESCRIPTION
<b>BSN304</b>	
1	gate
2	drain
3	source
<b>BSN304A</b>	
1	source
2	gate
3	drain

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	
$V_{DS}$	drain-source voltage		–	300	V
$I_D$	DC drain current		–	250	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ }^\circ\text{C}$	–	1	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 250\text{ mA};$ $V_{GS} = 10\text{ V}$	–	8	$\Omega$
$V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1\text{ mA};$ $V_{GS} = V_{DS}$	0.8	2	V



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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$I_D$	DC drain current		–	250	mA
$I_{DM}$	peak drain current		–	1	A
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ °C}$ ; note 1	–	1	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	operating junction temperature		–	150	°C

## THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient; note 1	125 K/W

### Note

- Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

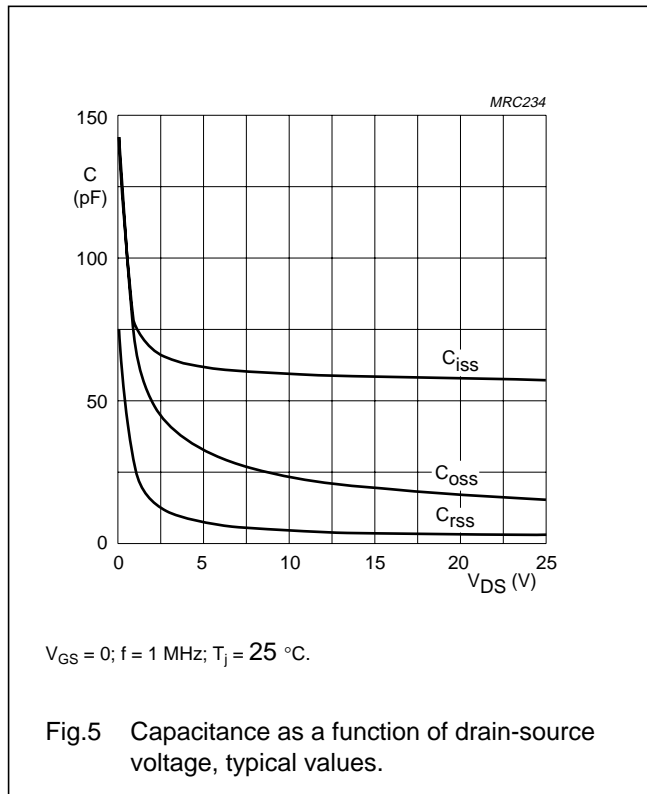
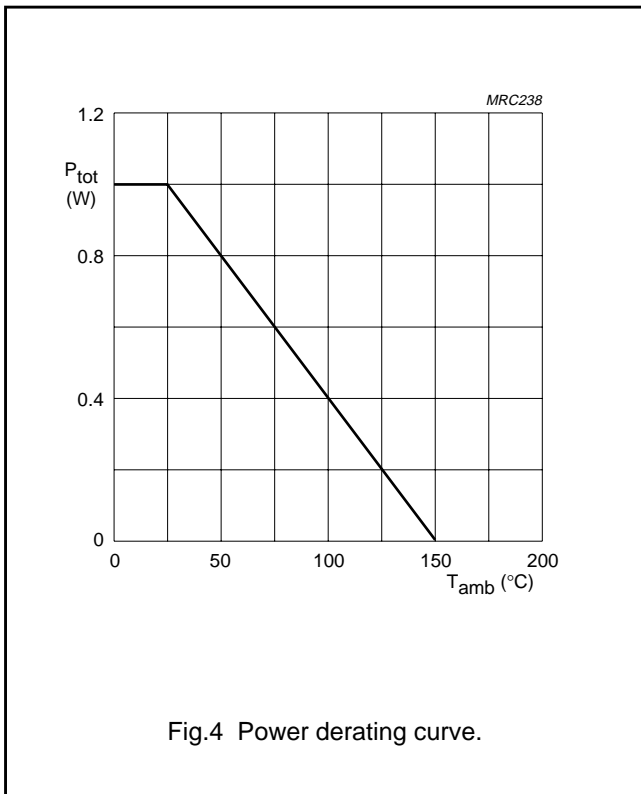
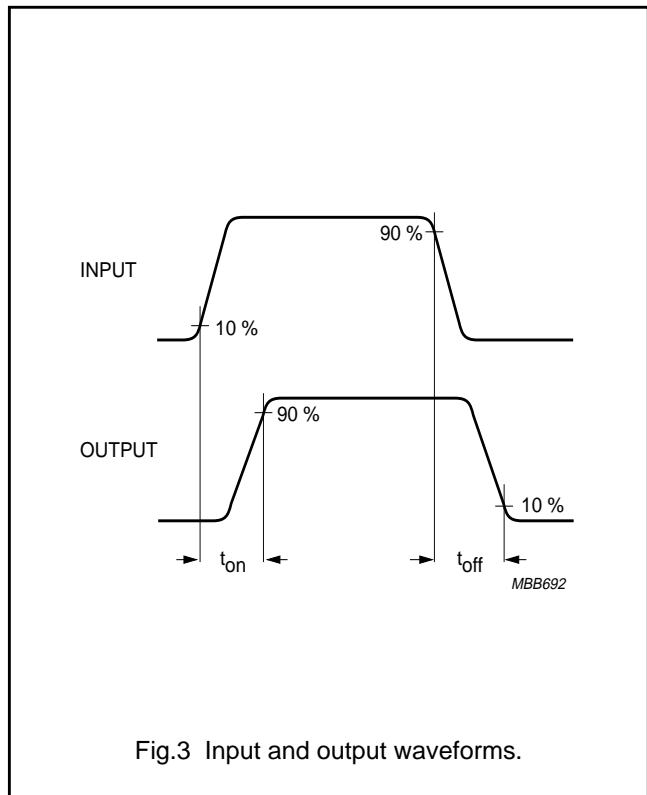
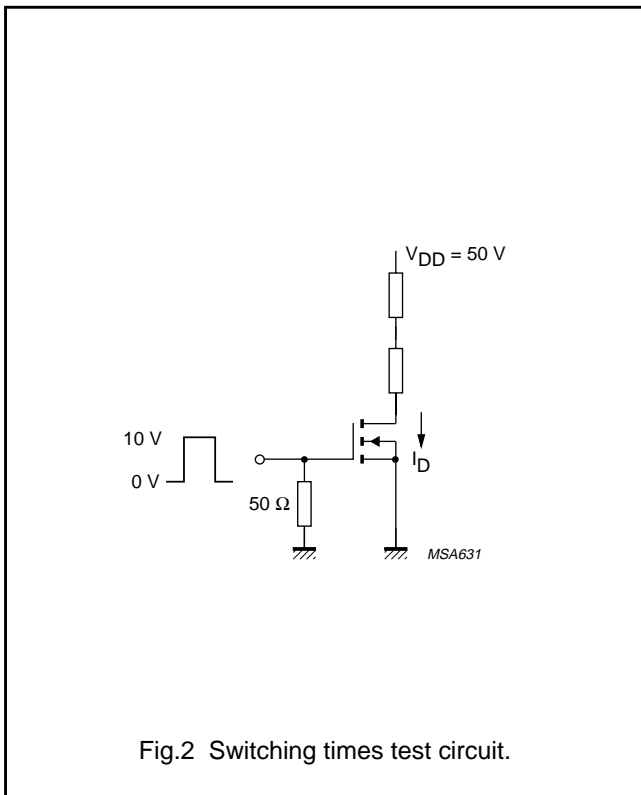
## STATIC CHARACTERISTICS

 $T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}$ ; $V_{GS} = 0$	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}$ ; $V_{DS} = 0$	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 250\text{ mA}$ ; $V_{GS} = 10\text{ V}$	–	6.7	8	$\Omega$
		$I_D = 20\text{ mA}$ ; $V_{GS} = 2.4\text{ V}$	–	7.9	14	$\Omega$
$I_{DSS}$	drain-source leakage current	$V_{DS} = 240\text{ V}$ ; $V_{GS} = 0$	–	–	100	nA
$ Y_{fs} $	transfer admittance	$I_D = 250\text{ mA}$ ; $V_{DS} = 25\text{ V}$	200	380	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\text{ V}$ ; $V_{GS} = 0$ ; $f = 1\text{ MHz}$	–	57	90	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\text{ V}$ ; $V_{GS} = 0$ ; $f = 1\text{ MHz}$	–	15	30	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 25\text{ V}$ ; $V_{GS} = 0$ ; $f = 1\text{ MHz}$	–	2.6	15	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$I_D = 250\text{ mA}$ ; $V_{DD} = 50\text{ V}$ ; $V_{GS} = 0\text{ to }10\text{ V}$	–	2.5	10	ns
$t_{off}$	turn-off time	$I_D = 250\text{ mA}$ ; $V_{DD} = 50\text{ V}$ ; $V_{GS} = 10\text{ to }0\text{ V}$	–	17	30	ns

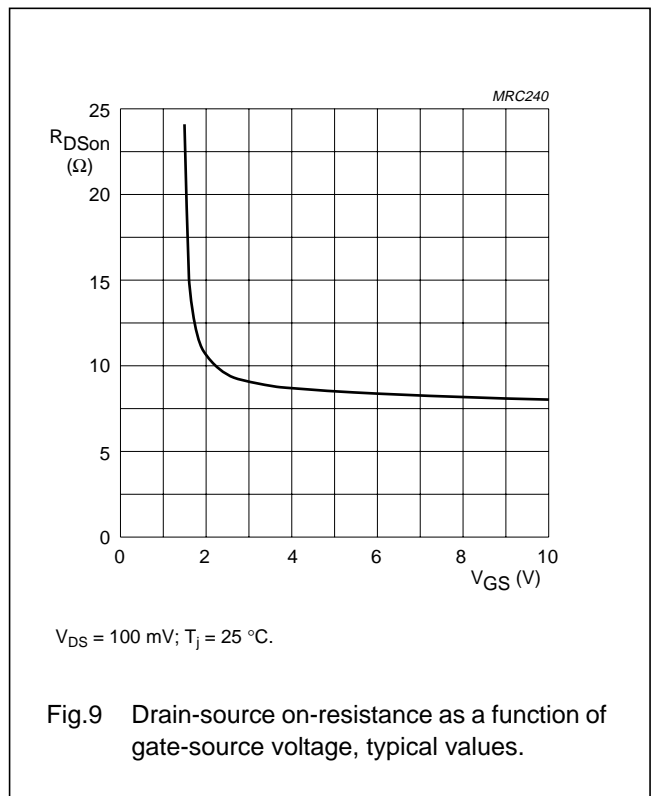
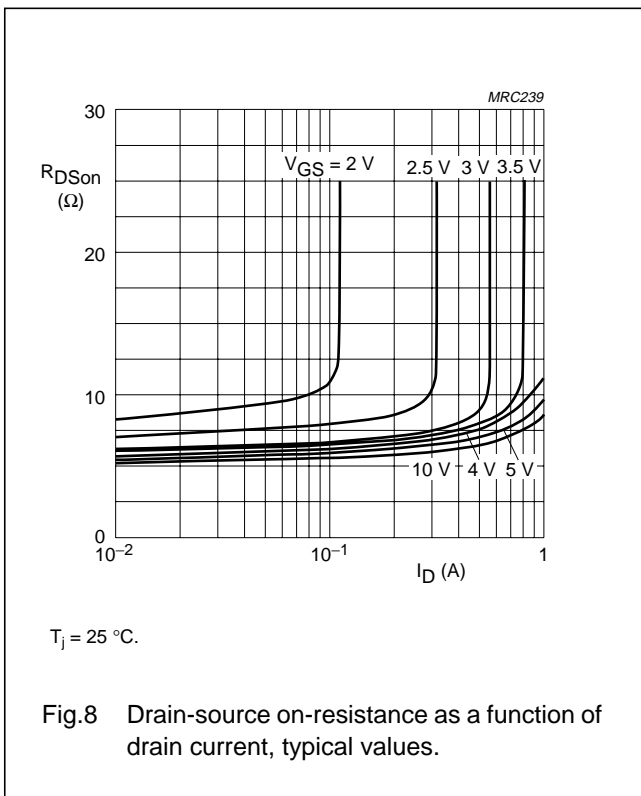
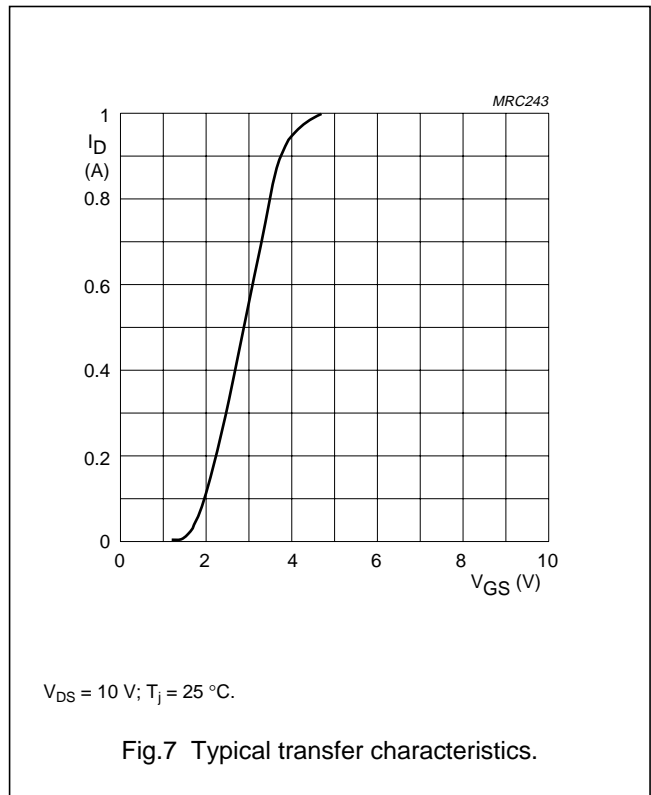
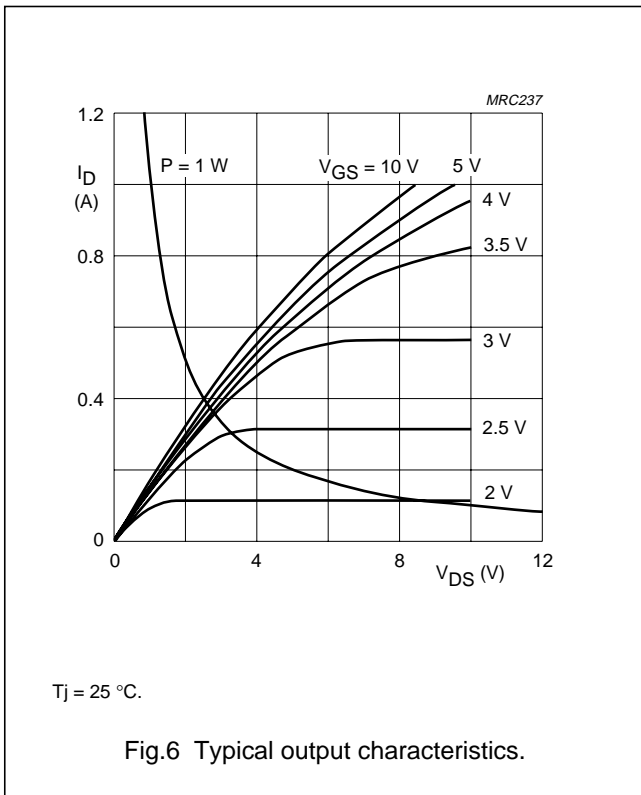
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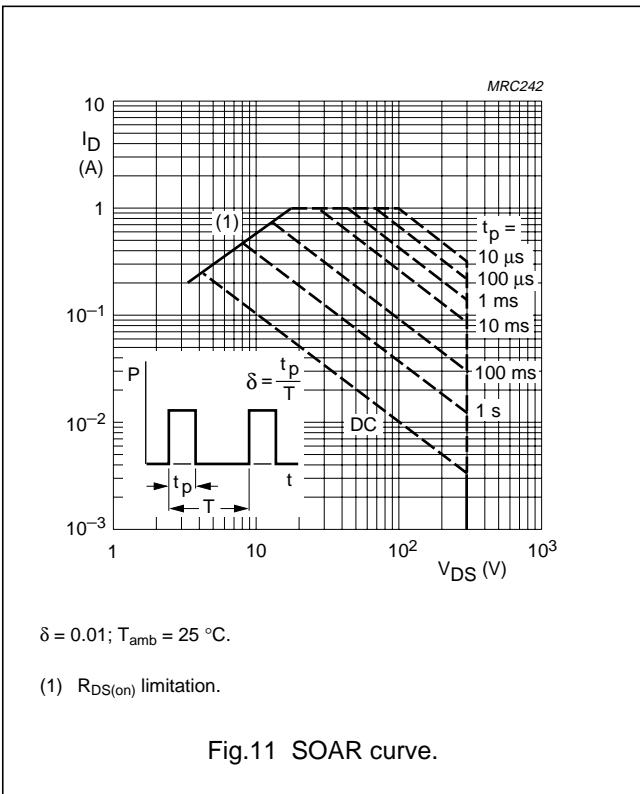
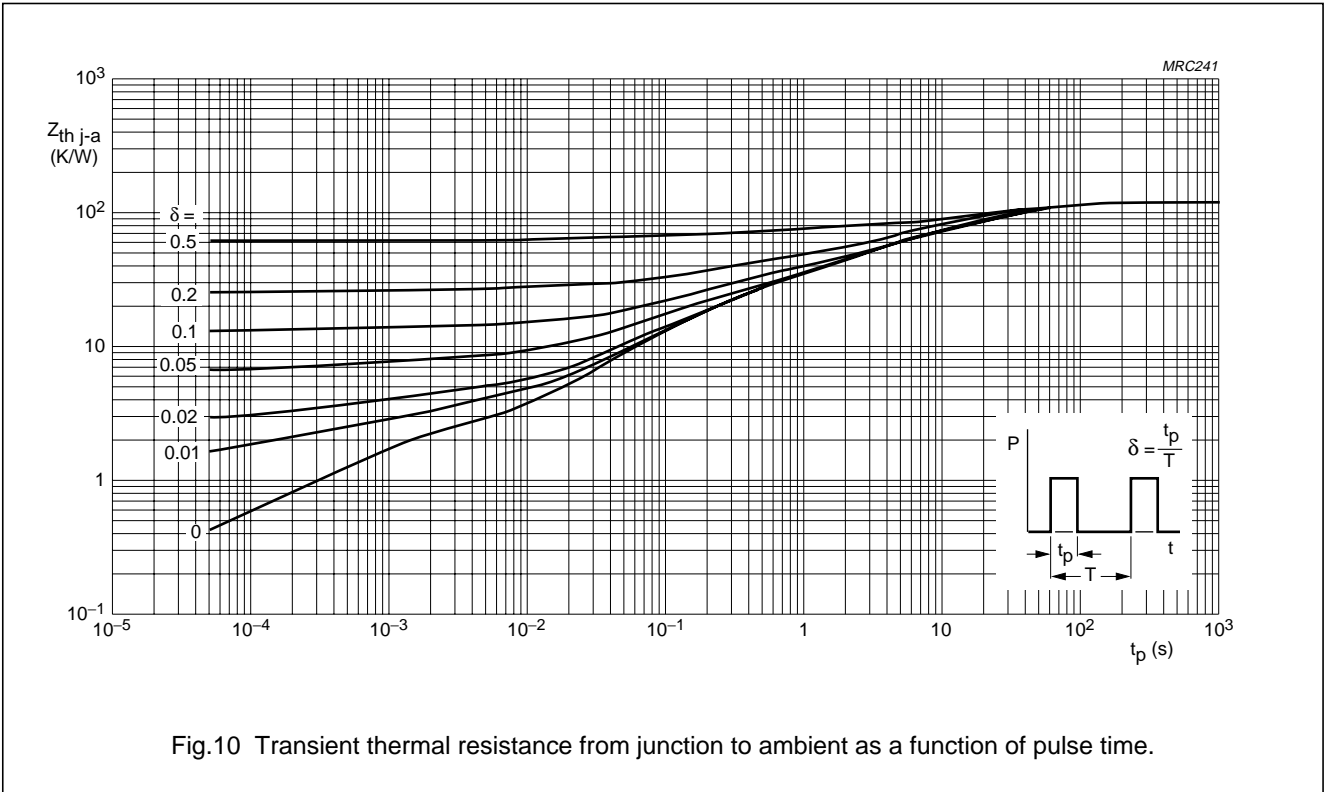
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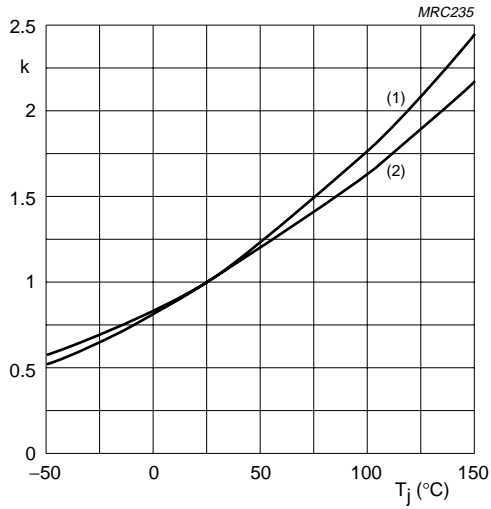
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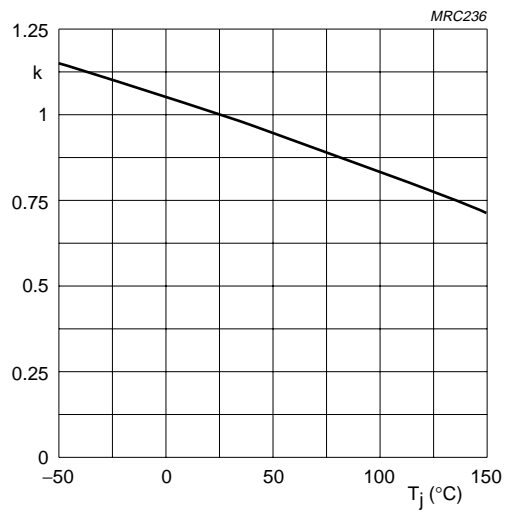


$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25^\circ\text{C}}$$

Typical R<sub>DS(on)</sub>:

- (1) I<sub>D</sub> = 250 mA; V<sub>GS</sub> = 10 V.
- (2) I<sub>D</sub> = 20 mA; V<sub>GS</sub> = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25^\circ\text{C}}$$

Fig.13 Temperature coefficient of gate-source threshold voltage.

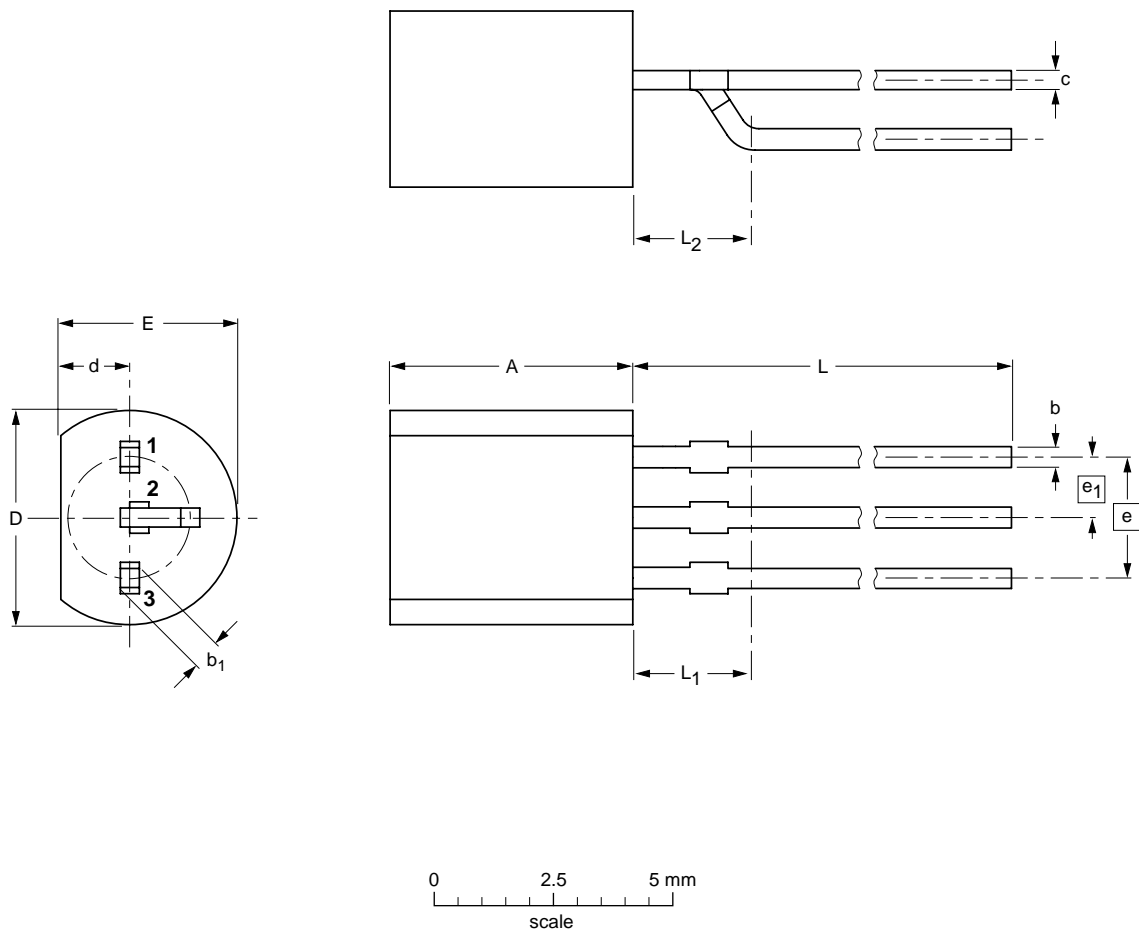
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## PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max	L <sub>2</sub> max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

**Notes**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14



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D-MOS transistors**

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**BSN304; BSN304A****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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**NOTES**

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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

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Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
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Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
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**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
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Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
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**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

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**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

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Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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