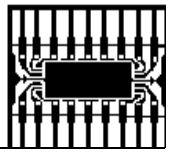
SIEMENS

HL Application Note



Consumer Electronics

Hardware

TVText Design Guide

Short hints for SDA 525x, SDA 525x-2 and SDA 545x

Prepared by
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Revision History

Appl. Version no.	HISTORY	DATE
1.0	TVText Design Guide - Short hints for SDA 525x, SDA 525x-2 and SDA 545x	04th of Mar. 1998
1.1	Revision of all chapters and appending the application note “TVTEXT SDA 525x-2 & SDA 545x - Port pin structure & RGB outputs”	13th of May 1998
1.2	Revision of all chapters	19th of May 1998
1.3	Preliminary values for B-version in chapter 3. Appending chapter 8 and added chapter 9. Added application circuit diagram in new chapter 10.	7th of July 1998
1.4	Inserted chapters „Software Changes“, „Current consumption“ and „EMC-Guidelines“. Canceled 3.2.	26th of August 1998

Table of contents

1 Overview

To get a fast overview about the most important hardware items, like slicer performance, LC-oscillator, crystal network and filter networks we give you short answers within that application note. This application note distinguishes between SDA 525x, SDA 525x-2 and SDA 545x (TVText plus). Differences between the new design steps of the SDA 525x-2 are implemented as well. All chapters contains information related to these chips:

- SDA 525x
- SDA 525x-2 (Design step A..)
- SDA 545x (Design step A..)
- SDA 525x-2 (Design step B)
- SDA 545x (Design step B)

2 LC-oscillator

2.1 SDA 525x

Additional information to the LC-oscillator that were extracted out of our measurements

- Using of high capacitances at LC_{IN}-pin causes small amplitudes at the LC-oscillator, therefore use the higher capacitor at LC_{OUT} !
- The LC-oscillator frequency affects your start point and end point of your OSD.
  Therefore we recommend:
  1. Use an inductor with 2% tolerance value
  2. Use capacitors between 33pF...56pF (1%)
- The LC-oscillator generates the pixel frequency. You may also use capacitors with more than 1% tolerance, but the tolerance of the OSD positioning window will increase.
- Pixel frequency is limited by the Display generator at 25.0 Mhz
- There exists a software routine (ADJUST_HORIZONTAL) to center the OSD window after power on of the TV set. That routine measures the actual size of an OSD window. The program calculates the start of a centered OSD window and corrects the horizontal position of the OSD window by using that information.

2.2 SDA 525x-2 & SDA 545x

- SDA 525x-2: The LC-oscillator is replaced by an internal digital pixel generator. No external components are needed. These pins are D.C. (don´t connect, means: must be left open)
- SDA 525x-2 & SDA 545x: You can select the pixel frequency in the new OSCON register.
- SDA 545x: New port pins are available: LCin-pin is redefined to P4.2 (SDIP52-pin 38; MQFP80-pin 52; PLCC84-pin 44), LCout-pin to P4.3 (SDIP52-pin 39; MQFP80-pin 53; PLCC84-pin 45) !

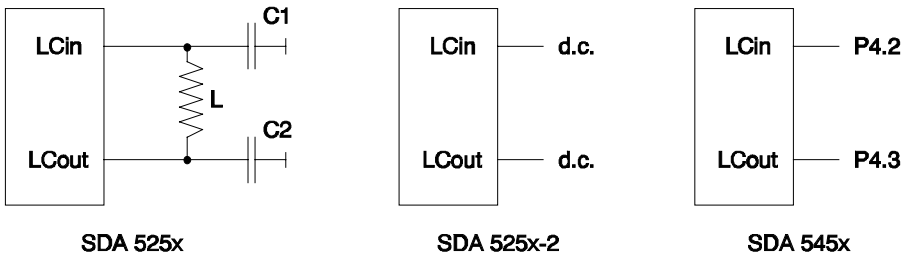


Figure 1: Differences related to SDA 525x at the LC-pin connections

- SDA 525x-2 & SDA 545x (MQFP-80-1 only): Pin 52 is \RD and Pin 53 is \WR. These are alternative functions to P4.2/P.4.3 and may be enabled by software.

3 Slicer (Filter network, IREF and clamping circuitry)

3.1 SDA 525x

- Filter 1 (SDIP52-pin 26; MQFP80-pin 70; PLCC84-pin 65)
  R=6k8 C=33nF
- Filter 2 (SDIP52-pin 27; MQFP80-pin 71; PLCC84-pin 64)
  R=6k8 C=33nF
- Filter 3 (SDIP52-pin 25; MQFP80-pin 69; PLCC84-pin 63)
  R=8k2 C=220nF
- Reference current resistor (SDIP52-pin 29; MQFP80-pin 73; PLCC84-pin 67)
  R=82k ,don´t change the value !
- CVBS resistor at CVBS input pin (SDIP52-pin 30; MQFP80-pin 74; PLCC84-pin 68)
  R= 470k (Range is 390k..560k)
- CVBS capacity at CVBS input pin (SDIP52-pin 30; MQFP80-pin 74; PLCC84-pin 68)
  C=330 nF (Range is 330n..1µ)
- optional: Additional filter network for frequency response (high pass, e.g. 2k2 and 150pF) at the CVBS input pin

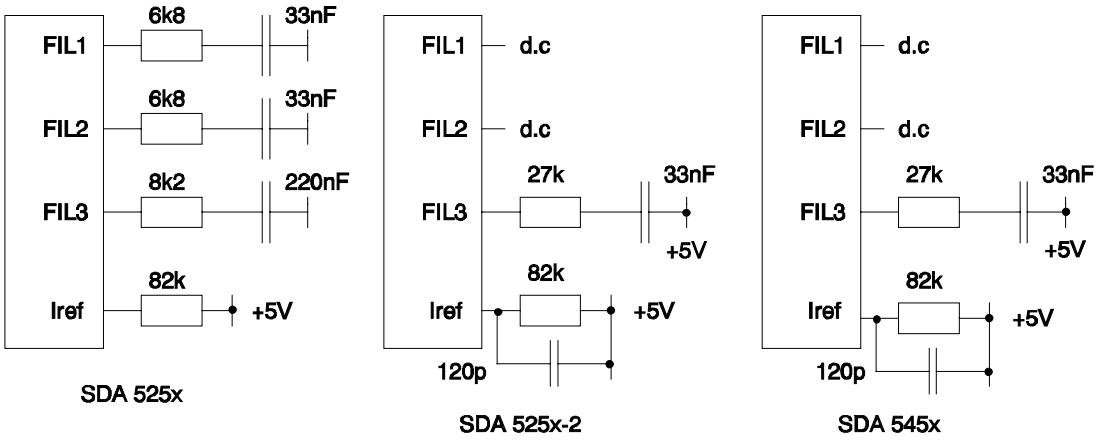


Figure 2: CVBS input network and filter network related to the SDA 525x

3.2 SDA 525x-2 & SDA 545x (Design step A)

- Filter 3 with different new values: (SDIP52-pin 25; MQFP80-pin 69; PLCC84-pin 63)
  R=27k C=33nF
- Reference current resistor at the IREF pin (SDIP52-pin 29; MQFP80-pin 73; PLCC84-pin 67)
  R=82k and in parallel 120 pF, don´t change the value !
- Use low impedance output driver (max. 220 ohms) to feed the CVBS input of TVText. A resistor in line to the CVBS input would cause spikes at the sync bottom. The voltage is calculated by $U_{SPIKE} = I_{CLAMP} * R$ (I_{CLAMP} = 85..95µA). That spikes could affect the sync slicer functionality if they exceed 100mV, only.
- Filter network 1 (SDIP52-pin 26; MQFP80-pin 70; PLCC84-pin 65) and Filter network 2 (SDIP52-pin 27; MQFP80-pin 71; PLCC84-pin 64) are not necessary (no external components). The former FIL1 and FIL2 pin must be left open (no function, do not connect !).
- Filter network 3 (SDIP52-pin 25; MQFP80-pin 69; PLCC84-pin 63) is to be tied to VDDA. You may tie it down to VSSA, if you can provide a proper supply voltage. Notice: The internal reference is related to VDDA. Ripple at the supply voltage can affect the slicer performance if you have tied down the filter to VSSA.

3.3 SDA 525x-2 & SDA 545x (Design step B)

- Filter 3 with different new values: (SDIP52-pin 25; MQFP80-pin 69; PLCC84-pin 63)
  R = 2k7 C = 33nF (**both values are preliminary**)
- Reference current resistor at the IREF pin (SDIP52-pin 29; MQFP80-pin 73; PLCC84-pin 67)
  R= 27k and in parallel 470 pF, don´t change the value ! (**both values are preliminary**)
- Use low impedance output driver (max. 220 ohms) to feed the CVBS input of TVText. A resistor in line to the CVBS input would cause spikes at the sync bottom. The voltage is calculated by $U_{SPIKE} = I_{CLAMP} * R$ (I_{CLAMP} = 85..95µA). That spikes could affect the sync slicer functionality if they exceed 100mV, only.
- Filter network 1 (SDIP52-pin 26; MQFP80-pin 70; PLCC84-pin 65) and filter network 2 (SDIP52-pin 27; MQFP80-pin 71; PLCC84-pin 64) are not necessary (no external components).
- Filter network 3 (SDIP52-pin 25; MQFP80-pin 69; PLCC84-pin 63) is to be tied to VDDA. You may tie it down to VSSA, if you can provide a proper supply voltage. Notice: The internal reference is related to VDD. Ripple at the supply voltage can affect the slicer performance if you have tied down the filter to VSSA.
- CVBS pin is the only one CVBS pin (SDIP52-pin 30; MQFP80-pin 74; PLCC84-pin 68)
- **Preliminary:** The CVBS resistor is changed. The clamping voltage was increased from 1.0 V to 2.0 V. Therefore the CVBS resistor needs to have the double value: 1 MOhm.

4 General items that affects slicer performance:

4.1 SDA 525x

- Filter 3: The higher the capacity, the better the noise immunity, but the slower the PLL settling time (e.g. after channel change).
- Separate data/adress lines (altering levels of port pins, PWM...) away from Filter 1-3 and their ground connection. Avoid coupling into filter network.
- Use filter network close to the TV text chip.
- Use bulky ground connection of filter network and VSSA-ground.
- Ground area under TV Text and external EPROM

4.2 SDA 525x-2 & SDA 545x (Design step A + B)

- Separate data/adress lines (altering levels of port pins, PWM...) away from Filter 3 and their connection to the power rail. Avoid coupling into filter network.
- Use filter network close to the TV text chip.
- Design step A: CVBS amplitude normally 1.0 Vpp (core area is between 0,7..1,4 V). Avoid CVBS levels outside that core area in order to get the optimized slicer performance.
- Design step B: The more CVBS level the better the slicer performance. Avoid CVBS levels below 1V.
- Ground area under TV Text and external EPROM
- You can improve the slicer performance when you smooth the +5 V supply voltage.
- In case of ripple at the supply voltage: It is recommend to tie the filter network at FIL3 to VDDA. Notice: The internal reference is related to the VDDA voltage. With smooth supply voltage you may tie the loop filter network to VSSA, also.
- Seperate the analog and digital supply voltage pins ! (Use only decoupled voltage for VDDA)
- Take SMD capacitors at the VDD and VDDA pins using the closest way to GND. Connect VSSA and VSS directly without any wire links.

5 Quartz / Ceramic resonator:

5.1 SDA 525x

- Use for both capacitors 33pF.
- Usually 18 MHz crystal is used. This crystal is used to generate the CPU clock only.
- You may change the crystal frequency without any affect to the slicer performance.
- You may use a ceramic resonator (for example MURATA type CSA18.000MXZ040 or MURATA type CST 18.000MXW040).

5.2 SDA 525x-2 & SDA 545x

- In order to get maximum slicer performance it is strictly recommended to use a 6.000 MHz crystal with tolerance of +/- 200ppm (over all). This crystal is used to generate the CPU clock, pixel clock and the clock frequency for the teletext slicer.
- Use for both capacitors 33pF.
- You may use resonator components with more tolerance when you won´t use the slicer unit.

6 External EPROM & SRAM

Timing values you can get in our seperate application note “SDA 5250 with external 128 TTX pages”. You can get that note via internet :

http://www.siemens.de/Semiconductor/products/ICs/32/3219.htm

7 100Hz application (only with SDA525x-100, SDA525x-2 (100Hz), SDA545x)

It is possible to use TV Text in 100Hz applications using H/V or Super Sandcastle. For more informations please see our seperate application note “How to use TVText SDA 525x in 100Hz applications.

http://www.siemens.de/Semiconductor/products/ICs/32/3219.htm

8 DisplayGenerator and RGB, Blank and COR output pins

8.1 SDA 525x

- 8 colours are available for OSD.
- All outputs (R, G, B, Blank and COR) provides TTL output signals (0...5V) with totem pole stages. To connect to a video switch it is necessary to use a resistor divider to get 0,5..0,7 Vpp.

8.2 SDA 525x-2

- You can use 8 colours.
- The R, G, B outputs are not TTL outputs! The output circuitry contains a DAC with current sources at the output. An external resistor of about 180 ohms is used to get a signal voltage of 1Vpeak.
- The Blank and the COR outputs provides TTL levels (0..5V) with totem pole stages.
- To lower cross-talking between the slicer input and the RGB outputs you must use a pull up capacitor at the IREF input.
- The RGB outputs issue a current of 5,3 mA (typ.)

8.3 SDA 545x

- You can use 16 colours out of 64 colours. 8 out of 64 colours you can use to define the foreground colour, 8 out of 64 you can use to define the background colour.
- It is possible to select different (not the default colours) colours for teletext pages in order to give your TV set a different outfit !
- The R, G, B outputs are not TTL outputs! The output circuitry contains a DAC with current sources at the output. An external resistor of 180 ohms is used to get a signal voltage of 1Vpeak.
- The Blank and the COR outputs provides TTL levels (0..5V) with totem pole stages.
- To lower cross-talking between the slicer input and the RGB outputs you must use a 120pF (design step A) or 330..470pF (desing step B) pull up capacitor at the Iref input.
- The RGB outputs issue a current of 5,3 mA (typ.)

8.4 SDA 525x-2 & SDA 545x : RGB output structure

Each of the RGB outputs consists of a current source, which is switched by a digital signal generated by the display control unit.

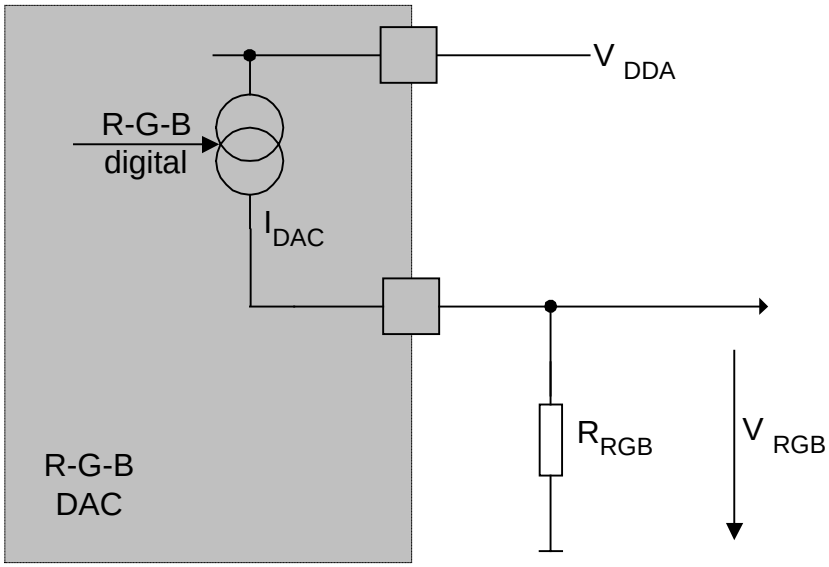


Figure 3: RGB output structure

If a pixel is ‚on', the DAC of the respective colour channel is switched to the external pin, otherwise the switch is off and no current is driven. Each RGB channel provides four current levels. The maximum current (white level) driven by the current source is 5,35 mA typical.

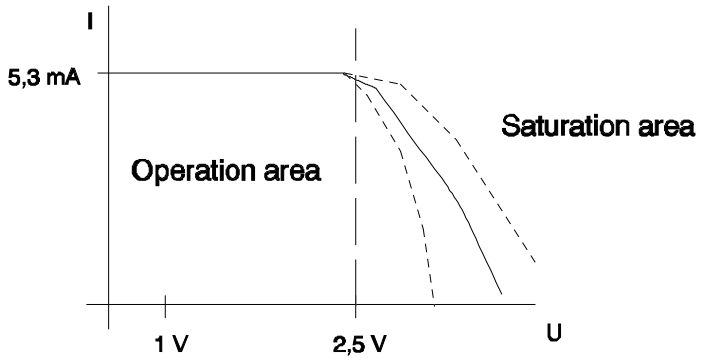


Figure 4: DC characteristic of the current source (DAC)

For example: You would like to get 1 Vpp RGB level, you would use 180 Ω, for 2,5 Vpp you would use 470 Ω.

Increased values of R_{RGB} = 470 ohms lead to higher output voltages, unless saturation mode of the current source is reached.

8.5 Block diagram and basic application circuits (SDA 525x-2 & SDA 545x)

The following shown solutions in figures 6 and figure 7 you can use with A-version (ROMless only) and with B-version (without restrictions), only. For A-version (ROM version only, cross talk !) you may use the principle shown below:

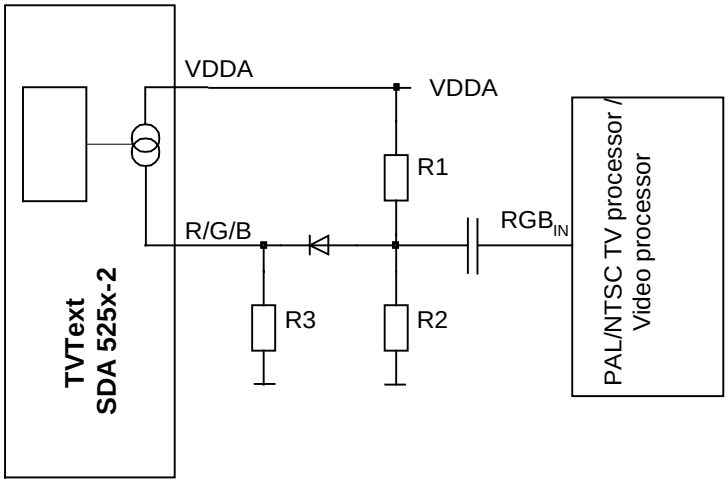


Figure 5: Principle of crosstalk suppression (resistor devider with load)

Figure 6 shows the usual way to connect the RGB outputs to the Video processor. One resistor per RGB-channel is enough to adjust the RGB output voltage. The desired voltage is calculated by

$$V_{RGB} = 5{,}35\ mA * R_{RGB}$$

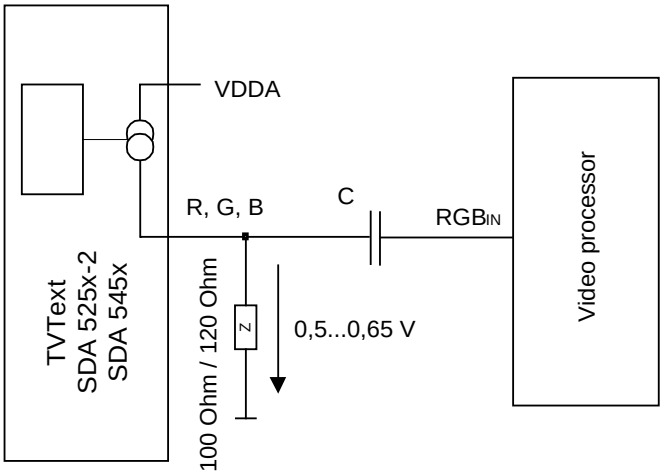


Figure 6: RGB outputs directly coupled to the Video processor

Figure 7 shows a possiblity for low cost applications. That circuitry avoids an additional AV-switch. You have to take care not to activate both input channels (AV and OSD). In that case the result will be a superposition of both signals. Therefore it is recommended to detect the Fastblank signal (at one of the port pins) in order to switch off the OSD.

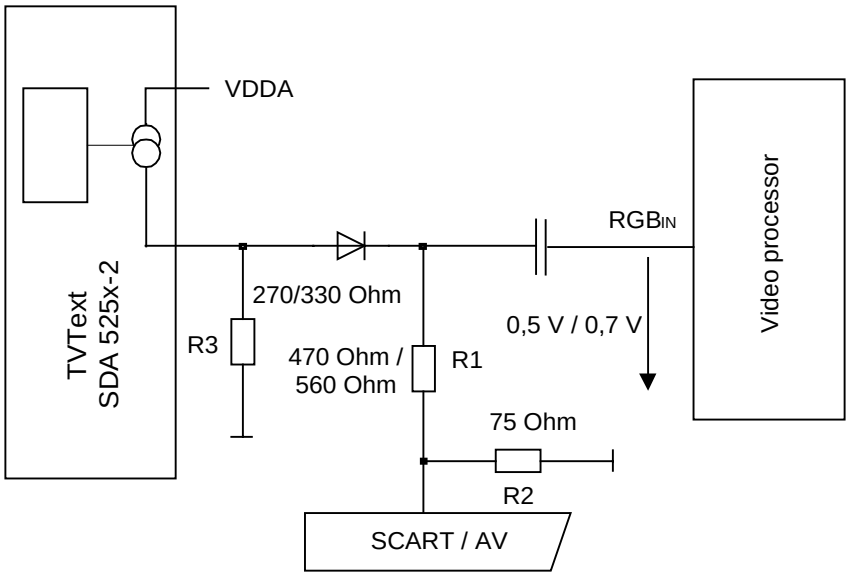


Figure 7: Low cost application to avoid an AV switch

The 75 Ohm resistor is to match the line. The serial resistor doesn´t matter in case of an AV-signal, because the input resistance of the Video processor is about 100 kOhms. The RGB output of TVText is switched off (high impedance).

If the OSD is switched on, the current source drives a current through the serial resistor and the matching resistor. The RGB_{IN} voltage is calculated by the formula:

$$V_{RGB} = I * (R1 + R2)$$

Figure 8 shows a workaround solution for TVText A-versions. The functionality is the same like in figure 7. The thick marked components are additionally necessary. The bias resistor divider is the common divider used for all three RGB-outputs. The diode 1N4148 at the base of the transistor compensates temperature effects. Without these diode the OSD amplitude would depend on temperature. The transistor is used to switch only. Therefore that circuitry makes sense for the SDA 525x-2 (A-version) only. An I_{RGB} current of the TVText will cut off the transistor nearly. The logic high current is coming from VDDA, hence it is with out crosstalk. When the chip internal current source is swiched off the transistor is switched on. The transistor is not in saturation mode to provide a minimum store time of the transistor. The diode at the collector decouples the SCART connector from the operation point (in low state) of the transistor. That makes SCART voltages with approximatly 700 mV possible (with 700mV input voltage).

Measurements shows: The OSD voltage is about 660 mV, the AV input voltage is 660 mV at RGB_{IN} of the video processor.

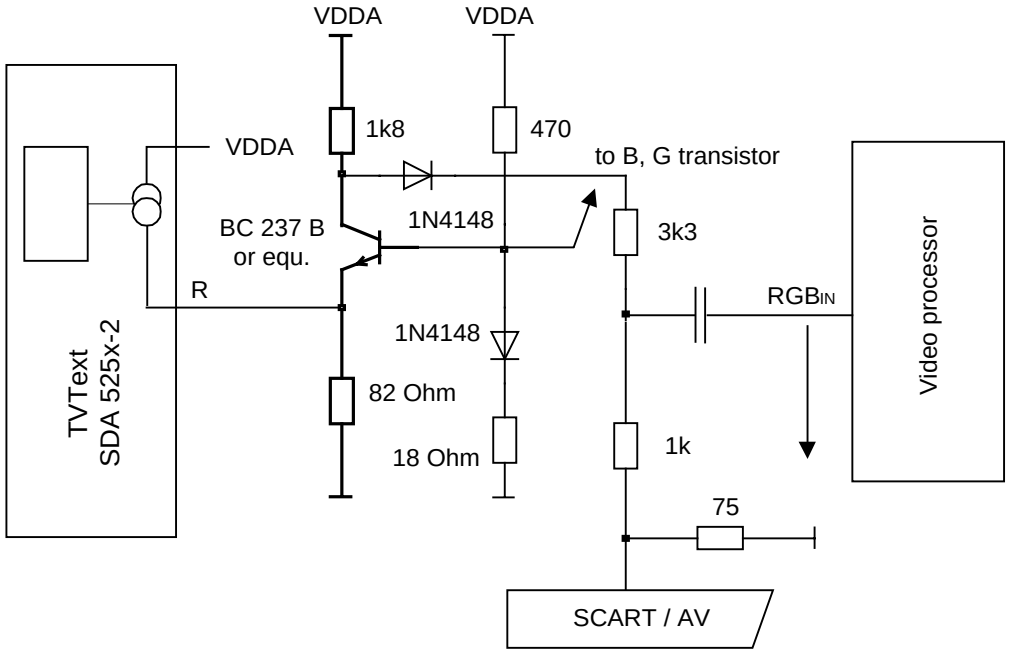


Figure 8: Suppressing cross-talk with transistors

8.6 New feature allows bypassing the video processor (B-version only)

Figure 9 shows an other low cost application. In that circuitry the video processor is bypassed. A resistor network in front of the video amplifier is used to get the right OSD output voltage at the triple video amplifier output. The PAL/NTSC TV processor is directly fed to the summary point of the video amplifier. You have to take care, that the automatic black-current stabilization (ABS) can work in the operation point, in spite of the R-network. You may use the resistor R_{TXT} (look at voltage V_{TXT}) to devide the current that is driven by the current source in the TVText inside. Please take care, that the voltage at the RGB-output of TVText cannot exceed 2,5 V (guaranted value). Beyond that voltage the current source will get less and less output resistance. That will affect your DC operation point of that circuitry.

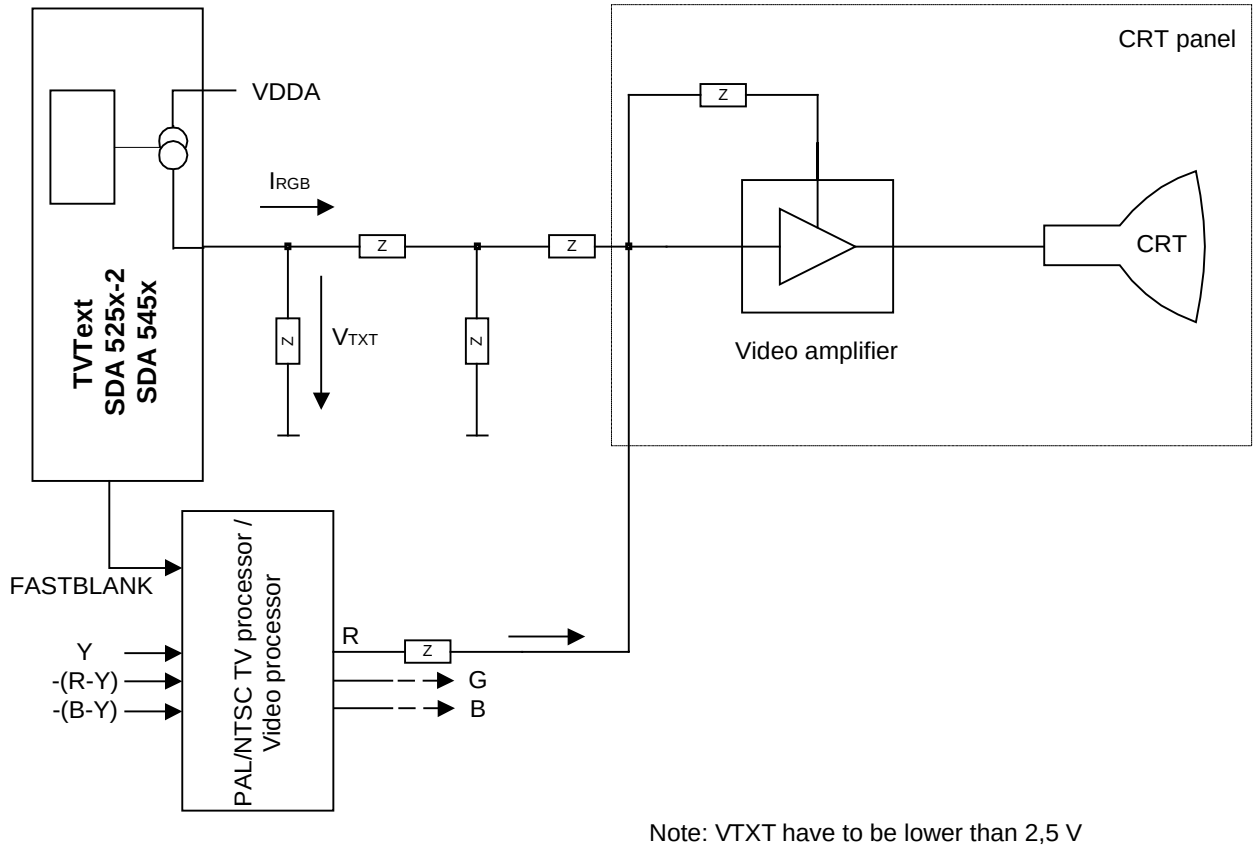


Figure 9: TVText and bypassed video processor

At the screen you will find the following problem (see figure 10). The RGB video path inside the TV processor/video processor provide a limited bandwidth. Therefore the whole path shows a propagation delay time of about 80..100ns (depends on type and bandwidth). That means: Fastblank is active (OSD starts), afterwards the RGB output of the video processor is 80..100ns longer active. The result is a superposition of the OSD/TEXT and the video picture at every start line of the OSD window (very bright stripe). When the OSD will disappear (Fastblank not active) the video picture will appear 80..100ns later (black stripe).

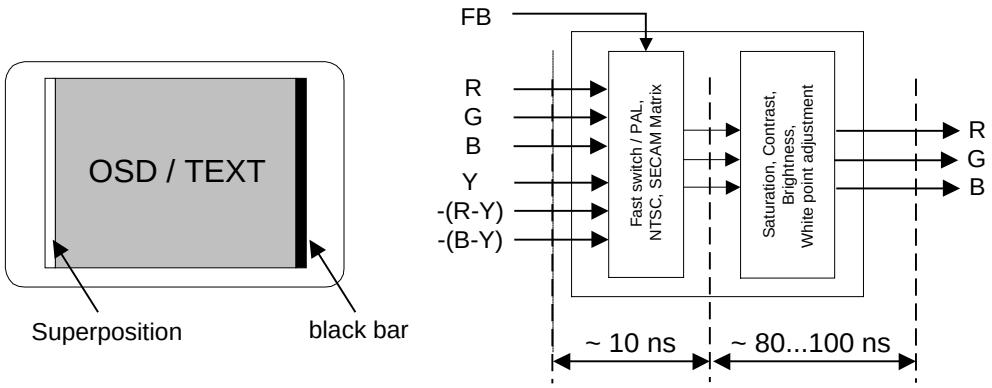


Figure 10: Superposition and black gap on screen

To overcome that problem you can use a new feature: the RGB delay line. Usually the Fastblank signal and the RGB information occurs at the same time. That guarantees mixed mode ability.

In the new DAFR2 register (Display Advanced Function) you can use 2 bits (RGBD.0 & RGBD.1) to delay the RGB information in order to compensate the delay time of the video processor. The delay time steps uses the pixel raster, therefore the delay time depends on the selected pixel frequency.

9 Port pin behaviour

The port pin structure of the new SDA 525x-2 & SDA 545x is changed (compared to the SDA 525x). The new chips use internal highside driver that are switched on beyond a threshold voltage V_{TH}.

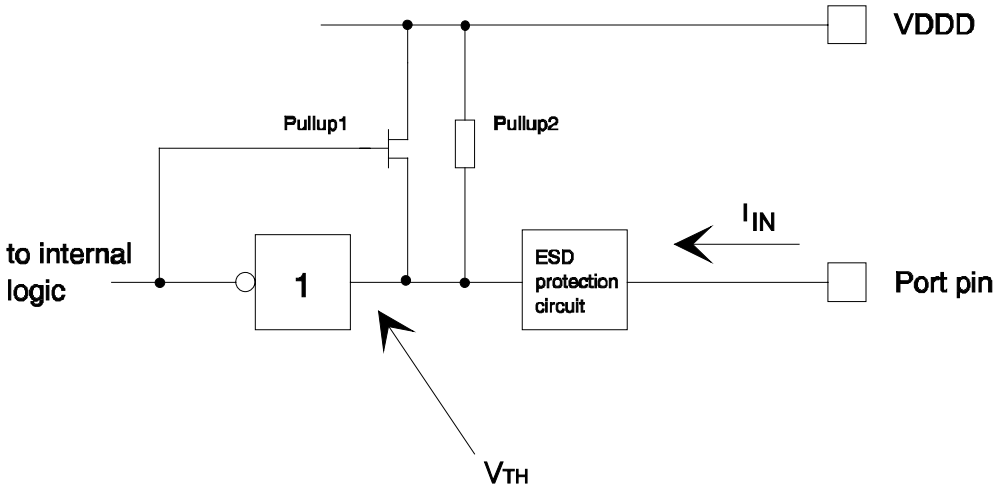


Figure 11: The port pin structure (e.g. VSYNC input pin)

The port pin input circuit consists a standard ESD protection structure, an input stage and two pullup devices (Pullup1 and a non-linear pullup2).

Pullup device 1 is only active, if the input voltage is above the threshold voltage V_{TH} (pullup current I_{P1}), pullup device 2 is always active (pullup current I_{P2}).

The following table decribes the current limits checked during final device testing. A voltage (V_{IN}) is applied to the pin and the current flowing into the pin (I_{IN}) is measured. The threshold voltage V_{TH} is the maximum voltage allowed, before the pullup device1 is activated.

	min	typ	max	Condition
I_{IN}	-400 µA	-300 µA	-10 µA	V_{IN} < 3.0 V
I_{IN}	-300 µA	-250 µA	-100 µA	V_{IN} = 3.0 V
I_{IN}	-150 µA	-80 µA	-10 µA	V_{IN} = 4.5 V
V_{TH1}	1.0 V	1.5 V	2.0 V	

Table 1: Input current of the I/O pins

That means below 1.0 V the high side driver is switched off (low state). Beyond at least 2.0 V the high side driver is switched on (high state).

The source resistor at these input pins have to be less than 1,0 V / 400µA < 2,5 kOhm (worst case) to ensure the possibility of a H-L-edge ! Otherwise the internal pullup resistor will overdrive your external pull down mechanism with an High-state as result.

Affected pins are:	Not affected pins are:
Port P1.0...1.7 Port P3.0...P3.7 Port P4.x VS input/P4.7 D0..D7 WR, RD, ALE, PSEN	Port P0.0...P0.7 Port P2.0...2.3 (input only) HS/VS (input only) A0...A16 (output only) COR, Blank, Reset

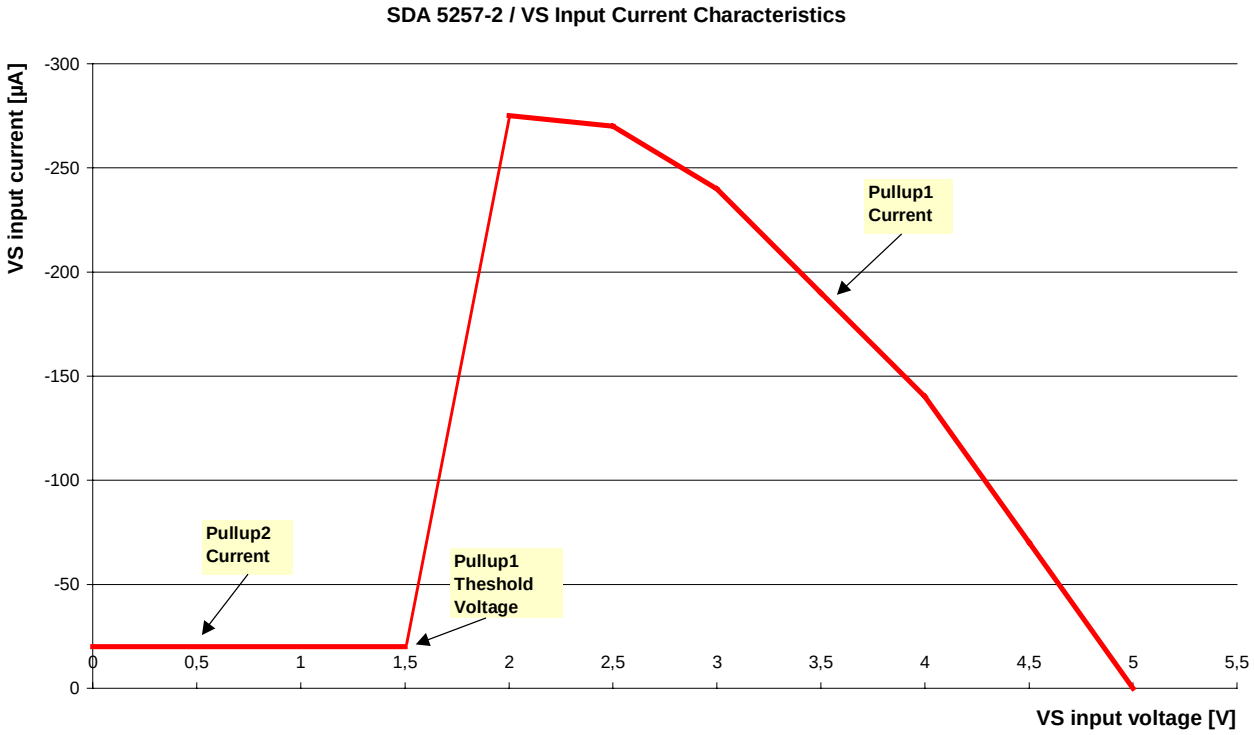


Figure 12: DC characteristic of port pin input structure (e.g. VSync)

10 Software Changes (SDA 525x → SDA 525x-2 / SDA 545x)

A change from the SDA 525x to the versions SDA 525x-2 or SDA 545x cause some software changes in order to be compatible.
All calls of the subroutine adjust_horizontal (inside the module IFRDEMO.C51 on the Firmware Demo Disk) must be removed from the external controller software. This routine was developed to adjust the display to the middle of the screen according to tolerances of the LC-oscillator. This oscillator is not used any more. The pixel clock is derived from the single external crystal.
A possibility of an horizontal/vertical adjust of the OSD position in the service mode is strongly recommended.

Furthermore, due to some changes in the special function registers, the software needs to be checked. The changes are in detail:

1.) The serial interface is not supported any longer. By this, registers SCON and SBUF are no longer available. The Serial Interrupt Enable Flag ES of the Interrupt Enable register (Bit 4 of A8) must not be written (default after reset=0).
2.) The functions and bits Prescaler Control (PSC) and ADC sample time (STADC) of the Special Function Register ADCON are not available any more. Bits 7 and 6 of D8 must be 0.
3.) The following registers and bits must not be written and need to be checked:

SBUF (99):	Bits 0 to 7	
SCON (98):	Bits 0 to 7	
ACQMS2 (C2):	Bits 0 to 7	
DMODE2 (C7):	Bits 5 to 7	(Bits 0-4 used by the firmware)
ADCON (D8):	Bits 6 and 7	
IE (A8):	Bit 4	
DMOD (D6):	Bits 1-6	

11 Current Consumption

The current consumption of the new SDA 525x-2 and SDA 545x is different from SDA 525x.
The power consumption of TVText plus (ROM-Version) is at maximum 100mA and in ROMless versions at max. 95 mA (0,5 W; @ 18MHz CPU clock). There exist several way´s to reduce the power consumption:

- Reduction of the DRAM refresh rate (SDA 525x, SDA 525x-2 & SDA 545x)

The new technology used for SDA 5450 provides increased DRAM data retention times. Therefore, the refresh rat can be reduced compared to the SDA 5250(-1). This setting can be used generally, not only for idle mode. The reduction of supply current depends on the DRAM data contents and can be up to 8 mA. The refresh rate has to be selected as follows:

```
MOV DRCON, #0E0h
```

- Aquisition Power Down (SDA 525x, SDA 525x-2 & SDA 545x)

If the data aquisition is not used, the corresponding circuit can seperately be switched into power down mode. This is done by the operation:

```
ORL AFR,#01h
```

The WakeUp is done by

```
ANL AFR, #0FEh
```

After wake up, the circuit needs some time to restart, a wait time of 0 second should be sufficient before acquiring new data. This mode will save about 10 mA.

- Reduction of processor speed (SDA 525x-2 & SDA 545x)

The CPU frequency can be reduced from 18 MHz to 6 MHz by setting

```
MOV OSCON, #01h
```

and is reset to 18MHz again by

```
MOV OSCON, #03h
```

This will reduce the power consumption by about 10 mA

- Further reduction of processor speed with CLC bit (SDA 525x-2 & SDA 545x)

```
MOV AFR,  #80h
```

- Deactivating of display (SDA 525x, SDA 525x-2 & SDA 545x)

  The display clock can be switched off completly. This is done by the command:

  ```
  ORL 0CDh, #03h
  ```

  To reactivate the display clock use the command:

  ```
  ANL 0CDh, #0FCh
  ```

  Estimated current reduction is 3 mA

- Switching the slicer off (only in SDA 545x, B-Version)

  In our new B-design step you will have the posssibility to switch off the slicer circuit. It is estimated to reduce the power consumption by 5mA. You can do that with

  ```
  ANL DAFR3,#80h
  ```

  and release with

  ```
  ANL DAFR3, #00h
  ```

- Idle mode (SDA 525x, SDA 525x-2 & SDA 545x)

- PowerDown mode(SDA 525x, SDA 525x-2 & SDA 545x)

12 EMC Guidelines

The EMC requirements for an electronic module must be considered as early as the design stage allows. EMC affects mostly following items:

- Crosstalk (especially CVBS into the RGB outputs, or clock rests in RGB output)
  One can look ´through´ the OSD: a set on edge of the CVBS is visible. Light dark vertical stripes are visible.
- Slicer performance reduction
  Eyeheight performance and noise performance suffers
- Electro-magnetic radiation

There are some ways to overcome that problems:

General items

1.) Board layout for optimizing EMC
The impedance between the supply lines can be very significantly reduced by using a complete board surface as a ground or VDD layer. Use bulky ground lines in order to reduce ground bounce. Avoid wire links in the ground line that might introduce inductance into ground.

2.) Use blocking capacitors with low feed inductance
A VDD and a ground pin are located next to each of them to improve blocking by capacitors at low feed inductances (Ceramik types in SMD package). Use blocking capacitors connected to the pin (VDD and VDDA) at the shortest way as possible ! Use bulky ground lines to connect the VSS pins and the blocking capacitors. Use more capacitors with different values (e.g: 1nF and 10nF and 100nF) to block a wide frequency spectrum.
An electrolytic decoupling capacitor may be placed some cm away from the chip. A choke (e.g. 10µH) can be used to supply that capacitor.

3.) Short distances for wires with high clock rates
Take care that e.g. the PWM line is seperated from analog lines like FIL3 network or IREF network. A well-designed board layout will keep fastclocked signal lines as short as possible in order to minimize emissions by antenna structures.

4.) Use serial resistors in line to the adress lines
In applications with the ROMless TVText it is necessary to connect an external EPROM via a adress/data bus. Measurement shows, that the adress bus causes additional noise at VDD when the adress lines shows oversweeps. To overcome that you might use serial resistors with about 100 ohms. That avoids big watt-less and re-charging current during the edges.

TVText related items (SDA 525x-2 & SDA 545x)

5.) Seperate the analog and digital supply voltage pins VDD and VDDA
You can improve the slicer performance and avoid a clock crosstalk into the RGB outputs by using an inductor (68µH) between VDDA and VDD (minimum requirement). The best way is to seperate that pins with two power blocking filter networks (refer figure 13).

6.) Use and vary the capacitor at IREF pin (B-Version only)
In parallel to the R_{IREF} one can vary the C_{IREF} capacitor in order to overcome crosstalk of CVBS into the RGB outputs and to overcome the superimposed clock frequency (vertical light-darked strips). Our measurements shows good suppression with 330...470pF (B-Version).

7.) If item 4.) isn´t possible (placing and routing problems on your PCB) you can use an additional capacitor (1..10nF) between IREF pin and VSSA. That will suppress the clock crosstalk, too.

Note: No exact values in 2.), 5.) 6.) and 7.) are given, because it depends on your layout.

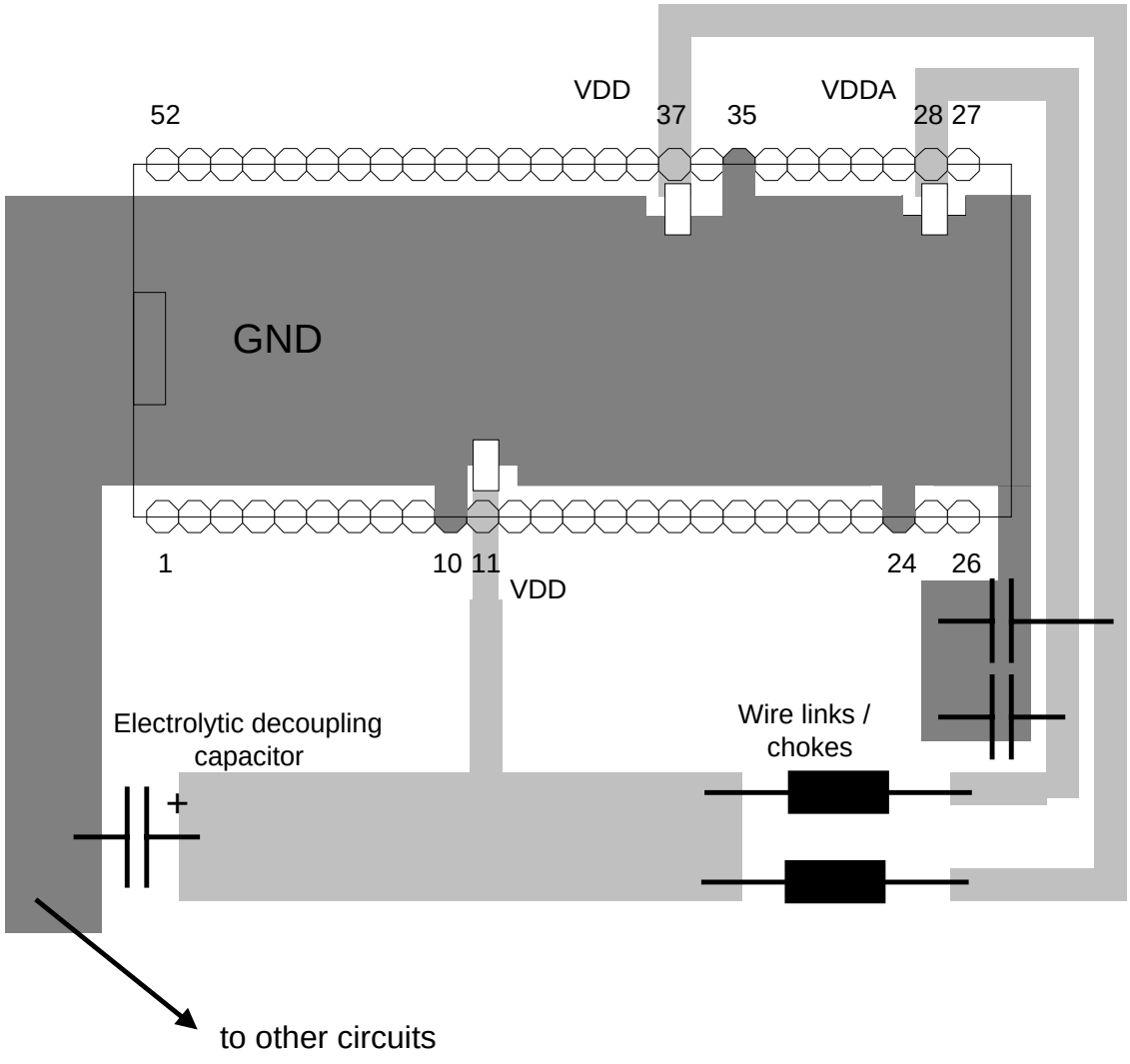
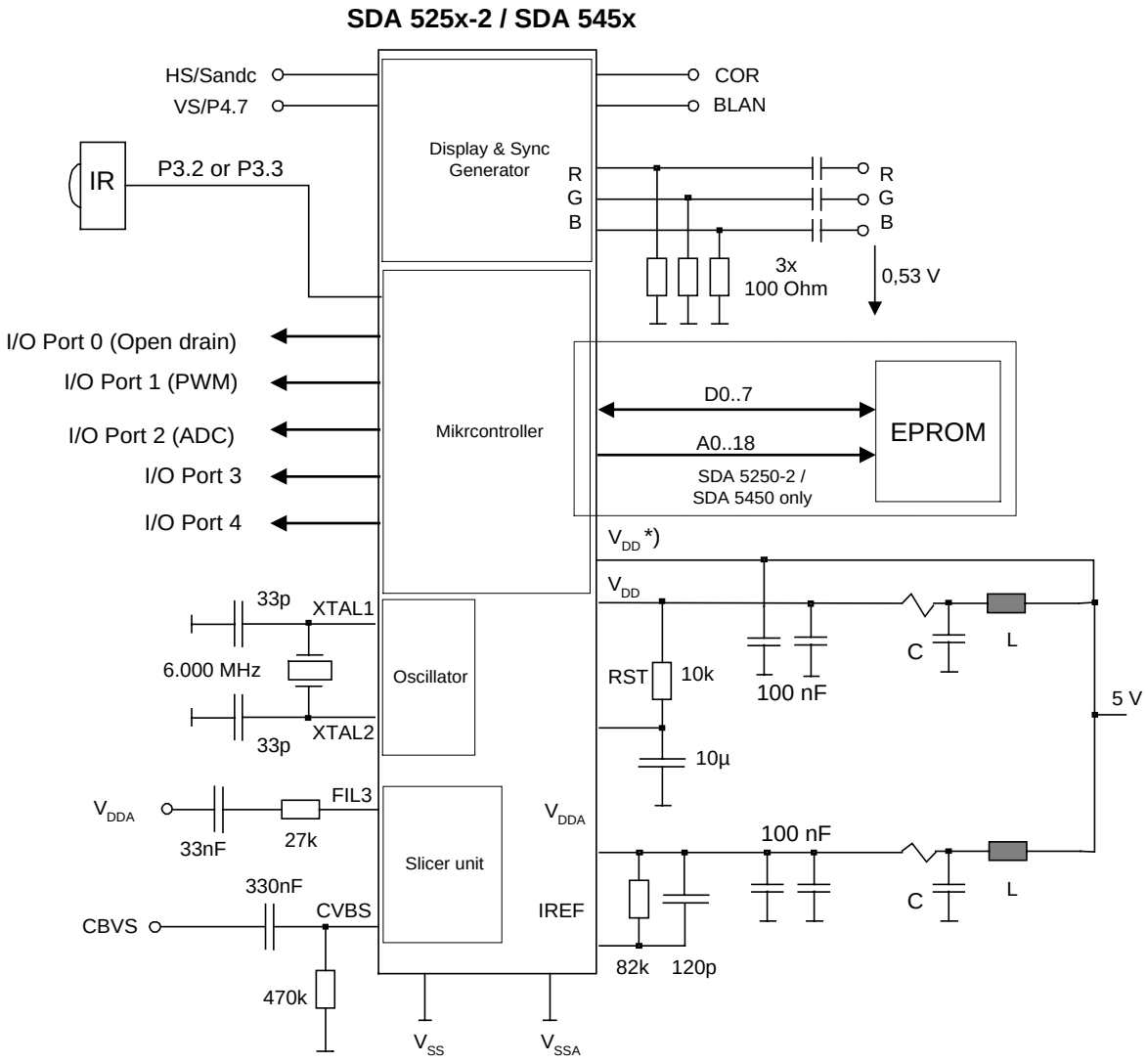


Figure 13: Power supply and GND connections

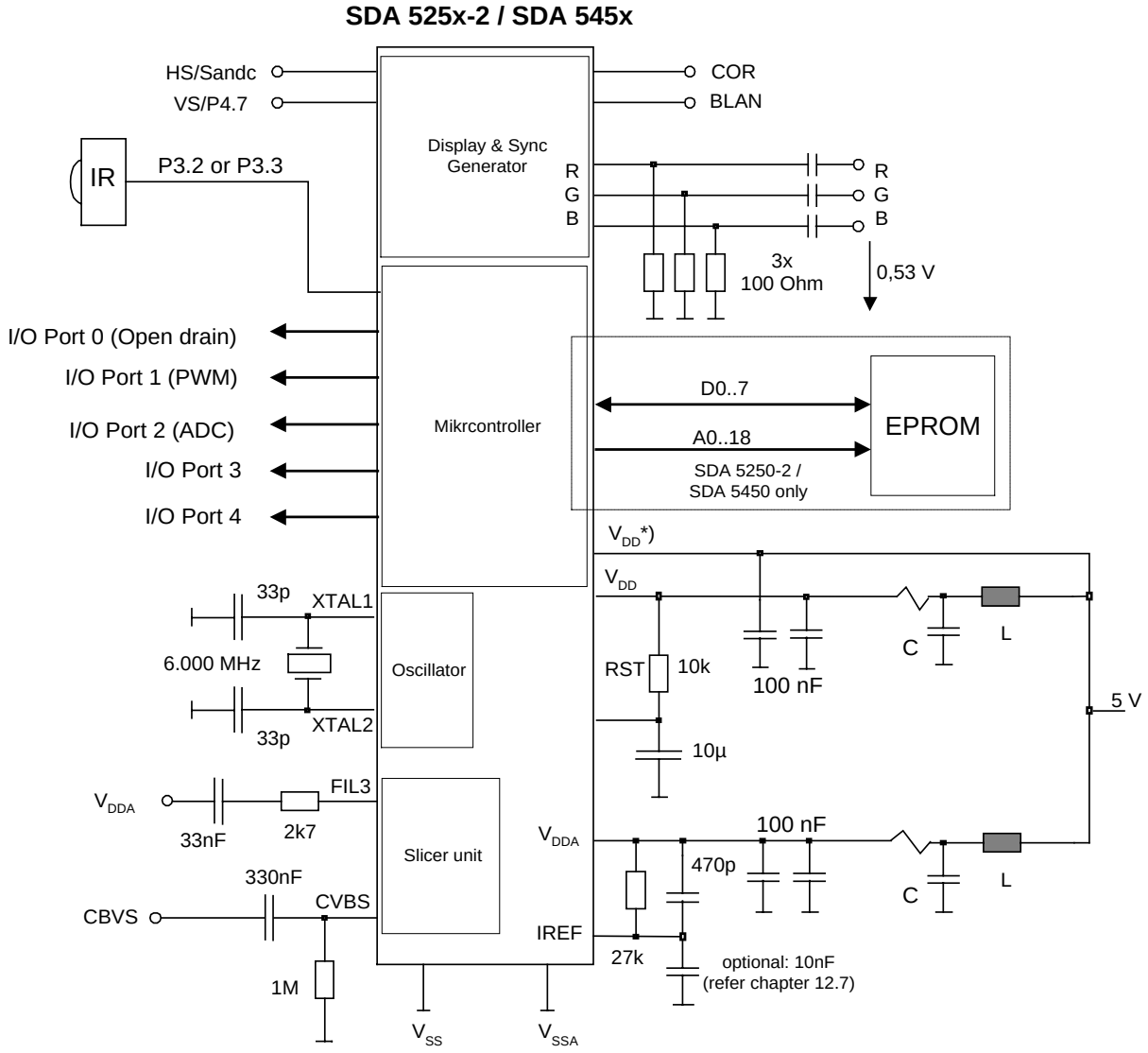
13 Application circuits



**) Pin 2 at PLCC, pin 11 at SDIP*

Figure 14: SDA 525x-2 / SDA 545x Application circuit diagram for **A-version**

Note: The data (D0..7) and adress lines (A0..18) are available in the ROMless versions only.



**) Pin 2 at PLCC, pin 11 at SDIP*

Figure 15: SDA 525x-2 / SDA 545x Application circuit diagram for **B-version (preliminary)**

Note: The data (D0..7) and adress lines (A0..18) are available in the ROMless versions only.