TSTTNR1 Analog IPs control register

7	6	5	4	3	2	1	0
Reserved		ADC_PON	ADC_INMODE	Reserved		OSCI_POFF	REG_POFF

Address: 0x42
Type: Read/write (accessible in standby mode)
Reset: 0x00
Description: See also Chapter 9: *DC regulator on page 28*.

[7:6] **Reserved**: must be set to 0

[5] **ADC_PON:** ADCs power on
0: adc in standby mode 1: adc active

[4] **ADC_INMODE:** differential Input Voltage
0: 1 Vpp 1: 2 Vpp

[3:2] **Reserved**: must be set to 0

[1] **OSCI_POFF:** OSCI power off
0: OSCI active 1: OSCI in standby

[0] **REG_POFF:** REGULATOR power off
0: REGULATOR active 1: REGULATOR in standby mode

SYMBCTRL Constellation sources control register

7	6	5	4	3	2	1	0
Reserved						SYMB_CHOICE	

Address: 0x4A
Type: Read/write
Reset: 0x00
Description: See also Section 7.3.5: *I, Q symbol monitoring and bypass on page 21*.

[7:2] **Reserved**: must be set to 0

[1:0] **SYMB_CHOICE**: I&Q choice for reading
00: after demodulation 01: after polyphase filter
10: after derotation 11: after dc_adjust

ISYMB I symbol register

7	6	5	4	3	2	1	0
I_SYMB							

Address: 0x4B
Type: Read only
Description: See also Section 7.3.5: *I, Q symbol monitoring and bypass on page 21*.

[7:0] **I_SYMB[7:0]:** 8 bits of I symbol (signed value)

QSYMB Q symbol register

7	6	5	4	3	2	1	0
Q_SYMB							

Address: 0x4C
Type: Read only
Description: See also Section 7.3.5: *I, Q symbol monitoring and bypass* on page 21.

[7:0] **Q_SYMB**: 8 bits of Q symbol (signed value)

GPIOxCFG General purpose I/O control registers

7	6	5	4	3	2	1	0
GPIOx_OD	GPIOx_CFG						GPIOx_XOR

Address: 0x60 to 0x69
Type: Read/write (accessible in standby mode)
Reset: 0x82(1000 0010, GPIOxCFG in input mode)
Description: See also Chapter 3: *General purpose I/O (GPIO)* on page 9.

[7] **GPIOx_OD:** open drain configuration of GPIO pin
0: push-pull 1: open-drain.

[6:1] **GPIOx_CFG[5:0]:** see Table 6.

[0] **GPIOx_XOR:** when high XOR the result of GPIO_CFG configuration.

Table 6: General-purpose input and output configuration

Value	Signal	Description
0	0	Force output to 0
1	1	Force output to 1
2-7	-	Reserved
8	AGC	AGC output
9-15	-	Reserved
16	DISEQC_OUT	Diseqc 2.0 output
17-20	-	Reserved
21	OUTBIT	-
22	DAC	DAC output
23	IRQ	IT output
24-27	-	Reserved
28	SDAT	Tuner dedicated SDA signal
29	SCLT	Tuner dedicated SCL signal
26-51	-	Reserved
52	AUX_CK	Auxiliary signal
53	COARSE	Coarse mode indicator
54	FINE	Fine mode indicator
55-63	-	Reserved

SDATCFG SDAT I/O control register

7	6	5	4	3	2	1	0
SDAT_OD	SDAT_CFG						SDAT_XOR

Address: 0xB0
Type: Read/write (accessible in standby mode)
Reset: 0xB8(1011 1000)
Description: Same as GPIOxCFG except for address and reset values.

SCLTCFG SCLT I/O control register

7	6	5	4	3	2	1	0
SCLT_OD	SCLT_CFG						SCLT_XOR

Address: 0xB1
Type: Read/write (accessible in standby mode)
Reset: 0x3A(0011 1010)
Description: Same as GPIOxCFG except for address and reset values.

AGCCFG AGC I/O control register

7	6	5	4	3	2	1	0
AGC_OD	AGC_CFG						AGC_XOR

Address: 0xB2
Type: Read/write (accessible in standby mode)
Reset: 0x90(1001 0000)
Description: Same as GPIOxCFG except for address and reset values.

DIRCLKCFG DIRCLK I/O control register

7	6	5	4	3	2	1	0
DIRCLK_OD	DIRCLK_CFG						DIRCLK_XOR

Address: 0xB3
Type: Read/write (accessible in standby mode)
Reset: 0x80 (1000 0000)
Description: Same as GPIOxCFG except for address and reset values.

AUXCKCFG AUXCK I/O control register

7	6	5	4	3	2	1	0
AUXCK_OD	AUXCK_CFG						AUXCK_XOR

Address: 0xB4
Type: Read/write (accessible in standby mode)
Reset: 0x68(0110 1000)
Description: Same as GPIOxCFG except for address and reset values.

STDBYCFG **STDBY I/O control register**

7	6	5	4	3	2	1	0
STDBY_OD	STDBY_CFG						STDBY_XOR

Address: 0xB5
Type: Read/write
Reset: 0x80(1000 0000) (accessible in standby mode)
Description: Same as GPIOxCFG except for address and reset values.

CS0CFG **CS0 I/O control register**

7	6	5	4	3	2	1	0
CS0_OD	CS0_CFG						CS0_XOR

Address: 0xB6
Type: Read/write (accessible in standby mode)
Reset: 0x80(1000 0000)
Description: Same as GPIOxCFG except for address and reset values.

CS1CFG **CS1 I/O control register**

7	6	5	4	3	2	1	0
CS1_OD	CS1_CFG						CS1_XOR

Address: 0XB7
Type: Read/write (accessible in standby mode)
Reset: 0x80(1000 0000)
Description: Same as GPIOxCFG except for address and reset values.

DISEQCOCFG **DISEQC_OUT I/O control register**

7	6	5	4	3	2	1	0
SDAT_OD	SDAT_CFG						SDAT_XOR

Address: 0xB8
Type: Read/write (accessible in standby mode)
Reset: 0x20(0010 0000)
Description: Same as GPIOxCFG except for address and reset values.

GPIOVALx GPIO status registers 2 to 0

7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
7	6	5	4	3	2	1	0
CS1	CS0	STDBY	AUXCLK	DIRCLK	AGC	GPIO9	GPIO8
7	6	5	4	3	2	1	0
							DISEC_OUT

Address: 0x6A (GPIOVAL0), 0x6B (GPIOVAL1), 0x6C (GPIOVAL2)
Type: Read only (accessible in standby mode)
Description: See also Chapter 3: *General purpose I/O (GPIO)* *on page 9*.

IRQSTATx Interrupt request status registers 1 to 0

7	6	5	4	3	2	1	0
TMG_LOCK	NOT(TMG_LOCK)	CF_SYNC	NOT(CF_SYNC)	DISEQCTX	DISEQCRX	OV_RSFIFO	LOCK_VIT
7	6	5	4	3	2	1	0
NOT(LOCK_VIT)	Reserved						

Address: 0x45 (IRQSTAT2) and 0x46 (IRQSTAT1)
Type: Read/write (accessible in standby mode)
Reset: 0x00,0x00
Description: Status register block giving the list of currently pending interrupt request occurrences.
0: no occurrence since last erase of this bit.
1: an interrupt request has occurred since last erase of this bit.

IRQMSKx Interrupt mask control registers 1 to 0

7	6	5	4	3	2	1	0
MTMG_LOCK	MNTMG_LOCK	MCF_SYNC	MNCF_SYNC	MDISEQCTX	MDISEQCRX	MOV_RSFIFO	MLOCK_VIT
7	6	5	4	3	2	1	0
MNLOCK_VIT	Reserved						

Address: 0x43 (IRQMSK2) and 0x44(IRQMSK1)
Type: Read/write (accessible in standby mode)
Reset: 0x00 and 0x00
Description: Enable interrupt mask. This register block gives the list of interrupt request that are enabled to generate the IRQ signal.
0: interrupt request not enabled to generate IRQ signal.
1: interrupt request enabled to generate IRQ signal.

12.4 Fast channel acquisition and blind search registers

ASCTRL Autoscan control register

7	6	5	4	3	2	1	0
Reserved		FROZE_LOCK	KI		CENTER	FINE	COARSE

Address: 0x50
Type: Read/write
Reset: 0x10 (0001 0000)
Description: See also Chapter 10: *Fast channel acquisition and blind search* on page 29.

[7:6] **Reserved**: must be set programmed to 0.

[5] **FROZE_LOCK:** control, when high, froze accu1 and accu2 (see ACCU1VAL and ACCU2VAL registers)

[5:3] **KI[1:0]:** control, integration ratio of power spectrum measurements in coarse mode
00: freeze mode 01: 1/4
10: 1/8 11: 1/16

[2] **CENTER:** control, when high, reduce residual offset of Fs.

[1] **FINE:** when high, enabled fine mode

[0] **COARSE:** control, when high, enable COARSE mode

COARP1 Autoscan control register

7	6	5	4	3	2	1	0
Reserved	KT						

Address: 0x51
Type: Read/write
Reset: 0x3A (0011 1010)
Description: See also Section 10.1.1: *First step: coarse autosearch* on page 30.

[7] **Reserved**: must be set programmed to 0.

[6:0] **KT[6:0]:** control, fixed parameter KT

COARP2 Autoscan control register

7	6	5	4	3	2	1	0
Reserved		KC			KS		

Address: 0x52
Type: Read/write
Reset: 0x09 (0000 1001)
Description: See also Section 10.1.1: *First step: coarse autosearch* on page 30.

[7:6] **Reserved**: must be set programmed to 0.

[5:3] **KC[2:0]:** control, frequency carrier correction ratio.

[2:0] **KS[2:0]:** control, frequency timing correction ratio.

FMINM FMIN register (MSB)

7	6	5	4	3	2	1	0
STOPON_FMIN	FMIN						

Address: 0x53
Type: Read/write
Reset: 0x00
Description: See also Section 10.1.2: *Second step: fine scan on page 30*.

[7] **STOPON_FMIN**: control, when high, stop Fine mode if current timing frequency is below FMIN value.

[6:0] **FMIN[14:8]:** control, minimum frequency bound.

FMINL FMIN register (LSB)

7	6	5	4	3	2	1	0
FMIN							

Address: 0x54
Type: Read/write
Reset: 0x00
Description: See also Section 10.1.2: *Second step: fine scan on page 30*.

[7:0] **FMIN[7:0]:** control, minimum frequency bound.

FMAXM FMAX register (MSB)

7	6	5	4	3	2	1	0
STOPON_FMAX	FMAX						

Address: 0x55
Type: Read/write
Reset: 0x00
Description: See also Section 10.1.2: *Second step: fine scan on page 30*.

[7] **STOPON_FMAX:** control, when high, stop Fine mode if current timing frequency is above FMAX value.

[6:0] **FMAX[14:8]:** control, maximum frequency bound.

FMAXL FMAX register (LSB)

7	6	5	4	3	2	1	0
FMAX							

Address: 0x56
Type: Read/write
Reset: 0x00
Description: See also Section 10.1.2: *Second step: fine scan on page 30*.

[7:0] **FMAX[7:0]:** control, maximum frequency bound.

FINEINC Fine increment register

7	6	5	4	3	2	1	0
FINE_INCR							

Address: 0x57
Type: Read/write
Reset: 0x00
Description: See also Section 10.1.2: *Second step: fine scan* on page 30.

[7:0] **FINE_INCR[7:0]:** 8bits signed increment step (signed).

STEP2 STEP2 register

7	6	5	4	3	2	1	0
STEP2_MINUS				STEP2_PLUS			

Address: 0x58
Type: Read/write
Reset: 0x54 (0101 0100)
Description: Section 7.2.3: *Timing lock indicator* on page 20.

[7:4] **STEP2_MINUS[3:0]:** control, decrease by STEP2MINUS the accumulator of the second indicator.

[3:0] **STEP2_PLUS[3:0]:** control, increase by STEP2PLUS the accumulator of the second indicator.

TH2 Threshold2 (MSB) register

7	6	5	4	3	2	1	0
TH2							

Address: 0x59
Type: Read/write
Reset: 0x86 (1000 0110)
Description: Section 7.2.3: *Timing lock indicator* on page 20.

[7:0] **TH2[9:2]:** threshold2 value.

TH2ATH1 Threshold 2 (LSB) and 1 (MSB) register

7	6	5	4	3	2	1	0
TH2		Reserved					TH1

Address: 0x5A
Type: Read/write
Reset: 0x00
Description: Section 7.2.3: *Timing lock indicator* on page 20.

[7:6] **TH2[1:0]:** LSB of TH2

[5:2] **Reserved:** must be programmed to 0.

[1:0] **TH1[9:8:0]:** MSB of TH1.

TH1 Threshold 1 (LSB) register

7	6	5	4	3	2	1	0
TH1							

Address: 0x5B
Type: Read/write
Reset: 0x9B(1001 1011)
Description: Section 7.2.3: *Timing lock indicator on page 20*.

[7:0] **TH1[7:0]:** LSB of TH1

THH Threshold H register

7	6	5	4	3	2	1	0
Reserved		THH					

Address: 0x5C
Type: Read/write
Reset: 0x08(0000 1000)
Description: Section 7.2.3: *Timing lock indicator on page 20*.

[7:6] **Reserved**: must be programmed to 0.

[5:0] **THH[5:0]:** unsigned value.

IND1MAX Indicator 1 limit register

7	6	5	4	3	2	1	0
IND1_THRESHOLD							

Address: 0x5D
Type: Read/write
Reset: 0x1D(00011 1101)
Description: Section 7.2.3: *Timing lock indicator on page 20*.

[7:0] **IND1_THRESHOLD[7:0]**: if IND1 is above this limit tmg_lock is asserted.

ACCU1VAL Accu1 status register

7	6	5	4	3	2	1	0
ACCU1_VAL							

Address: 0x5E
Type: Read/write
Description: Section : *ASCTRL on page 61*.

[7:0] **ACCU1_VAL[7:0]:** MSB of ACCU1. you can preset the ACCU1 MSB by writing in this register.

ACCU2VAL **Accu2 status register**

7	6	5	4	3	2	1	0
ACCU2_VAL							

Address: 0x5F
Type: Read/write
Description: Section : *ASCTRL on page 61*.

[7:0] **ACCU2_VAL[7:0]:** MSB of ACCU2. you can preset the ACCU1 MSB by writing in this register.

13 Application block diagrams

Figure 17: STV0288 application block diagram with the STB6000

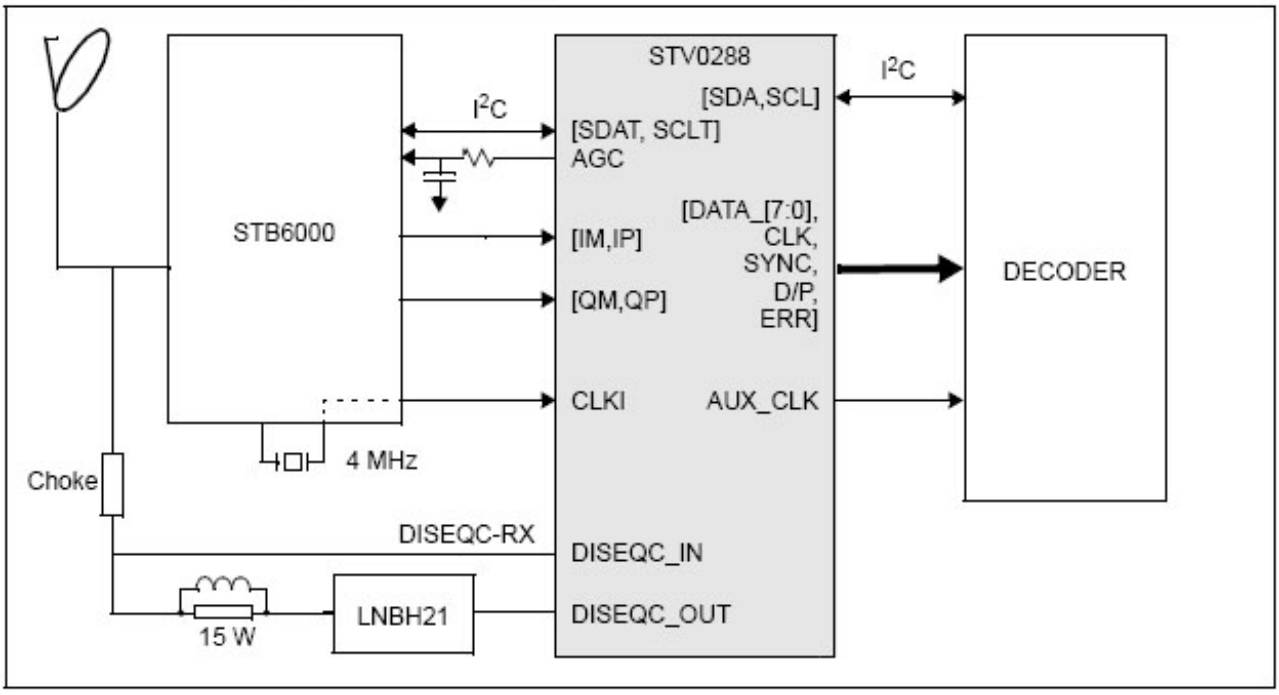
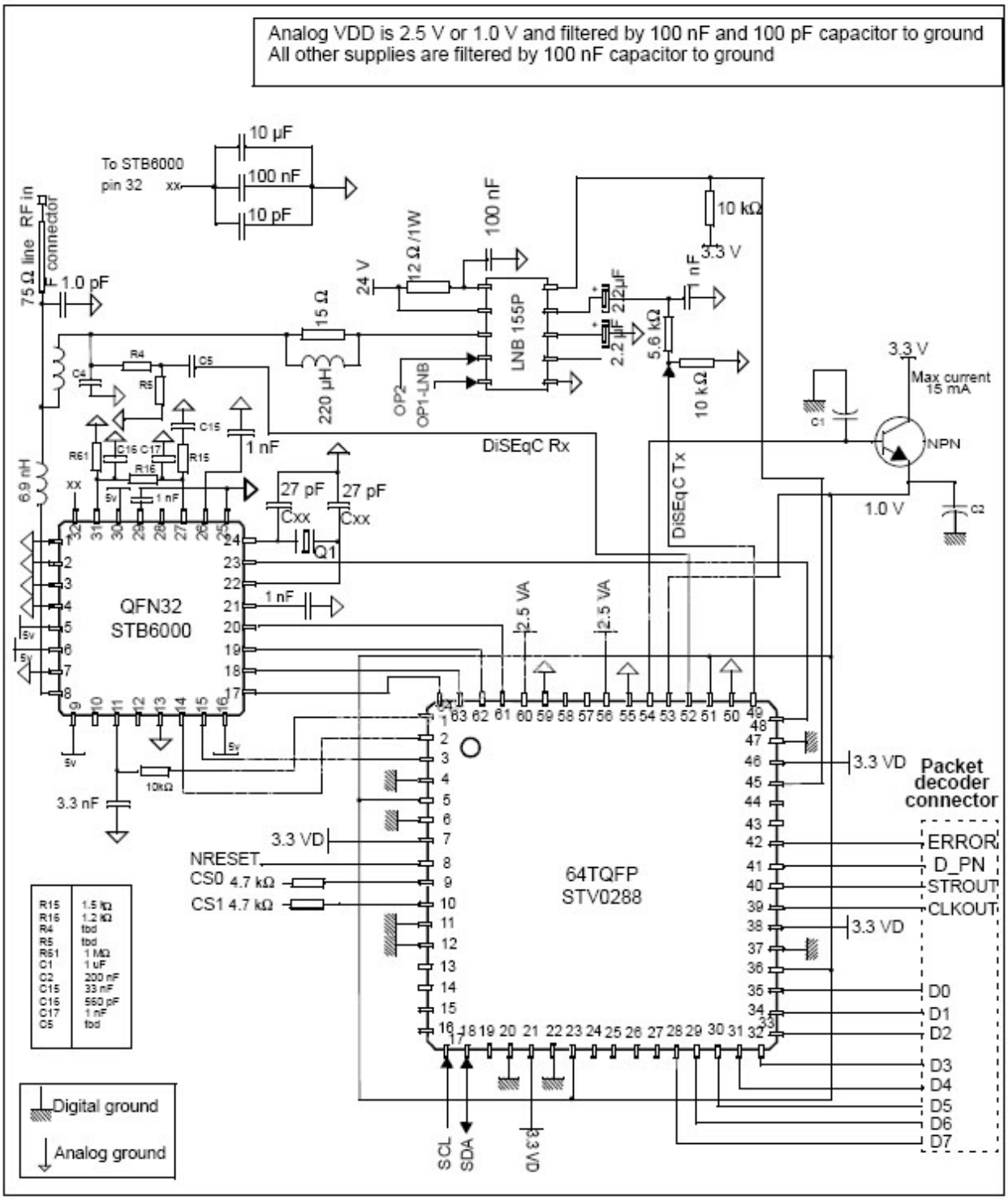
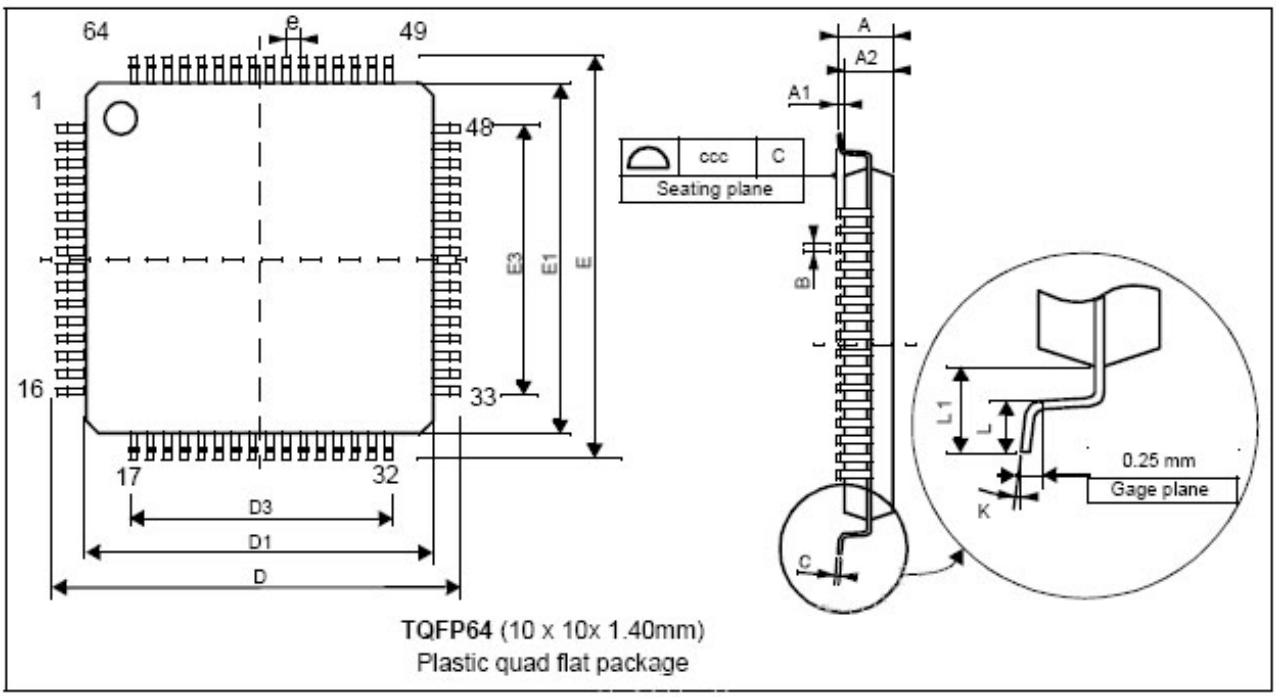


Figure 18: STV0288 typical application diagram with STB6000



14 Package mechanical data

Figure 19: STV0288 package diagram



TQFP64 (10 x 10x 1.40mm)
Plastic quad flat package

Table 7: STV0288 package dimensions

Dimensions	Millimeters		
	Min	Typical	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
B	0.17	0.22	0.27
C	0.09		0.20
D		12.00	
D1		10.00	
D3		7.50	
e		0.50	
E		12.00	
E1		10.00	
E3		7.50	
L	0.45	0.60	0.75
L1		1.00	

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marke on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademar ECOPACK specifications are available at: www.st.com.

15 Electrical characteristics

15.1 Absolute maximum rating

Table 8: Absolute maximum ratings[a]

Symbol	Parameter	Value	Unit
V_{dd_1v0}	DC supply voltage	-0.1, +2.2	V
V_{dd_2v5}	DC supply voltage	-0.25, +2.75	V
V_{dd_3v3}	DC supply voltage	-0.3, +3.63	V
V_{in}	Voltage on input pins	-0.3, $V_{dd\_3.3}$ +0.3	V
t_{oper}	Operating ambient temperature	-10, +70	°C
t_{stg}	Storage temperature	-40, +150	°C
t_j	Junction temperature	+125	°C

a. These are maximum limits. Exceeding them may result in permanent damage to the device. Operation at these limits is not intended.

15.2 Thermal data

Table 9: Thermal data

Symbol	Parameter	Maximum value	Unit
$r_{th(j-a)}$	Junction-ambient thermal resistance	21[a]	°C/W
$r_{th(j-c)}$	Junction-case thermal resistance	TBD	°C/W

a. Four-layer PCB

15.3 DC electrical characteristics

Table 10: DC electrical characteristics

Symbol	Parameter	Min	Typical	Max	Unit
Supply					
V_{dd_1v0}	Digital core supply voltage	0.9	1.0	1.1	V
V_{dd_3v3}	Digital pads supply voltage	3.0	3.3	3.6	V
V_{dda_1v0}	Analog supply voltage	0.9	1.0	1.1	V
V_{dda_2v5}	Analog supply voltage	2.25	2.5	2.75	V
I/Os					
V_{il} V_{ih}	Input logic low Input logic high	-0.5 2.0		0.8 3.6	V V
V_{ol} V_{oh}	Output logic low Output logic high	-0.5 2.4		0.3 3.6	V V
i_{lk}	Input leakage current (V_{in} = 0 V to 3.3 V)	TBD	TBD	TBD	µA
i_{ol}	Output sink current	TBD	TBD	TBD	µA

Note: The 3.3 V digital I/Os comply to the JEDEC standard JESD8b.

15.4 AC electrical characteristics

Table 11: AC electrical characteristics (Tamb = 25 °C, VDD = 1.0 V unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Unit
f_{clk_in}	CLKI or XTAL frequency	4	27	33	MHz
Idd_1.0	Current consumption (1.0 V)		TBD	100	mA
Idd_3.3	Current consumption (3.3 V)		TBD		mA
Idd_2.5	Current consumption (2.5 V)		TBD		mA
P_{max}	Maximum power			300	mW

15.5 Dual ADC 8-bit characteristics

Table 12: ADC figures

Symbol	Parameter	Min	Typical	Max	Unit
	Resolution		8		bits
DC specifications					
dle	Differential linearity error			±0.5	LSB
ilepp	Integral linearity error, peak to peak			±1	LSB
	Codes exist	Yes	Yes	Yes	
	Offset error		20		mV
	Gain error			5	%FSR
Analog input					
	Differential input voltage			2.0	Vpp
	Input common mode voltage		0.5		V_{DD_2v5}
	ADC differential input impedance		1		KΩ
	Input capacitance		TBD		pF
	Analog bandwidth			TBD	MHz
Switching performance					
	Maximum conversion rate	90	108	120	MHz
	Aperture uncertainty			2	ps rms
	Duty cycle sampling clock			55	%
Dynamic performance					
enob	Effective number of bits	7.2			bits
thd	Total harmonic distortion	TBD			dB
sinad	Signal-to-noise ratio with distortion	-45			dB
snr	Signal to noise ratio	TBD		TBD	
sfdr	Spurious free dynamic range	TBD		TBD	

16 Timing characteristics

16.1 Transport stream timing characteristics

Table 13: STV0288 transport stream timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{clk_in}	CLKI or XTAL frequency (dispersion including thermal drift and aging)	-100 ppm	30	+100 ppm	MHz
Parallel output DATA[7:0], D/P, CLK, SYNC, ERR output characteristics					
Bit CLK_POL = 0 in RS control register (0x39). Refer to Figure 20.					
t_{cksu}	DATA[7:0], D/P, SYNC, ERR stable before CLK falling edge	TBD			ns
t_{ckh}	DATA[7:0], D/P, SYNC, ERR stable after CLK falling edge	TBD			ns
Bit CLK_POL = 1 in RS control register (0x39). Refer to Figure 20.					
t_{cksu}	DATA[7:0], D/P, SYNC, ERR stable before CLK falling edge	TBD			ns
t_{ckh}	DATA[7:0], D/P, SYNC, ERR stable after CLK falling edge	TBD			ns
Serial output DATA_7, D/P, CLK, SYNC, ERR output characteristics					
Bit CLK_POL = 0 in RS control register (0x39). Refer to Figure 21.					
t_{cksu}	DATA_7, D/P, SYNC, ERR stable before CLK falling edge	TBD			ns
t_{ckh}	DATA_7, D/P, SYNC, ERR stable after CLK falling edge	TBD			ns
Bit CLK_POL = 1 in RS control register (0x39). Refer to Figure 21.					
t_{cksu}	DATA_7, D/P, SYNC, ERR stable before CLK falling edge	TBD			ns
t_{ckh}	DATA_7, D/P, SYNC, ERR stable after CLK falling edge	TBD			ns

Figure 20: Parallel output timing diagram

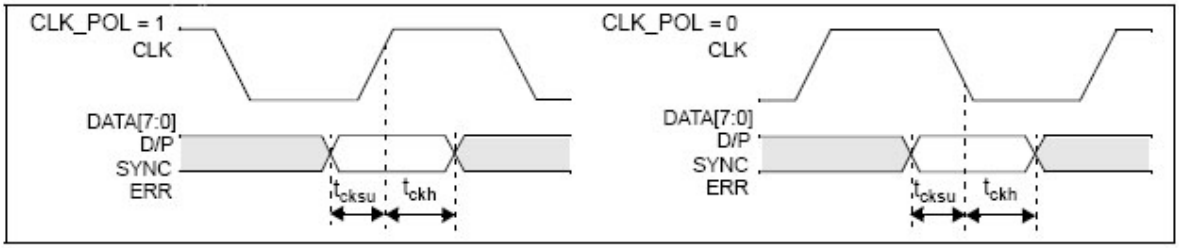
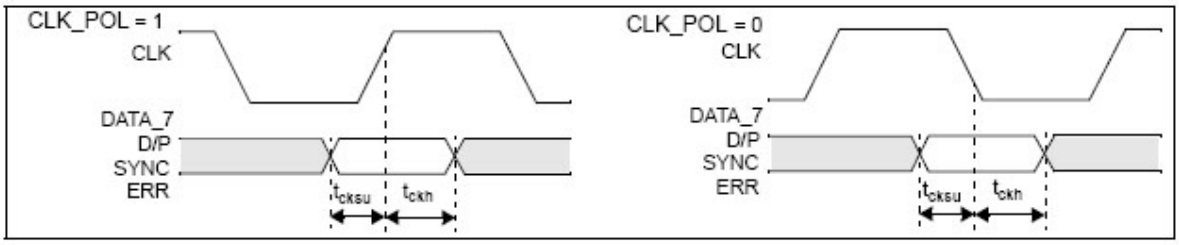


Figure 21: Serial output timing diagram



16.1.1 I²C bus characteristics

Table 14: I²C bus characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{scl}	SCL clock frequency	Normal mode	0		TBD	kHz
t_{buf}	Bus free time between a stop and start condition		1.3			µs
$t_{hd, sta}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.		0.6			µs
t_{low} t_{high}	Low period of the SCL clock High period of the SCL clock		1.3 0.6			µs µs
t_r	Rise time for SDA and SCL signals	Fast mode			300	ns
t_f	Fall time for SDA and SCL signals	Fast mode			300	ns
$t_{su, sta}$	Setup time for a repeated start condition		0.6			µs
$t_{su, sto}$	Setup time for stop condition		0.6			µs
$t_{su, dat}$	Data setup time		100			ns
t_{sp}	Pulse width of spikes to be suppressed by input filter	Fast mode	0		50	ns

Figure 22: I²C bus timing diagram