

RTFM **Timing recovery control register**

7	6	5	4	3	2	1	0
TIMING_LOOP_FREQ_MSB							

Address: 0x22

Type: Read/write

Reset:

Description: See also [Section 7.2.1: Timing control on page 19](#).[7:0] **TIMING_LOOP_FREQ_MSB**: timing frequency register MSB (signed number)**RTFL** **Timing recovery control register**

7	6	5	4	3	2	1	0
TIMING_LOOP_FREQ_LSB							

Address: 0x23

Type: Read/write

Reset:

Description: See also [Section 7.2.1: Timing control on page 19](#).[7:0] **TIMING_LOOP_FREQ_LSB**: timing frequency register LSB**SFRH** **Timing recovery control register**

7	6	5	4	3	2	1	0
SYMB_FREQ_HSB							

Address: 0x28

Type: Read/write

Reset: 0x80 (1000 0000)

Description: See also [Section 7.2.1: Timing control on page 19](#).[7:0] **SYMB_FREQ_HSB**: symbol frequency register (MSBs). The reset value corresponds to $f_{M_CLK}/2$.**SFRM** **Timing recovery control register**

7	6	5	4	3	2	1	0
SYMB_FREQ_MSB							

Address: 0x29

Type: Read/write

Reset: 0x00

Description: See also [Section 7.2.1: Timing control on page 19](#).[7:0] **SYMB_FREQ_MSB**: symbol frequency register (middle byte)

SFRL **Timing recovery control register**

7	6	5	4	3	2	1	0
SYMB_FREQ_LSB				Reserved			

Address: 0x2A

Type: Read/write

Reset: 0x00

Description: See also [Section 7.2.1: Timing control on page 19](#).[7:4] **SYMB_FREQ_LSB**: symbol frequency register (LSBs)[3:0] **Reserved**: must be programmed to zero.**STEP1** **Timing lock control register**

7	6	5	4	3	2	1	0
STEP1_MINUS				STEP1_PLUS			

Address: 0x14

Type: Read/write

Reset: 0x84 (1000 1000)

Description: [Section 7.2.3: Timing lock indicator on page 20](#).[7:4] **STEP1_MINUS**: timing lock setting register. Must be programmed to 8.[3:0] **STEP1_PLUS**: timing lock setting register. Must be programmed to 4.**TLIRM** **Timing lock control register**

7	6	5	4	3	2	1	0
TMG_LOCK							TMG_FINAL_IND_MSB

Address: 0x1E

Type: Read only

Reset:

Description: See also [Section 7.2.3: Timing lock indicator on page 20](#).[7] **TMG_LOCK**: timing lock flag.[4:0] **TMG_FINAL_IND_MSB**: timing lock indicator register (not signed)**TLIRL** **Timing lock control register**

7	6	5	4	3	2	1	0
TMG_FINAL_IND_LSB							

Address: 0x1F

Type: Read only

Reset:

Description: See also [Section 7.2.3: Timing lock indicator on page 20](#).

AGC2COEF **Post Nyquist AGC coeff control register**

7	6	5	4	3	2	1	0
							AGC2_COEFF

Address: 0x12

Type: Read/write

Reset: 0x03 (0000 0011)

Description: See also [Section 7.1.4: Nyquist root and interpolation filters on page 18](#).

[2:0] AGC2_COEFF[2:0]: gain coefficient of AGC2

AGC2REF **Post Nyquist AGC reference control register**

7	6	5	4	3	2	1	0
							AGC2_REF

Address: 0x13

Type: Read/write

Reset: 0x48(0100 1000)

Description: See also [Section 7.1.4: Nyquist root and interpolation filters on page 18](#).

[6:0] AGC2_REF[6:0]: reference value of AGC2. This parameter corresponds to m2.

AGC2IM **AGC2 and offset control register (MSB)**

7	6	5	4	3	2	1	0
							AGC2_INTEGRATOR_MSB

Address: 0x20

Type: Read/write

Reset: 0x00

Description: See also [Section 7.1.4: Nyquist root and interpolation filters on page 18](#).

[7:0] AGC2_INTEGRATOR_MSB: MSB of post Nyquist filter AGC integrator.

AGC2IL **AGC2 and offset control register (LSB)**

7	6	5	4	3	2	1	0
							AGC2_INTEGRATOR_LSB

Address: 0x21

Type: Read/write

Reset: 0x00

Description: See also [Section 7.1.4: Nyquist root and interpolation filters on page 18](#).

[7:0] AGC2_INTEGRATOR_LSB: LSB of post Nyquist filter AGC integrator.

CFD Carrier lock control register

7	6	5	4	3	2	1	0
CFD_ON	BETA_FC			FDCT		LDL	

Address: 0x15

Type: Read/write

Reset: 0xF7 (1111 0111)

Description: See also [Section 7.3.4: Carrier frequency offset detector on page 21](#).

[7] CFD_ON: carrier frequency offset detector enable
 0: disabled 1: coupled to carrier recover loop

[6:4] BETA_FC[2:0]: gain for carrier frequency offset detector

[3:2] FDCT[1:0]: time constant for carrier frequency offset detector

[1:0] LDL[1:0]: lock detector threshold to disable the carrier frequency offset detector:
 00: -16 01: -32
 10: -48 11: -64

LDI Carrier lock control register

7	6	5	4	3	2	1	0
LOCK_DET_INTEGR							

Address: 0x25

Type: Read only

Reset:

Description: See also [Section 7.3.4: Carrier frequency offset detector on page 21](#).

[7:0] LOCK_DET_INTEGR: lock detector value (signed number)

LDT Carrier lock control register

7	6	5	4	3	2	1	0
LOCK_THRESHOLD							

Address: 0x19

Type: Read/write

Reset: 0x14 (0001 0100)

Description: See also [Section 7.3.2: Carrier lock detector on page 21](#).

[7:0] LOCK_THRESHOLD: lock threshold 1 (signed number)

LDT2 Carrier lock control register

7	6	5	4	3	2	1	0
LOCK_THRESHOLD2							

Address: 0x1A

Type: Read/write

Reset: 0x00

Description: See also [Section 7.3.2: Carrier lock detector on page 21](#).

[7:0] LOCK_THRESHOLD2: lock threshold 2 (signed number)

ACLC**Carrier recovery control register**

7	6	5	4	3	2	1	0
DEROT_ON_OFF	ACLC	NOISE		ALPHA			

Address: 0x16

Type: Read/write

Reset: 0x88 (1000 1000)

Description: See also [Section 7.3.3: Derotator frequency on page 21](#).

[7] DEROT_ON_OFF: derotator on/off

0: off

1: on

[6] ACLC: a coefficient for $\alpha = (2 + a) \times 2^b \times 2^{14}$

[5:4] NOISE[1:0]: noise estimator time constant

00: 4 k symbols

01: 16 k symbols

10: 64 k symbols

11: 256 k symbols

[3:0] ALPHA[3:0]: b coefficient [3:0] for $\alpha = (2 + a) \times 2^b \times 2^{14}$ **BCLC****Carrier recovery control register**

7	6	5	4	3	2	1	0
ALGO		BETA					

Address: 0x17

Type: Read/write

Reset: 0x58 (0101 1000)

Description: See also [Section 7.3: Carrier recovery and derotator loop on page 20](#).

[7:6] ALGO[1:0]: Phase detector algorithm:

00: Algorithm 0 (BPSK application)

01: Algorithm 1 (QPSK application)

10: Algorithm 2 (QPSK application)

11: Reserved

[5:0] BETA[5:0]

Bit 1: c

Bits 5 to 2: e[3:0]

Bit 0: d

CFRM**Carrier recovery frequency (MSBs) register**

7	6	5	4	3	2	1	0
CARRIER_FREQUENCY_MSB							

Address: 0x2B

Type: Read/write

Reset:

Description: See also [Section 7.3: Carrier recovery and derotator loop on page 20](#).

[7:0] CARRIER_FREQUENCY_MSB: carrier frequency (MSB) (signed value)

CFRL Carrier recovery frequency (LSBs) register

7	6	5	4	3	2	1	0
CARRIER_FREQUENCY_LSB							

Address: 0x2C

Type: Read/write

Reset:

Description: See also [Section 7.3: Carrier recovery and derotator loop on page 20](#).

[7:0] CARRIER_FREQUENCY_LSB: carrier frequency (LSB) (signed value)

NIRM Noise indicator (MSBs) register

7	6	5	4	3	2	1	0
NOISE_IND_MSB							

Address: 0x2D

Type: Read only

Reset:

Description: See also [Section 7.4: Noise indicator on page 22](#).

[7:0] NOISE_IND_MSB: noise indicator (MSB) (not signed)

NIRL Noise indicator (LSBs) register

7	6	5	4	3	2	1	0
NOISE_IND_LSB							

Address: 0x2E

Type: Read only

Reset:

Description: See also [Section 7.4: Noise indicator on page 22](#).

[7:0] NOISE_IND_LSB: noise indicator (LSB) (not signed)

ROLLOFF Roll Off control register

7	6	5	4	3	2	1	0
Reserved				MODE_COEF	Reserved		

Address: 0x18

Type: Read/write

Reset: 0x00

Description: See also [Section 7.1.4: Nyquist root and interpolation filters on page 18](#).

[7:4] Reserved: must be set to 0.

[3] MODE_COEF: Nyquist filter
0: raised cosine at 35% (DVB)

1: raised cosine at 20% (DIRECTV System)

[2:0] Reserved

VSTATUS**Viterbi status register**

7	6	5	4	3	2	1	0
CF	Reserved		PRF	LK	PR		

Address: 0x24

Type: Read only (accessible in standby mode)

Reset: 0x00

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] CF: carrier found flag. When CF (see [Section 7.3.4: Carrier frequency offset detector on page 21](#)) is set, a QPSK signal is present at the input of the Viterbi decoder.

[6:5] **Reserved:** must be programmed to zero.

[4] PRF: puncture rate found. PRF indicates the state of the puncture rate research. 0 for searching and 1 when found. This bit is irrelevant in manual mode.

[3] LK: locked/searching sync word. LK indicates the state of the sync word search: 0 for searching and 1 when found.

[2:0] PR[2:0]: current puncture rate. The current puncture rate (CPR) bits hold the current puncture rate indices, as follows:

000: punctured 1/2

001: punctured 2/3

010: punctured 3/4

011: punctured 5/6

100: punctured 6/7

101: punctured 7/8

110: reserved

111: reserved

VEERROR**Viterbi error register**

7	6	5	4	3	2	1	0
ERROR_VAL							

Address: 0x2F

Type: Read only

Reset: 0x00

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7:0] ERROR_VAL (not signed): Number of bits corrected by the Viterbi decoder per packets of 256 bits.

FECM FEC mode register

7	6	5	4	3	2	1	0
Reserved	FECMODE[2]	FECMODE[1:0]		Reserved		SYNC	SYM

Address: 0x30

Type: Read/write

Reset: 0x00

Description: See also [Section 7.5.1: FEC modes on page 22](#).

[7] **Reserved:** must be programmed to zero.

[6] **FECMODE[2]:** This field indicates the FEC operation mode:
 0: DVB 1: DIRECTV System

[5:4] **FECMODE[1:0]:**
 00: normal IQ flow IQ/IQ/IQ/IQ 01: BPSK extension lx/lx/lx/lx
 10: reserved 11: reserved

[3:2] **Reserved:** must be programmed to zero.

[1] **SYNC:** sync disable.
 0: sync search enable. Sync is processed
 1: sync byte search disable. Bit to byte conversion is frozen in the current state

[0] **SYM:** I, Q symmetry

VITPROG Viterbi metric control register

7	6	5	4	3	2	1	0
Reserved			SWAP_ENABLE	Reserved		MDIVIDER	

Address: 0x3C

Type: Read/write

Reset: 0x00

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7:5] **Reserved:** must be programmed to zero.

[4] **SWAP_ENABLE:** allow automatic research of IQ symmetry

[3:2] **Reserved:** must be programmed to zero.

[1:0] **MDIVIDER:** Viterbi coefficient. Selects division ratio at Viterbi decoder input:
 00: divide by 4 (for PR 1/2 and 2/3) 01: divide by 1
 10: divide by 2 11: divide by 1/2 (for PR 3/4, 5/6, 6/7 and 7/8)

VTH12 Viterbi 1/2 threshold register

7	6	5	4	3	2	1	0
Reserved	VTH12						

Address: 0x31

Type: Read/write

Reset: 0x1E (0001 1110)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] **Reserved:** must be programmed to zero.

[6:0] **VTH12:** rate = 1/2 puncture rate threshold.

VTH23 Viterbi 2/3 threshold register

7	6	5	4	3	2	1	0
Reserved	VTH23						

Address: 0x32

Type: Read/write

Reset: 0x14 (0001 0100)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] Reserved: must be programmed to zero.

[6:0] VTH23: rate = 2/3 puncture rate threshold.

VTH34 Viterbi 3/4 threshold register

7	6	5	4	3	2	1	0
Reserved	VTH34						

Address: 0x33

Type: Read/write

Reset: 0x0F (0000 1111)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] Reserved: must be programmed to zero.

[6:0] VTH34: rate = 3/4 puncture rate threshold.

VTH56 Viterbi 5/6 threshold register

7	6	5	4	3	2	1	0
Reserved	VTH56						

Address: 0x34

Type: Read/write

Reset: 0x09 (0000 1001)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] Reserved: must be programmed to zero.

[6:0] VTH56: rate = 5/6 puncture rate threshold.

VTH67 Viterbi 6/7 threshold register

7	6	5	4	3	2	1	0
Reserved	VTH67						

Address: 0x35

Type: Read/write

Reset: 0x0C (0000 1100)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] Reserved: must be programmed to zero.

[6:0] VTH67: rate = 6/7 puncture rate threshold.

VTH78**Viterbi 7/8 threshold register**

7	6	5	4	3	2	1	0
Reserved	VTH78						

Address: 0x36

Type: Read/write

Reset: 0x05 (0000 0101)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).[7] **Reserved:** must be programmed to zero.[6:0] **VTH78:** rate = 7/8 puncture rate threshold.**PR****Puncture rate and sync register**

7	6	5	4	3	2	1	0
Reserved	PR_7_8	PR_6_7	PR_5_6	PR_3_4	PR_2_3	PR_1_2	

Address: 0x37

Type: Read/write

Reset: 0x1F (0001 1111)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).[7:6] **Reserved:** must be programmed to zero.[5] **PR_7_8:** enable punctured rate 7/8[4] **PR_6_7:** enable punctured rate 6/7[3] **PR_5_6:** enable punctured rate 5/6[2] **PR_3_4:** enable punctured rate 3/4[1] **PR_2_3:** enable punctured rate 2/3[0] **PR_1_2:** enable punctured rate 1/2

VSEARCH**Viterbi and sync search register**

7	6	5	4	3	2	1	0
AM	F	SN		TO		H	

Address: 0x38

Type: Read/write

Reset: 0x19 (0001 1001)

Description: See also [Section 7.5.2: Viterbi decoder and synchronization on page 22](#).

[7] **AM**

0: automatic search mode

1: manual search mode

[6] **F**: freeze

[5:4] **SN[1:0]**: this is the averaging period. The field gives the number of bits required to calculate the rate error.

00 = 1024 bits

01 = 4096 bits (reset value)

10 = 16384 bits

11 = 65536 bits

[3:2] **TO[1:0]**: time out value (given in 1024-bit periods). This is used to program the maximum duration of the sync word search in automatic mode. If no sync is found within this time, and if bit RS6 (sync enable) is set in the Reed-Solomon register, another phase or puncture rate is tried. If RS6 = 0, the time-out has no effect.

00 = 16 Kbit

01 = 32 Kbit

10 = 64 Kbit (reset value)

11 = 128 Kbit

[1:0] **H[1:0]**: This is the hysteresis value. This field is used to program the maximum value of the Sync counter. The unit is the block duration (204 bytes in DVB, 147 in DIRECTV System).

00: 16 blocks

01: 32 blocks (reset value)

10: 64 blocks

11: 128 blocks

Reed-Solomon control register

RSOUT**Reed-Solomon and output control register**

7	6	5	4	3	2	1	0
INV_DVALID	INV_DSTART	INV_DERROR	EN_STBACKEN D	ENA8_LEVEL			

Address: 0x3A

Type: Read/write

Reset: 0x00

Description: See also [Chapter 8: Output interface on page 25](#).

- [7] **INV_DVALID**: 0: normal mode 1: DVALID inverted
- [6] **INV_DSTART**: 0: normal mode 1: DSTART inverted
- [5] **INV_DERROR**: 0: normal mode 1: DERROR inverted
- [4] **EN_STBACKEND**: rate compensation mode:
0: DP/packet clock puncturing. 1: CLK_OUT/byte clock puncturing
- [3:0] **ENA8_LEVEL**: Reed-Solomon output FIFO clock division ratio, on CLK_OUT/byte clock
0000: output FIFO disable.
Parallel mode: output clock period = ENA8_LEVEL x 4 x T_{M_CLK}.
0001: 4 x T_{M_CLK} 0010: 8 x T_{M_CLK}
0011: 12 x T_{M_CLK} 0100: 16 x T_{M_CLK}
...
1110: 56 x T_{M_CLK} 1111: 60 x T_{M_CLK}
Serial mode: output clock period = (ENA8_LEVEL[3:2] + 1) x T_{M_CLK}.
0001: T_{M_CLK} 0101: 2 x T_{M_CLK}
1001: 3 x T_{M_CLK} 1101: 4 x T_{M_CLK}

ERRCTRL**Error 1 control register**

7	6	5	4	3	2	1	0
ERRMODE	Reserved	ERR_SOURCE		Reserved	RESET_CNT	NOE	

Address: 0x3B

Type: Read/write

Reset: 0x01 (0000 0001)

Description: See also [Section 7.5.3: Error monitoring on page 23](#).

- [7] **ERRMODE**: error mode
0: error rate 1: error count
- [6] **Reserved**: must be programmed to zero.
- [5:4] **ERR_SOURCE**: error source. The error sources are as follows:
00: QPSK bit errors 01: Viterbi bit errors
10: Viterbi byte errors 11: Packet errors.
- [3] **Reserved**: must be programmed to zero.
- [2] **RESET_CNT**:
0: running counter 1: counter reset
- [1:0] **NOE**: The NOE bits represent the count period in bytes (NB):
00: 2¹² bytes 01: 2¹⁴ bytes
10: 2¹⁶ bytes 11: 2¹⁸ bytes

ECNTM Error 1 count register (MSB)

7	6	5	4	3	2	1	0
ERROR_COUNT_MSB							

Address: 0x26

Type: Read only

Reset:

Description: See also [Section 7.5.3: Error monitoring on page 23](#).

[7:0] ERROR_COUNT_MSB: error count register MSB byte (not signed)

ECNTL Error 1 count register (LSB)

7	6	5	4	3	2	1	0
ERROR_COUNT_LSB							

Address: 0x27

Type: Read only

Reset:

Description: See also [Section 7.5.3: Error monitoring on page 23](#).

[7:0] ERROR_COUNT_LSB: error count register LSB byte (not signed)

ERRCTRL2 Error 2 control register

7	6	5	4	3	2	1	0
ERRMODE2	Reserved	ERR_SOURCE2	Reserved	RESET_CNT2	NOE2		

Address: 0x3D

Type: Read/write

Reset: 0x01 (0000 0001)

Description: See also [Section 7.5.3: Error monitoring on page 23](#).

[7] ERRMODE2: error mode

0: error rate

1: error count

[6] **Reserved:** must be programmed to zero.

[5:4] ERR_SOURCE2[1:0]: error source. The error sources are as follows:

00: QPSK bit errors

01: Viterbi bit errors

10: Viterbi byte errors

11: Packet errors.

[3] **Reserved:** must be programmed to zero.

[2] RESET_CNT2:

0: running counter

1: counter reset

[1:0] NOE2[1:0]: The NOE bits represent the count period in bytes (NB):

00: 2¹² bytes01: 2¹⁴ bytes10: 2¹⁶ bytes11: 2¹⁸ bytes

ECNTM2 Error 2 count register (MSBs)

7	6	5	4	3	2	1	0
ERROR_COUNT2_MSB							

Address: 0x3E

Type: Read only

Reset:

Description: See also [Section 7.5.3: Error monitoring on page 23](#).

[7:0] ERROR_COUNT2_MSB: error count register MSB byte (not signed)

ECNTL2 Error 2 count register (LSBs)

7	6	5	4	3	2	1	0
ERROR_COUNT2_LSB							

Address: 0x3F

Type: Read only

Reset:

Description: See also [Section 7.5.3: Error monitoring on page 23](#).

[7:0] ERROR_COUNT2_LSB: error count register LSB byte (not signed)

12.3 General purpose registers**I2CRPT Serial bus repeater control register**

7	6	5	4	3	2	1	0
I2CT_ON	ENARPT_LEVEL[2:0]			SCLT_DELAY	SCLT_VALUE	STOP_ENABLE	SDAT_VALUE

Address: 0x01

Type: Read/write (accessible in standby mode)

Reset: 0x57

Description: See also [Section 4.6: I2C bus repeater on page 11](#).

[7] I2CT_ON: when high, repeater line is turned on.

[6:4] ENARPT_LEVEL[2:0]: value of delay to apply to sdat line.
 001: 128 internal sampling clock delay (90 MHz line) 010:64
 011: 32 100:16
 101: 8 110: 4
 111: 2

[3] SCLT_DELAY: when high, the delay feature is turned also on SCLT line, with the same ENARPTLEVEL delay as SDAT one.

[2] SCLT_VALUE: force SCLT value I2CT_ON must be off.

[1] STOP_ENABLE: STOP condition is turned on repeater line.

[0] SDAT_VALUE: force sdat_value, I2CT_ON must be off.

ACR Auxiliary clock register

7	6	5	4	3	2	1	0
PRESCALER				DIVIDER			

Address: 0x02

Type: Read/write

Reset: 0x2A (0010 1010)

Description: See also [Section 5.1.2: Clock registers on page 13](#).

[7:0] ACR prescaler and divider

This register is made up of the ACR [7:5] prescaler field and the ACR [4:0] divider field. The values in these fields configure the auxiliary clock function, the prescaler value, the clock signal frequency.

The frequency range is given for $f_{M_CLK} = 150$ MHz.

ACR[7:0]	FunctionPrescalerSignal FrequencyRange
000X XXX0	Output PortN/Aoutput port = 0N/A
000X XXX1	Output PortN/Aoutput port = 1N/A
001X XXXX	HF generator $f_{M_CLK}/2/ACR[4:0]$ 2.3 to 75 MHz
010X XXXX	LF generator $64f_{M_CLK}/2048/(32+ACR[4:0])$ 2.3 to 1.16 kHz
011X XXXX	LF generator $128f_{M_CLK}/4096/(32+ACR[4:0])$ 580 to 1150 Hz
100X XXXX	LF generator $256f_{M_CLK}/8192/(32+ACR[4:0])$ 290 to 572 Hz
101X XXXX	LF generator $512f_{M_CLK}/16384/(32+ACR[4:0])$ 145 to 286 Hz
110X XXXX	LF generator $1024f_{M_CLK}/32768/(32+ACR[4:0])$ 72 to 143 Hz
111X XXXX	LF generator $2048f_{M_CLK}/65536/(32+ACR[4:0])$ 36 to 71 Hz

In the LF generator, the programmable division factor is $32 + ACR[4:0]$. In the HF generator, it is simply $ACR[4:0]$. This allows the building of any frequency from 24 Hz to 1.1 kHz (within $\pm 1.5\%$) in the full operating range. The output signal is square in all cases. When the auxiliary register is written, the prescaler and the programmable divider are reset.

DACR1 DAC register (MSB)

7	6	5	4	3	2	1	0
DACMODE			Reserved	DACMSB			

Address: 0x1B

Type: Read/write (accessible in standby mode)

Reset: 0x00

Description: See also [Section 4.7: General purpose DAC on page 11](#).

[7:5] DACMODE: This field controls the DAC:

- 000: Functions as output port. DAC permanently outputs 0.
- 001: Functions as output port. DAC permanently outputs 1.
- 010: High impedance mode.
- 100: Functions as DAC. Duty cycle modulated at $f_{M_CLK}/16$.
- 101: Functions as DAC. Duty cycle modulated at $f_{M_CLK}/4$.
- 110: Functions as DAC. Duty cycle modulated at f_{M_CLK} .
- Other: Reserved functions.

[4] Reserved: This bit must be programmed to zero.

[3:0] DACMSB: 4 MSBs

DACR2 DAC register (LSB)

7	6	5	4	3	2	1	0
DACLSB							

Address: 0x1C

Type: Read/write (accessible in standby mode)

Reset: 0x00

Description: See also [Section 4.7: General purpose DAC on page 11](#).

[7:0] DACLSB: 8 LSBs

PLLCTRL Analog PLL divider control register

7	6	5	4	3	2	1	0
PLL_DIV							

Address: 0x40

Type: Read/write (accessible in standby mode)

Reset: 0x00

Description: See also [Section 5.1.1: Internal clock generation on page 12](#).
$$f_{pll} = f_{xtal} \times (PLL_DIV)/4 \text{ or } f_{pll} = f_{clk_i} \times (PLL_DIV)/4 \text{ when } PLL_SELRATIO = 1$$

$$f_{pll} = f_{xtal} \times (PLL_DIV)/6 \text{ or } f_{pll} = f_{clk_i} \times (PLL_DIV)/6 \text{ when } PLL_SELRATIO = 0$$
SYNTCTRL Frequency synthesis control register

7	6	5	4	3	2	1	0
STANDBY	Reserved		PLL_STOP	SEL_OSCI	PLL_SELRATIO	Reserved	BYPASS_PLL

Address: 0x41

Type: Read/write (accessible in standby mode)

Reset: 0x08

Description: See also [Figure 4: Clock signal generation on page 13](#).

[7] **STANDBY**: stop all clocks except I2C clock.
0: device active 1: device in standby

[6:5] **Reserved**: must be set to 0

[4] **PLL_STOP**: set PLL in standby
0: PLL active 1: PLL in standby mode

[3] **SEL_OSCI**: select OSCI cell or notT
0: clock input from clk_i 1: clock input from xtal

[2] **PLL_SELRATIO**: choice of divider ration in PLL
see PLLCTRL description

[1] **Reserved**: must be set to 0

[0] **BYPASS_PLL**: bypass pll
0: internal clock generated by PLL 1: internal clock coming from xtal or clk_i