

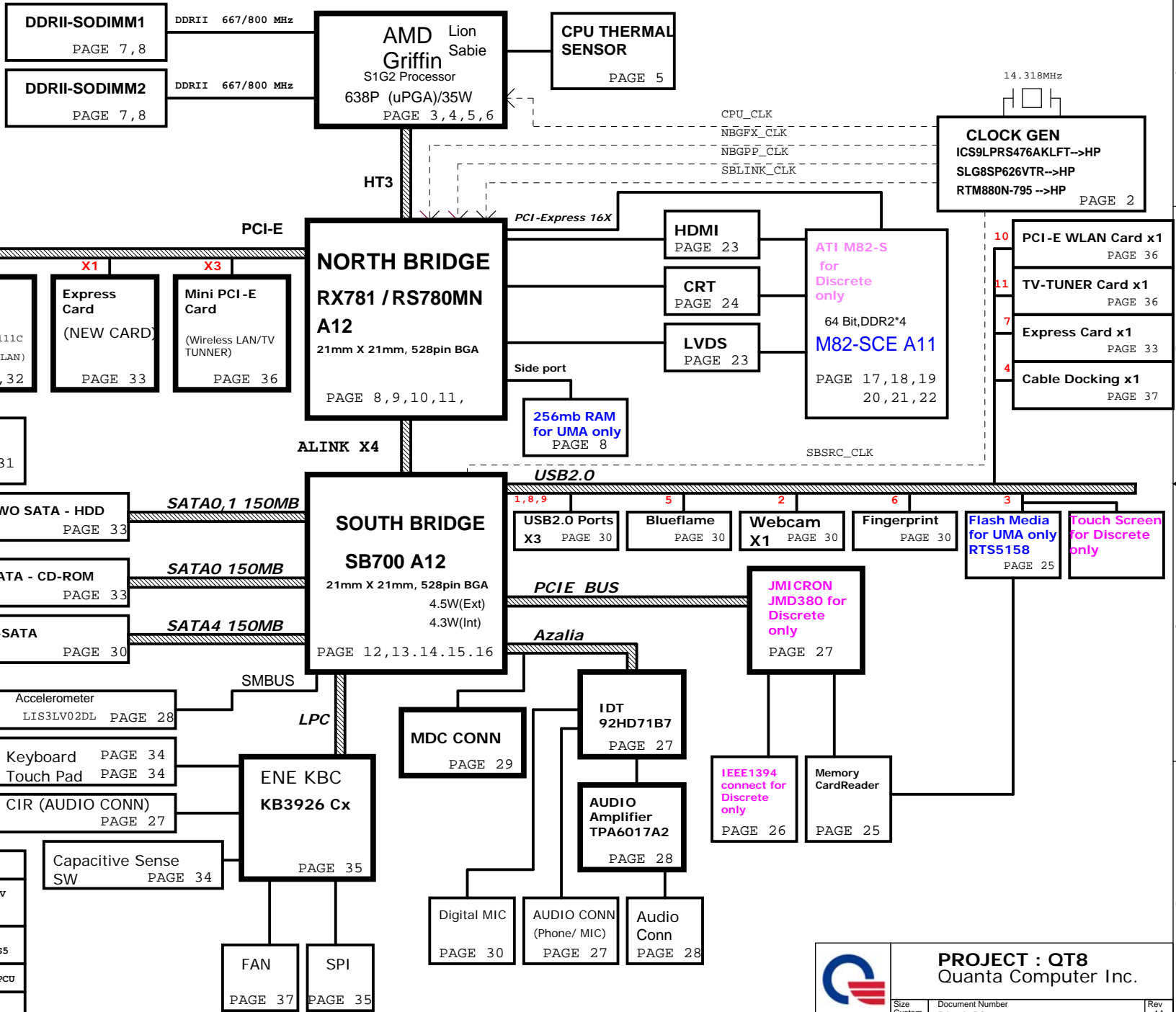
QT8 SYSTEM DIAGRAM



01

PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : IN1
 LAYER 3 : IN2
 LAYER 4 : VCC
 LAYER 5 : IN3
 LAYER 6 : BOT



Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 37

SYSTEM CHARGER(ISL6251A)
PAGE 44

SYSTEM POWER ISL6236IRZA-T
PAGE 38

DDR II SMD DR_VTERM
1.8V/1.8VSUS(TPS51116REGR)
PAGE 41

VCCP +1.1V AND +1.2V(MAX8717)
PAGE 39

VGACORE(1.1V~1.2V)Oz8118
PAGE 42

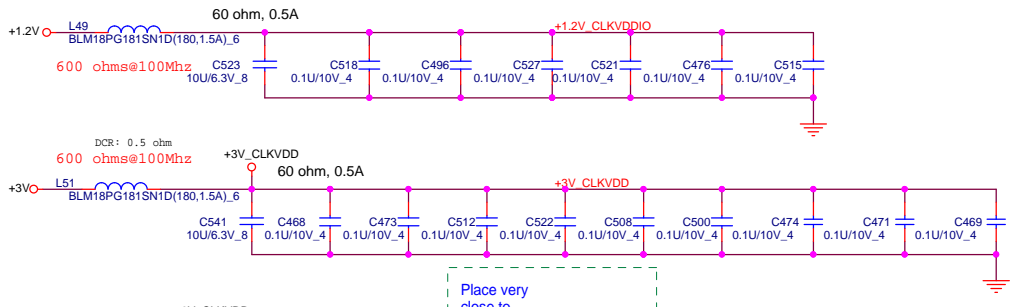
CPU CORE ISL6265A
PAGE 40

SMBUS TABLE

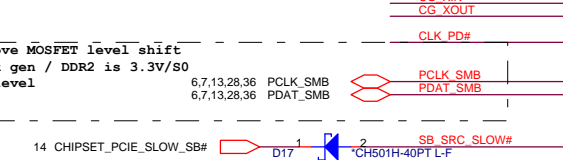
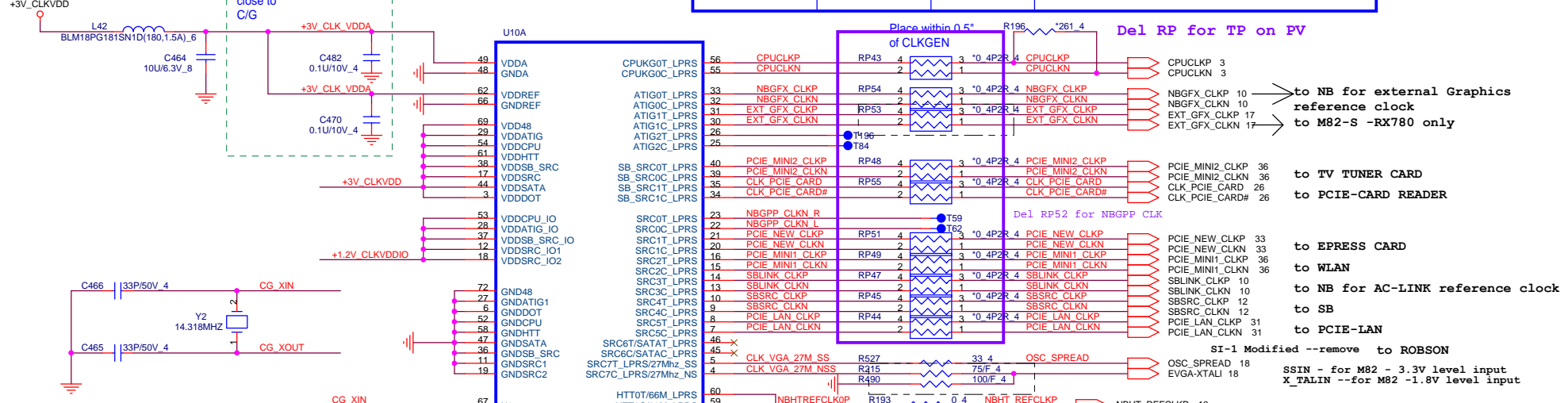
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	+3VS5
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

PROJECT : QT8
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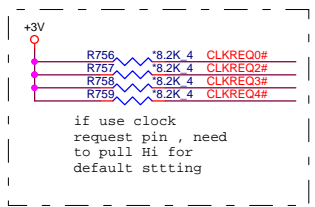
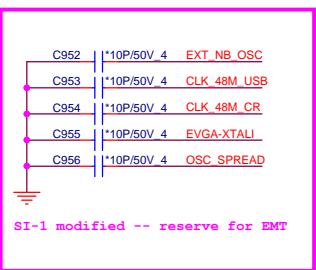
Size Custom Document Number Block Diagram Rev 1A
 Date: Tuesday, February 19, 2008 Sheet 1 of 45



CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT GFX_CLKP EXT GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGP_P_CLKP NBGP_P_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653, R656, R612 STUFF	R653, R656, R612 NC	To M82-S 27MHz - RX780 only



when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

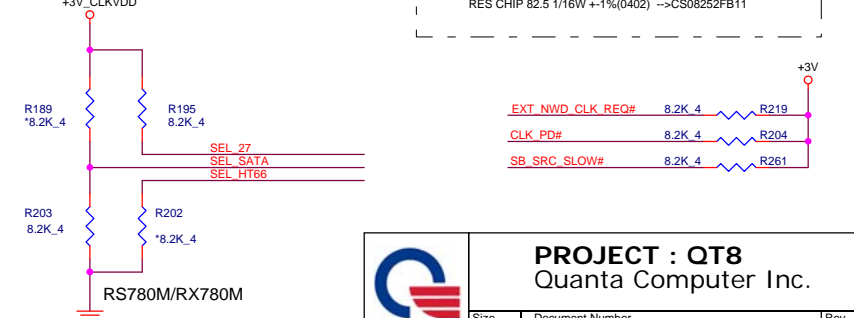
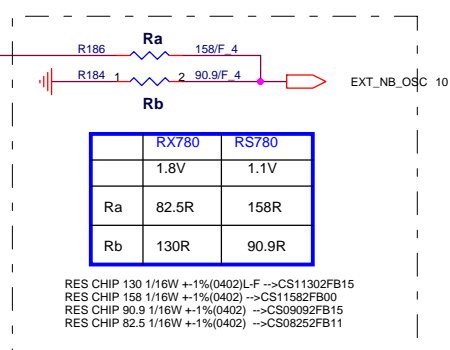


ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

* default	
SEL_HTT66	1
SEL_SATA	1
SEL_27	1

1	66 MHz 3.3V single ended HTT clock
0*	100 MHz differential HTT clock
1	100 MHz non-spreading differential SRC clock
0*	100 MHz spreading differential SRC clock
1*	27MHz non-spreading singled clock
0	100 MHz spreading differential SRC clock

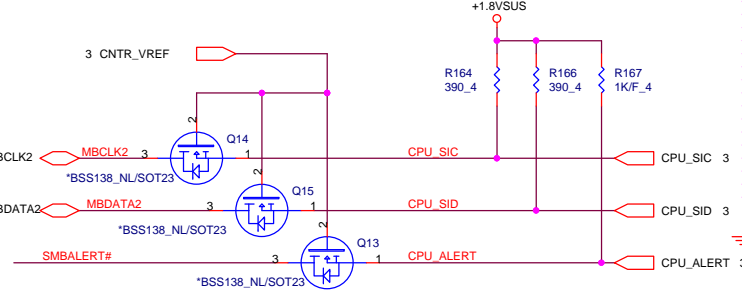
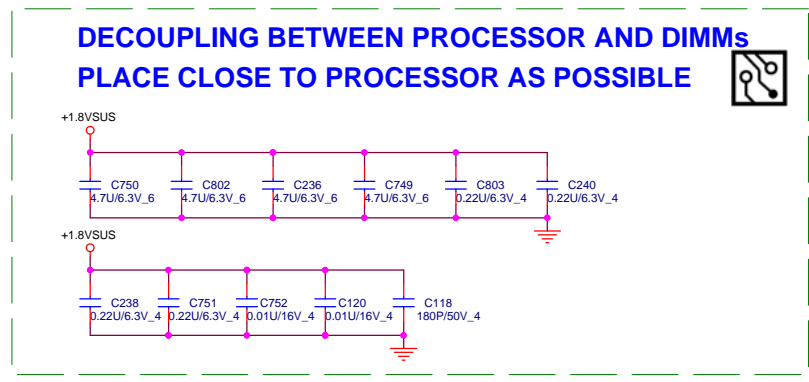
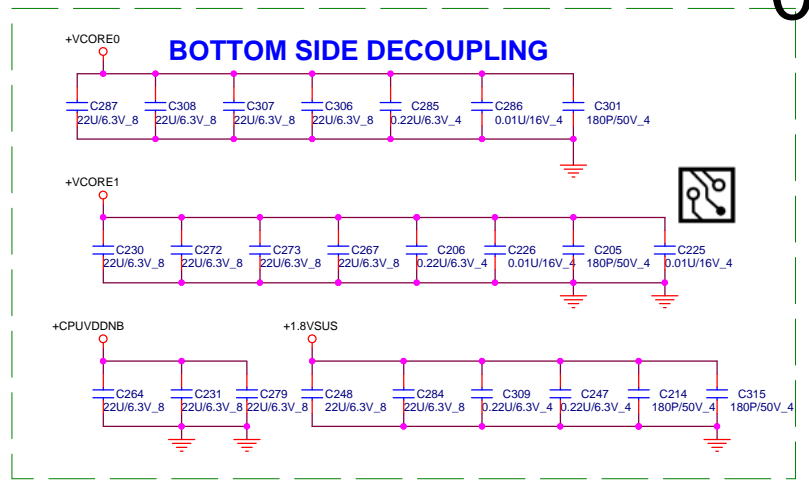
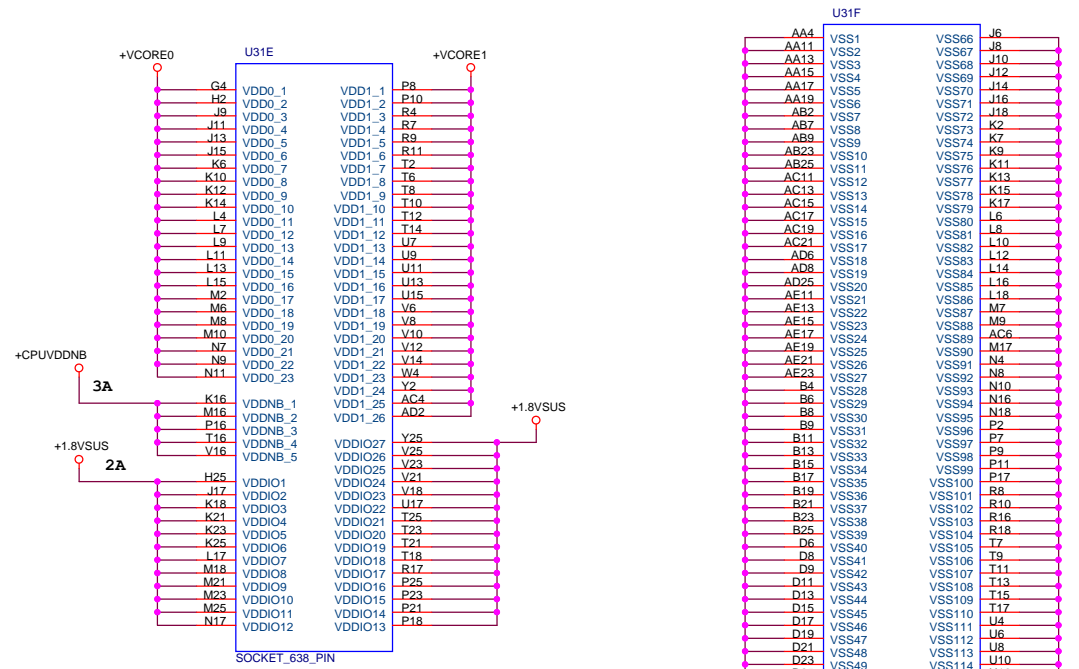
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



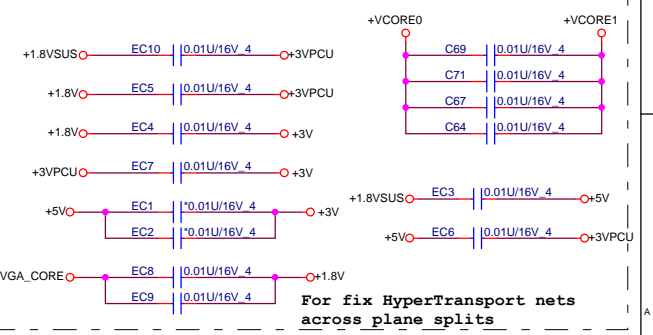
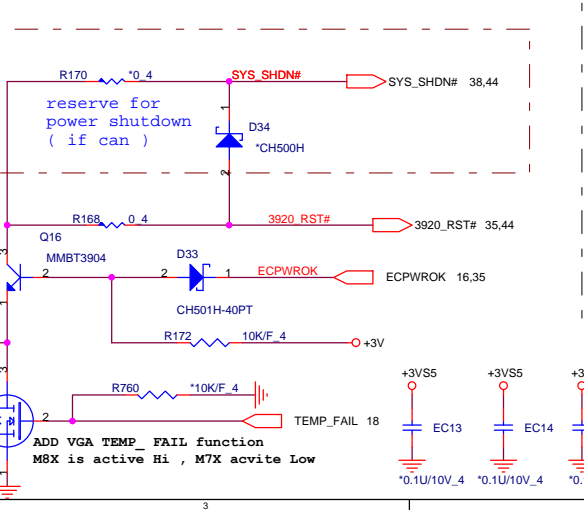
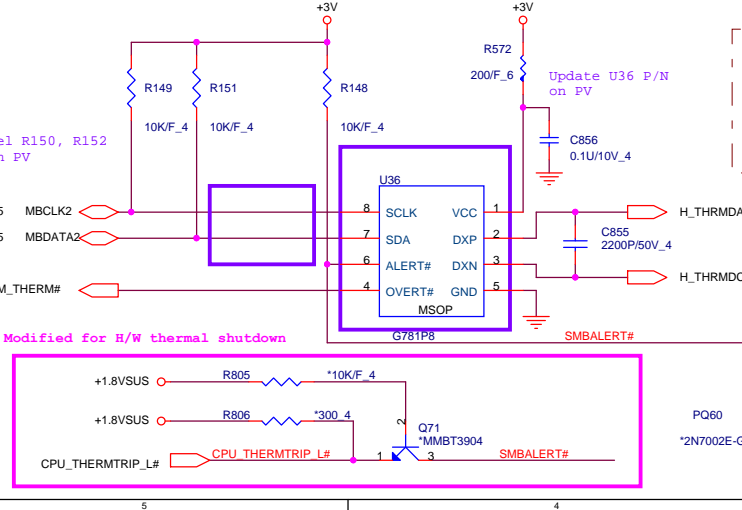
PROJECT : QT8

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Size Custom	Document Number	Rev 1A
	Clock Generator	
Date: Tuesday, February 19, 2008	Sheet 2 of 45	

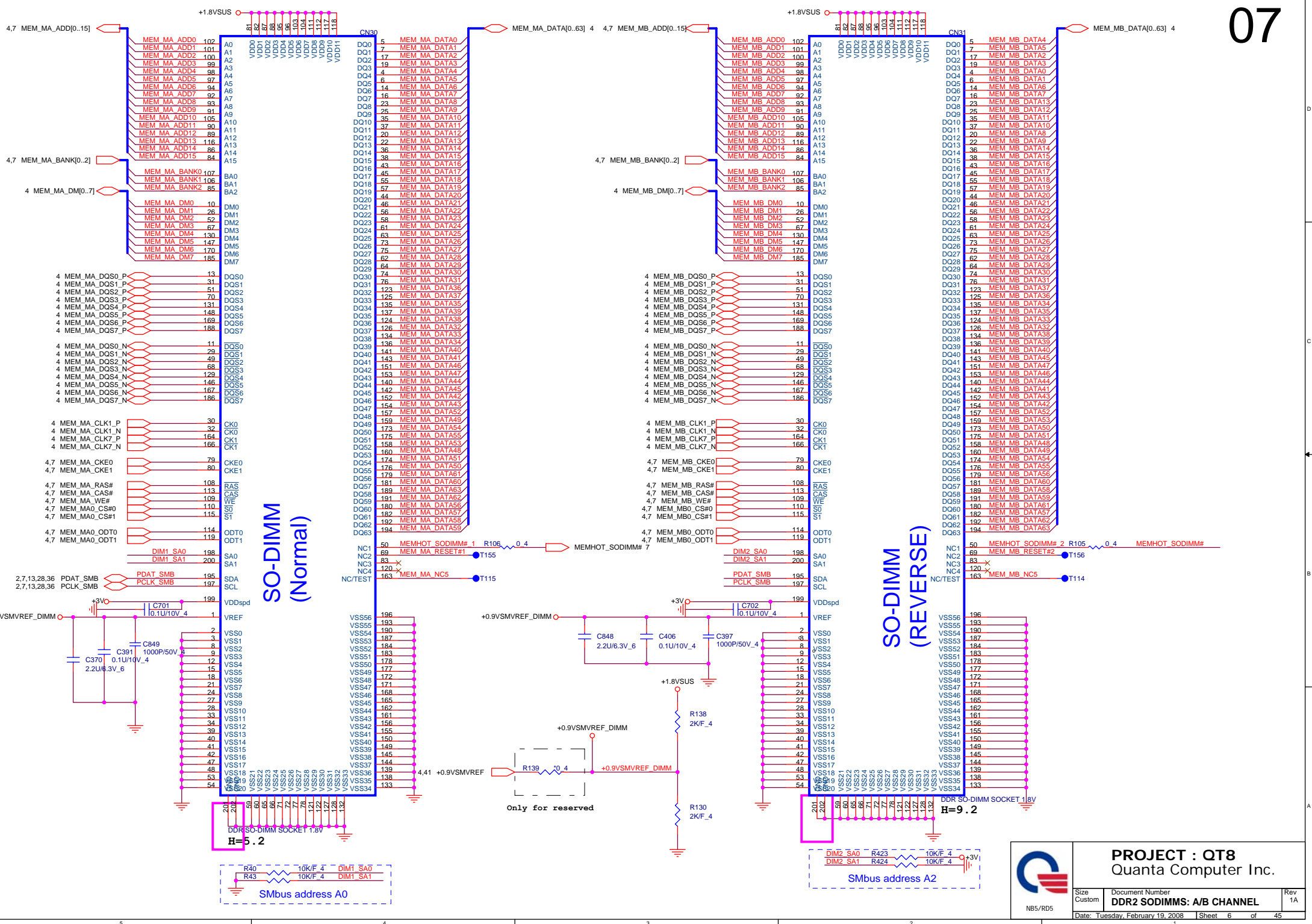


PROCESSOR POWER AND GROUND



PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	SIG2 PWR & GND 3/3	
Date: Tuesday, February 19, 2008		Sheet 5 of 45



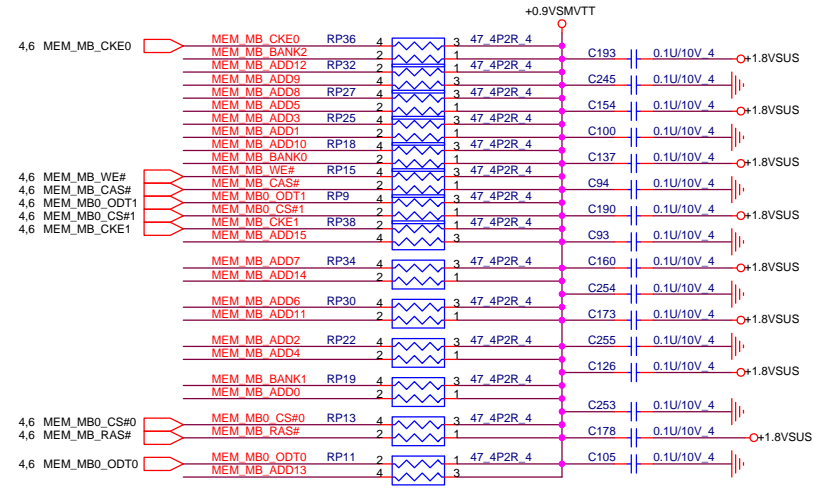
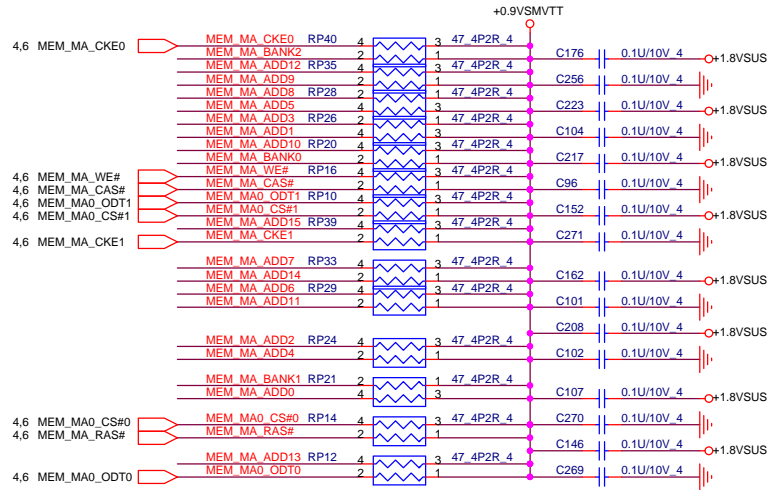
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number **DDR2 SODIMMS: A/B CHANNEL** Rev 1A
 Date: Tuesday, February 19, 2008 Sheet 6 of 45

NB5/RD5

4,6 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

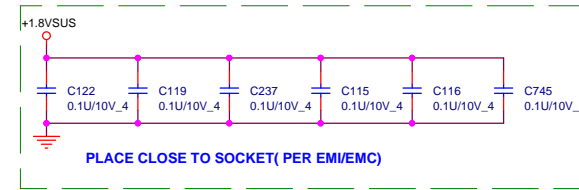
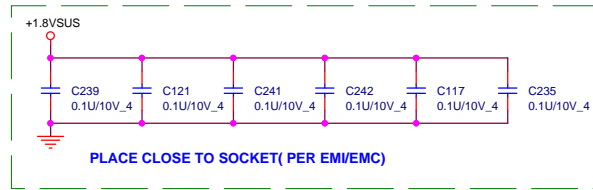
4,6 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]



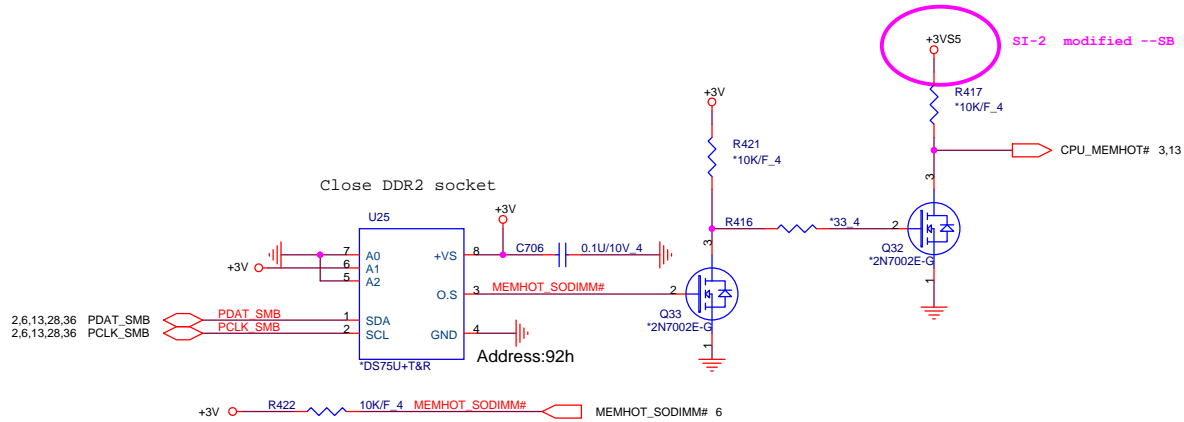
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



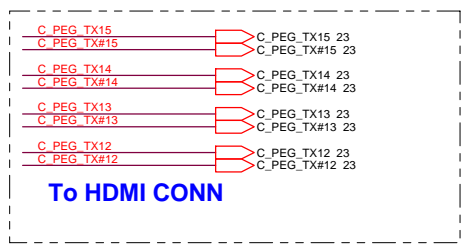
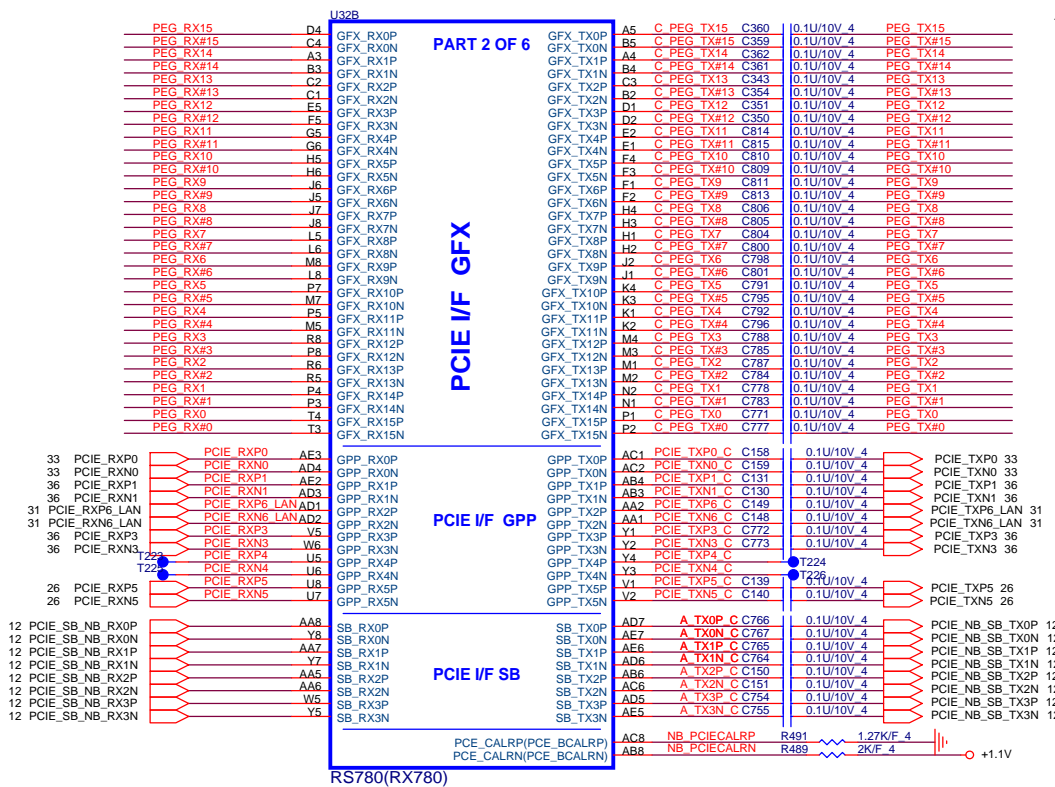
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



SI-2 modified --SB internal pull HI to 3vs5



	PROJECT : QT8 Quanta Computer Inc.	
	Size Custom	Document Number DDR2 SODIMMS TERMINATIONS
NB5/RD5	Date: Tuesday, February 19, 2008	Rev 1A
	Sheet 7 of 45	



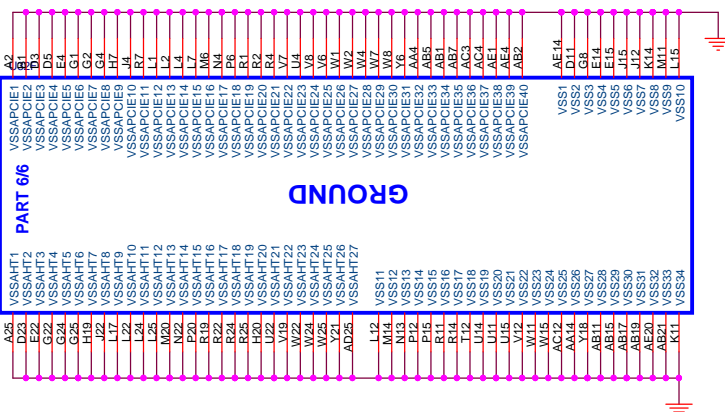
- TO EXPRESS CARD
- TO WLAN
- TO PCIE-LAN
- TO TV TUNNER
- TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

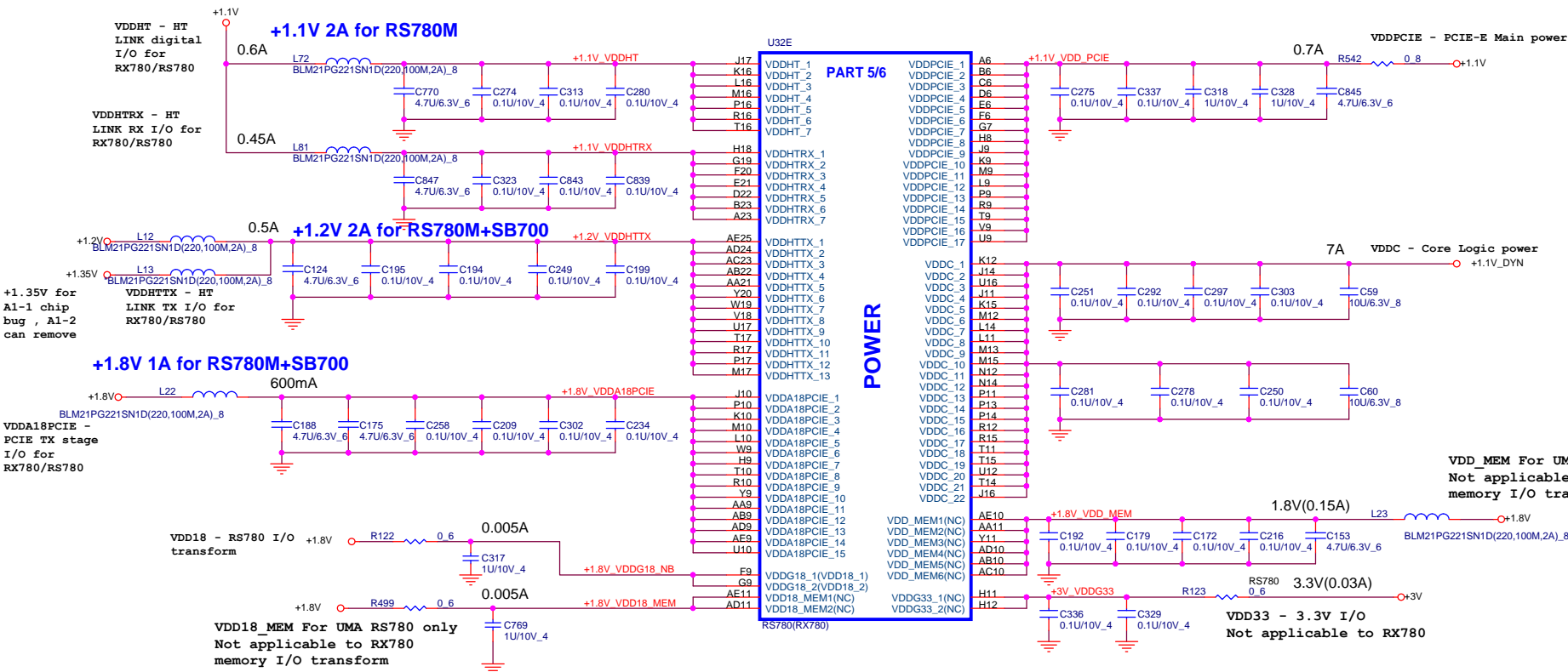
RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC

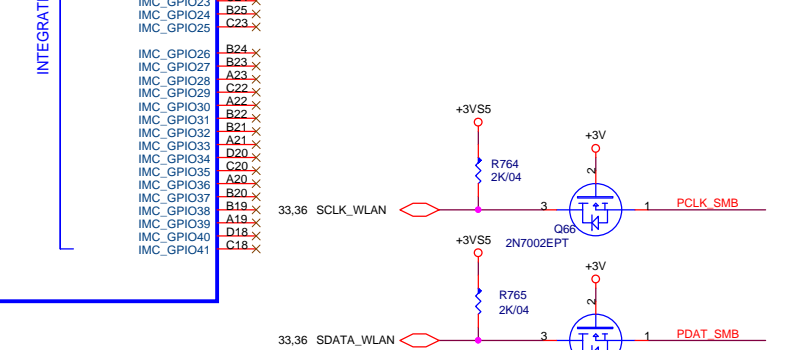
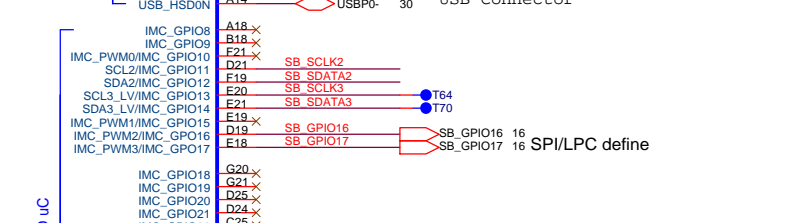
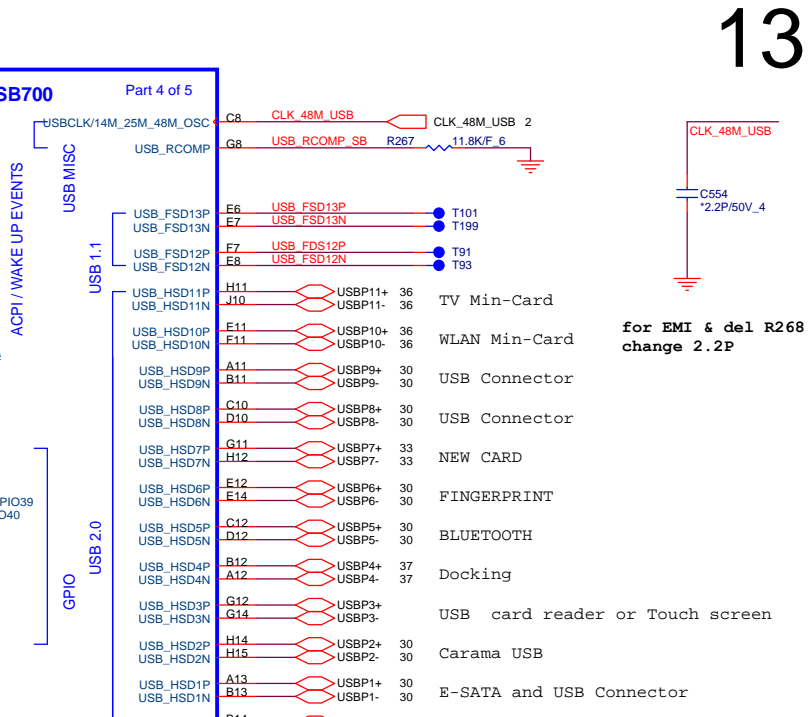
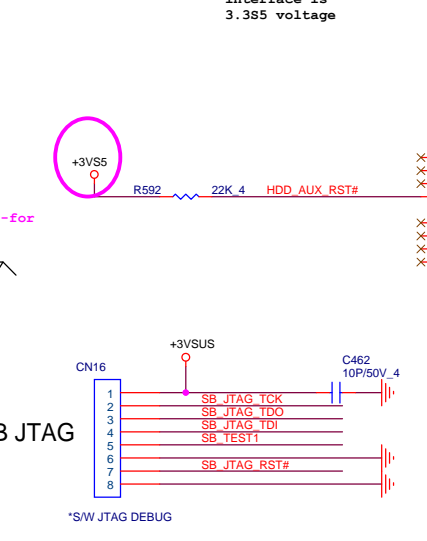
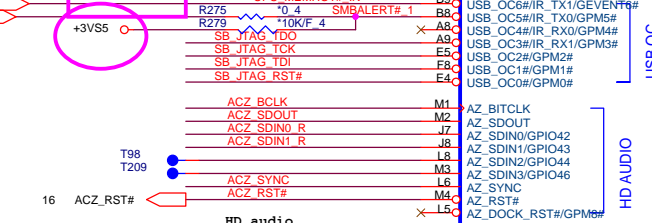
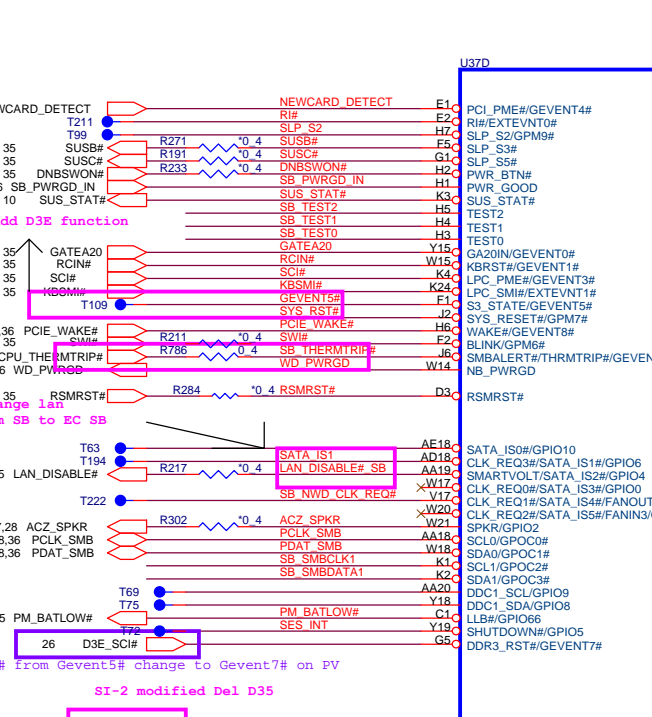
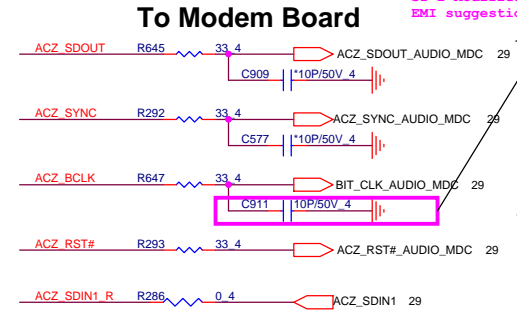
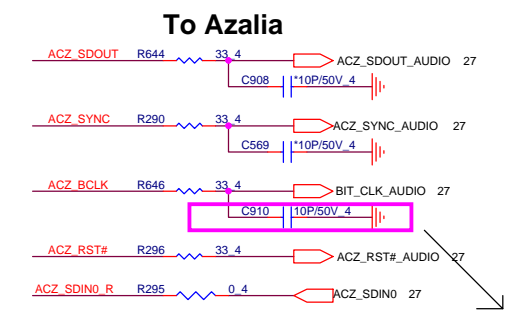
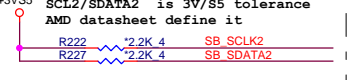
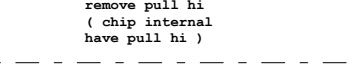
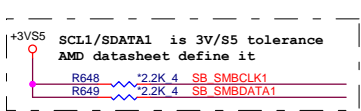
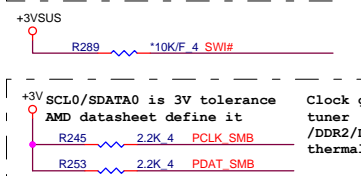
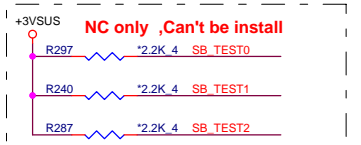


VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

VDD33 - 3.3V I/O
Not applicable to RX780



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for EMI & del R268 change 2.2P

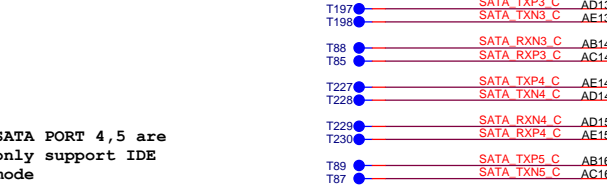
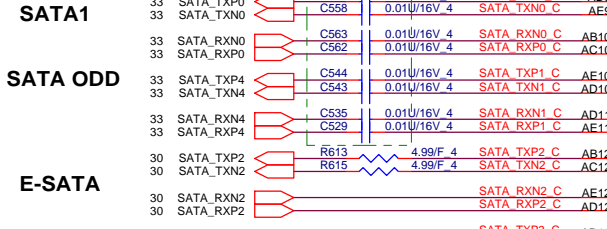
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number **SB700-ACPI/GPIO/USB 2/4** Rev 1A

Date: Tuesday, February 19, 2008 Sheet 13 of 45

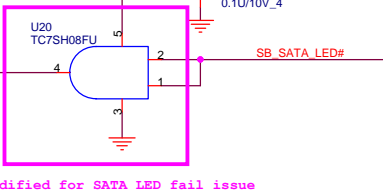
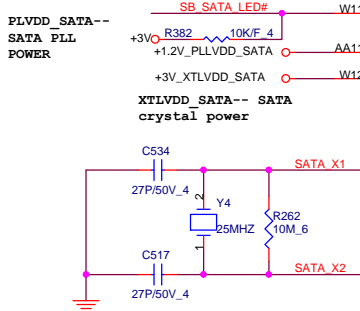
SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

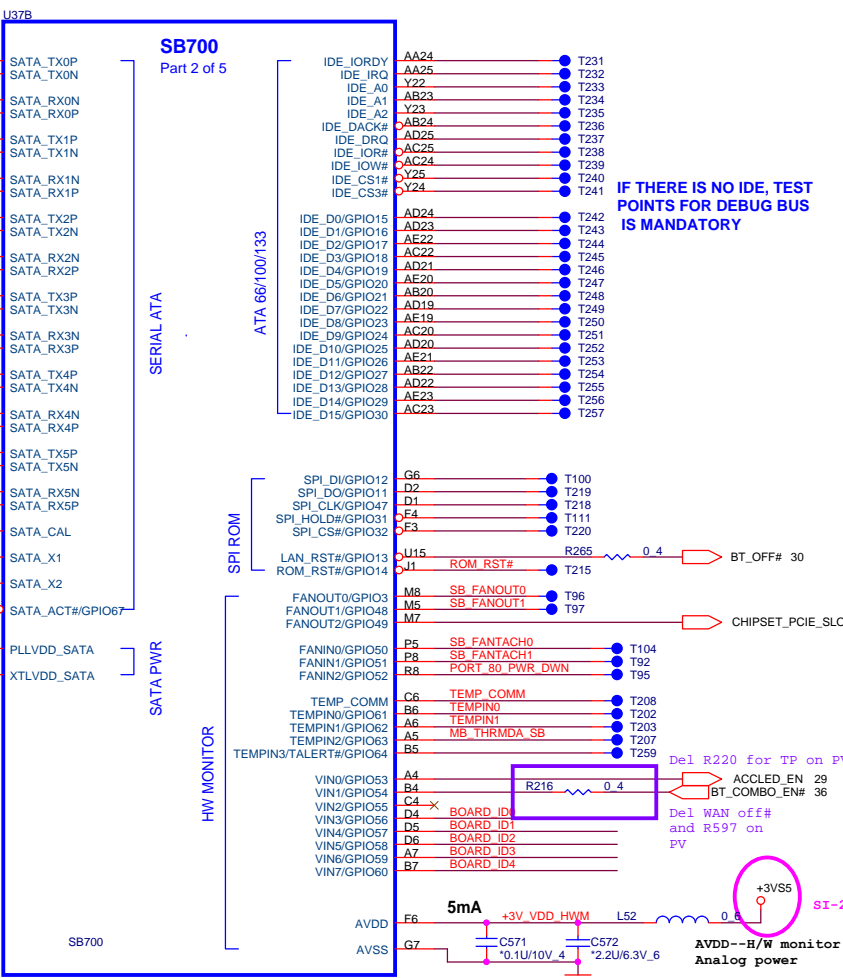
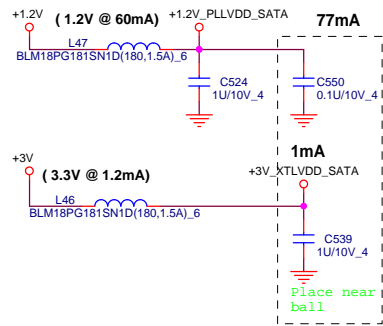


SATA PORT 4,5 are
only support IDE
mode

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

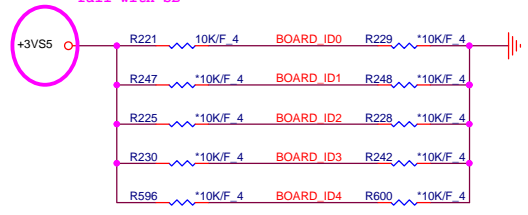


SI-2 modified for SATA LED fail issue



IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SI-2 modified -- SB
internal pull Hi to 3V5S
, modified to same power
rail with SB



SI-2 modified -- for fix +3V power leakage in S5 mode

ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	



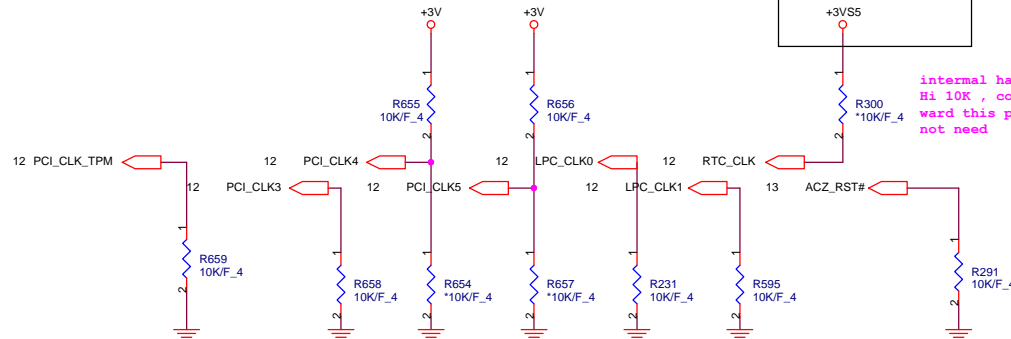
PROJECT : QT8
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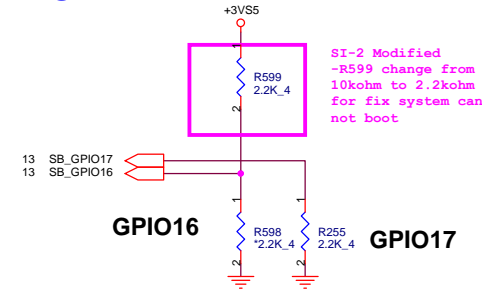
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



internal have pull Hi 10K , confirm AMD ward this pull Hi not need



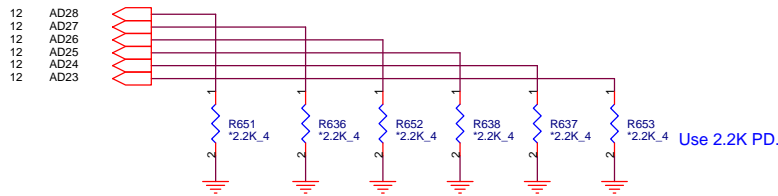
SI-2 Modified -R599 change from 10kohm to 2.2kohm for fix system can not boot

	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

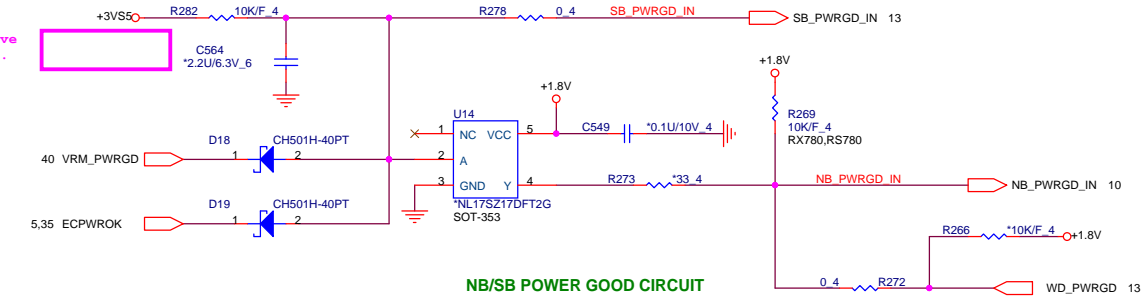
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN: RS780/RX780 = 1.8V; RS740 = 3.3V Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff



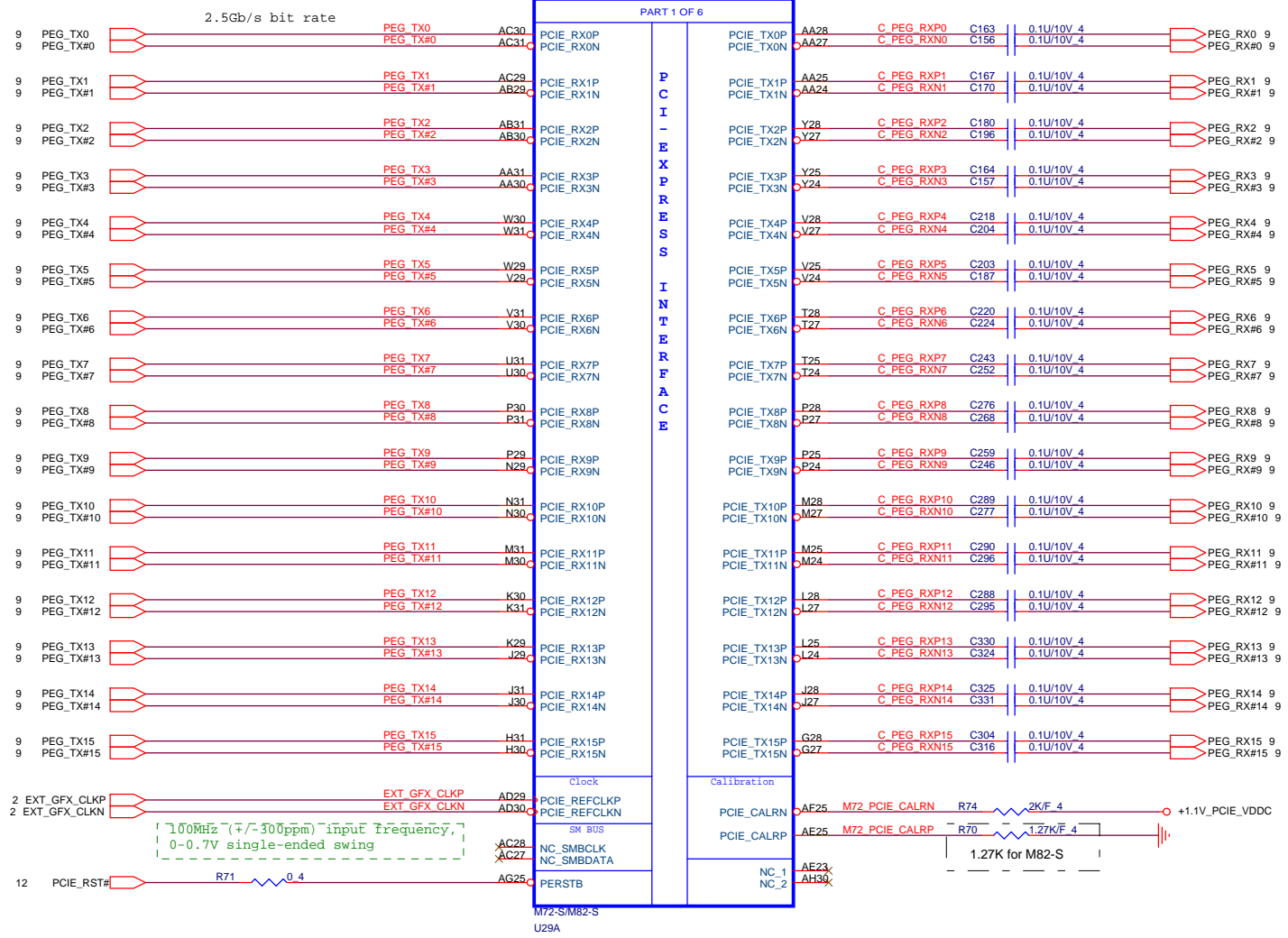
NB/SB POWER GOOD CIRCUIT

AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



PROJECT : QT8
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IC CTRL (632P) 216-0707001-00 (BGA)
VGA P/N : AJ070700T00

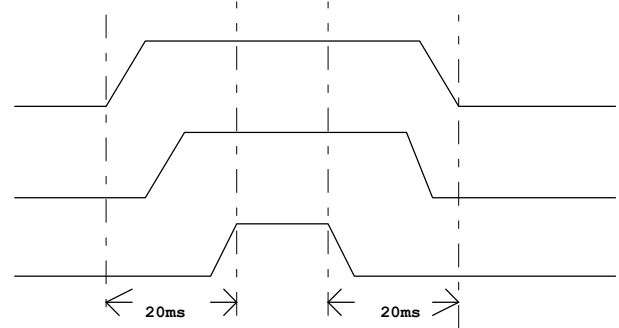


POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S

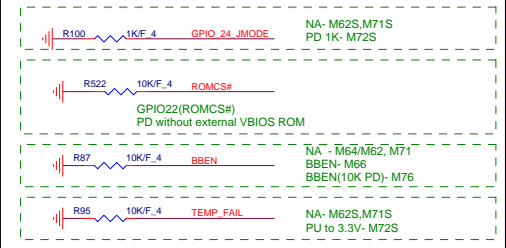
VGA Core BPP
VGA Core VDDC

+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1

3.3V_Delay VDDR3



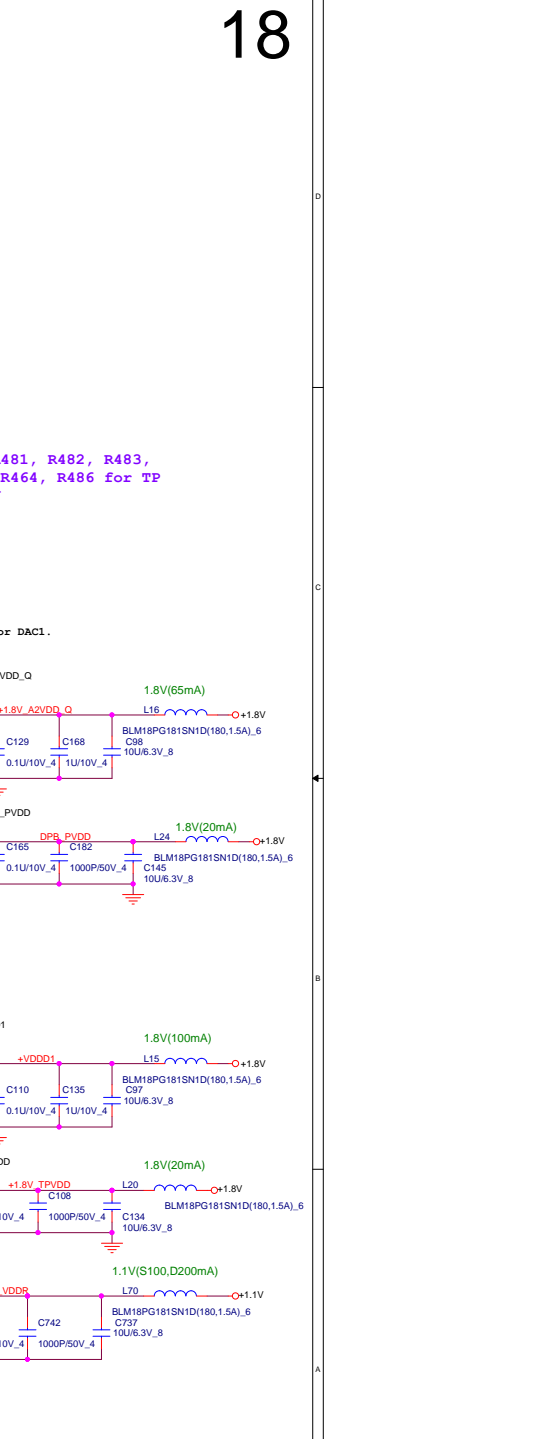
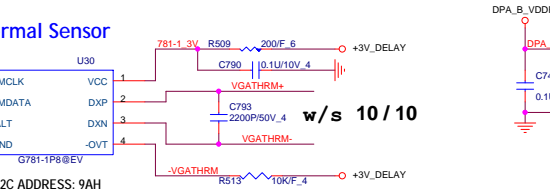
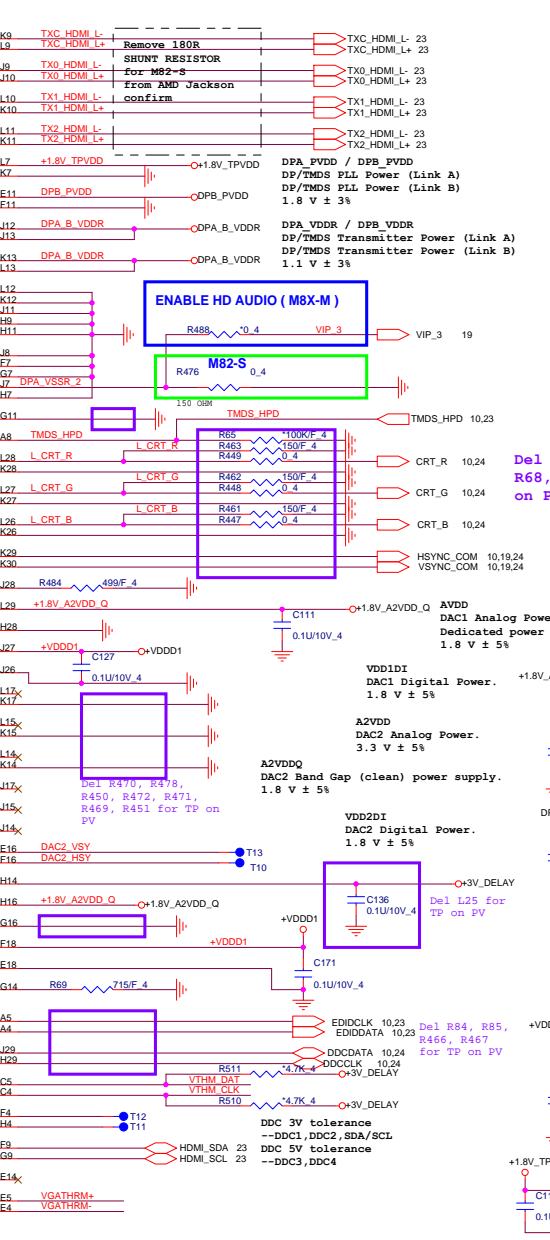
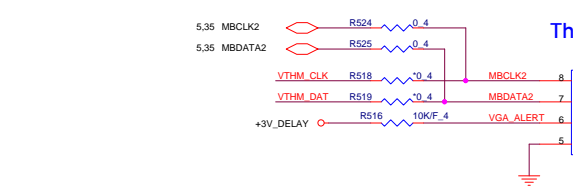
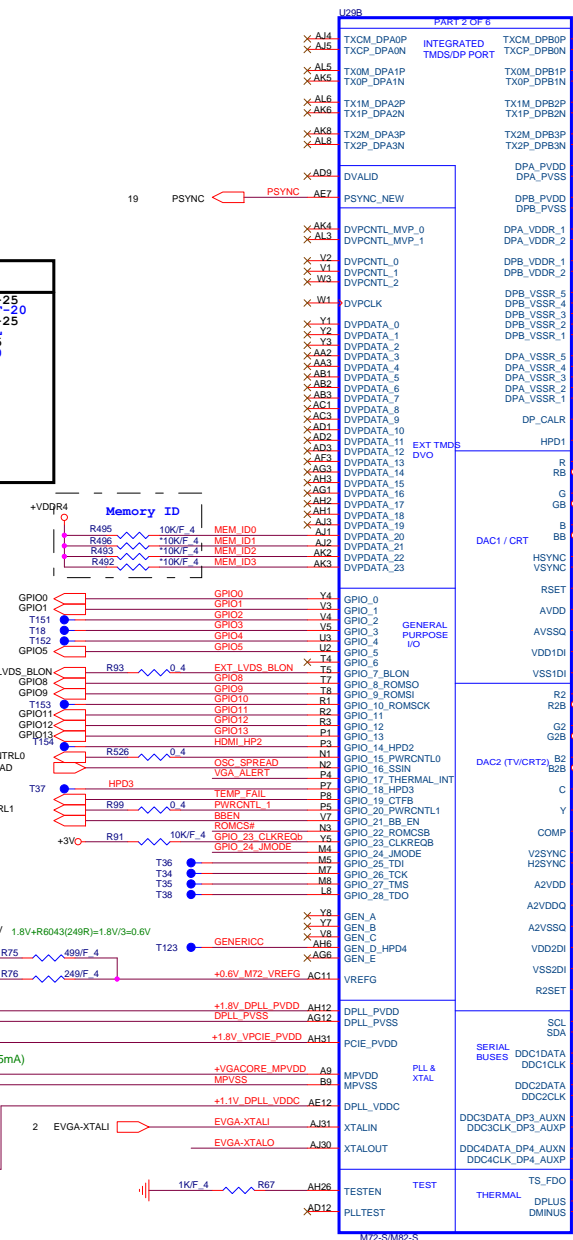
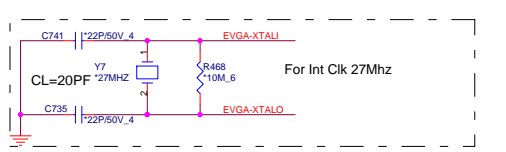
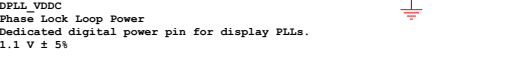
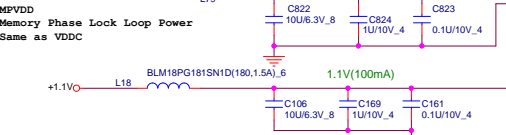
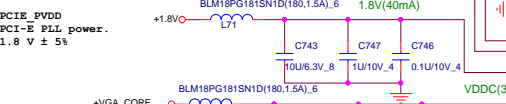
PROJECT : QT8
Quantia Computer Inc.

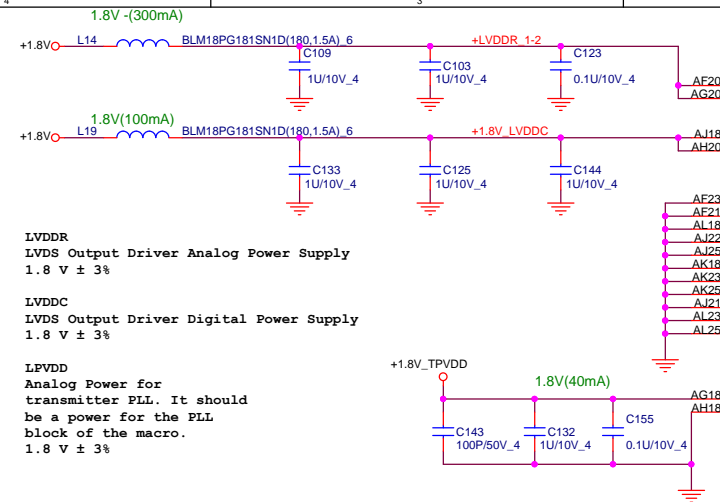
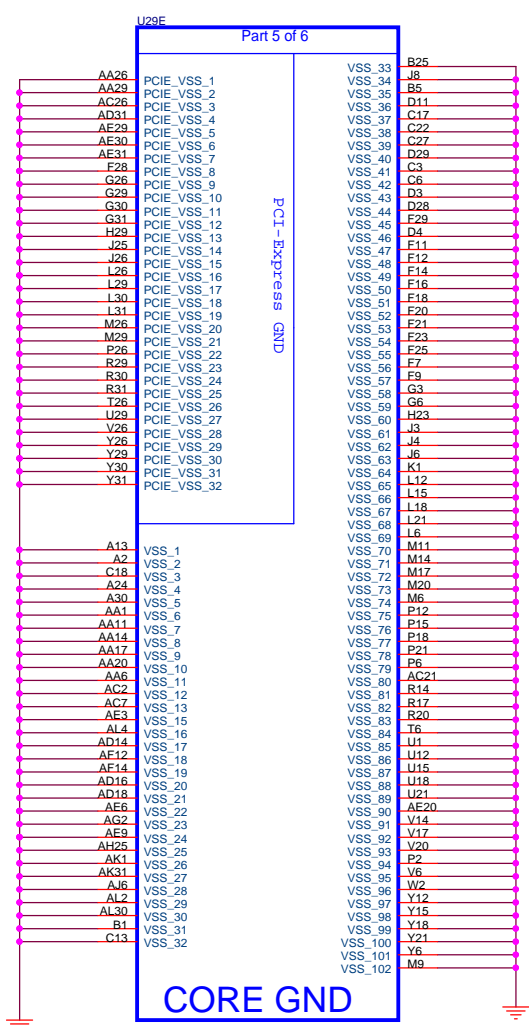


MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161B2F-20
0010	Hynix	16*16	HY5PS56162IAFP-25
0011	Hynix	32*16-500MHZ	HY5PS162IFR-20
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-RC20
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP	V-CORE
L	0		
H	1		+1.8V





LVDDR
LVDS Output Driver Analog Power Supply
1.8 V ± 3%

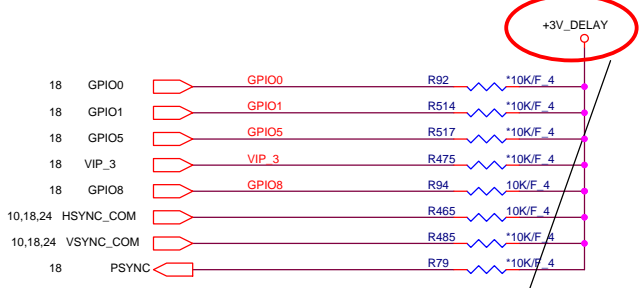
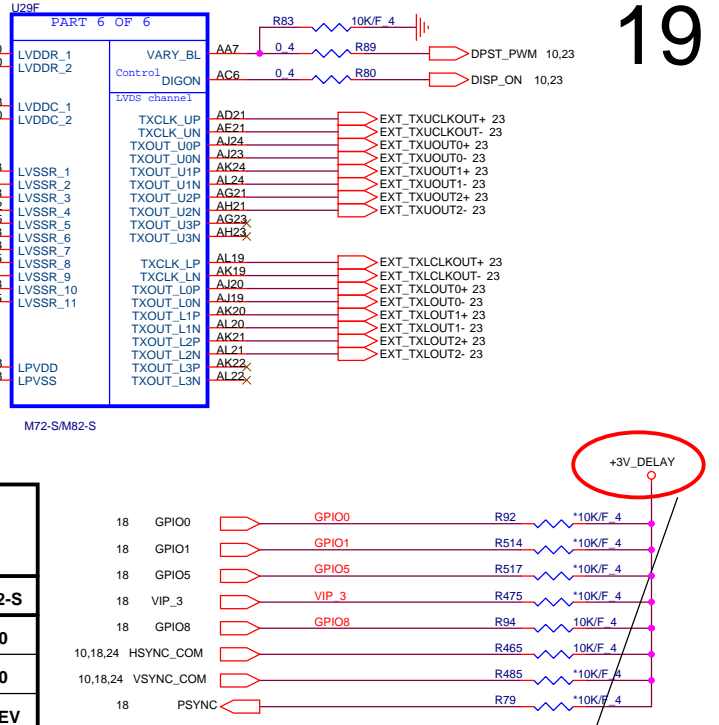
LVDDC
LVDS Output Driver Digital Power Supply
1.8 V ± 3%

LPVDD
Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
1.8 V ± 3%

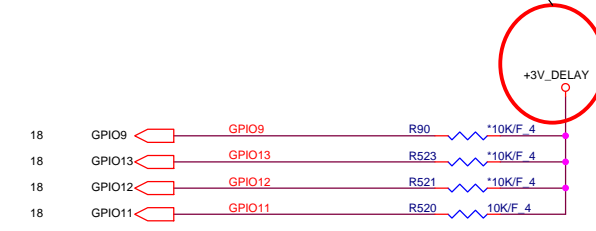
CONFIGURATION STRAPS		
PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows either PCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1

Memory Aperture size				
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

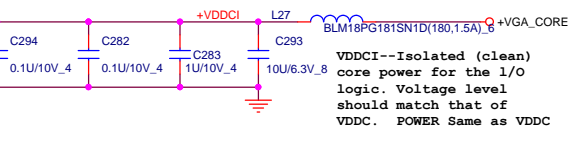
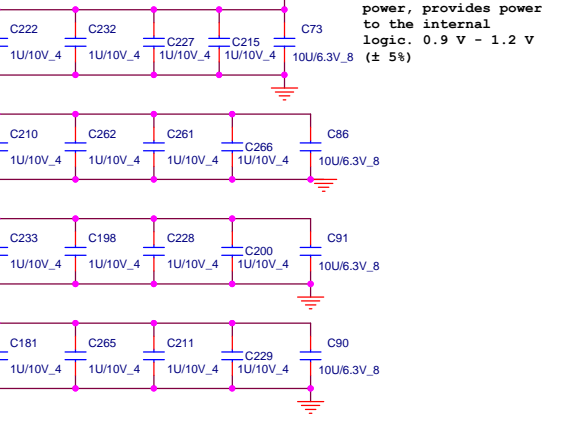
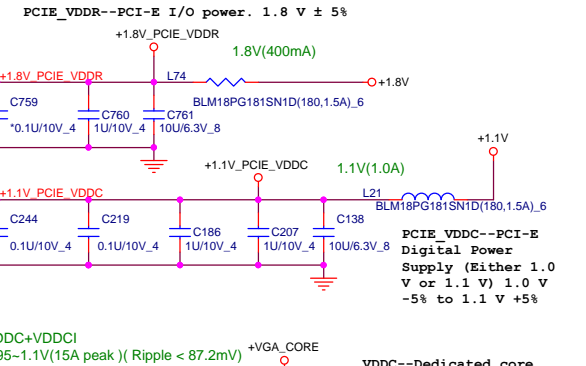
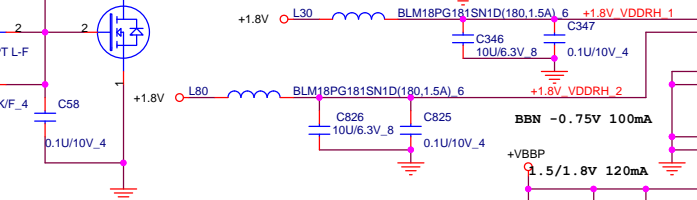
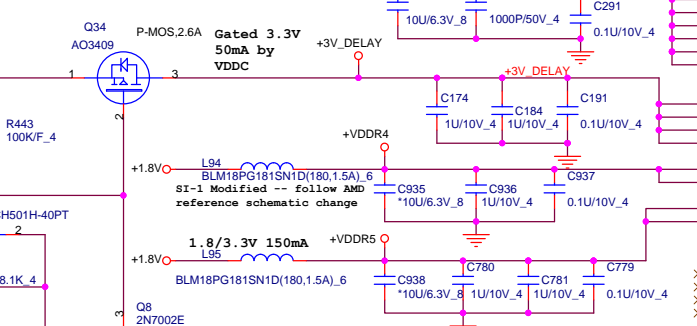
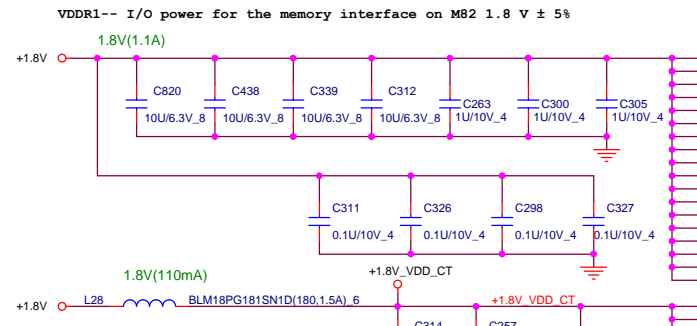
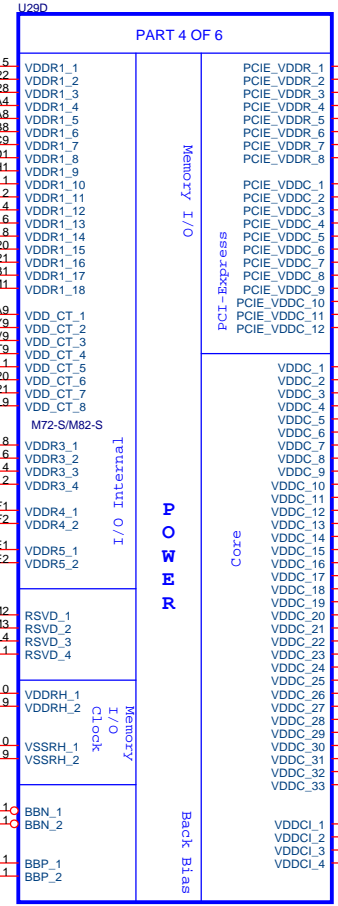
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



SI-1 Modified -- follow AMD reference schematic change for reduce leakage to VDDR3 BUS



PROJECT : QT8
Quantia Computer Inc.



VDD CT -- Level translation between core and I/O, excluding memory receivers. 1.8 V ± 5%

VDD R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

VDD R4 -- Power for DVPPDATA [23:12] - external TMS or GPIO; corresponds to DV0A_MSB VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDD R5 -- Power for DVP control pins (DVPCNTL [0-2] and DVPCCLK) and DVPPDATA [11:0] - external TMS or GPIO; corresponds to DV0A_LSB VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDDRH 1 & VDDRH 2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

VDDC+VDDCI (0.95-1.1V(15A peak) (Ripple < 87.2mV)) +VGA_CORE

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.

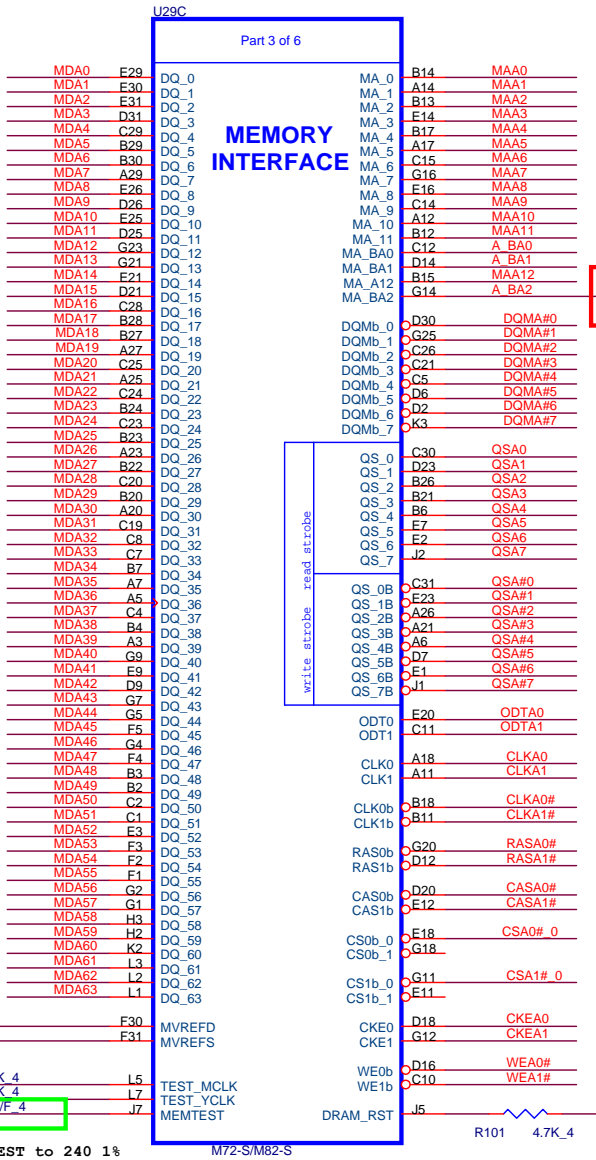
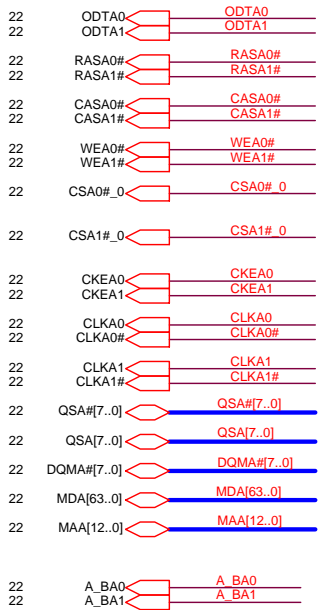
Back Bias Enabled: (GPIO_21_BB_EN = 3.3 V): 1.5 V or 1.8 V

Back Bias Disabled: (GPIO_21_BB_EN = 0 V): VDDC



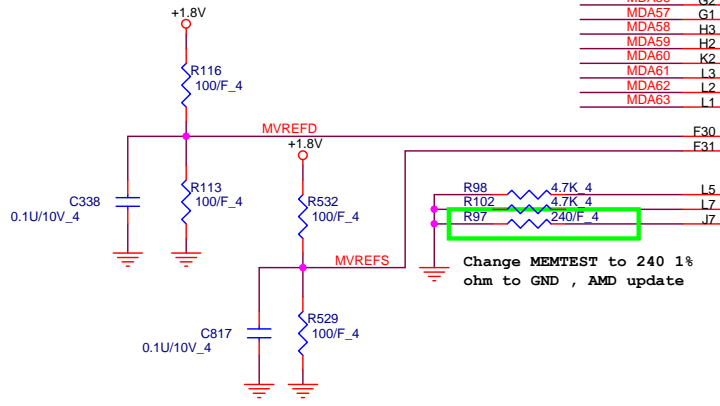
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number M7X/M8X_Power_and_NC	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 20 of 45	



A_BA2 22

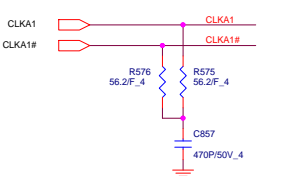
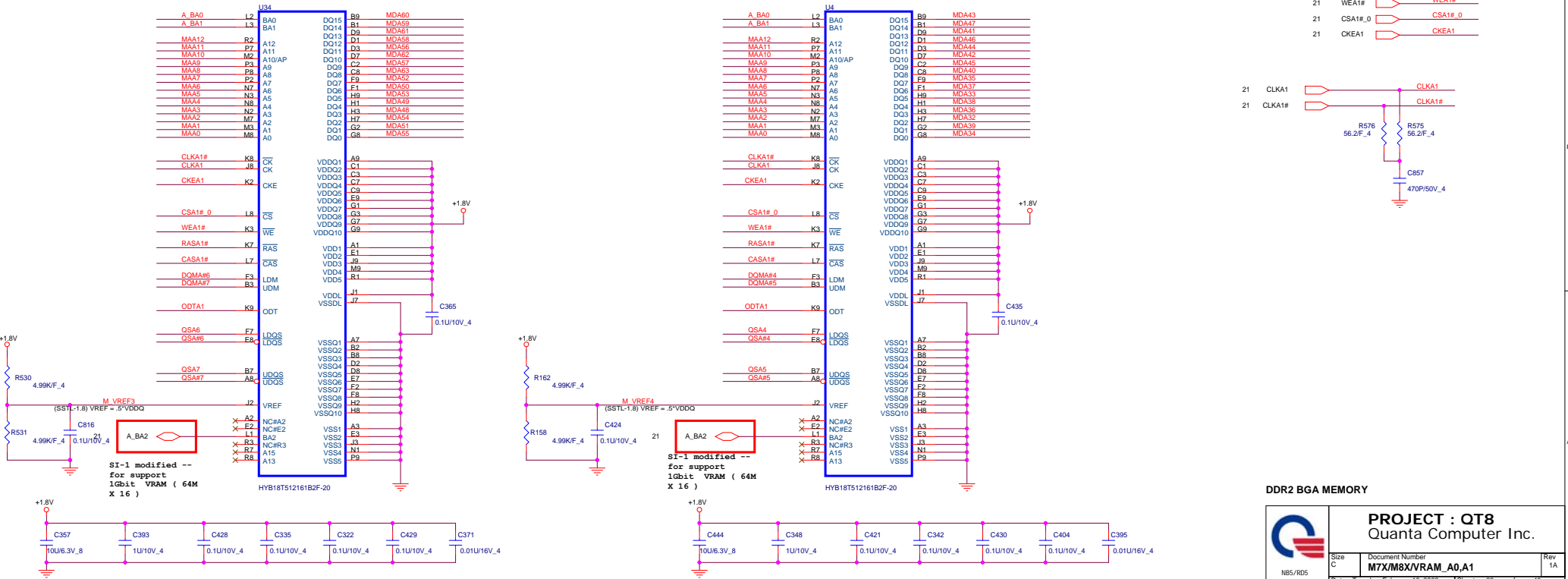
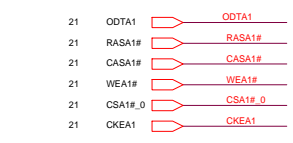
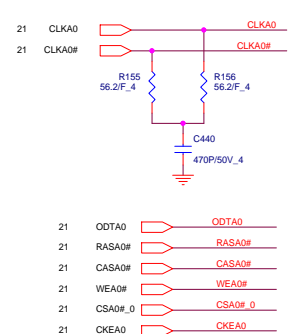
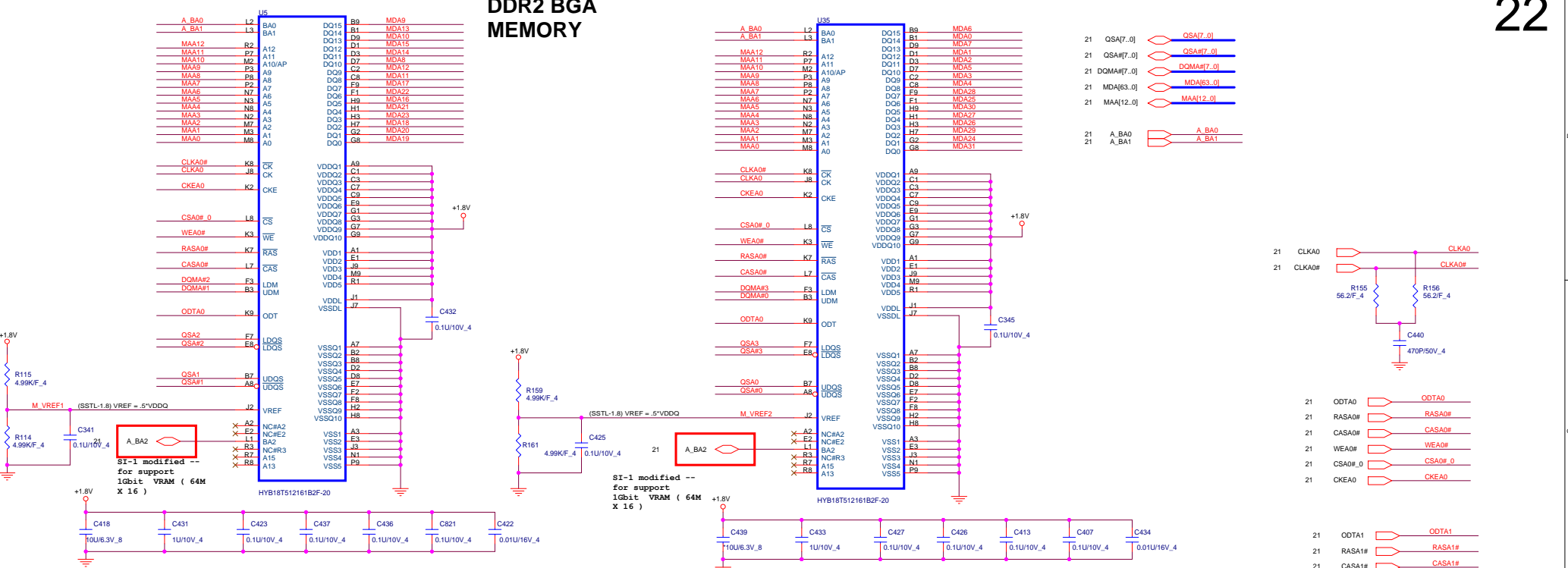
SI-1 modified --
for support
1Gbit VRAM (64M
x 16)



PROJECT : QT8
Quanta Computer Inc.

Size B	Document Number M7X/M8X/MEM_Interface	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 21	of 45

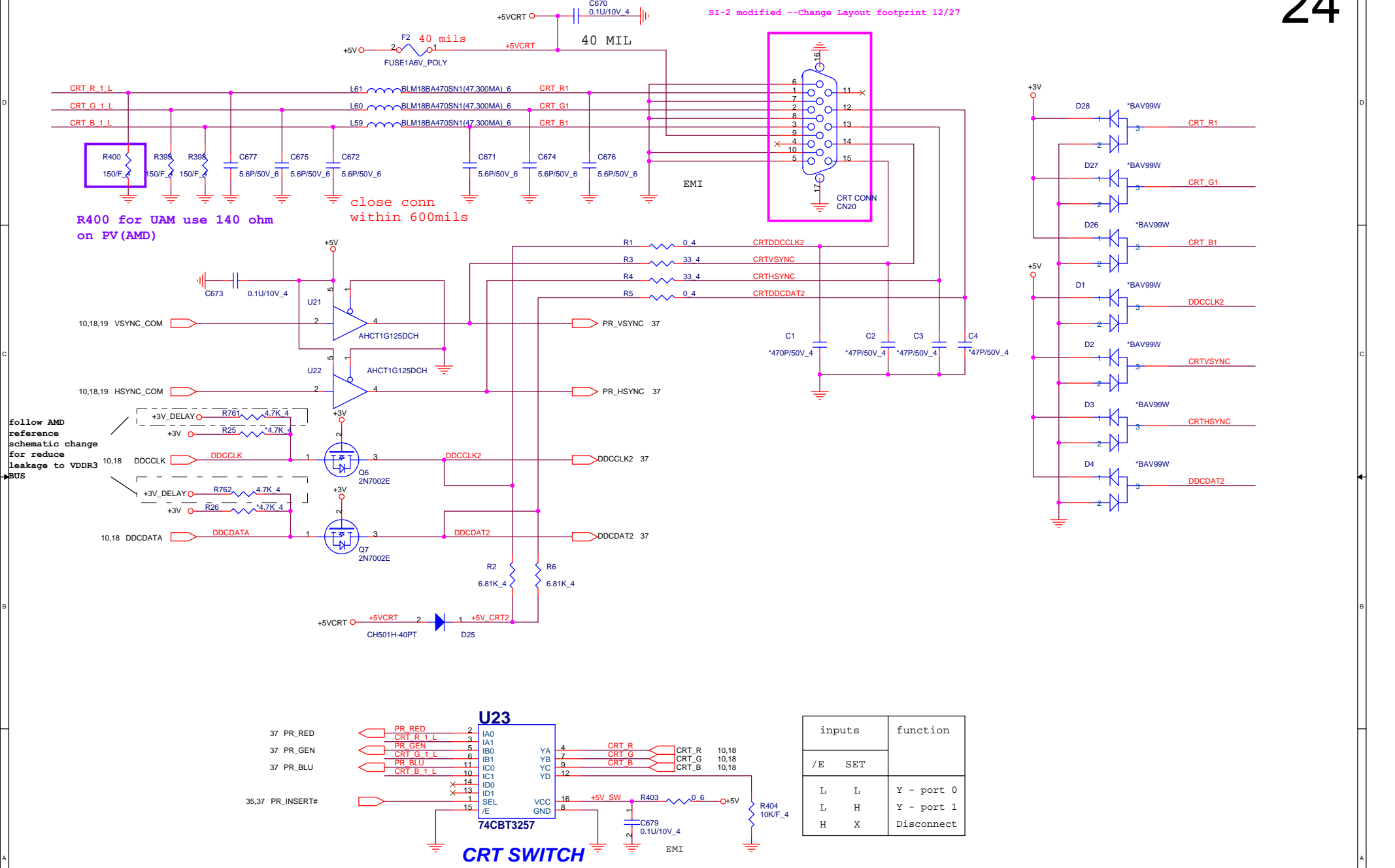
DDR2 BGA MEMORY



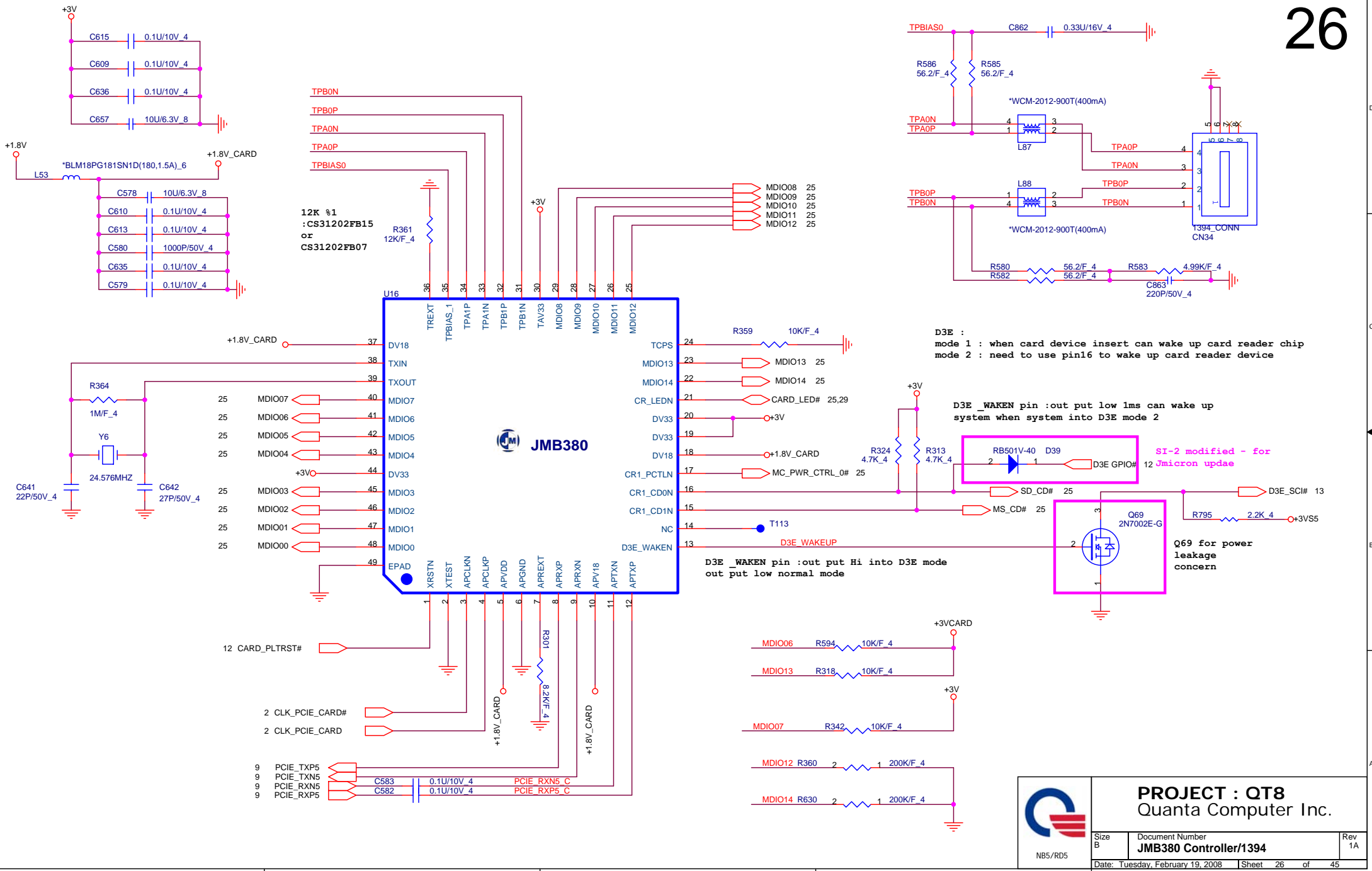
DDR2 BGA MEMORY

PROJECT : QT8
Quanta Computer Inc.

Size C Document Number **M7X/M8X/VRAM_A0,A1** Rev 1A
Date: Tuesday, February 19, 2008 Sheet 22 of 45



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect



D3E :
 mode 1 : when card device insert can wake up card reader chip
 mode 2 : need to use pin16 to wake up card reader device

D3E_WAKEN pin : out put low lms can wake up system when system into D3E mode 2

SI-2 modified - for Jmicron updae

D3E_WAKEN pin : out put Hi into D3E mode
 out put low normal mode

Q69 for power leakage concern



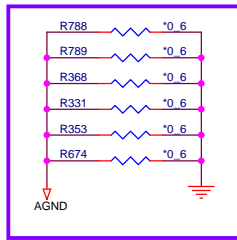
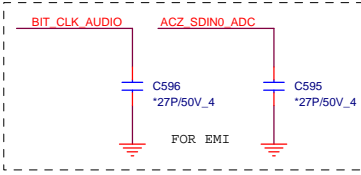
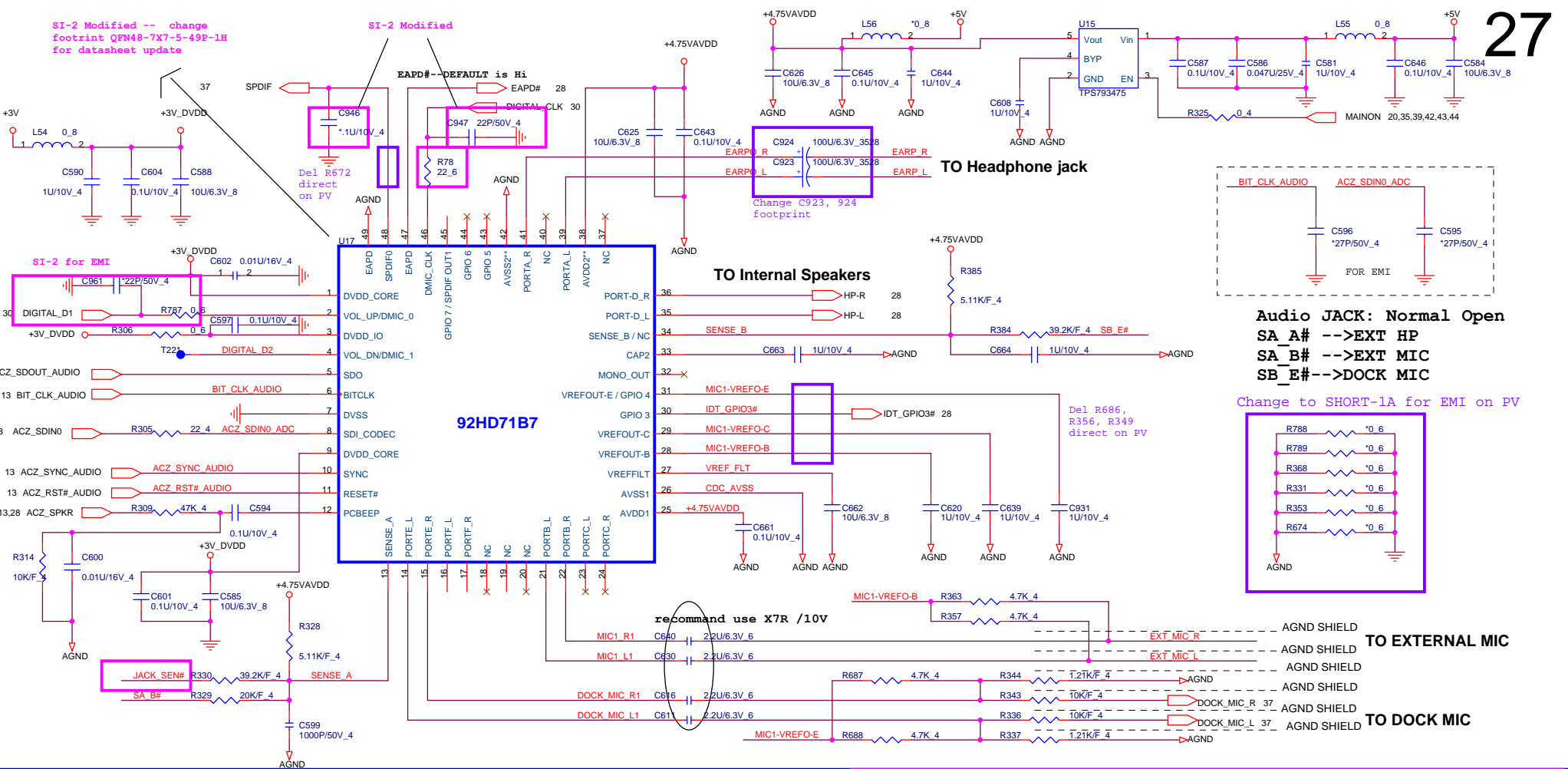
PROJECT : QT8
 Quanta Computer Inc.

Size B	Document Number JMB380 Controller/1394	Rev 1A
Date: Tuesday, February 19, 2008		Sheet 26 of 45

NB5/RD5

SI-2 Modified -- change footprint QFN48-7X7-5-49P-1H for datasheet update

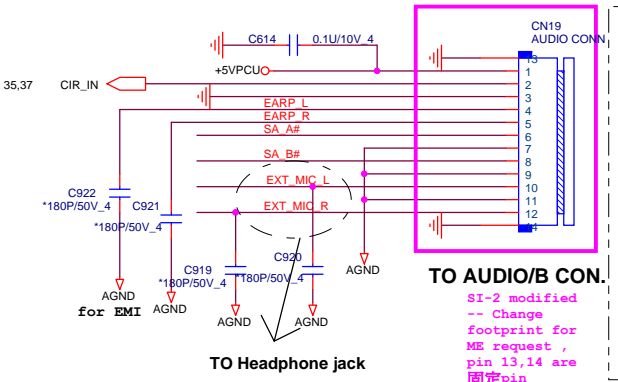
SI-2 Modified



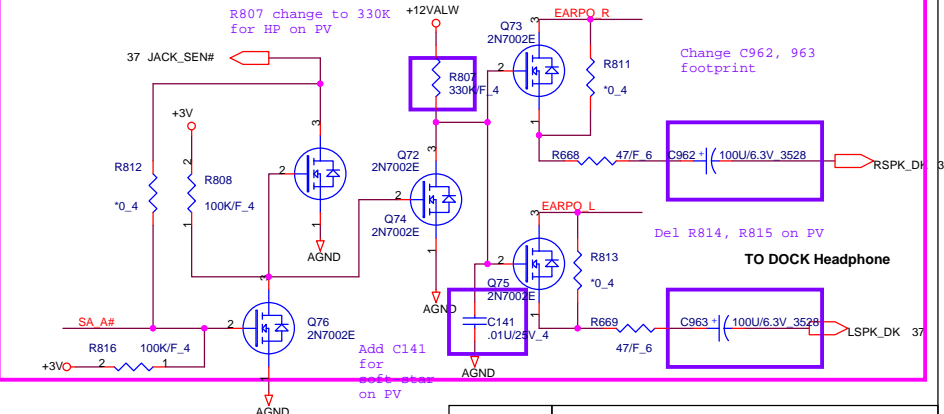
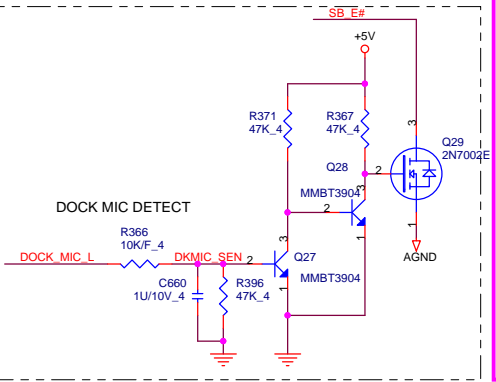
recommand use X7R /10V

TO EXTERNAL MIC

TO DOCK MIC



SI-2 modified -- Change footprint for ME request, pin 13,14 are 固定pin

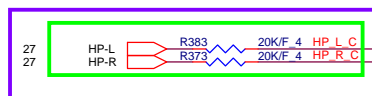


PROJECT : QT8
 Quanta Computer Inc.

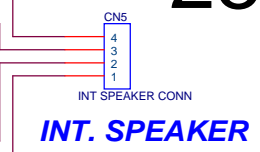
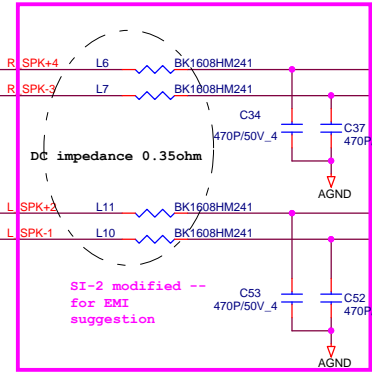
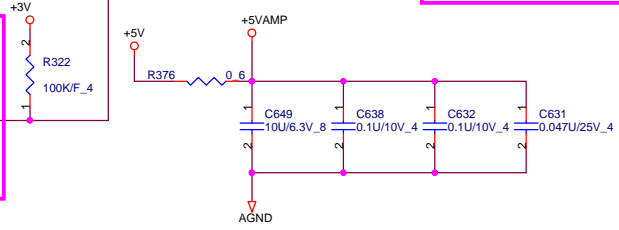
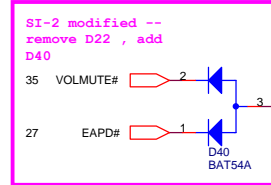
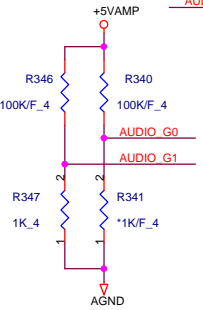
Size Custom	Document Number	Rev 1A
NB5/RD5	Azalia AD1883	
Date: Tuesday, February 19, 2008	Sheet 27 of 45	

SI-2 Modified -- remove C621/C623

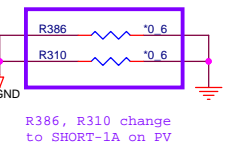
LIN-,RIN- and LIN+,RIN+ swap for BOBO noise on PV



PV-1 Modified --R383 , R373 change from 20Kohm to 0 ohm for Volume too low issue



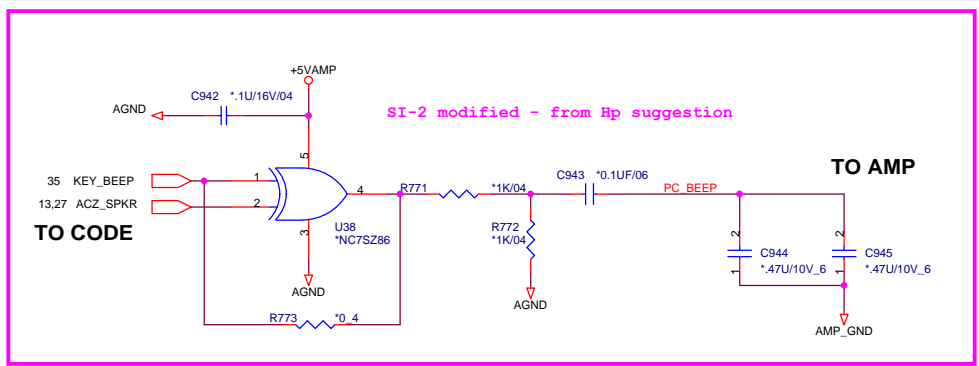
$V_{rms} = V_{pp} / 2 \sqrt{2}$
 $Power = (V_{rms})^2 / R$
 QT8 speaker -- 3.2ohm / 2W



6017A2 Gain Table

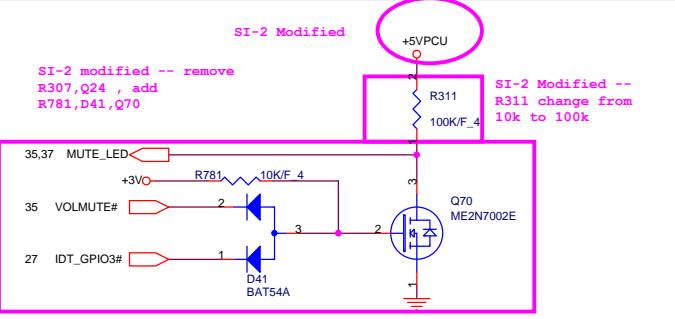
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

PC-BEEP

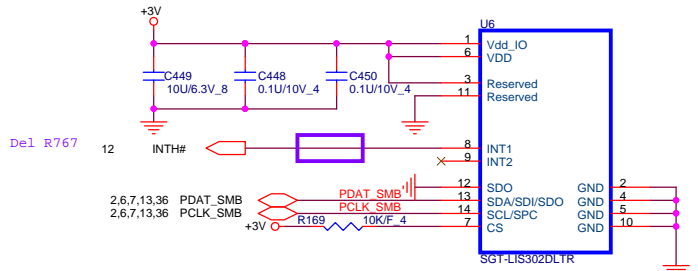


MUTE_LED

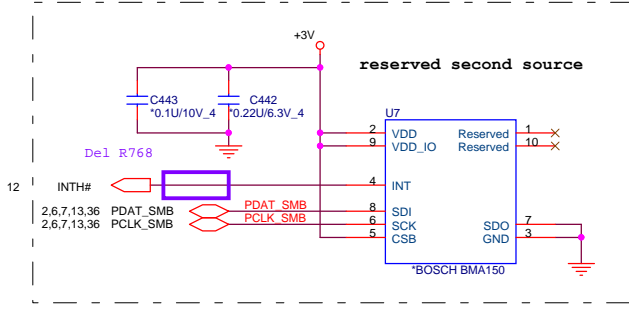
Low --> un-MUTE
 High --> Mute



Acceleration sensor

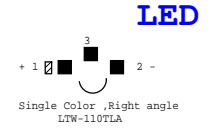
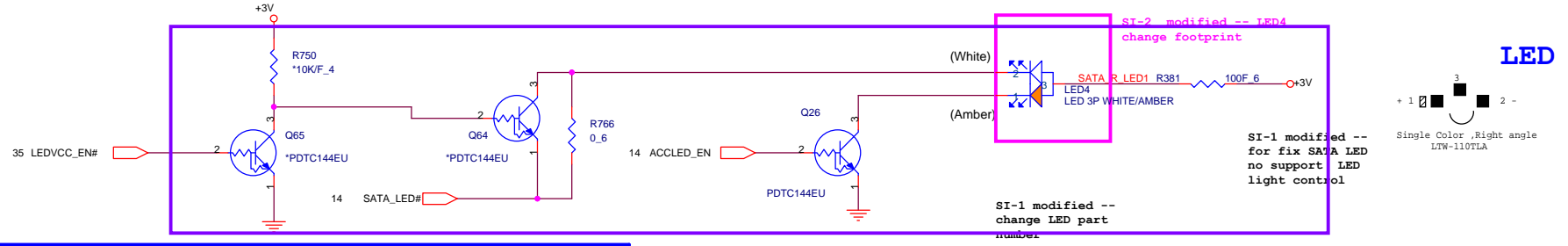
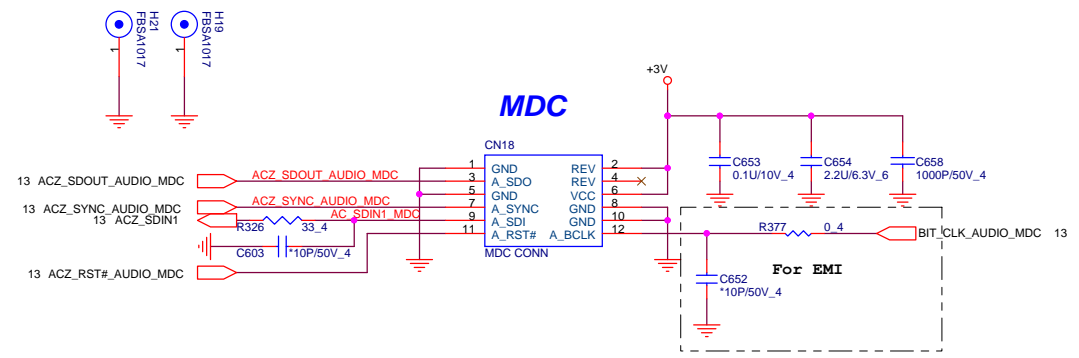


SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

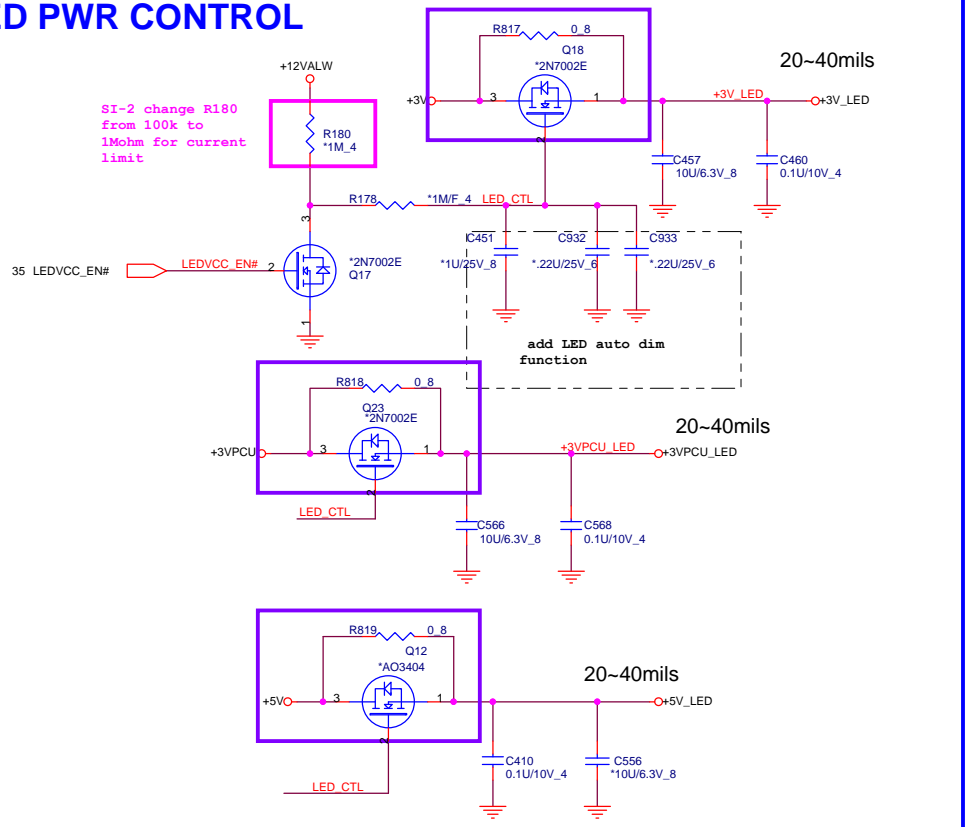


PROJECT : QT8
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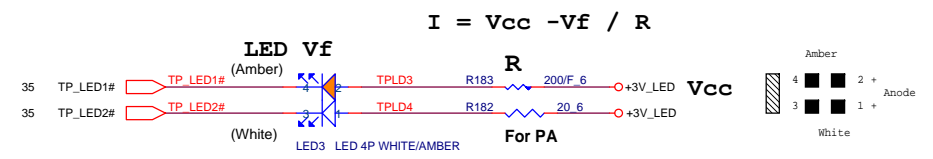
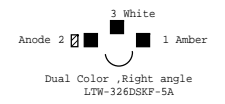
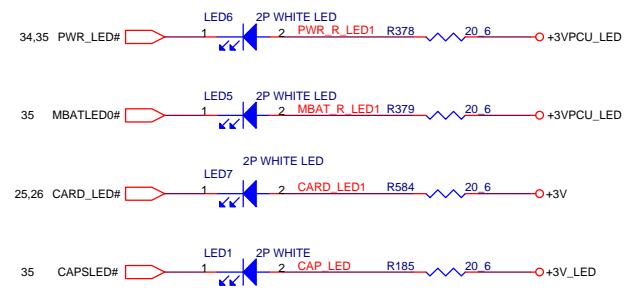
Modem CONN



LED PWR CONTROL



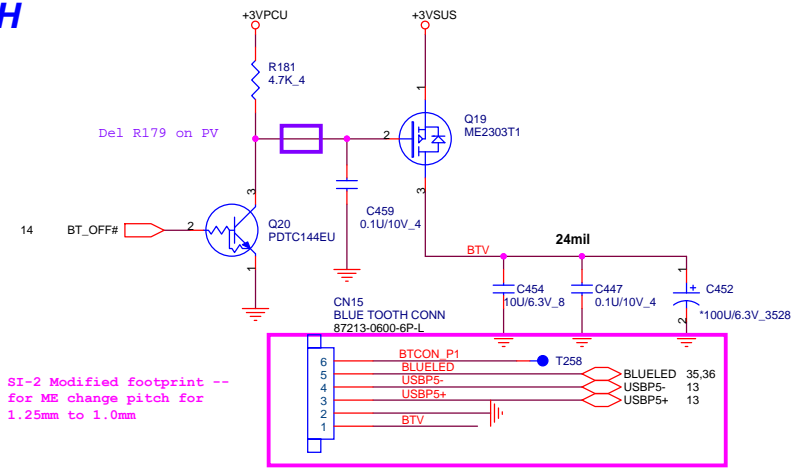
Del R380
Change R381 to 100
Add R766, R817, R818,
R819
LED PWR control no-stuff
on PV



PROJECT : QT8
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Size Custom	Document Number MDC1.5 Con Accelerometer/LED	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 29 of 45	

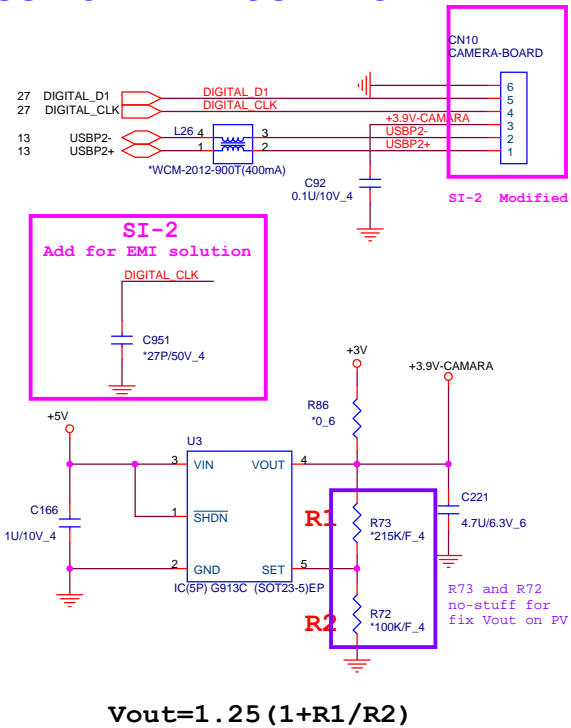
BLUETOOTH



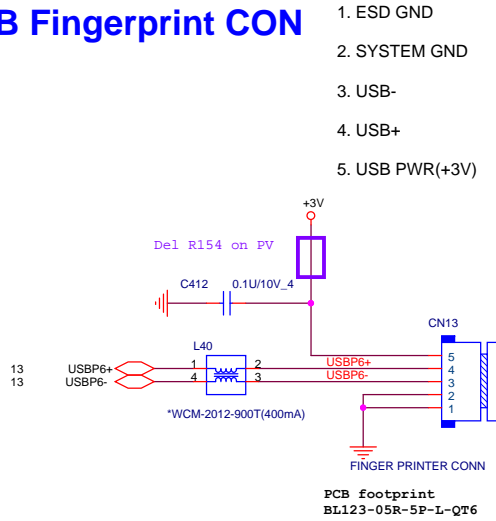
For Discrete Touch-Screen



USB CAMERA CONNECT



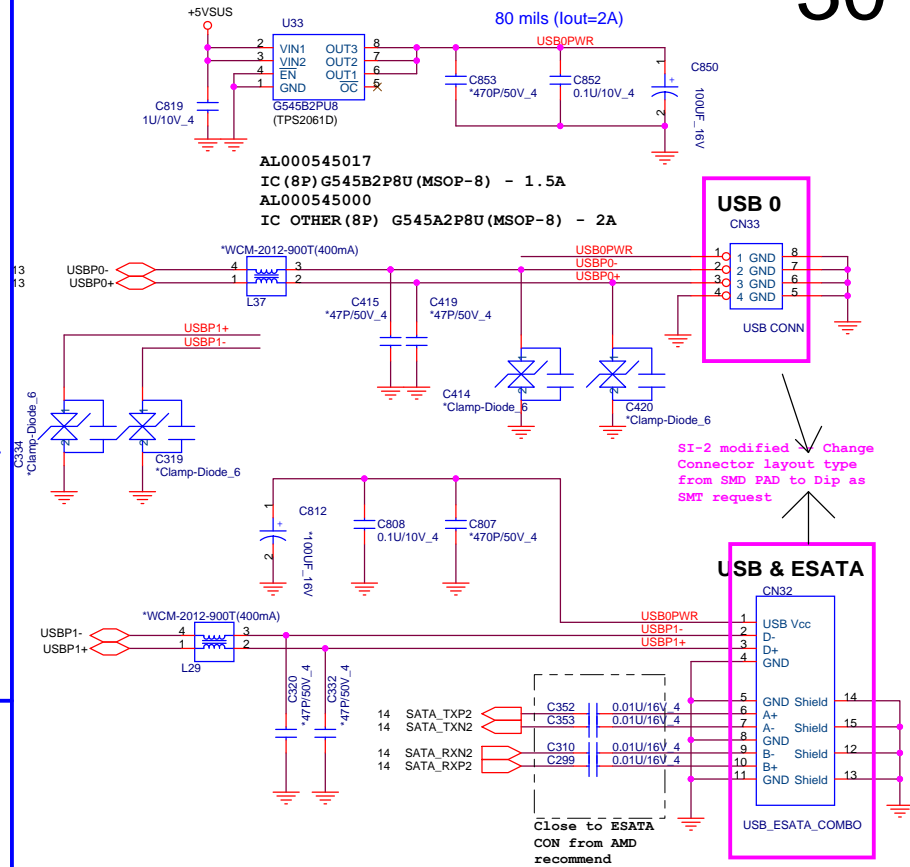
USB Fingerprint CON



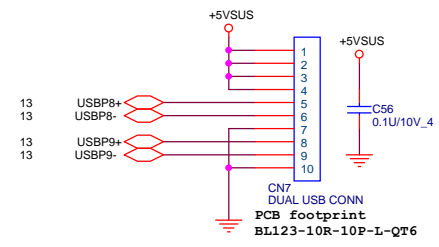
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

LEFT SIDE USBX1 and E-SATA/USB COMBO

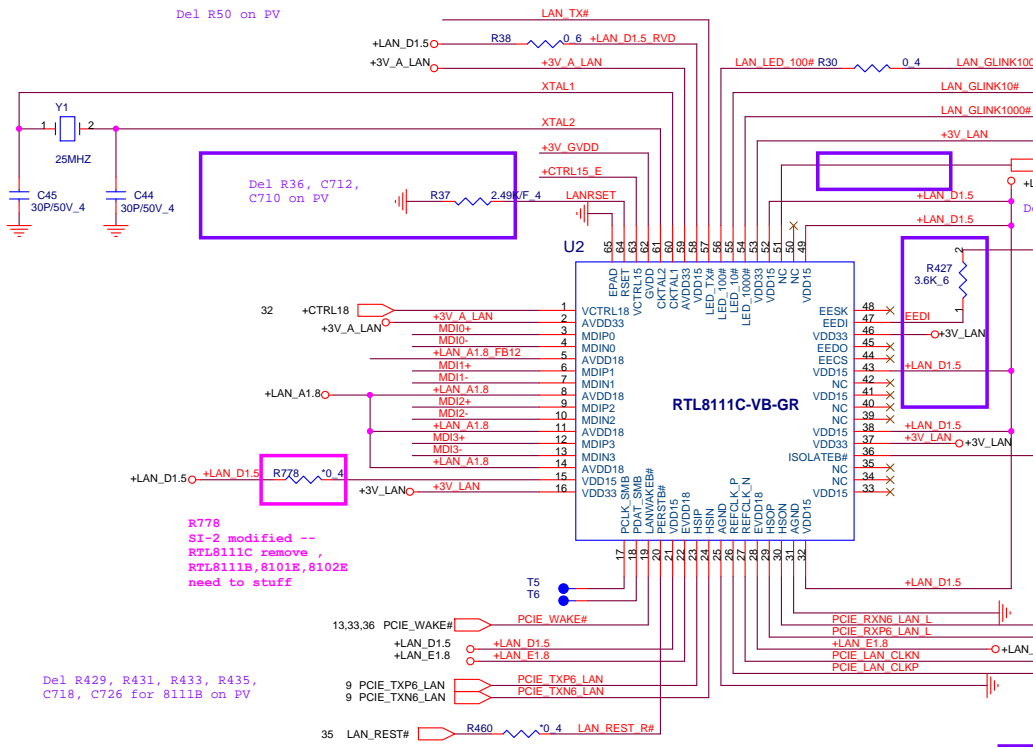
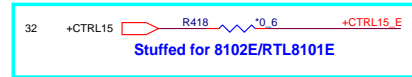
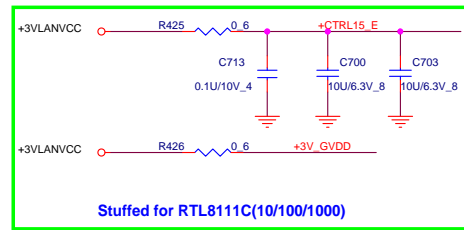
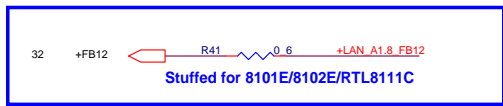
30



RIGHT SIDE USBX2



	PROJECT : QT8 Quanta Computer Inc.		Rev 1A
	Size Custom Document Number BT/WEBCAM/FT/USBX4/ESATA	Date: Tuesday, February 19, 2008	Sheet 30 of 45

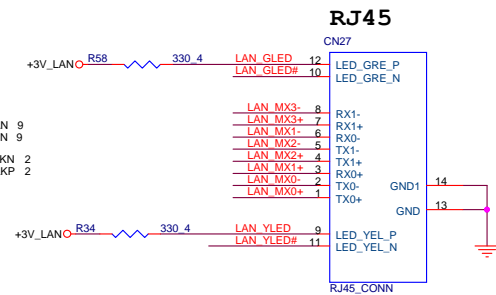
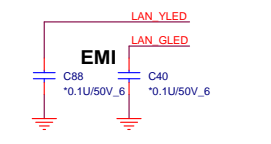


use BIOS to programming EEPROM , EEDI should be pull Hi

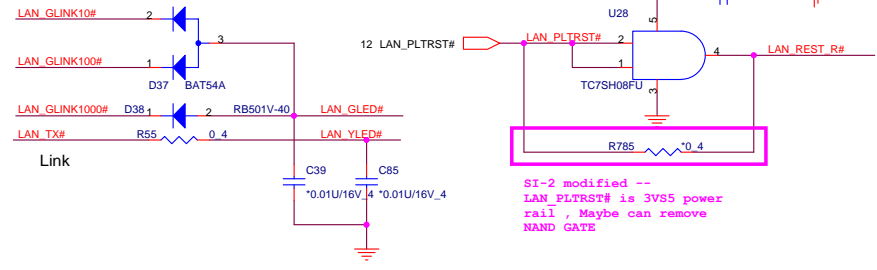
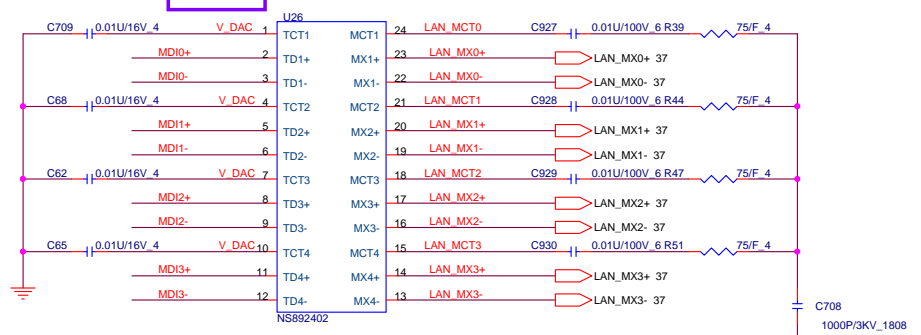
R46 only for 8111B, 8101E&8102E&8111C can remove

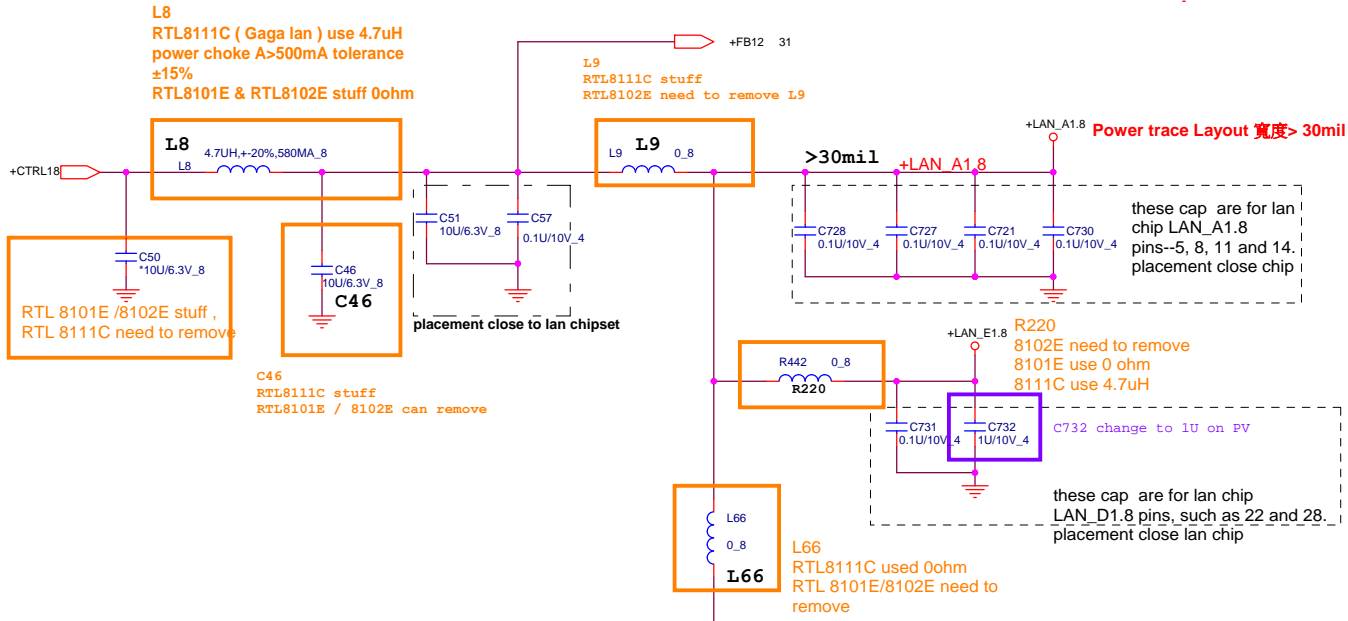
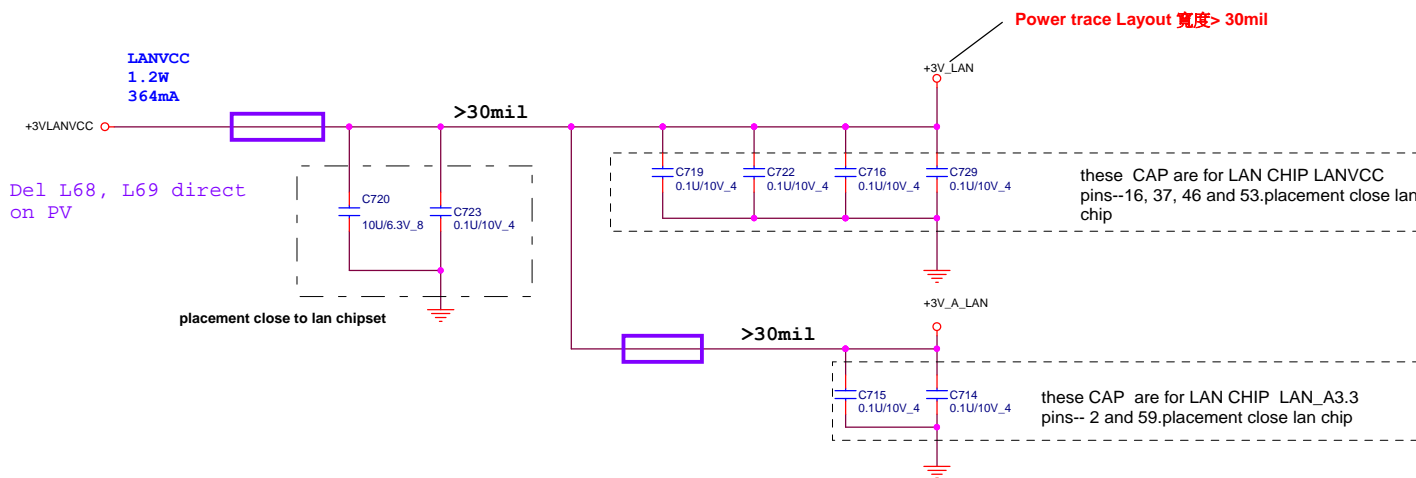
Remove R456 and Add D42 on PV

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCI_E_WAKE# pin)



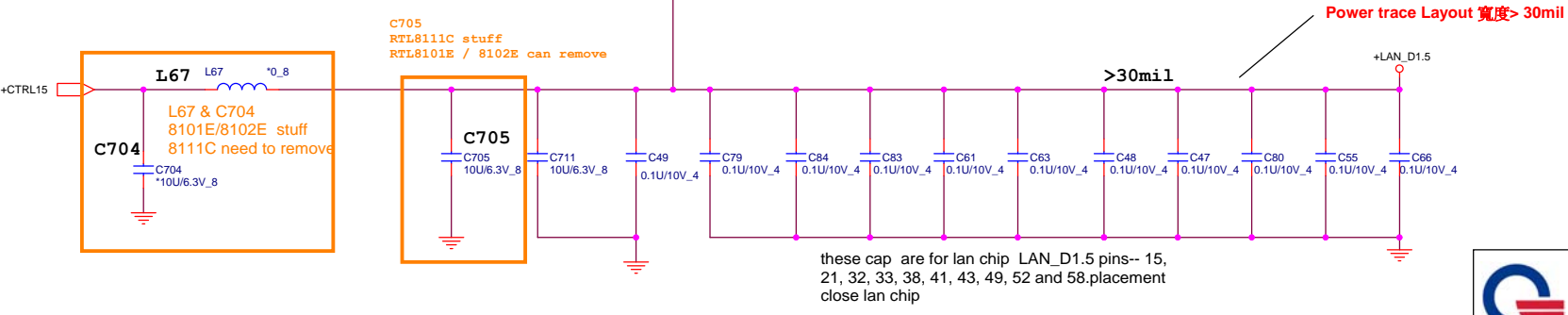
AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08101E005 IC(64P)RTL8101E-GR(QFN)





Power domain chart

	RTL8111B/ RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

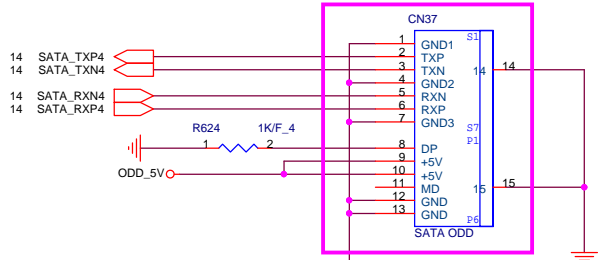


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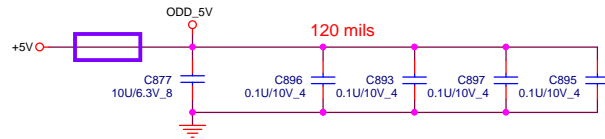
Size Custom	Document Number LAN Power	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 32 of 45		

SATA CD-ROM

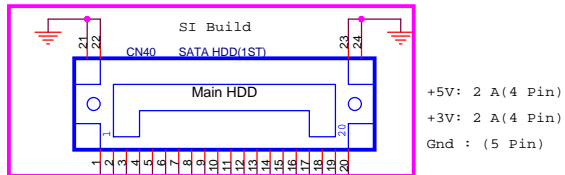
SI-2 Modified footprint -- Modify 12/27



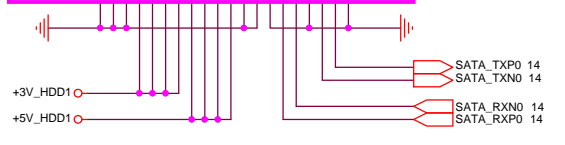
Del L90 direct on PV



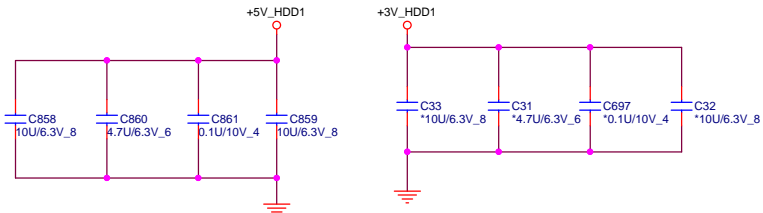
SI-2 Modified footprint -- Modify 固定孔 Size as SMT request



+5V: 2 A (4 Pin)
+3V: 2 A (4 Pin)
Gnd: (5 Pin)

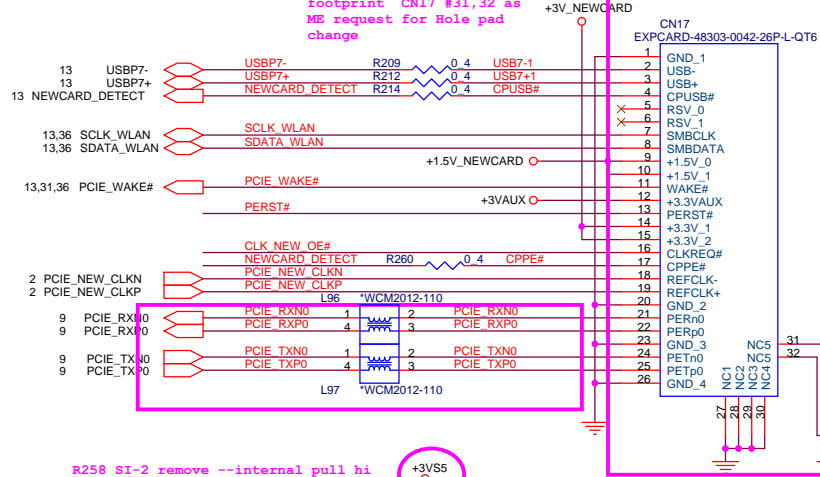


Del R578 direct on PV

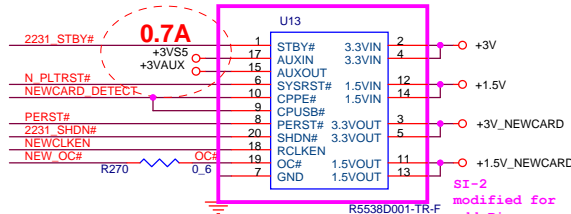
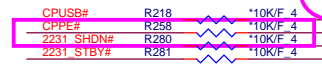


NEWCARD

SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change



R258 SI-2 remove -- internal pull hi

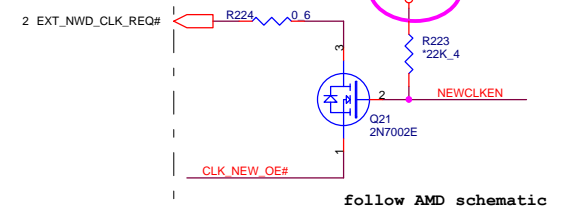
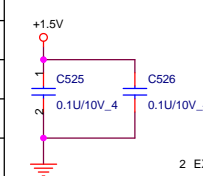


2A
1A

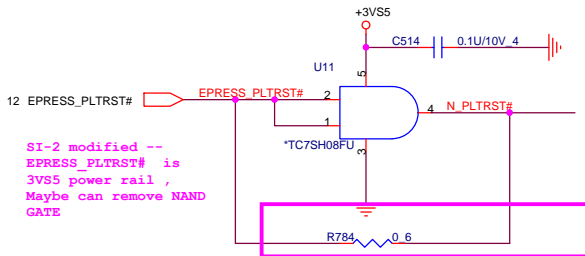
Del R790, R791, R792, R793 for RF on PV

SI-2 modified for add Pin 21-25 as U25 Thermal pad tied to Gnd

R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN



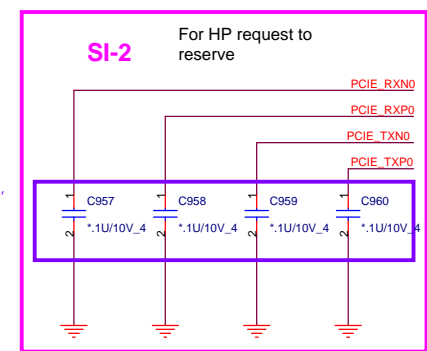
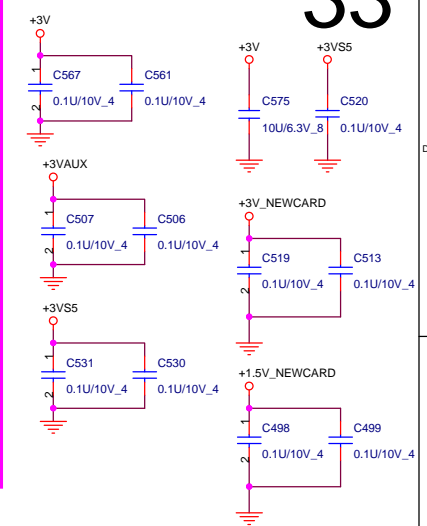
follow AMD schematic



SI-2 modified -- EPRESS_PLTRST# is 3VSS power rail, Maybe can remove NAND GATE

NEWCARD (PCIEXPRESS*1 + USB*1)

33

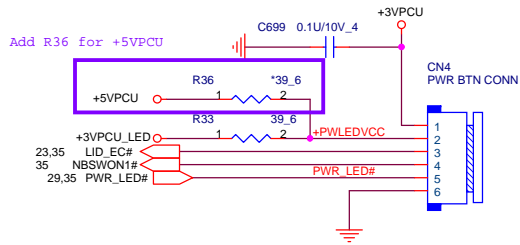


For HP request to reserve

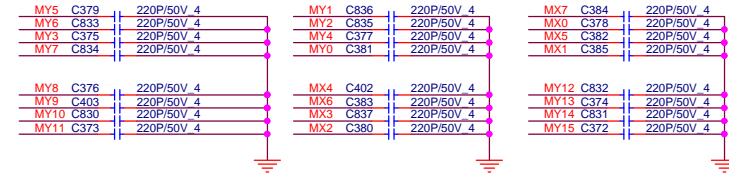
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number NEW CARD/SATA ODD/SATA HDD	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 33 of 45	

POWER BUTTON CONNECT

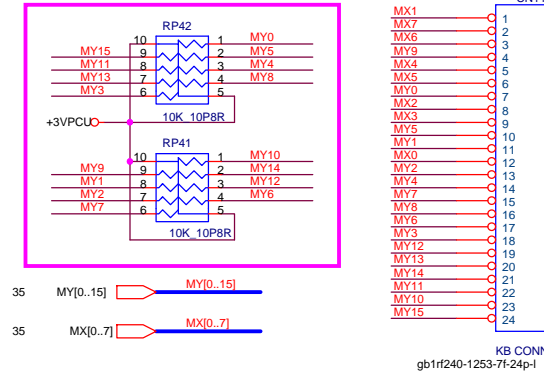


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWLED#
6. GND



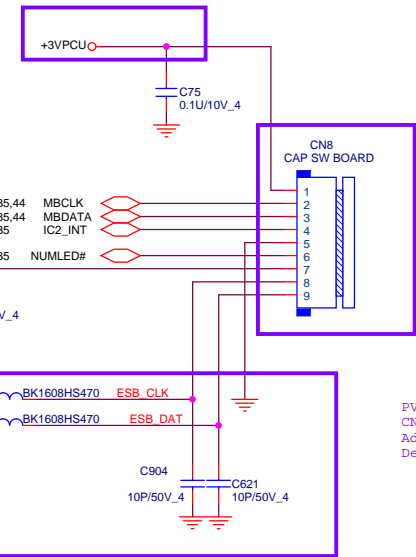
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



KB CONN
gb1rf240-1253-7f-24p-1

CAP SW CONNECT

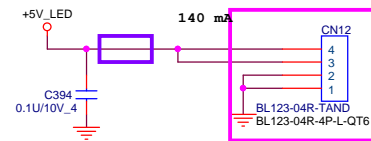


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103

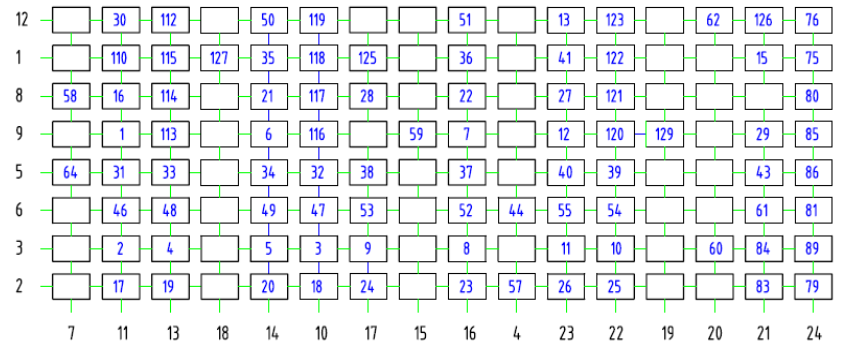
Del R770 on PV

SI-2 Modified 12/27

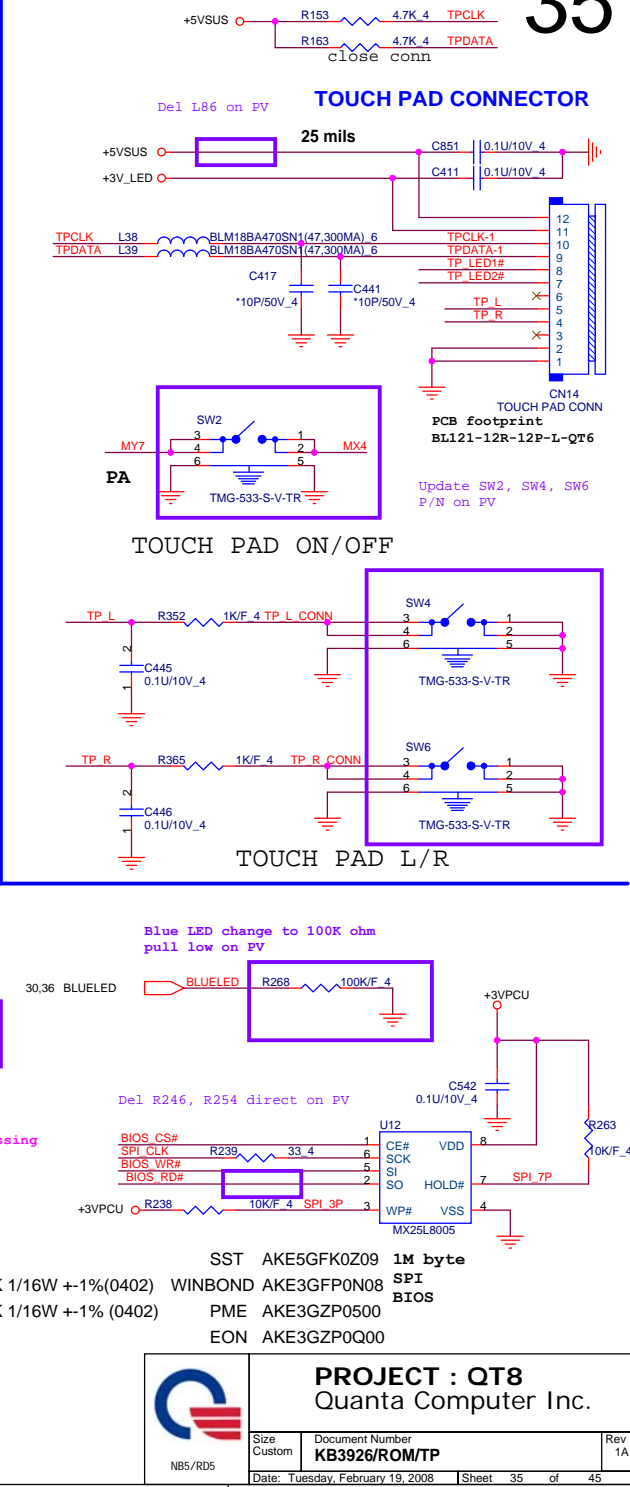
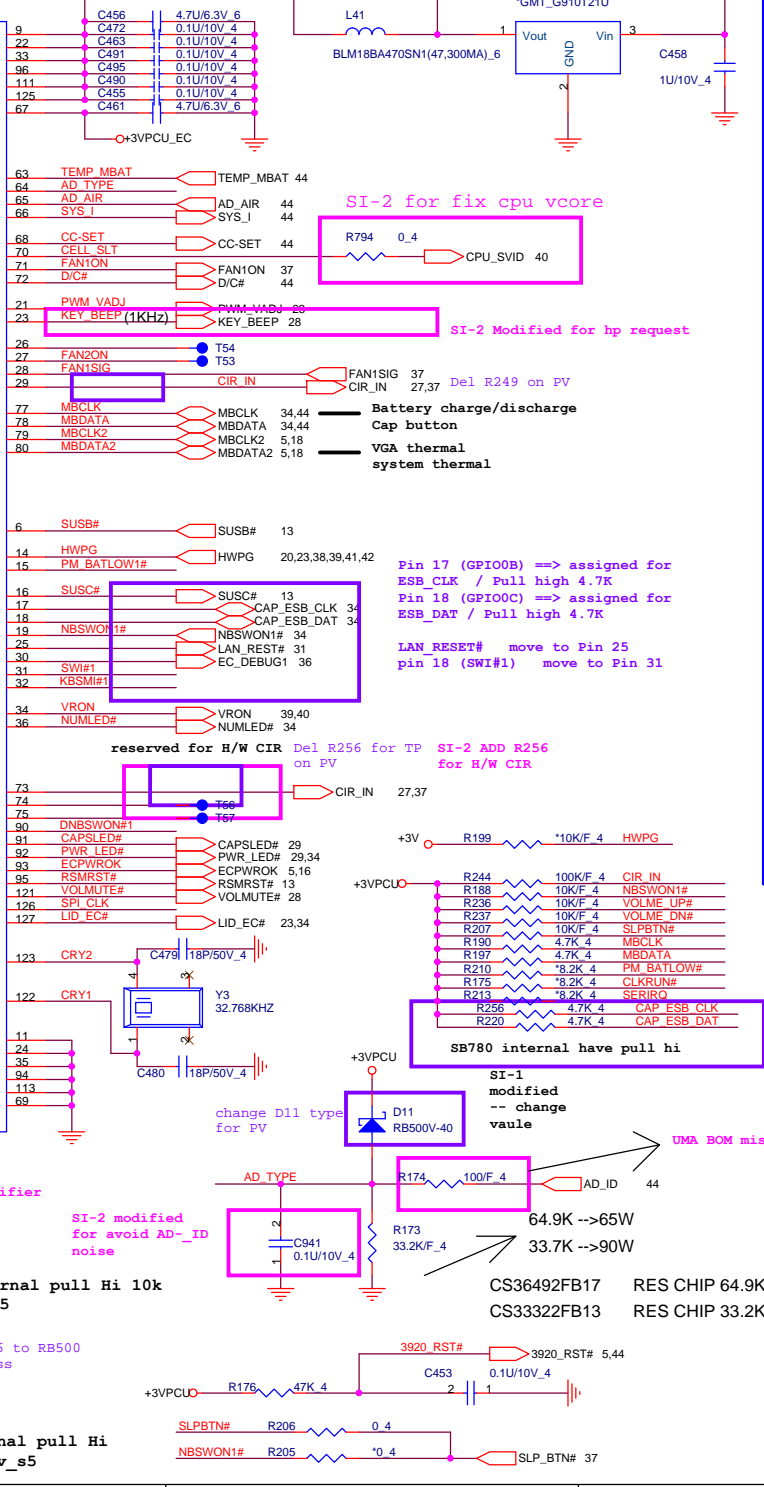
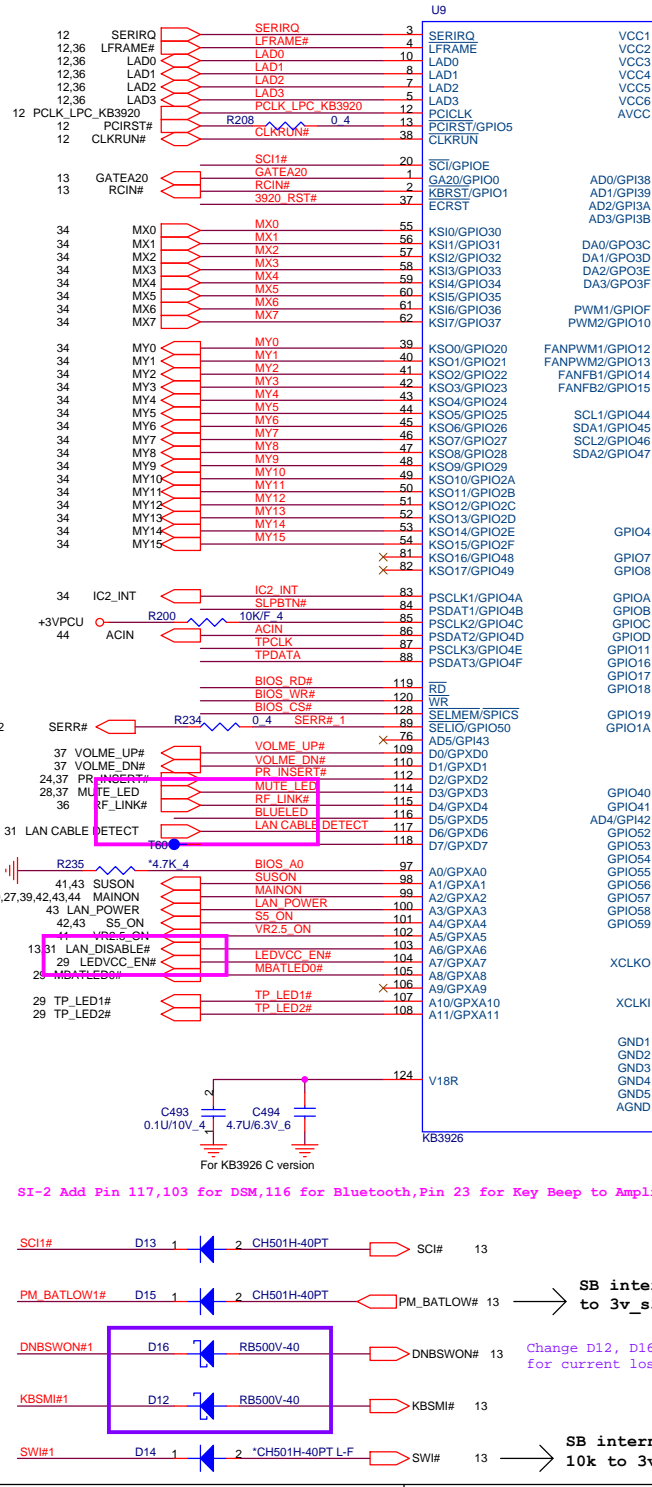


1. LEDVCC
2. LEDVCC
3. NC
4. GND

SI-2 Modified



Change U9 layout footprint to LQFP128-16X16-4-A1



SI-2 for fix cpu vcore
CPU_SVID 40

SI-2 Modified for hp request

Pin 17 (GPIO0B) ==> assigned for ESB_CLK / Pull high 4.7K
Pin 18 (GPIO0C) ==> assigned for ESB_DAT / Pull high 4.7K

LAN_RESET# move to Pin 25
pin 18 (SWI#1) move to Pin 31

reserved for H/W CIR
Del R256 for TP on PV
SI-2 ADD R256 for H/W CIR

SB780 internal have pull hi

SI-1 modified -- change vaule

UMA BOM missing

change D11 type for PV

SI-2 modified for avoid AD_ID noise

change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

change D11 type for PV

Blue LED change to 100K ohm pull low on PV

Del R246, R254 direct on PV

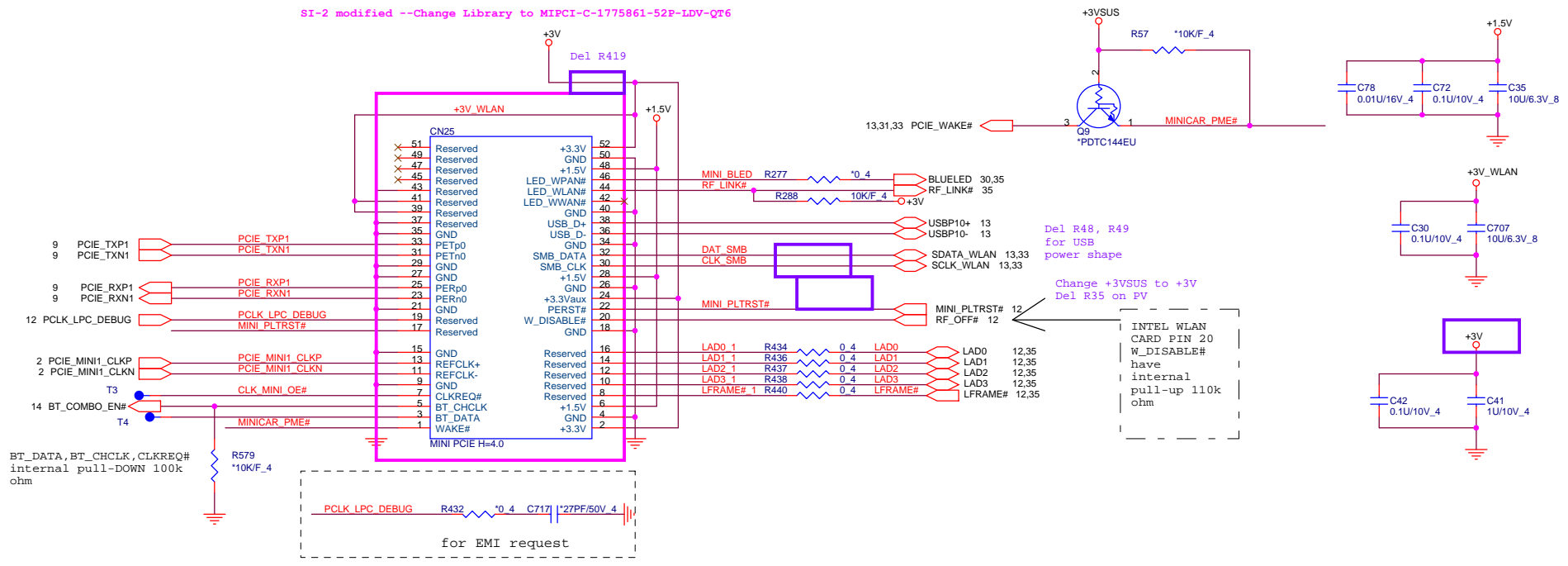
SST AKE5GFK0Z09 1M byte SPI BIOS
RES CHIP 64.9K 1/16W +-1%(0402)
WINBOND AKE3GFP0N08
PME AKE3GZP0500
EON AKE3GZP0Q00

PROJECT : QT8
Quanta Computer Inc.

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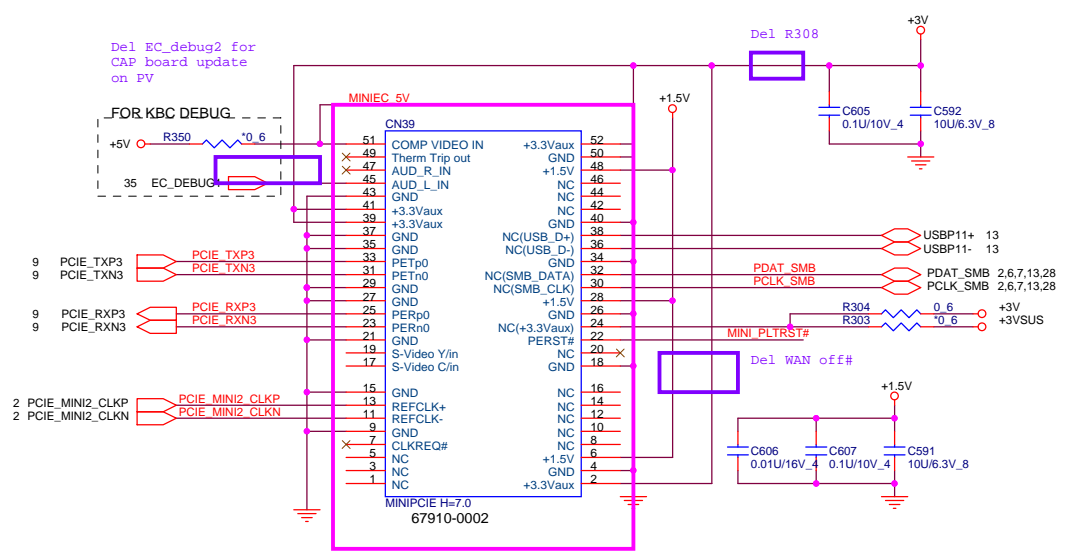
Mini PCI-E Card 1 WLAN

SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6




Mini PCI-E Card 2 TV tuner card

Del EC_debug2 for CAP board update on PV

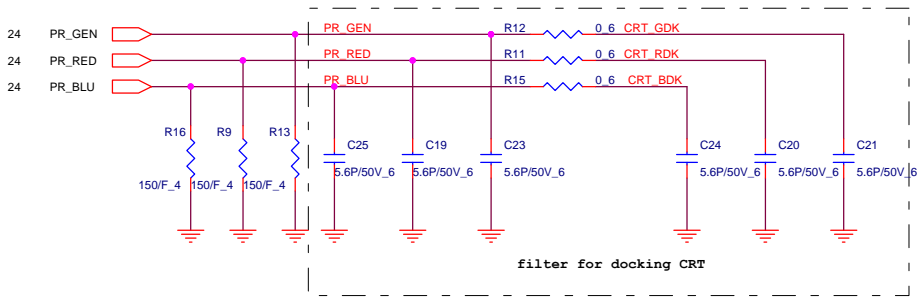
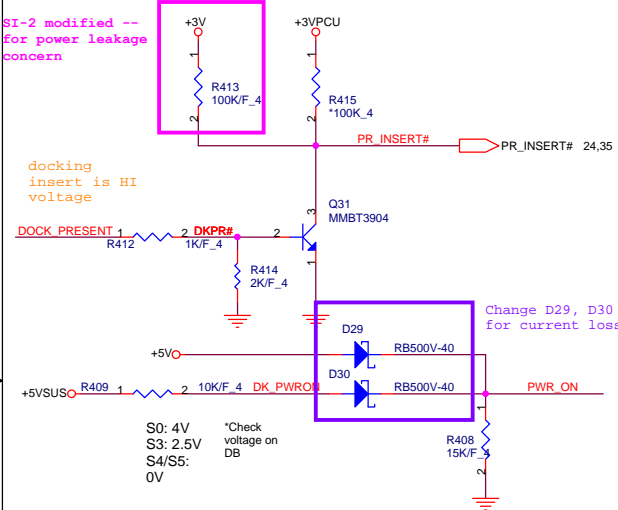
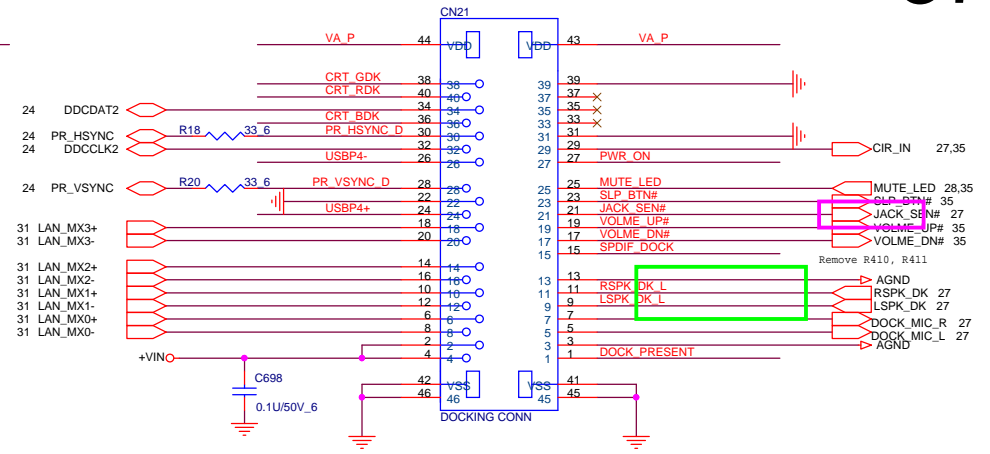
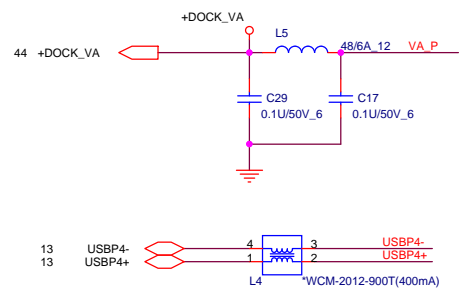
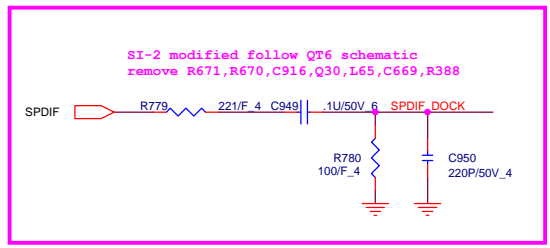


SI-2 modified --Change Library to MIPCI-P04-FJ504-170-52P-QT6

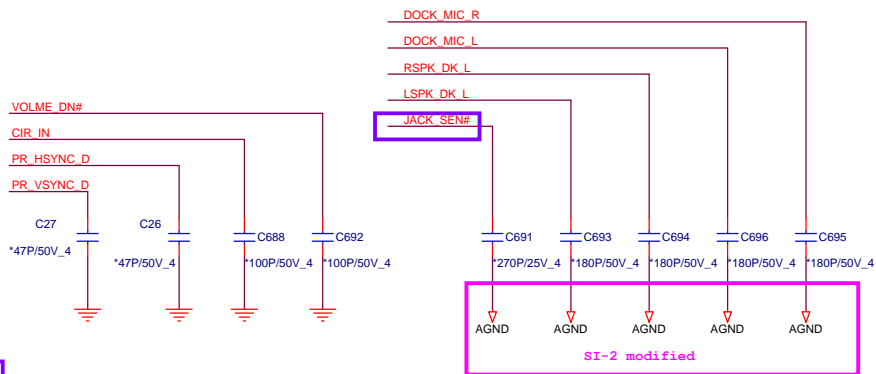
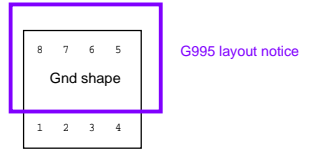
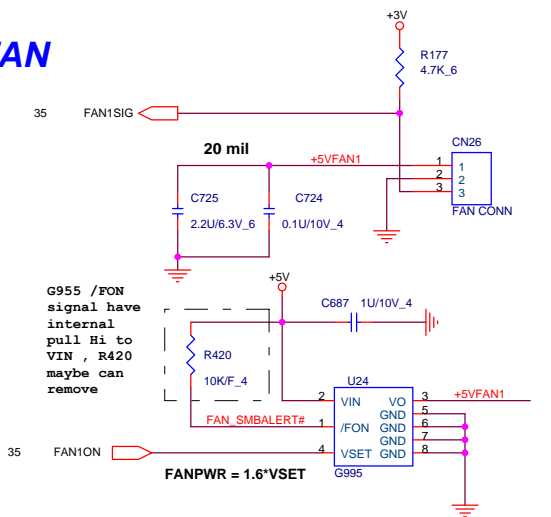
 NBS/RD5	PROJECT : QT8 Quanta Computer Inc.	
	Size Custom Date: Tuesday, February 19, 2008	Document Number Mini CARD X 3 Sheet 36 of 45

CABLE DOCK

support 6A 200mils
CX000480005



CPU FAN



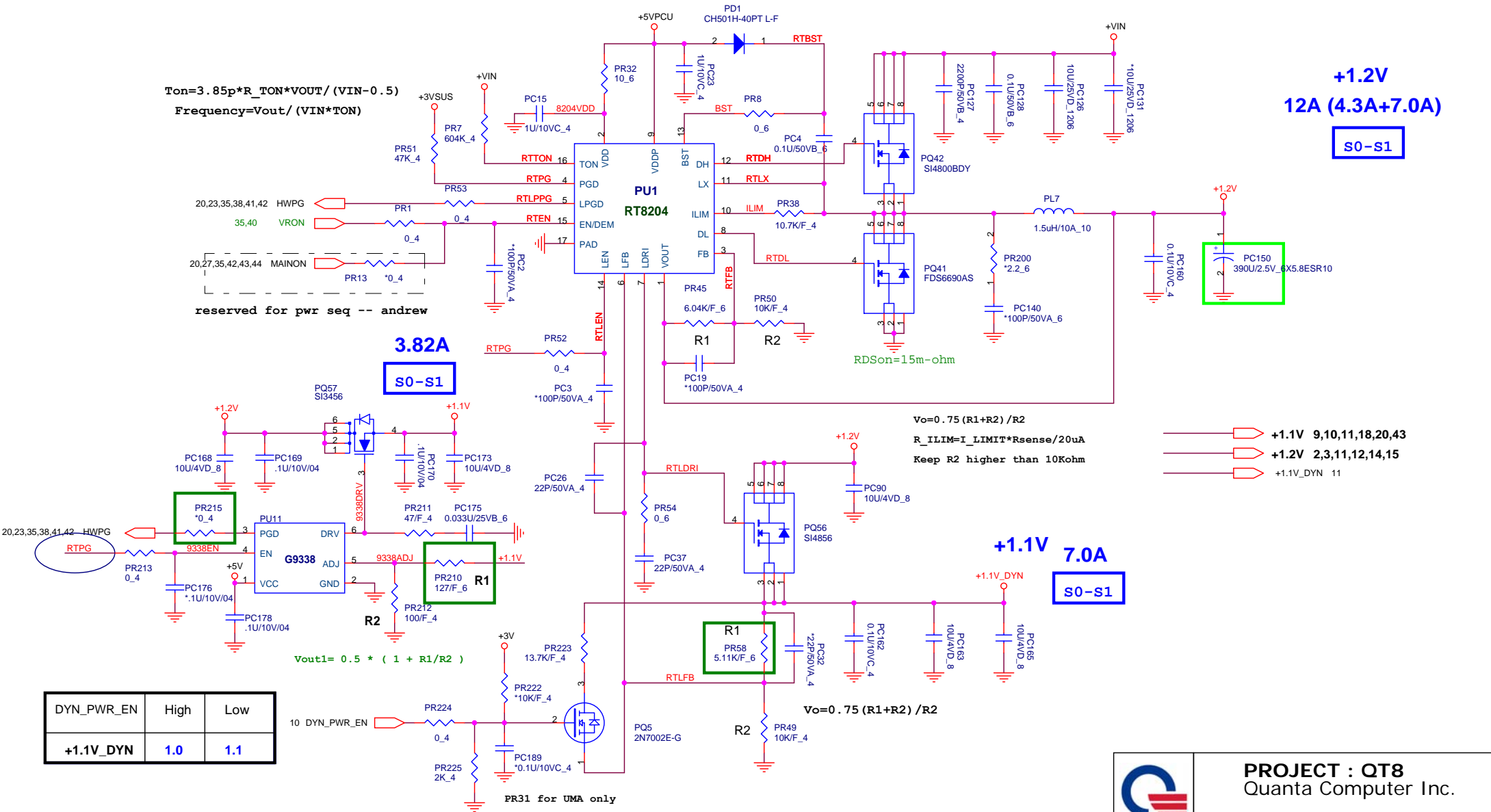
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number CABLE DOCKING/FAN	Rev 1A
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NB5/RD5

$$T_{on} = 3.85p * R_{TON} * V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} * TON)$$



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1



PROJECT : QT8
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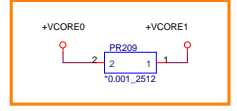
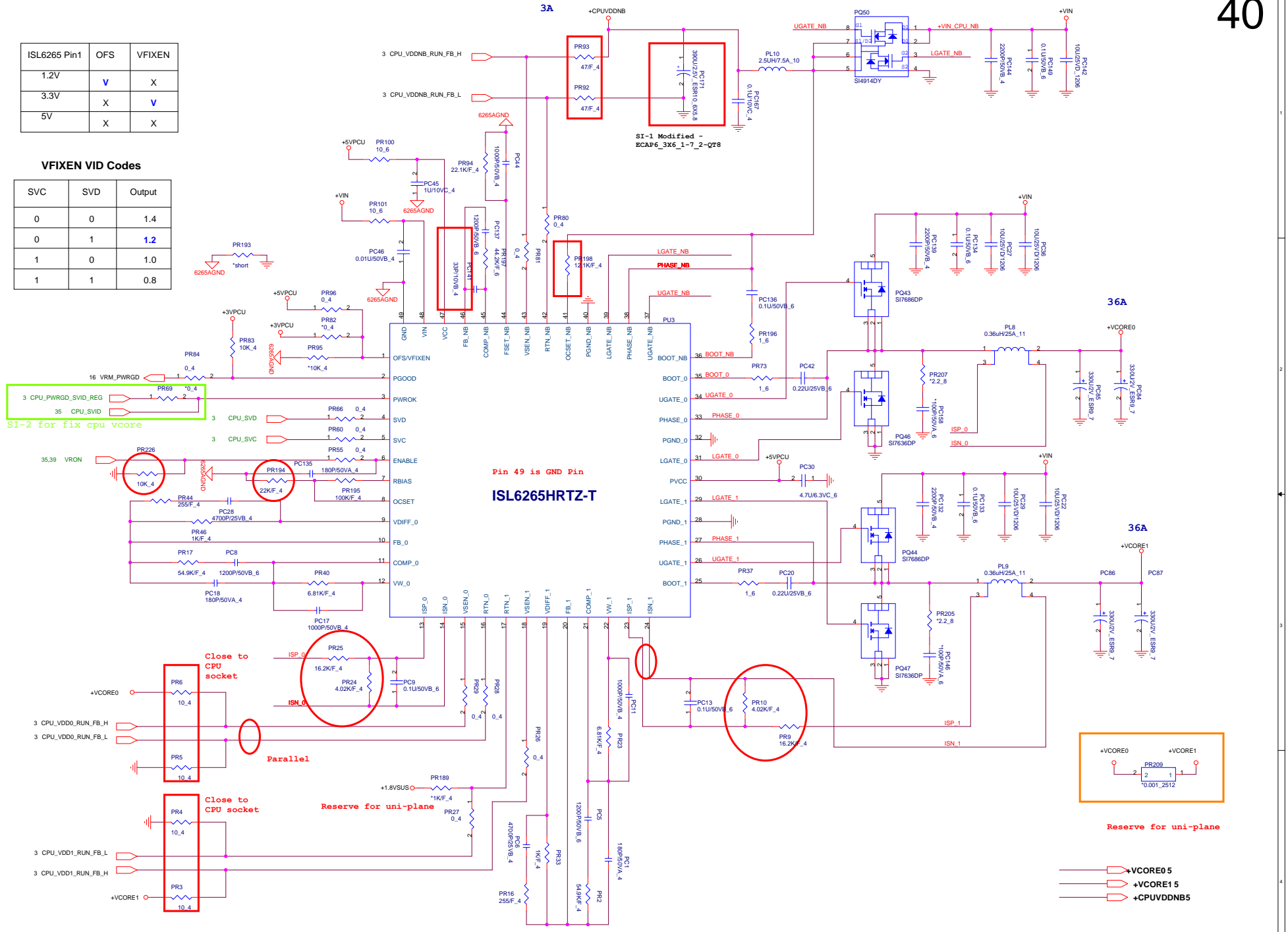
Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 1A
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

SI-2 for fix cpu vcore
 3 CPU_PWRGD_SVID_REG
 35 CPU_SVID



+2.5V 3
+1.8VSUS 3,4,5,6,7,40,42,43

+1.8VSUS
23.65A
S0~S3

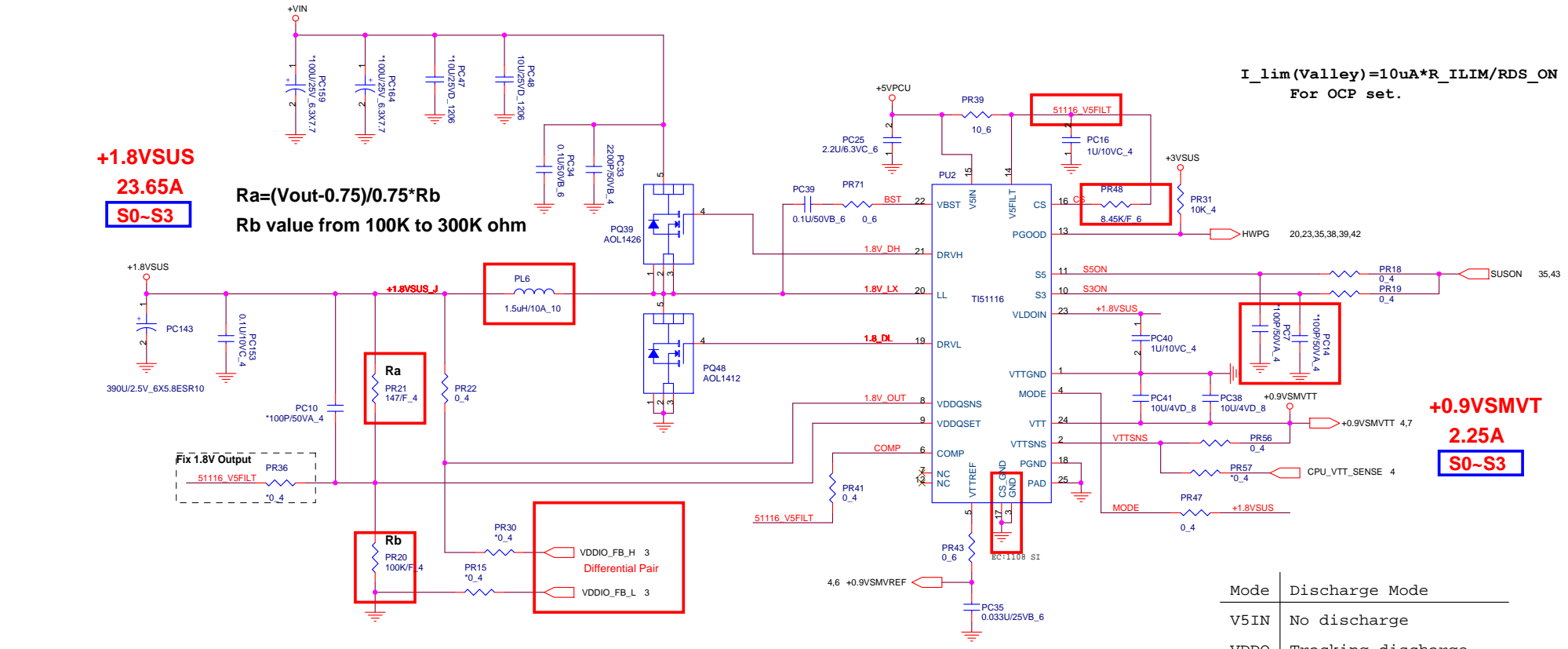
$Ra = (V_{out} - 0.75) / 0.75 * Rb$
Rb value from 100K to 300K ohm

$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS_ON}$
For OCP set.

+0.9VSMVT
2.25A
S0~S3

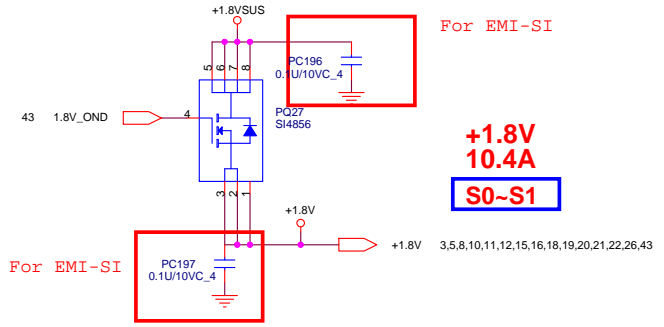
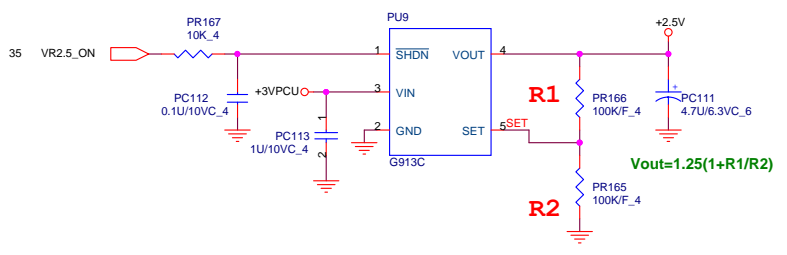
+2.5V
0.25A
S0~S1

+1.8V
10.4A
S0~S1



Fix 1.8V Output
51116_VSFILT

Close to CPU
SI power



Discrete: SI4856
UMA: SI4800

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_TRIP(mV) = R_TRIP(Kohm) * 10(\mu A)$

$I_OCP = V_trip / R_{ds_on} + I_Ripple / 2$

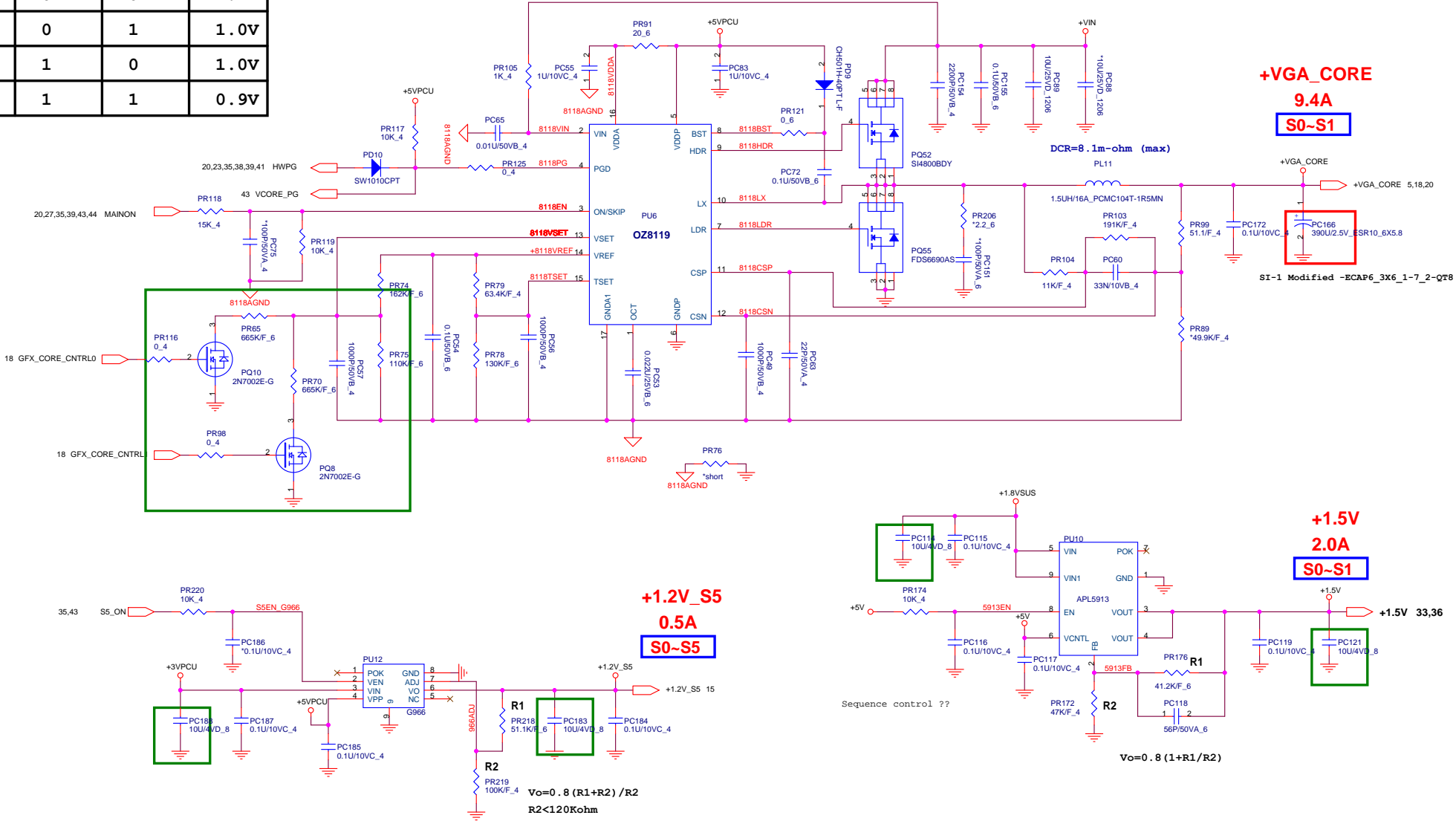
VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_vddqsns / 2$	DDR
V5IN	1.8	$V_vddqsns / 2$	DDR2
FB	adjustable	$V_VDDQSNS / 2$	$1.5V < VDDQ < 3V$


	PROJECT : QT8		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	1.8VSUS/DDR_VTER/+1.8V/2.5V	
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ATI M82-SE

-  +VGA_CORE5,18,20
-  +1.2V_S5 15
-  +1.5V 33,36

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V



+VGA_CORE 5,18,20

SI-1 Modified -ECAP6_3X6_1-7_2-QT8

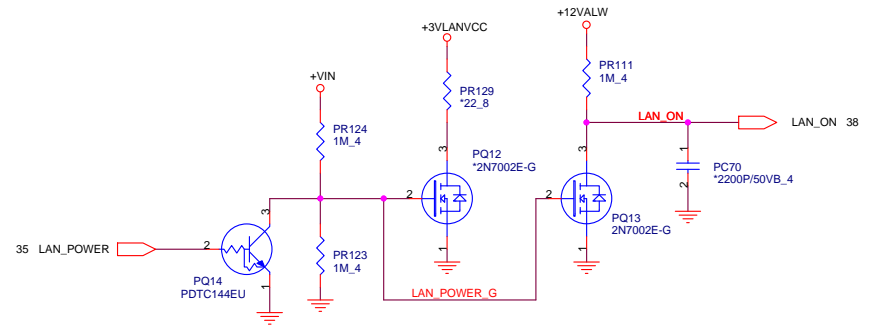
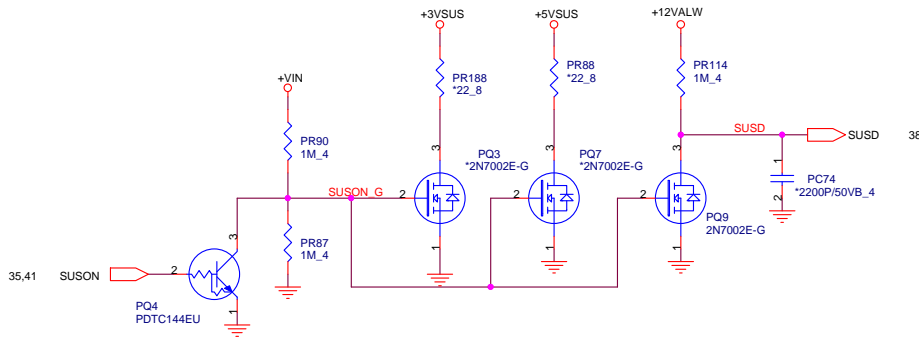
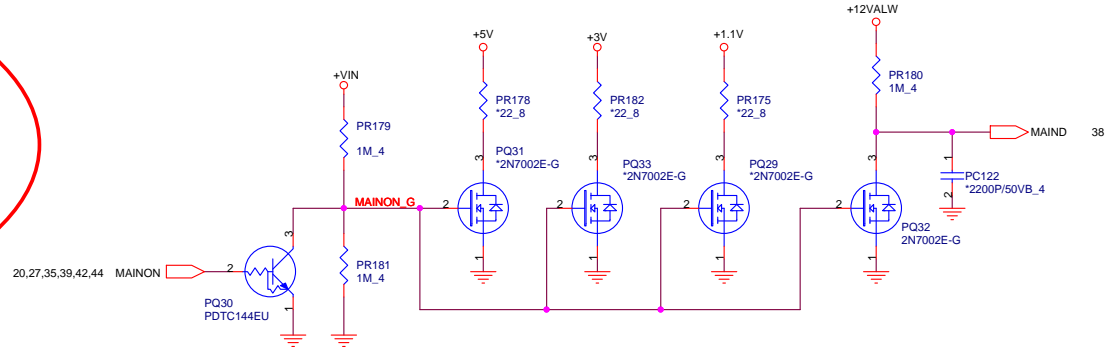
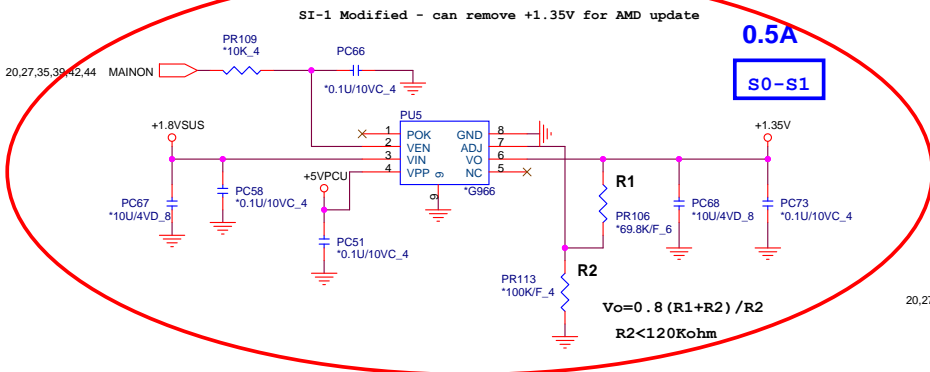
+1.2V_S5
0.5A
S0-S5

+1.5V
2.0A
S0-S1

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 Quanta Computer Inc.



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For Discrete Only

