N-Channel 1.8-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.018 @ V_{GS} = 4.5 V	7.2
	0.022 @ V_{GS} = 2.5 V	6.5
	0.025 @ V_{GS} = 1.8 V	6.0

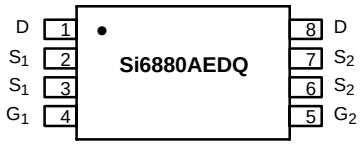
FEATURES

- TrenchFET® Power MOSFET
- ESD Protected: 3500 V
- Common Drain

APPLICATIONS

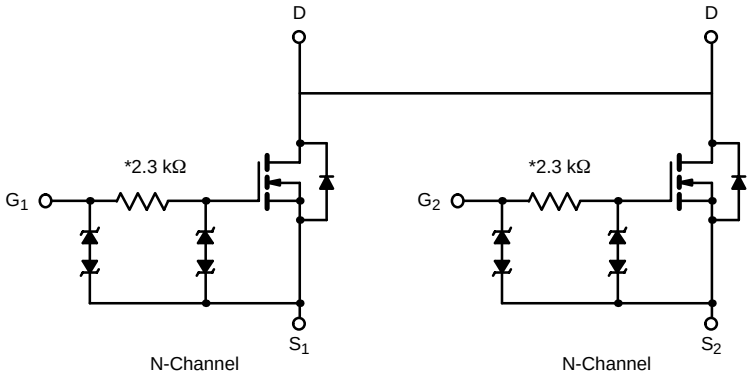
- 1-2 Cell Battery Protection Circuitry

TSSOP-8



Top View

Ordering Information: Si6880AEDQ-T1



N-Channel N-Channel

*Typical value by design

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	7.2	5.8	A
	T_A = 70°C		5.7	4.7	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	30		
Continuous Source Current (Diode Conduction)[a]		I_S	1.5	1.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	1.0	W
	T_A = 70°C		0.96	0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec.	R_{thJA}	70	83	°C/W
	Steady State		100	120	
Maximum Junction-to-Foot (Drain)[a]	Steady State	R_{thJF}	55	70	

Notes
a. Surface Mounted on FR4 Board.
b. t ≤ 10 sec.

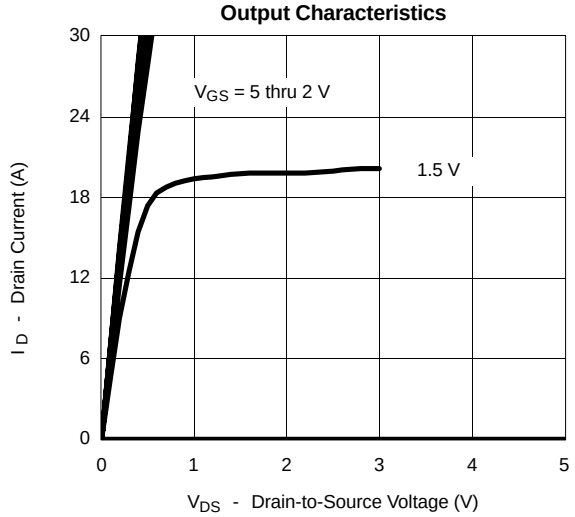
SPECIFICATIONS (T_J =25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	0.40		0.90	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±1	μA
		V_{DS} = 0 V, V_{GS} = ±12 V			±10	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 70°C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 7.2 A		0.014	0.018	Ω
		V_{GS} = 2.5 V, I_D = 6.5 A		0.016	0.022	
		V_{GS} = 1.8 V, I_D = 6.0 A		0.018	0.025	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 7.2 A		45		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.5 A, V_{GS} = 0 V		0.61	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 7.2 A		22	35	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		1.0	1.5	μs
Rise Time	t_r			1.6	2.5	
Turn-Off Delay Time	$t_{d(off)}$			6	10	
Fall Time	t_f			5.5	10	

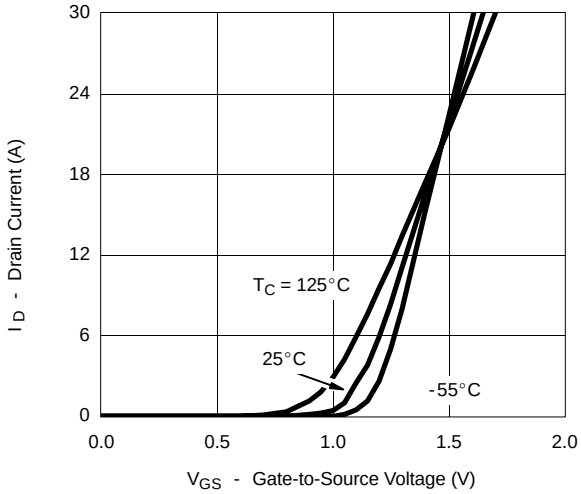
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

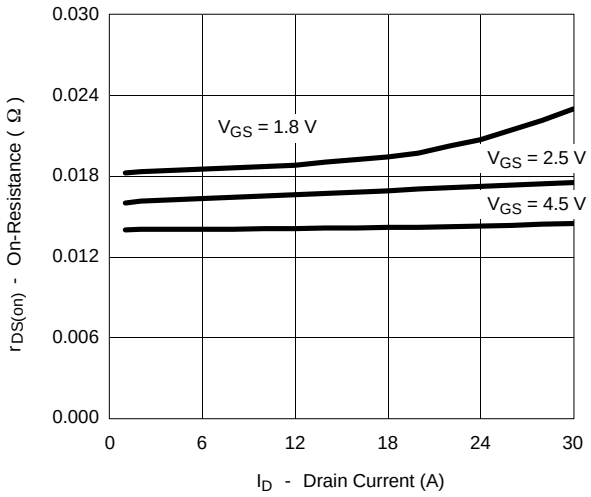


Transfer Characteristics

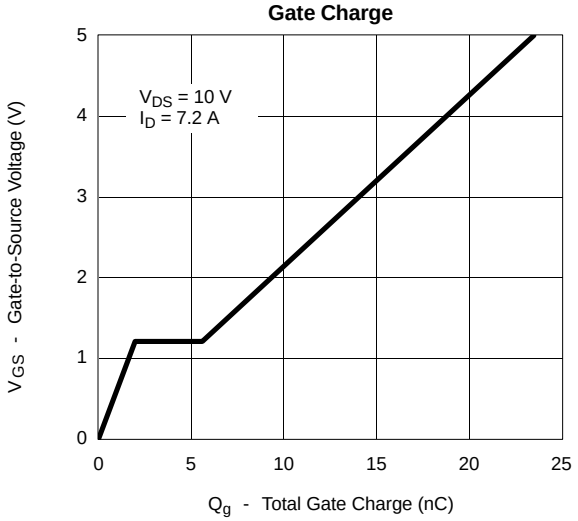


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

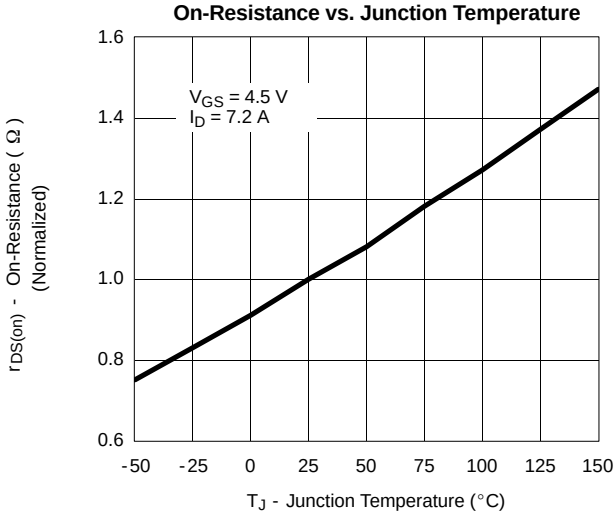
On-Resistance vs. Drain Current



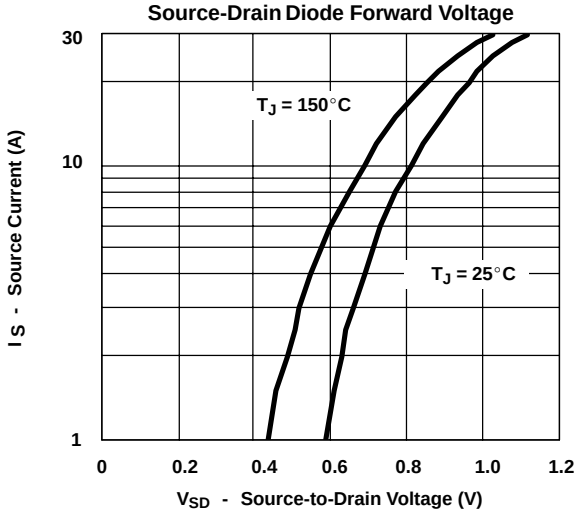
Gate Charge



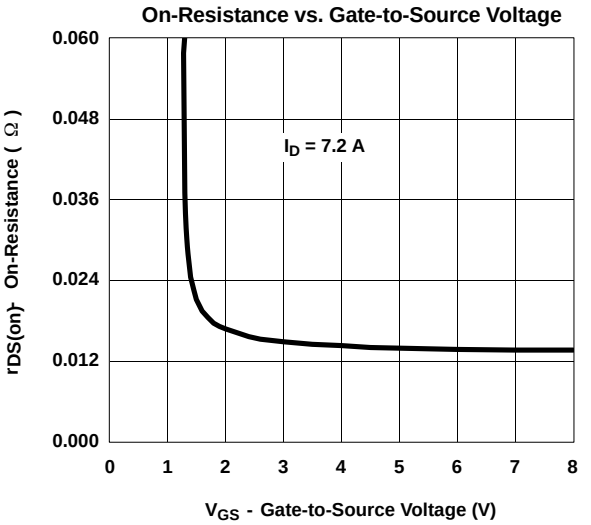
On-Resistance vs. Junction Temperature



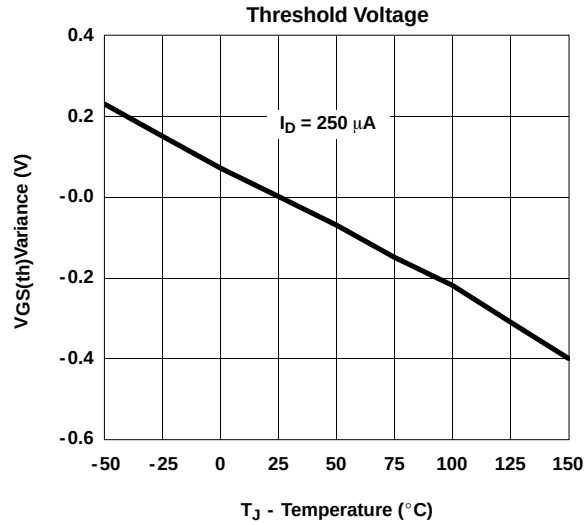
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

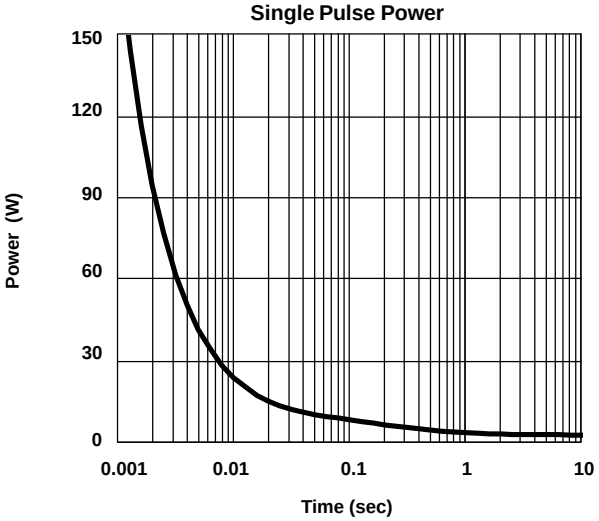


Threshold Voltage

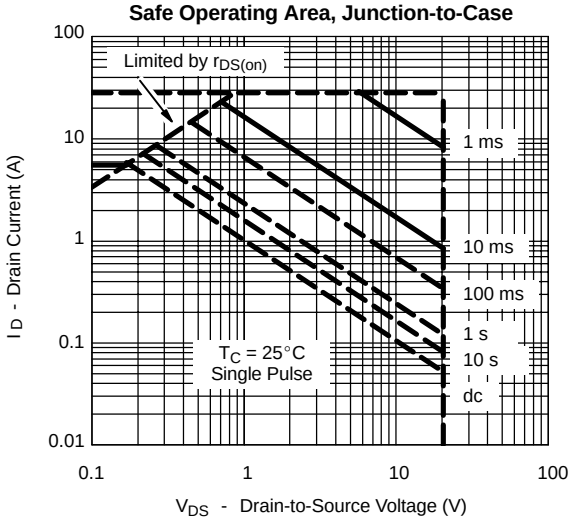


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

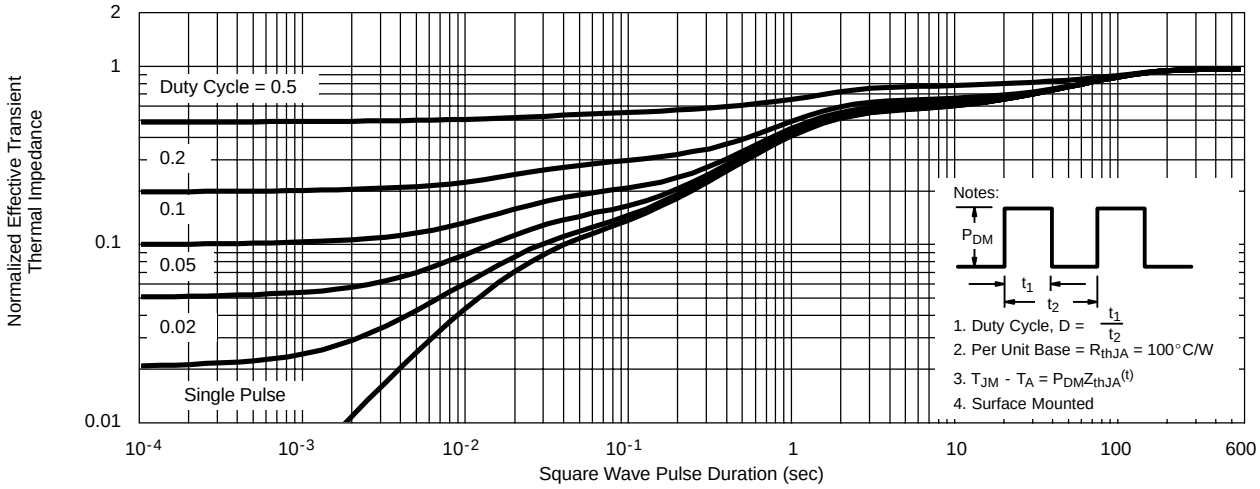
Single Pulse Power



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot