

This is trial version,
If you want get full version,please register it,thank you.

Web site:
<http://www.adultpdf.com/>

E-mail:
support@adultpdf.com



Terawins, Inc.

***Advanced Information
Version 0.2***

September 12, 2005

T101A Video Display Controller

Confidential

Table of Contents

1	INTRODUCTION	3
1.1	FEATURES	3
1.2	GENERAL DESCRIPTION	4
1.3	APPLICATIONS	4
1.4	SYSTEM ARCHITECTURE	5
1.5	SYSTEM CONFIGURATIONS	6
1.6	PINOUT DIAGRAM	7
1.7	PIN DESCRIPTION	9
2	THEORY OF OPERATIONS	12
2.1	I ² C COMMAND PROTOCOL	12
2.2	ANALOG FRONT END	14
2.3	Y/C SEPARATION AND CHROMA DECODER	14
2.4	DIGITAL COLOR TRANSIENT IMPROVEMENT (DCTI)	16
2.5	DIGITAL LUMINANCE TRANSIENT IMPROVEMENT (DLTI)	17
2.6	FIR SCALER	17
2.7	BLACK-LEVEL EXTENSION (BLE)	18
2.8	COLOR SPACE CONVERTER	18
2.9	GAMMA CORRECTION	19
2.10	OSD	20
2.11	TCON	33
3	REGISTER DESCRIPTION	36
3.1	ADC REGISTER SET	36
3.2	PICTURE ENHANCEMENT REGISTER SET	47
3.3	SCALING REGISTER SET	49
3.4	COLOR SPACE CONVERTER REGISTER SET	54
3.5	OSD REGISTER SET	57
3.6	LCD OUTPUT CONTROL REGISTER SET	57
3.7	TCON REGISTER SET	68
3.8	ITU-656 REGISTER SET	72
3.9	Y/C SEPARATION AND CHROMA DECODER REGISTER SET	75
4	ELECTRICAL CHARACTERISTICS	83
4.1	DIGITAL I/O PAD OPERATION CONDITION	83
4.2	OUTPUT CLOCK, VIDEO DATA, TCON TIMING	84
4.3	I ² C HOST INTERFACE TIMING	85
4.4	ANALOG PROCESSING AND A/D CONVERTERS	86
4.5	ABSOLUTE MAXIMUM RATING	86
5	PACKAGE DIMENSIONS	87
6	ORDERING INFORMAT	89
7	REVISIONS NOTE	89
8	GENERAL DISCLAIMER	89
9	CONTACT INFORMATION	90

1 Introduction

1.1 Features

■ Cost Effective Highly Integrated Triple ADCs + 2D Video Decoder + OSD + VBI Data Decoder+ Scaler + TCON

- Integrates 9-bit Triple Analog to Digital Converters (ADC) & Phase Locked Loop (PLL)
- Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ratio.
- Requires no external Frame Buffer Memory for deinterlacer.
- Advanced On Screen Display (OSD) function
- Programmable Timing Controller (Tcon) for Car TV applications
- Multi-standard color decoder with 2D adaptive comb filter
- Innovative and flexible design to reduce total system cost

Triple 9-bit Analog to Digital Converters (ADC)

■ 27MSPS Conversion Rate

- Built-in Pre-amp, mid-level & ground clamp circuit
- Automatic Clamp Control for CVBS, Y and C
- Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
- Max Input configuration up to 9xCVBS, 3xS-video and 3xCVBS, 3xYPbPr,

Digital Video Enhancement

■ Separate Luminance and Chroma Enhancer

- Y Supports Luminance Peaking, DLTi, Black Level Expansion, Contrast and Brightness adjustment
- C Supports DCTi, Saturation and Hue adjustment.

Advanced Scaling Engine

■ Two Dimensions FIR Scaler

- Coefficient based sharpness filters
- 2-D edge enhancement
- Independent vertical and horizontal scaling ratio
- 16:9 Non-linear Aspect ratio

■ LCD Interface

- Provides Gamma correction for panel compensation
- Supports image pan functions
- Programmable Timing Controller
- RGB Single Channel output

■ Color Management

- YcbCr-to-RGB Color Space Converter
- RGB Gamma Correction
- Dithering engine converts
RGB888 to RGB777
RGB888 to RGB666
RGB888 to RGB555
RGB888 to RGB444

■ Built-in On Screen Display Engine

- 3K-word OSD SRAM memory
- Supports font or bitmap modes
- Supports character blinking, overlay, shadow and border functions
- Fully programmable character mapping
- Supports alpha blending & Zoom-in/Zoom-out function
- Optional fonts can be stored in off-chip serial EEPROM

■ Versatile VBI Data Decoder

- Supports Close Caption, Wide Screen Signalling and Teletext

■ Crystal Oscillator Circuit

- Direct interface to a (27.0MHz) Crystal
- Also provide a buffered clock output for external Micro-controller

■ Digital Test Pattern Generator

- Programmable standard & special panel burn-in test patterns
- Support special border frame blocking mode

■ Independent Display Phase Lock Loop

- Generates pixel clock output to panel
- Supports free run OSD mode

■ Flexible Data Output Formatting

- Four software configurable output modes:
 1. 8-bit mode = SerialRGB & 1pixel/3clocks
 2. 18-bit mode = R6G6B6 & 1 pixel/clock
 3. 24-bit mode = R8G8B8 & 1 pixel/clock
 4. Progressive or Interlaced 24-bit 4:4:4 YCbCr mode
- Complex output data bits swap, reverse, re-direct capability to reduce PCB layout work
- Selectable LVDS output data re-mapping

- **Serial Bus Interface**
 - Supports 2-wire (normal speed) or 4-wire (high speed) modes
- **Pulse Width Modulation Outputs**
- **Design For Testability**
 - Scan chain insertion
 - Separated analog & digital test modes
- **Power Supply: +2.5V & +3.3V**
- **Package: 100-pin PQFP or 100-pin TQFP**

1.2 General Description

The T101A is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T101A has built-in high performance Triple ADCs, TCON, Scaling Machine with sophisticated upscaling and downscaling algorithms. The innovative integrated

“Frame-Buffer-Less” De-interlacer can significantly reduce system cost. The T101A also integrates On Screen Display engine with 3K-DW of font RAM. The device can interface to an external micro-controller through 2-wire serial bus interface.

1.3 Applications

1. 10-inch portable DVD or in-car TV
2. 20-inch LCD TV

1.4 System Architecture

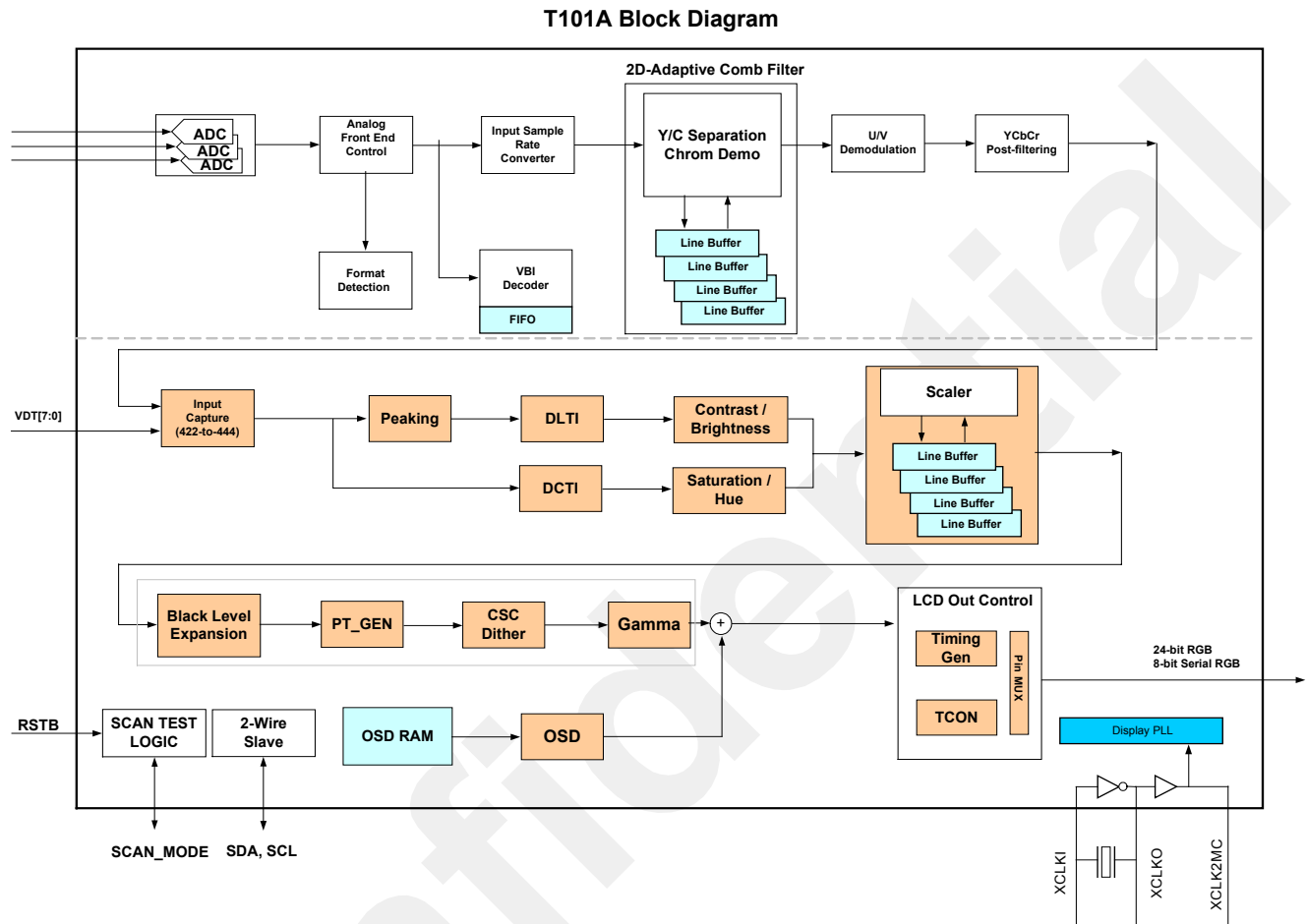


Figure 1-1 System Architecture

1.5 System Configurations

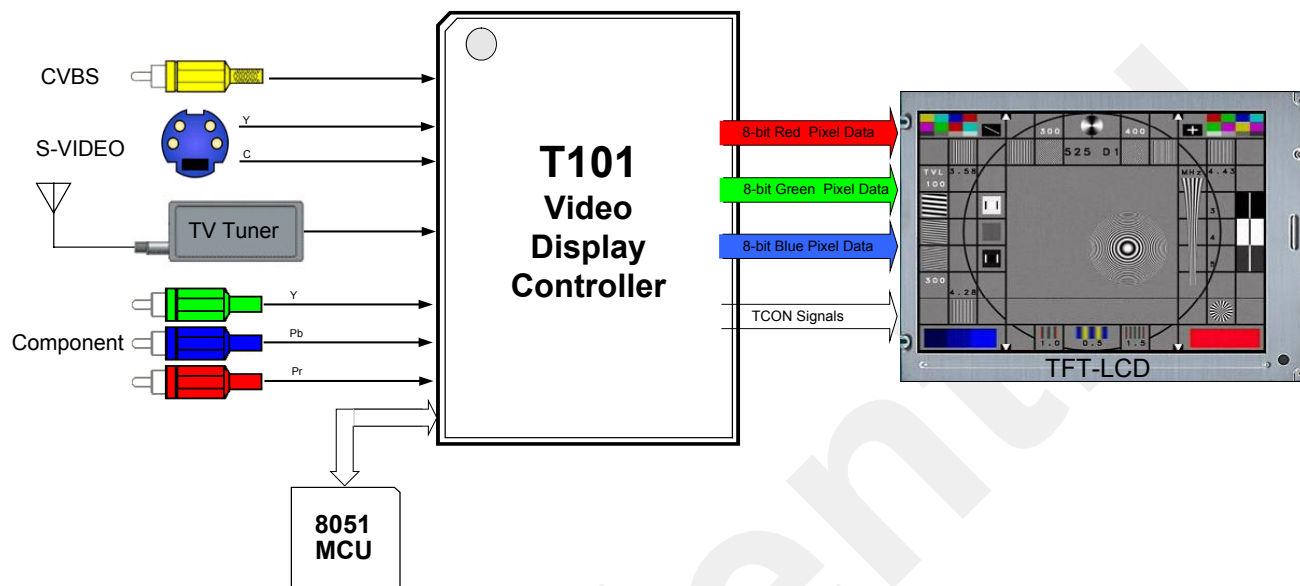


Figure 1-2 System Configurations

1.6 Pinout Diagram

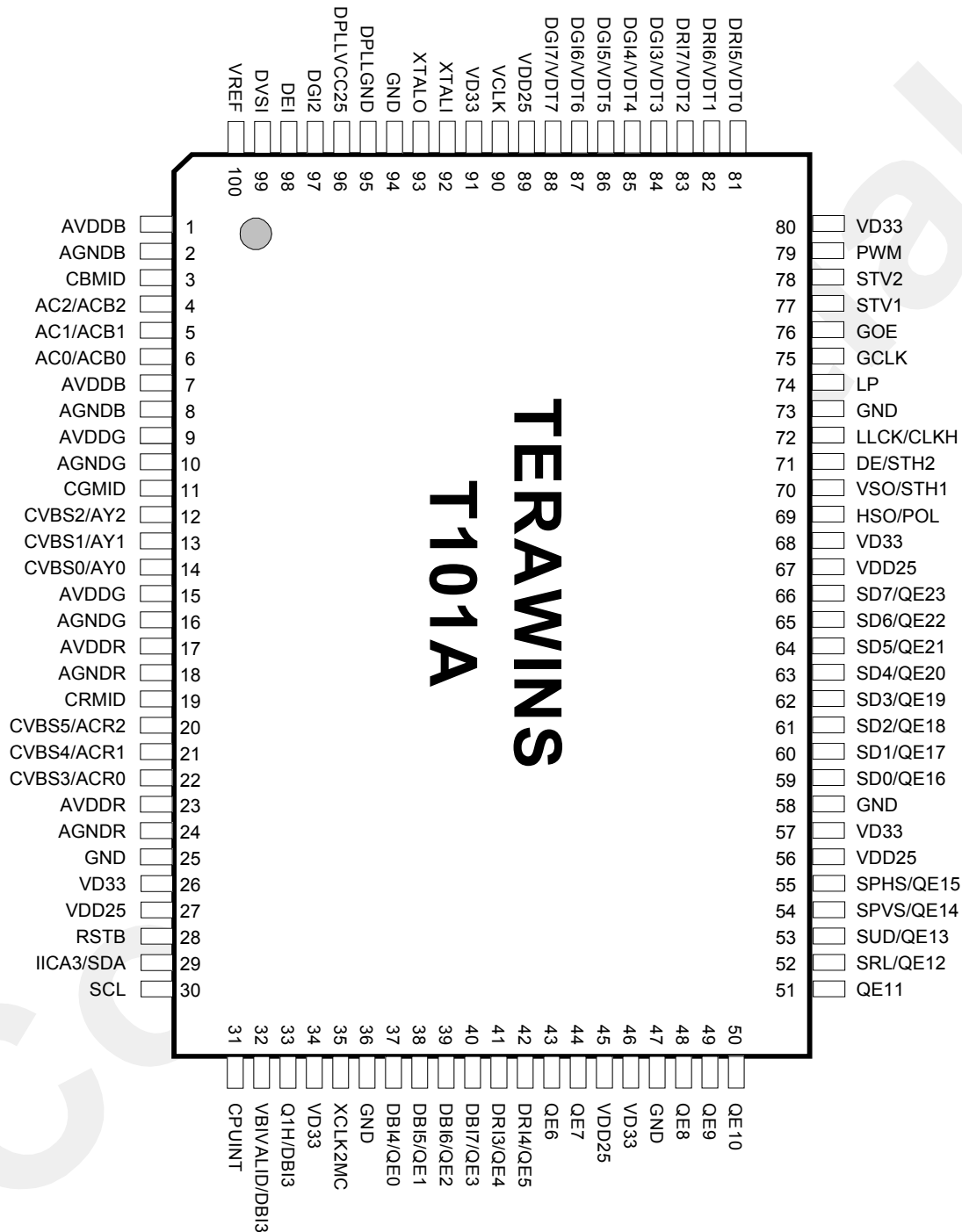


Figure 1-3 PQFP Pinout Diagram

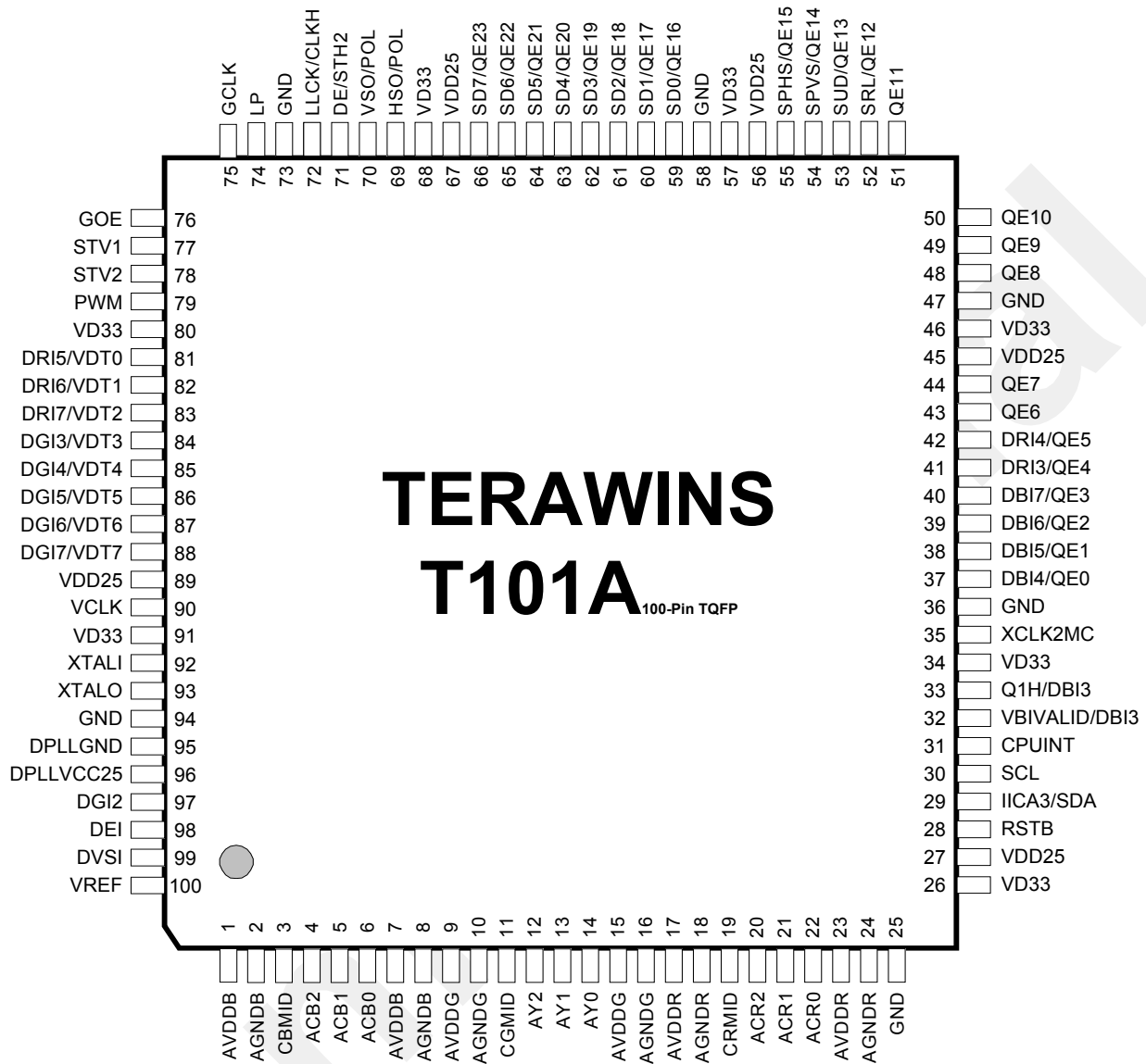


Figure 1-4 TQFP Pinout Diagram

1.7 Pin Description

Table 1-1 Pin Description

Symbol	Pin #	Type	Description
Power Supplies			
VDD25	27, 45, 56, 67, 89, 96	PWR	+2.5V Digital Core Power Supply
VD33	26, 34, 46, 57, 68, 80, 91	PWR	+3.3V Digital Output Power Supply
AVDDDB	1, 7	PWR	+3.3V Analog Power Supply for ADC channel 2
AVDDG	9, 15	PWR	+3.3V Analog Power Supply for ADC channel 1
AVDDR	17, 23	PWR	+3.3V Analog Power Supply for ADC channel 0
GND	25, 36, 47, 58, 73, 94, 95	GND	Digital Ground
AGNDB	2, 8	GND	Analog Ground for ADC channel 2
AGNDG	10, 16	GND	Analog Ground for ADC channel 1
AGNDR	18, 24	GND	Analog Ground for ADC channel 0
Digital Output Bus Interface Signals			
QE[23:0]	37– 44, 48 – 55, 59 – 66	DO	Pixel Data Output 23~0. QE[23:16] = RE[7:0], QE[15:8] = GE[7:0], QE[7:0] = BE[7:0]. The output data is synchronized with the Output Data Clock (LLCK). When the T101 enters Power Down/Pull Down mode, the QE[23:0] data output drivers can be tri-stated. There are internal pull-down resistors on each output pins. When the data driver is tri-stated, all output pins will be pulled to ground. For RGB-565 input mode, QE[5:0] becomes input ports, QE[5] =DRI4 QE[4] =DRI3 QE[3] =DBI7 QE[2] =DBI6 QE[1] =DBI5 QE[0] =DBI4
DE	71	DO	Output Data Enable. This signal indicates that the data is ready. During the active display time, the DE pin MUST be high. During the blanking period, the DE pin MUST be low.
LLCK	72	DO	Output Data Clock
VSO	70	DO	Vertical Synchronization Output Control Signal.
HSO	69	DO	Horizontal Synchronization Output Control Signal.
Timing Controller Interface Signals			
LP	74	DO	Latch pulse for column driver
GCLK	75	DO	Gate driver clock
GOE	76	DO	Gate driver output enable
STV1	77	DO	Gate driver start pulse
STV2	78	DO	Gate driver start pulse
Q1H	33	DI/O	Source Driver Q1H For RGB-565 input mode, this pin becomes input port for DBI3 See register P0_E3[3] and P0_E1[1] for detail
2-wire serial bus Interface Signals			
SCL	30	DI	2-wire serial bus clock. Power down does not affect SCL.

Symbol	Pin #	Type	Description
			Need external 10K ohm P/U.
SDA	29	I/O	2-wire serial bus data. Power down does not affect SDA.
Configuration interface Signals			
CPUINT	31	I/O	Internal Interrupt.
RSTB	28	DI	Whole chip reset. (Internal Pull-up)
Test Pins			
FILED	33	DO	Field flag
VBIVALID	32	DO	VBI data valid For RGB-565 input mode, this pin becomes input port for DBI3 See register P0_E3[3] and P0_E1[1] for detail
ADC Interface			
ACB2	4	AI	Analog input 2 of channel 2
ACB1	5	AI	Analog input 1 of channel 2
ACB0	6	AI	Analog input 0 of channel 2
AY2	12	AI	Analog input 2 of channel 1
AY1	13	AI	Analog input 1 of channel 1
AY0	14	AI	Analog input 0 of channel 1
ACR2	20	AI	Analog input 2 of channel 0
ACR1	21	AI	Analog input 1 of channel 0
ACR0	22	AI	Analog input 0 of channel 0
Video-In Interface			
VCLK	90	DI/O	ITU-656 video clock
VDT0	81	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DRI5
VDT1	82	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DRI6
VDT2	83	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DRI7
VDT3	84	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DGI3
VDT4	85	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DGI4
VDT5	86	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DGI5
VDT6	87	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DGI6
VDT7	88	DI/O	ITU-656 video port For RGB-565 input mode, this pin becomes input port for DGI7
RGB 565 Interface			
DEI	98	DI	Input data enable
DVSI	99	DI	Input Vsync
DGI2	97	DI	Input Green bit 2
PLL Reference Clock			
XTALI	92	DI	Output PLL reference clock input
XTALO	93	DO	Output PLL reference clock output
XCLK2MC	35	DO	Buffered XTALI for external microprocessor

Symbol	Pin #	Type	Description
Power Management Interface Signals			
PWM	79	DO	Pulse Width Modulation for backlight control

2 Theory of Operations

2.1 I²C Command Protocol

Before your tester writes I²C commands to T101, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. SDA(A3) can affect slave address. Set low for 40h. Set high for 50h.

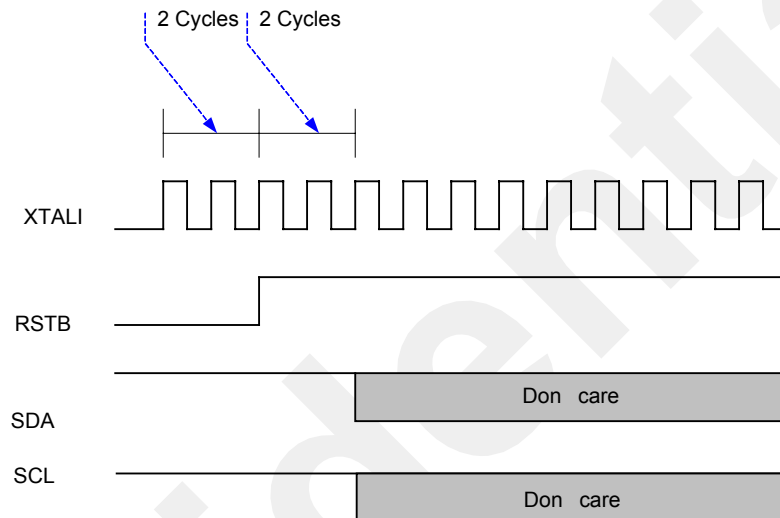


Figure 2-1 Power-up initialization

When tester issues commands to the T101, the only way the user can program the T101 is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. **The frequency of SCL can be from 50 KHz up to 1 Mhz.**

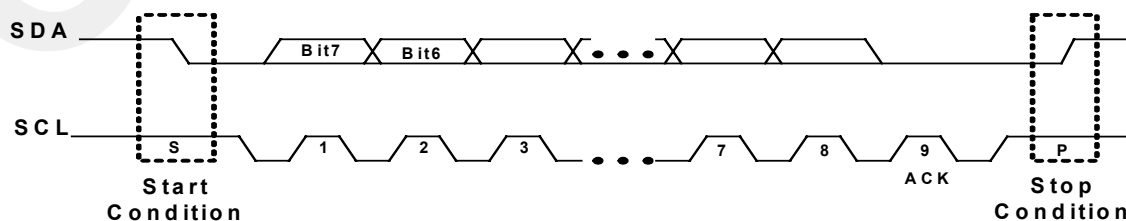


Figure 2-2 2-wire serial bus protocol

The timing below shows a typical T101 IIC single byte write command,

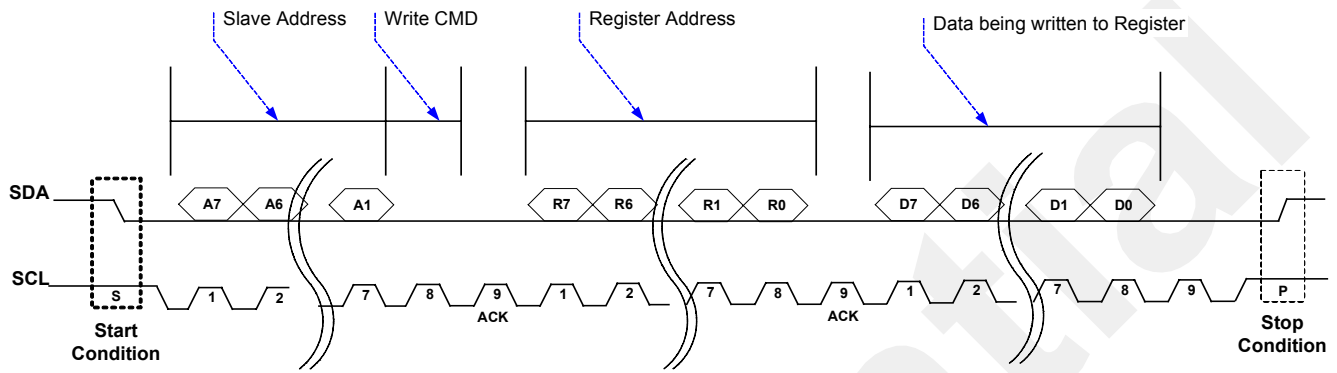


Figure 2-3 T101 IIC single byte write command

The timing below shows a typical T101 IIC single byte read command,

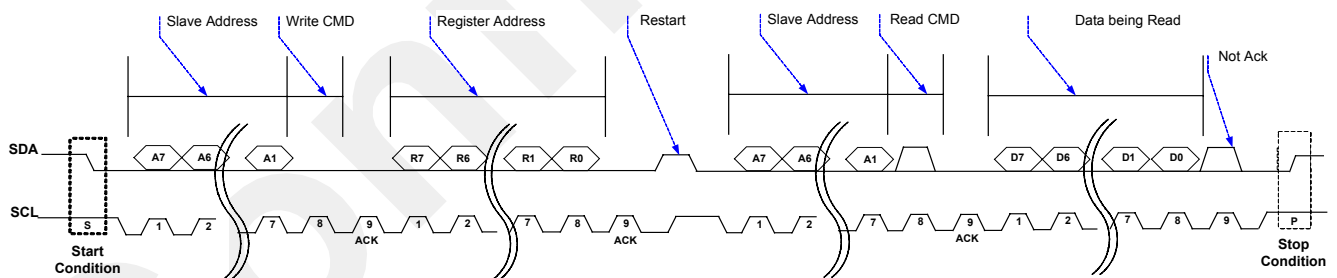


Figure 2-4 T101 IIC single byte read command

2.2 Analog Front End

T101 contains 3 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV signals from analog to digital. The figure shown below can describe how to select a SDTV signal from 3 inputs prior to ADC.

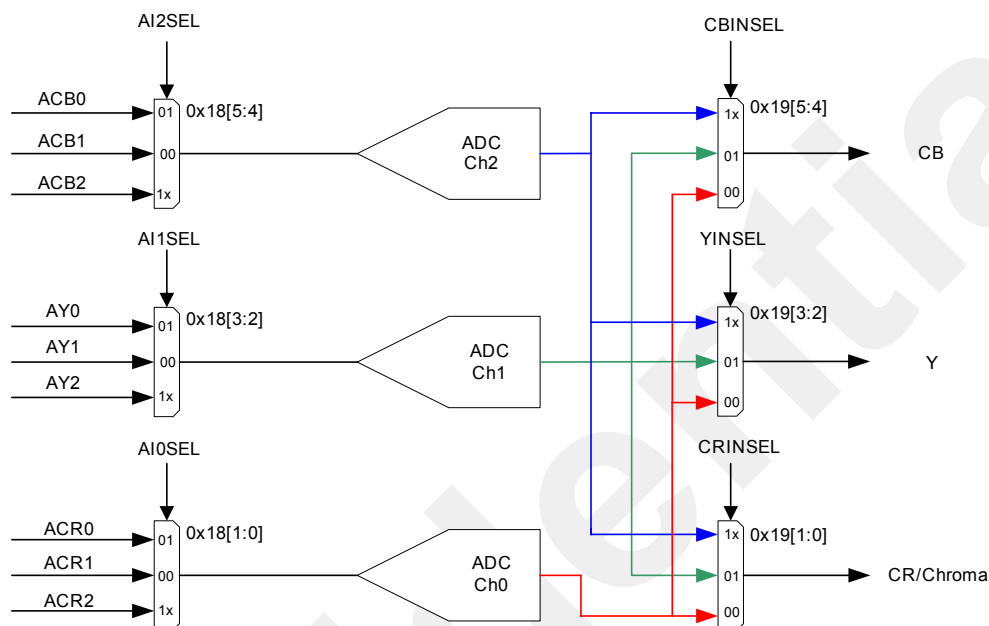


Figure 2-5 Analog Front End

2.3 Y/C Separation and Chroma Decoder

A composite video has luma(Y) and chroma(C) information mixed in the same video signal. This video signal can also be represented by the equation below,

$$CVBS = Y + U * \sin(wt) + V * \cos(wt)$$

Where $w = 2\pi f_{SC}$, $f_{SC} = 3.58\text{Mhz}$ if NTSC, $f_{SC} = 4.43\text{Mhz}$ if PAL

The figure below shows a typical composite signal. The 2-D adaptive comb filter inside T100 is designed to separate Y and C from a composite video signal.

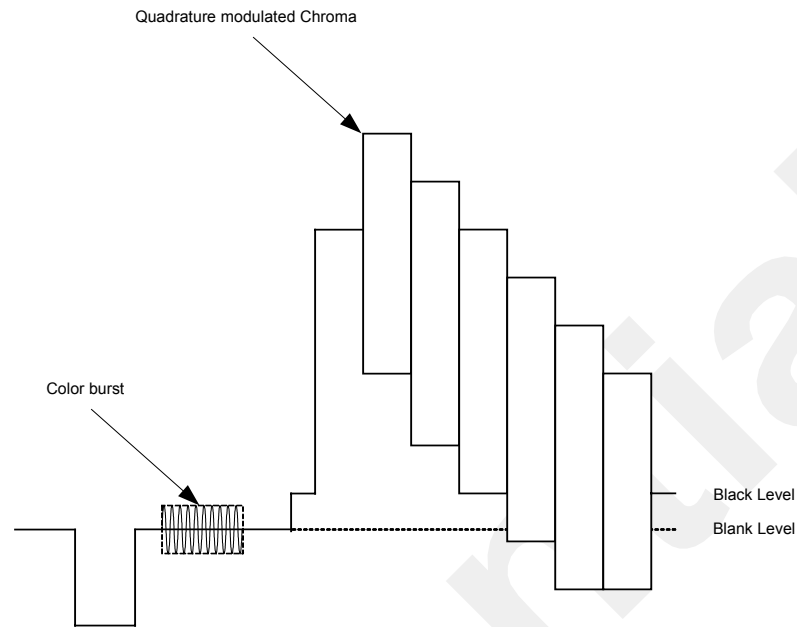


Figure 2-6 Typical Color SDTV Signal

. The conventional 3-line comb filter fails to separate Y and C if there is a vertical transition. The 2-D adaptive comb filter is based on equally weighting factors that color changes along vertical and horizontal edges. Let the amount of color change along vertical and horizontal direction DC_v and DC_h , the weighting factors can be expressed as following equations,

$$W_h = \frac{DC_v}{DC_v + DC_h}$$

$$W_v = \frac{DC_h}{DC_v + DC_h}$$

By employing adaptive method, chroma can be recovered by following equation,

$$C = Ch * W_h + C_v * W_v$$

After Y/C separation, Y and C should look like waveforms shown as in following figure. Y only contains low frequency part, while C contains high frequency part that is centered around sub-carrier f_{sc} .

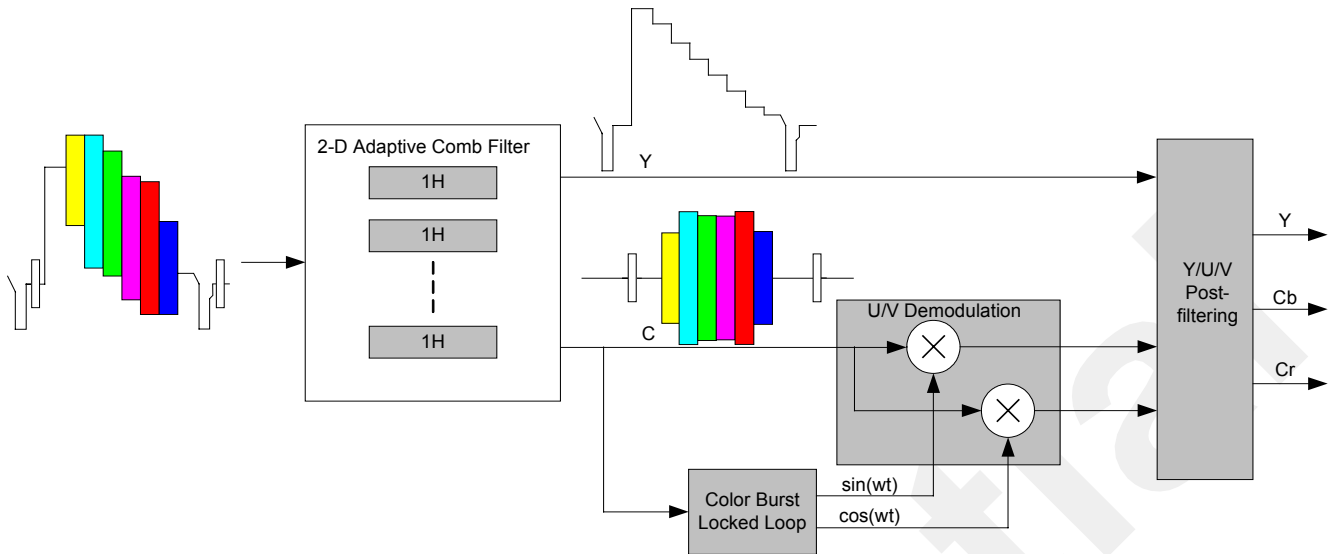


Figure 2-7 Typical Color SDTV Signal

2.4 Digital Color Transient Improvement (DCTI)

Usually, a composite or S-video SDTV signal may have bandwidth limitation that causes the loss chroma detail around two different color bars. Two pictures shown below illustrate the result before and after DCTI block. Without DCTI (the upper picture), we may see color transient wider than several pixels. A slow transient edge usually blurs image. T101 DCTI algorithm can sharpen those color transient edges. The lower picture shows that chroma data is enhanced by increasing the slope of edge transient without introducing the ring effects.



Figure 2-7 Comparison of DCTI

2.5 Digital Luminance Transient Improvement (DLTI)

The Digital Luminance Transient Improvement is intended to sharpen luminance edge transient. The figure shown below is DLTI transfer function. DLTI doesn't increase peak-to-peak amplitude; rather it turns sloped waveforms into rectangular waveforms.

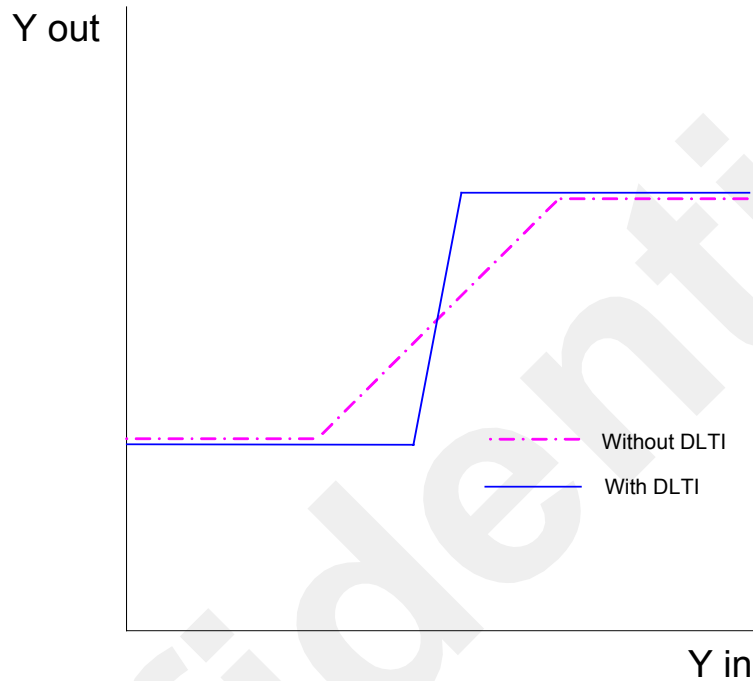


Figure 2-8 DLTI Transfer Curve

2.6 FIR Scaler

FIR Scaler can scale input H/V sizes to fit any LCD panel resolution. The flexible and independent H/V scalers allow users to program display area in 16:9 full mode, 16:9 non-linear wide mode and 4:3 mode. FIR scaler also provides coefficient-based 2-D sharpness that can sharpen detail of picture.

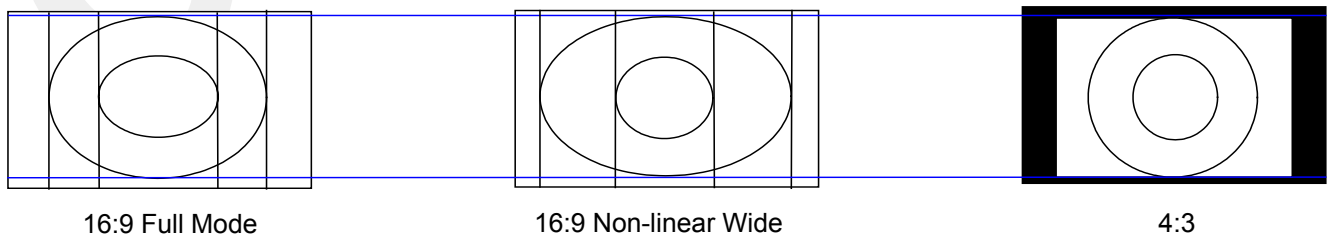


Figure 2-9 Practical Applications of FIR Scaler

2.7 Black-Level Extension (BLE)

Black Level Expansion (BLE) can enhance image contrast that makes dark regions of image darker, while bright regions remain unchanged. The figure shown below is BLE transfer function.

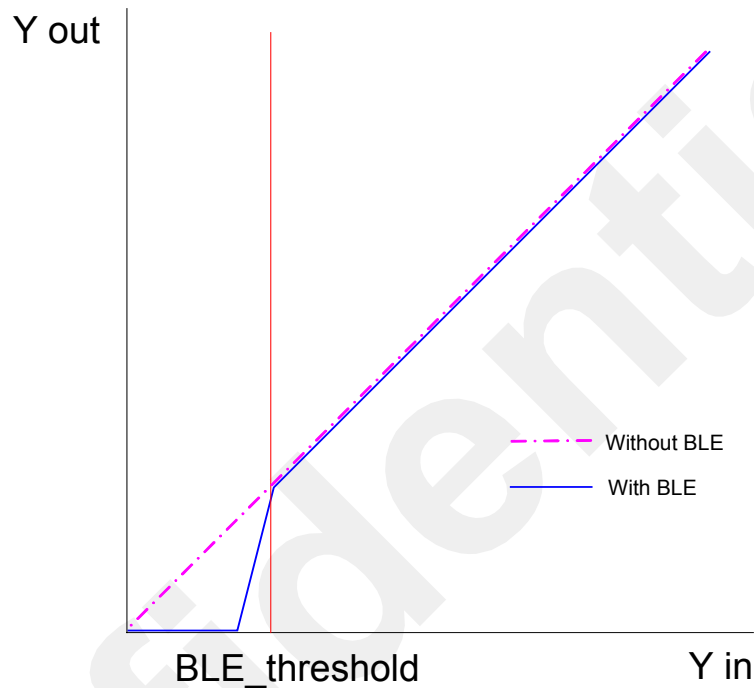


Figure 2-10 BLE Transfer Curve

$$Y_{out} = Y_{in} - (Y_{offset} - Y_{in}) * BLE_Gain / 16$$

Where Y_{offset} and BLE_Gain can be programmed by register P0_96h.

2.8 Color Space Converter

A pixel in YCbCr color space can be converted to RGB color space by using following equations,

$$R = YCoefCSC * (Y - 16) + CrCoef_R * (Cr - 128)$$

$$G = YCoefCSC * (Y - 16) - CrCoef_G * (Cr - 128) - CbCoef_G * (Cb - 128)$$

$$B = YCoefCSC * (Y - 16) + CbCoef_B * (Cb - 128)$$

Where $YCoef_{CSC}$ is in 1.7-bit fixed point with default 1.164. $CrCoef_R$ in 1.7-bit fixed point with default 1.596. $CrCoef_G$ in 0.8-bit fixed point with default 0.813. $CbCoef_G$ in 0.8-bit fixed point with default 0.392. $CbCoef_B$ in 2.6-bit fixed point with default 2.017

The equations shown as below correspond to a typical YCbCR-to-RGB converter. In T101, we make those coefficients adjustable.

$$R = 1.164 * (Y - 16) + 1.596 * (Cr - 128)$$

$$G = 1.164 * (Y - 16) - 0.813 * (Cr - 128) - 0.392 * (Cb - 128)$$

$$B = 1.164 * (Y - 16) + 2.017 * (Cb - 128)$$

2.9 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,

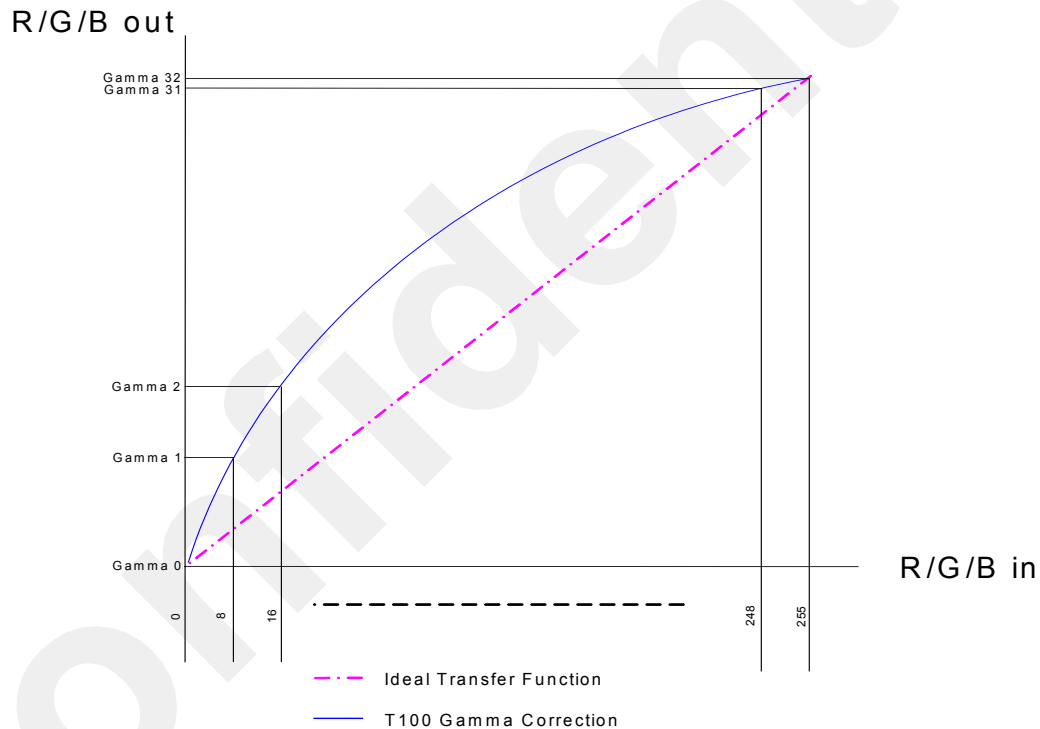


Figure 2-11 Gamma Transfer Curve

T101 uses 33-point piece-wise linear interpolation instead of RAM-based LUTs. Each point can be programmed via register at P0_93h and P0_94h.

2.10 OSD

2.10.1 OSD Access

Table 2-1 OSD Access

I/O Port	Index	Default	Description
A0h – Cfg_Index A1h – Cfg_Data	00h	00h	OSD Control Register
	01h	00h	Character Delay_1
	02h	10h	Character Delay_2
	03h	08h	Character Delay_3
	04h	09h	Character Font Size
	05h	50h	Char_RAM Base Address
	06h	00h	Character Border / Shadow Control
	07h	00h	Character Border / Shadow Color
	08h	20h	Character Height Scaling
	09h	0Ah	Blinking Control
	0Ah	00h	Bit_Map Window Size : Width/Height Upper Bits
	0Bh	80h	Bit_Map Window Size : Width
	0Ch	60h	Bit_Map Window Size : Height
	0Dh	11h	Bit_Map Dot Enlarge
	0Eh	-	OSD LUT RAM Data R/W, address automatically increased after R or W
	0Fh	00h	Char RAM Byte Access Control
	10h	00h	Window_1 Start Character Row Number / BMP Start Address LSB
	11h	00h	Window_1 End Character Row Number / BMP Start Address MSB
	12h	00h	Window_1 Start Character Column Number
	13h	00h	Window_1 End Character Column Number
	14h	00h	Window_1 Shadow Size
	1Ah	00h	Char2BP Base Address LSB
	1Bh	08h	Char2BP Base Address MSB
	1Ch	00h	Alpha Blending Control (available Revision >=02h)
	1Dh	03h	Revision ID
	1Eh	60h	Char_RAM Stop Address (available Revision >=01h)
	Other	00h	Reserved
A2h – ORAM_AL		00h	OSD RAM Low Address Port of Starting Access
A3h – ORAM_AH		00h	OSD RAM High Address Port of Starting Access
A4h – ORAM_D		00h	OSD RAM Data Port (Low Byte first, then High Byte). After two R/W, the address will be increased by 1.

2.10.2 RAM Addressing A[11:0]

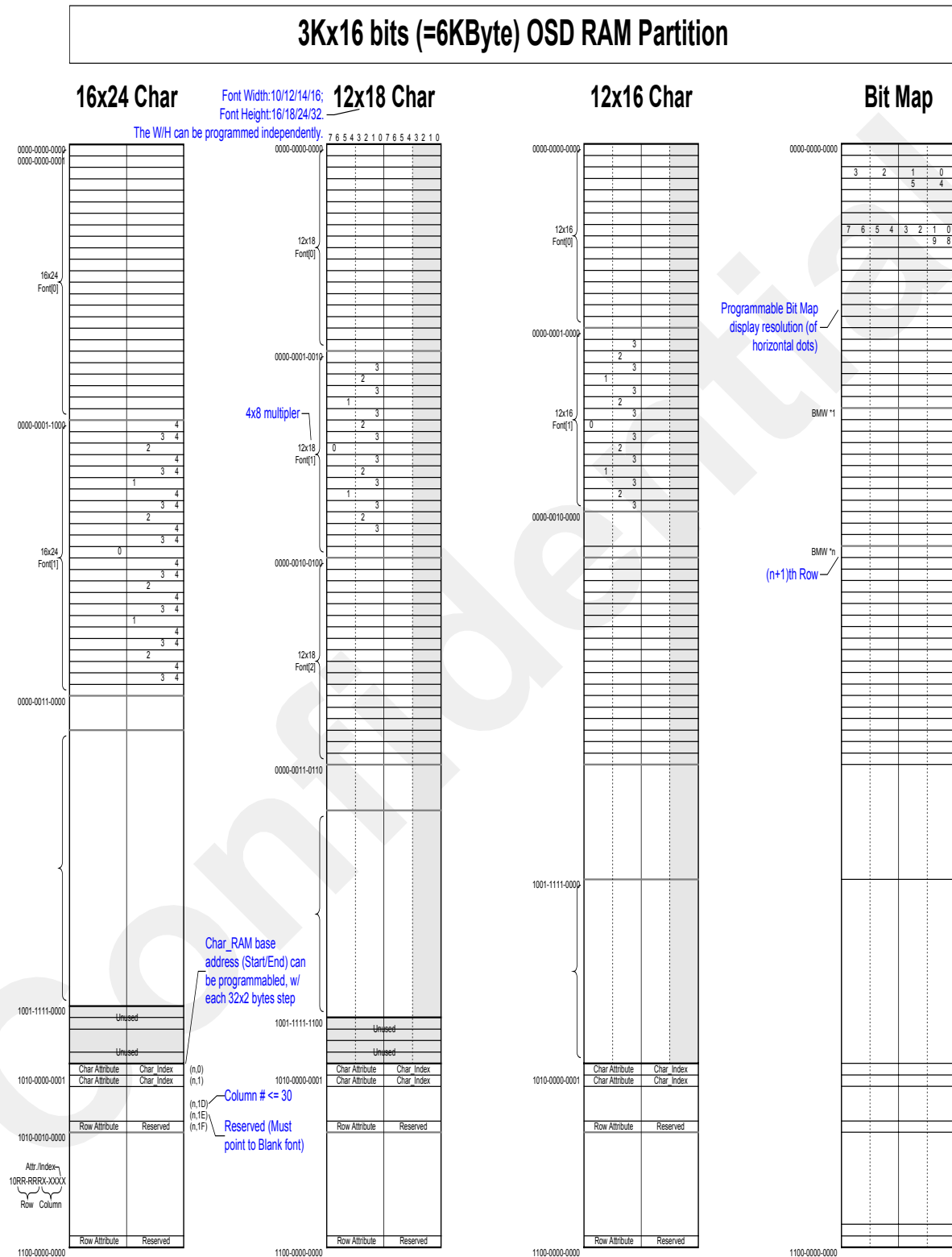


Figure 2-12 OSD RAM Partition

2.10.3 Character RAM Format

In Character Mode (contrast to Bit_Map Mode), the Characters displayed on OSD can be grouped to few rows, each row has its own row attribute (the high byte of Word #1F_h, ref. Section 2.10.3.3) which defines the behavior of current character row. And, there is maximum 30 characters in one row (Word #00_h ~ #1D_h), each character has two bytes to define its character font number (ref. Section 2.10.3.1) and its colors (ref. Section 2.10.3.2). And the Word #1E_h is reserved, which must be filled with transparent color and pointed to blank font.

2.10.3.1 Character Data (Address to Font Select) (Default=XXXXXXXXb¹)

Table 2-2 Character Data

7	6	5	4	3	2	1	0
CHRA[7]	CHRA[6]	CHRA[5]	CHRA[4]	CHRA[3]	CHRA[2]	CHRA[1]	CHRA[0]
Bit 7-0 CHRA[7:0] – Character Address (Index), selects the character font (i.e., 0,1,2,.. A,B,C, a,b,c,\$,%,...). If the value is number N, then it selects the N th font, and that font starting address is (N x Font_Height). The Font_Height is defined in Cfg_04h<4:3> (ref. Section 0). Index 00h~BFh for indexing 1BP (mono colored) fonts. Index: C0h~FFh for indexing 2BP (color) fonts							

2.10.3.2 Character Attribute (Default=XXXXXXXXb)

Table 2-3 Character Attribute

7	6	5	4	3	2	1	0
BG_R	BG_G	BG_B	Blink	FG_R	FG_G	FG_B	FG_I
Bit 7-5 BG_R/G/B – Background R/G/B Color (Intensity=0). If all 0, then no background, i.e. transparent. Bit 4 Blink – Enable this Character display with blinking feature. Refer to section 0 for detail blinking control. Bit 3-0 FG_R/G/B/I or R_C2BP[3:0] – when Character Data = 00h~BFh, Foreground R/G/B/Intensity Color. If the value is set as 0000b, then there will be no foreground, i.e. transparent. when Character Data = C0h~FFh, these 4 bits act as a pointer to one of 16 the Character 2BP color sets							

2.10.3.3 Row Attribute (Default=XXXXXXXXb)

Table 2-4 Row Attribute

7	6	5	4	3	2	1	0
RGAP_BG	RGAP[4]	RGAP[3]	RGAP[2]	RGAP[1]	RGAP[0]	CHS	CWS
Bit 7 RGAP_BG – Color Select of Row Gap. Set 1 for selecting the same color of background of current row character, 0 for selecting transparent color. Bit 6-2 RGAP[4:0] – Row Gap (=Row Space). Inserted range is 4 x (31 _d ~0) scan lines before current Row. Bit 1 CHS – Character Height Select. Set 1 for double height, 0 for single height. Bit 0 CWS – Character Width Select. Set 1 for double width, 0 for single width. When set to 1, only the even numbered characters will be shown, odd numbered characters are skipped.							

2.10.4 Configuration Register

2.10.4.1 Cfg_00h – OSD Control Register (Default=00h => 18h)

Table 2-5 Cfg_00h – OSD Control Register

7	6	5	4	3	2	1	0
OSD_En	Bit_Map	Bit2PP	Reserved	Reserved	Early_hDE	DCLK[1]	DCLK[0]
Bit 7 OSD_En – Enabling the OSD function. Set 1 for enabling, 0 for disabling OSD. Bit 6 Bit_Map – Select Bit Mapped OSD display mode. Set 1 for Bit_Map Mode, 0 for Character Mode. Bit 5 Bit2PP – Two bits per Pixel for Bit_Map mode. Set 1 for 2 Bits/Pixel, 0 for 4 Bits/Pixel. Bit 4-3 Reserved. Bit 2 Early_hDE – let OSD a little shift left. Bit 1-0 DCLK[1:0] – Dot Clock, is divided from Pixel Clock. 00b for no divide, 01b for divided by 2, 10b for divided by 3, 11b for divided by 4 (11b is reserved and not recommended). These two bits are used for widen global OSD characters.							

¹ The “b” after value means Binary; “d” means Decimal; “h” means Hex-Decimal.

2.10.4.2 Cfg_01h – Character Delay_1 (Default=00h)

Table 2-6 Cfg_01h – Character Delay_1

7	6	5	4	3	2	1	0
Reserved	VERTD[10]	VERTD[9]	VERTD[8]	Reserved	HORD[10]	HORD[9]	HORD[8]
Bit 7, 3	Reserved. (R/W)						
Bit 6-4	VERTD[10:8] – Vertical Starting Position (Upper bits) of Character displaying. These bits with Cfg_03h, total 11 bits, become 2048 steps, with an increment one pixel per step for each field.						
Bit 2-0	HORD[10:8] – Horizontal Starting Position (Upper bits) of Character displaying. These bits with Cfg_02h, total 11 bits, become 2048 steps, with an increment one pixel per step.						

2.10.4.3 Cfg_02h – Character Delay_2 (Default=10h)

Table 2-7 Cfg_02h – Character Delay_2

7	6	5	4	3	2	1	0
HORD[7]	HORD[6]	HORD[5]	HORD[4]	HORD[3]	HORD[2]	HORD[1]	HORD[0]
Bit 7-0	HORD[7:0] – Horizontal Starting Position (Lower bits) of Character displaying. This register with Cfg_01h<2:0>, total 11 bits, become 2048 steps, with an increment one pixel per step.						

2.10.4.4 Cfg_03h – Character Delay_3 (Default=08h)

Table 2-8 Cfg_03h – Character Delay_3

7	6	5	4	3	2	1	0
VERTD[7]	VERTD[6]	VERTD[5]	VERTD[4]	VERTD[3]	VERTD[2]	VERTD[1]	VERTD[0]
Bit 7-0	VERTD[7:0] – Vertical Starting Position (Lower bits) of Character displaying. This register with Cfg_01h<6:4>, total 11 bits become 2048 steps, with an increment one line per step for each field.						

2.10.4.5 Cfg_04h – Character Font Size (Default=09h)

Table 2-9 Cfg_04h – Character Font Size

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	FontH[1]	FontH[0]	Reserved	FontW[1]	FontW[0]
Bit 7-5	Reserved. (R/W)						
Bit 4-3	FontH [1:0] – Font Size (Height) Select. Set 00b for 16 lines, 01b for 18 lines, 10b for 24 lines, 11b for 32 lines. (default is 18 lines)						
Bit 2-0	FontW [1:0] – Font Size (Width) Select. Set 00b for 10 dots, 01b for 12 dots, 10b for 14 dots, 11b for 16 dots. (default is 12 dots)						

2.10.4.6 Cfg_05h – Char_RAM Base Address (Default=50h)

Table 2-10 Cfg_05h – Char_RAM Base Address

7	6	5	4	3	2	1	0
Reserved	CharBA[6]	CharBA[5]	CharBA[4]	CharBA[3]	CharBA[2]	CharBA[1]	CharBA[0]
Bit 7	Reserved. (R/W)						
Bit 6-0	CharBA[6:0] – Programmable Character RAM Base Address. Those 7 bits become 128 steps, each step is 64 bytes (one Character Row include Char_Index, Char_Attr, Row_Attr; i.e. 31 column maximum for each Row). The actual address will be RRRR-RRRX-XXXX (The RRRR-RRR means the value of CharBA[6:0]; the X-XXXX is the nth Char Column. For trading off Font number and Character number in a single RAM (this version is 3Kx16 bits), user should carefully setting this register.						

2.10.4.7 Cfg_06h – Character Border / Shadow Control (Default=00h)

Table 2-11 Cfg_06h – Character Border / Shadow Control

7	6	5	4	3	2	1	0
BDSEN	CSHD	ES_Only	Reserved	BDSH[1]	BDSH[0]	BDSW[1]	BDSW[0]
Bit 7	BDSEN – Character Border/Shadow Enable. 1 for enabling Border or Shadow (depends on CSHD setting, the Cfg_06h<6>).						
Bit 6	CSHD – Character Shadow Selected. If BDSEN (Cfg_06h<7>) is 0, then no Border/Shadow displaying for Character; it BDSEN=1, then set this CSHD as 1 for selecting Shadow, 0 for selecting Border.						
Bit 5	ES_Only – Shadow on Eastern South side of the displayed foreground dot only (due to the Northern West light source), if set to 1; else the shadow also exist on the both east & south side of displayed foreground dot.						
Bit 4	Reserved.						
Bit 3-2	BDSH [1:0] – Character Border/Shadow Height. Set 00b for 1 line, 01b for 2 lines, 10b for 3 lines, 11b for 4 lines. The BDSH[1:0] value must <= DCLK[1:0]; Only 00b (one line height) available in current version.						
Bit 1-0	BDSW [1:0] – Character Border/Shadow Width. Set 00b for 1 pixel, 01b for 2 pixels, 10b for 3 pixels, 11b for 4 pixels. The BDSW[1:0] value must <= CHD[2:0]; Only 00b (one pixel width) available in current version.						

2.10.4.8 Cfg_07h – Character Border / Shadow Color & Output Delay (Default=00h)

Table 2-12 Cfg_07h – Character Border / Shadow Color & Output Delay

7	6	5	4	3	2	1	0
BDS_R	BDS_G	BDS_B	BDS_Gray	Reserved	Reserved	Reserved	Reserved
Bit 7-4	BDS_R/G/B/Gray – Character Border (or Shadow) R/G/B color and Gray level select. When BDS_Gray=1, select 8 gray levels, else, select half the R/G/B value (Intensity=0) of OSD LUT color addressed by BDS_R/G/B. Note, these four bits = 0001 for black color, 0000 for half Character Background color.						
Bit 3-0	Reserved.						

2.10.4.9 Cfg_08h – Character Height Control (Default=20h)

Table 2-13 Cfg_08h – Character Height Control

7	6	5	4	3	2	1	0
CHD[2]	CHD[1]	CHD[0]	Reserved	Reserved	Reserved	Reserved	Reserved
Bit 7-0	CHD[2:0] – Character height duplicate, select the duplicate numbers of each lines (16/18/24/32). The CHD[2:0] must >= 1.						
Bit 4-0	Reserved.						

2.10.4.10 Cfg_09h – Blinking Control (Default=0Ah)

Table 2-14 Cfg_09h – Blinking Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	BCLK[1]	BCLK[0]	Duty[1]	Duty[0]
Bit 7-4	Reserved. (R/W)						
Bit 3-2	BCLK[1:0] – Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.						
Bit 1-0	Duty[1:0] – For adjusting the blinking duty cycle, Set: 00b for Global Blink Off, i.e., 0% Background, 100% OSD. 01b for 25% Background, 75% OSD. 10b for 50% Background, 50% OSD. 11b for 75% Background, 25% OSD.						

2.10.4.11 Cfg_0Ah – Bit_Map Window Size: Width/Height Upper Bits (Default=00h)**Table 2-15 Cfg_0Ah – Bit_Map Window Size**

7	6	5	4	3	2	1	0
Reserved	BMH[10]	BMH[9]	BMH[8]	Reserved	BMW[10]	BMW[9]	BMW[8]
Bit 7, 3	Reserved. (R/W)						
Bit 6-4	BMH[10:8] – Bit Map Window Height Upper bits (only available in Bit_Map mode). Please refer to Cfg_0Ch for detail. User must be careful of the OSD RAM size limitation.						
Bit 2-0	BMW[10:8] – Bit Map Window Width Upper bits (only available in Bit_Map mode). Please refer to Cfg_0Bh for detail. User must be careful of the OSD RAM size limitation.						

2.10.0.4.12 Cfg_0Bh – Bit_Map Window Size: Width (Default=80h)**Table 2-16 Cfg_0Bh – Bit_Map Window Size: Width**

7	6	5	4	3	2	1	0
BMW[7]	BMW[6]	BMW[5]	BMW[4]	BMW[3]	BMW[2]	BMW[1]	BMW[0]
Bit 7-0	BMW[7:0] – Bit Map Window Width Lower bits (only available in Bit_Map mode This register combined with Cfg_0Ah<2:0> and become 11 bits, i.e., 2047 steps (value 000h is not valid), each step is 4 or 8 dots depends on Bit2PP (Cfg_00h<5>) setting. When Bit2PP=0 (i.e., 4 bits/pixel), each step is 4 dots. When Bit2PP=1 (i.e., 2 bits/pixel), each step is 8 dots. User must be careful of the OSD RAM size limitation.						

2.10.4.13 Cfg_0Ch – Bit_Map Window Size: Height (Default=60h)**Table 2-17 Cfg_0Ch – Bit_Map Window Size: Height**

7	6	5	4	3	2	1	0
BMH[7]	BMH[6]	BMH[5]	BMH[4]	BMH[3]	BMH[2]	BMH[1]	BMH[0]
Bit 7-0	BMH[7:0] – Bit Map Window Height Lower bits (only available in Bit_Map mode). This register combined with Cfg_0Ah<6:4> and become 11 bits, i.e. 2048 height step: all 0 for 2048 lines, 11'h001 for 1 line, 11'h7FF for 2047 lines. User must be careful of the OSD RAM size limitation.						

2.10.4.14 Cfg_0Dh – Bit_Map Dot Enlarge (Default=11h)**Table 2-18 Cfg_0Dh – Bit_Map Dot Enlarge**

7	6	5	4	3	2	1	0
BMBigH[3]	BMBigH[2]	BMBigH[1]	BMBigH[0]	BMBigW[3]	BMBigW[2]	BMBigW[1]	BMBigW[0]
Bit 7-4	BMBigH[3:0] – Bit Map Window Vertical Enlarge (only available in Bit_Map mode). Set 0000b for 1 line per dot, 0001b for 2 lines per dot, 0010b for 3 lines, ..., 1111b for 16 lines per dot.						
Bit 3-0	BMBigW[3:0] – Bit Map Window Horizontal Enlarge (only available in Bit_Map mode). Set 0000b for 1 pixel per dot, 0001b for 2 pixels per dot, 0010b for 4 pixels per dot, 0011b for 6 pixels per dot, ..., 1111b for 30 pixels per dot.						

2.10.4.15 Cfg_0Eh – OSD Color LUT RAM Data Port (No Default)**Table 2-19 Cfg_0Eh – OSD Color LUT RAM Data Port**

7	6	5	4	3	2	1	0
LUT_D[7]	LUT_D[6]	LUT_D[5]	LUT_D[4]	LUT_D[3]	LUT_D[2]	LUT_D[1]	LUT_D[0]
Bit 7-0	LUT_D[7:0] –The data will be written to (or read from) OSD Color LUT RAM. After each Read or Write access to LUT RAM, then the LUT address will be increased automatically.						
Note:	Whenever the Configuration Index is programmed from other index value to 0Eh, the OSD Color LUT RAM becomes access capable and the address pointer is reset to 0 (the starting byte). In other words, whenever the index value is programmed to non-0Eh value, the OSD Color LUT RAM can not be access, and the pointer always kept at 0.						
Note: The order to fill LUT RAM is:	<ol style="list-style-type: none"> 1. LUT[0]_Green/Blue 2. LUT[0]_0000b/Red 3. LUT[1]_Green/Blue 4. LUT[1]_0000b/Red 5. LUT[0]_Green/Blue 6. ---- 31. LUT[15]_Green/Blue 						

32. LUT[15]_0000b/Red
 33. LUT[0]_Green/Blue (wrap to beginning)
 34. LUT[0]_0000b/Red

2.10.4.16 Cfg_0Fh – OSD Color LUT RAM Data Port (No Default)

Table 2-20 Cfg_0Fh – OSD Color LUT RAM Data Port

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRAM_ByteAccess[1:0]	
Bit 7-2		Reserved.					
Bit 1-0		When CRAM_ByteAccess[1:0] = 0X: Word (2-bytes) R/W; 10: Low byte only; 11: High byte only					

2.10.4.17 Cfg_10h - Window_1 Start Character Row Number (Default=00h)

Table 2-21 Cfg_10h - Window_1 Start Character Row Number

7	6	5	4	3	2	1	0
W1EN	W1_INT	W1RS[5]	W1RS[4]	W1RS[3]	W1RS[2]	W1RS[1]	W1RS[0]
Bit 7		W1EN – Window_1 Enable. 1 for enabled, 0 for disabled. Window_1 only can be enabled in Character mode, i.e. it is always disabled in Bit_Map mode.					
Bit 6		W1_INT – Window_1 Intensity. 1 for selecting high intensity color, 0 for low intensity color.					
Bit 5-0		W1RS[5:0] / BMP_StartA[5:0] – When in character mode, these bits defined as Window_1 Start @ nth Row (User must be careful of Character row number vary due to programmable Char_RAM base address). When in Bit_Map mode, these bits define the LSB of Bit mapped image starting address.					

2.10.4.18 Cfg_11h - Window_1 End Character Row Number (Default=00h)

Table 2-22 Cfg_11h - Window_1 End Character Row Number

7	6	5	4	3	2	1	0
W1SEN	W1S_Gray	W1RE[5]	W1RE[4]	W1RE[3]	W1RE[2]	W1RE[1]	W1RE[0]
Bit 7		W1SEN – Window_1 Shadow function enabling. 1 for enabled, 0 for disabled. If HalfTone=1, the color of Window Shadow is always the half R/G/B value of background; otherwise, color will be the pre-defined					
Bit 6		W1S_Gray – Window_1 Gray level select. Refer to W1S_R/G/B setting for detail.					
Bit 5-0		W1RE[5:0] / BMP_StartA[11:6] – When in character mode, these bits defined as Window_1 End @ nth Row (User must be careful of Character row number vary due to programmable Char_RAM base address). When in Bit_Map mode, these bits define the MSB of Bit mapped image starting address.					

2.10.4.19 Cfg_12h - Window_1 Start Character Column Number (Default=00h)

Table 2-23 Cfg_12h - Window_1 Start Character Column Number

7	6	5	4	3	2	1	0
W1_R	W1_G	W1_B	W1CS[4]	W1CS[3]	W1CS[2]	W1CS[1]	W1CS[0]
Bit 7-5		W1_R/G/B – Window_1 R/G/B color.					
Bit 4-0		W1CS[4:0] – Window_1 Start @ nth Column, available value of n is 29d~0. (n>29d is reserved)					

2.10.4.20 Cfg_13h - Window_1 End Character Column Number (Default=00h)

Table 2-24 Cfg_13h - Window_1 End Character Column Number

7	6	5	4	3	2	1	0
W1S_R	W1S_G	W1S_B	W1CE[4]	W1CE[3]	W1CE[2]	W1CE[1]	W1CE[0]
Bit 7-5		W1S_R/G/B – Window_1 Shadow Color of R/G/B. During display shadow area, the SHADOW output will be high, it can be used to select another 8-level gray (000b black ~ 111b light Gray) for OSD LUT (if W1S_Gray=1) or used as a half R/G/B value (Intensity=0) selection in last phase (if W1S_Gray=0).					
Bit 4-0		W1CE[4:0] – Window_1 End @ nth Column, available value of n is 29d~0. (n>29d is reserved)					

2.10.4.21 Cfg_14h - Window_1 Shadow Size (Default=00h)**Table 2-25 Cfg_14h - Window_1 Shadow Size**

7	6	5	4	3	2	1	0
W1SH[3]	W1SH[2]	W1SH[1]	W1SH[0]	W1SW[3]	W1SW[2]	W1SW[1]	W1SW[0]
Bit 7-4 W1SH[3:0] – Window_1 Shadow Height. The Shadow height = W1SH[3:0] * 2 (- 0/1) lines and must <= FontH setting.							
Bit 3-0 W1SW[3:0] – Window_1 Shadow Width. The Shadow Width = W1SW[3:0] * 2 pixels and must <= FontW setting.							

2.10.4.22 Cfg_1Ah – Char2BP Font Base Address -1 (Default=00h)**Table 2-26 Cfg_1Ah – Char2BP Font Base Address -1**

7	6	5	4	3	2	1	0
C2BP_BA[7]	C2BP_BA[6]	C2BP_BA[5]	C2BP_BA[4]	C2BP_BA[3]	C2BP_BA[2]	C2BP_BA[1]	C2BP_BA[0]
Bit 7-0 2BP Characters Base Address LSB.							

2.10.4.23 Cfg_1Bh – Char2BP Font Base Address -2 (Default=08h)**Table 2-27 Cfg_1Bh – Char2BP Font Base Address -2**

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	C2BP_BA[11]	C2BP_BA[10]	C2BP_BA[9]	C2BP_BA[8]
Bit 7-0 2BP Characters Base Address MSB.							

2.10.4.24 Cfg_1Ch – Alpha Blending Control (Default=00h)**Table 2-28 Cfg_1Ch – Alpha Blending Control**

7	6	5	4	3	2	1	0
FG_NoAB	Reserved	Reserved	Reserved	AB_Set[3]	AB_Set[2]	AB_Set[1]	AB_Set[0]
Bit 7 FG_NoAB – OSD Character ForeGround portion will be exclusive to be blended if set to one. Default is 0 as no matter the current displayed pixels are in Character foreground or border/shadow or background or in OSD window, all will be alpha blended with original Video source.							
Bit 6-4 Reserved. (R/W)							
Bit 3-0 AB_Set[3:0] – Alpha Blending percentage (n/16). If set 0000b, alpha blending is disabled (0/16 * Original Video Source + 16/16 * OSD display); If set 0001b, blending as 1/16 * Original Video Source + 15/16 * OSD display; If set N, blending as N/16 * Original Video Source + (16-N)/16 * OSD display;							

2.10.4.25 Cfg_1Dh – Revision ID**Table 2-29 Cfg_1Dh – Revision ID**

7	6	5	4	3	2	1	0
RID[7]	RID[6]	RID[5]	RID[4]	RID[3]	RID[2]	RID[1]	RID[0]
Bit 7-0 Revision ID (Read Only). add ORAM burst write feature.							

2.10.4.26 Cfg_1Eh – Char_RAM Stop Address (Default=60h)**Table 2-30 Cfg_1Eh – Char_RAM Stop Address**

7	6	5	4	3	2	1	0
Reserved	CharEA[6]	CharEA[5]	CharEA[4]	CharEA[3]	CharEA[2]	CharEA[1]	CharEA[0]
Bit 7 Reserved. (R/W)							
Bit 6-0 CharEA[6:0] – Programmable Character RAM Stop/End Address (Available if Revision ID >= 0h). Those 7 bits become 128 steps, each step is 64 bytes. The actual stop address will be RRRR-RRRX-XXXX (The RRRR-RRR means the value of CharEA[6:0]; the X-XXXX is the nth Char Column. and OSD will be displayed for Character Row >= CharBA and < CharEA.							

2.10.5 OSD Functional Description

2.10.5.1 Host Access OSD RAM

2.10.5.1.1 Writing Data

The OSD RAM size is 3Kx16, i.e., 3K word with each word is 2 bytes. The host interface is 8-bit data width, so whenever the host writes 2 times (one for data low byte, the other for data high byte) then it becomes one write with 16-bit data to OSD RAM.

Two methods to read/write OSD RAM data:

1. The original one (for all version)

The ORAM_DL (OSD module base address + 04h) port is a temporary data port for latching lower byte of OSD RAM writing data when the host want to program Font or Character, Attribute, BMP values.

The RAM Data Write Strobe is the Host Write to ORAM_DH (OSD module base address + 05h). Each time the host write to ORAM_DH port, it becomes a RAM write strobe with current 8 bits data and latched ORAM_DL data, total 16 bits, to OSD RAM.

2. The Burst method (for Revision number >= 02h)

The ORAM_DL (OSD module base address + 04h) port when writing in the 1st/3rd/5th/7th ..times, it will latch lower byte of OSD RAM writing data when the host want to program Font or Character, Attribute, BMP values; and when writing 2nd/4th/6th/8th ... times, it will use this 8bits data as high byte and write both two bytes to OSD RAM.

2.10.5.1.2 Reading Data

Whenever the host access the OSD RAM, the lower byte of current OSD RAM accessing data (the current RAM address pointer may be the host programmed pointer in ORAM_AL (OSD module base address + 02h) / ORAM_AH (OSD module base address + 03h) during non OSD display or the current OSD display information during OSD displaying period.

The OSD RAM pointer will not be increased when the host read ORAM_DL port, but it will be increased after access ORAM_DH port.

2.10.5.1.3 Access Address

The OSD RAM access pointer is programmed by the host write access to ORAM_AL and ORAM_AH ports. The OSD RAM size is 3Kx16, so the pointer is required to cover 3K words, i.e., 12 address lines => A[11:0]. When the host read these ORAM_AL/ORAM_AH ports, the pointer value reflects the current OSD RAM accessing pointer.

2.10.5.2 OSD Displaying in Character Mode

Character Mode

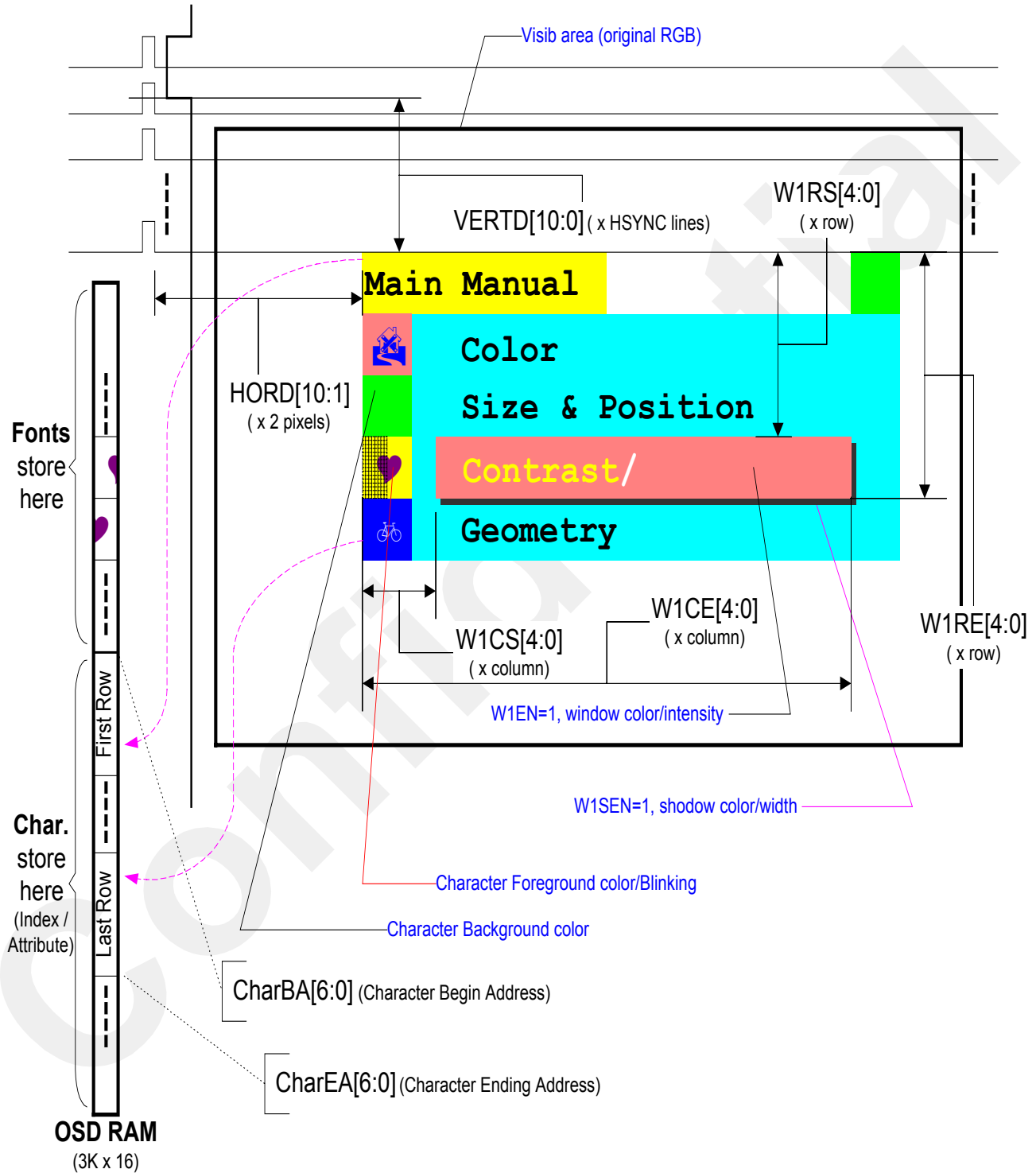


Figure 2-14 OSD Character Mode

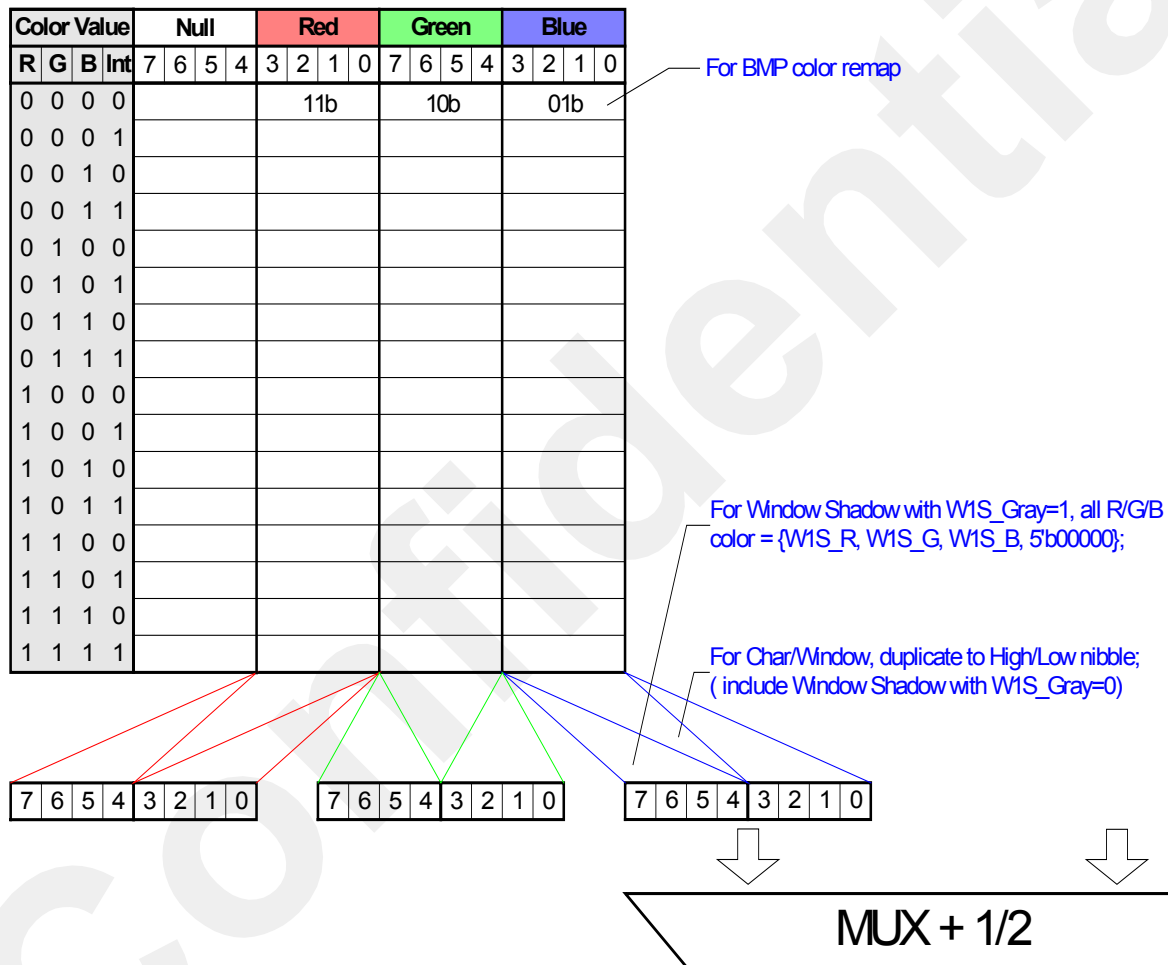
2.10.5.3 OSD LUT Color Mapping

OSD Color LUT RAM

Character Mode
(Char/Window)

Character Mode
(Window Shadow)

16x12 RAM



Bit_Map Mode

4 Bits/Pixel mode: Same as Character Mode

2 Bits/Pixel mode: Refer to LUT[0], then re-direct to other LUT[1..15]

Figure 2-15 OSD Color LUT

2.10.5.4 Character Mode Color Layer

Layer_1: Character Foreground Color. This is the Top layer.

Layer_2: Character Border/Shadow Color. (Gray, Non-HalfTone Half-color)

Layer_3: Window Color.

Layer_4: Window Shadow Color (Non-HalfTone).

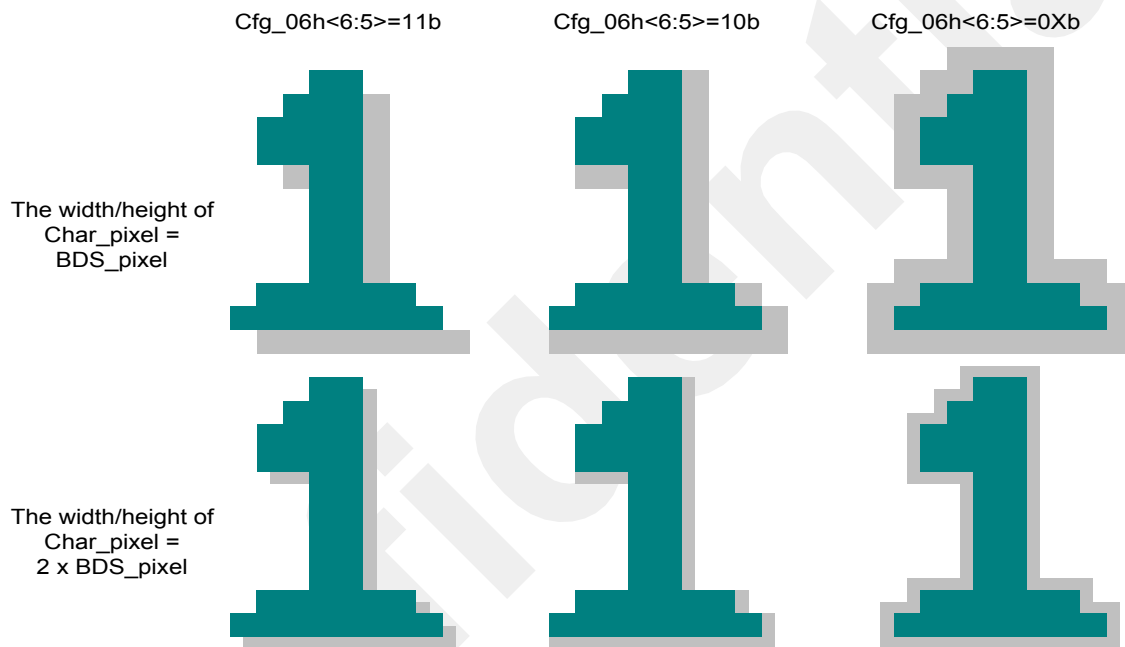
Layer_5: Character Background Color.

Layer_6: Original Background Color (+ HalfTone Window Shadow). This is the bottom layer.

2.10.5.5 Halt Tone Display

The Halftone feature is automatically applied to the shadow area (both the Character Shadow and Window Shadow), if its shadow RGB color (the BDS_RGB or W1S_RGB settings) is set as 000b and its Gray control (the BDS_Gray or W1S_Gray settings) is set as 0. Then the displayed color will be the half of the RGB color of next lower layer.

2.10.5.6 Character Border /Shadow Consideration



Hardware Border/Shadow Calculation

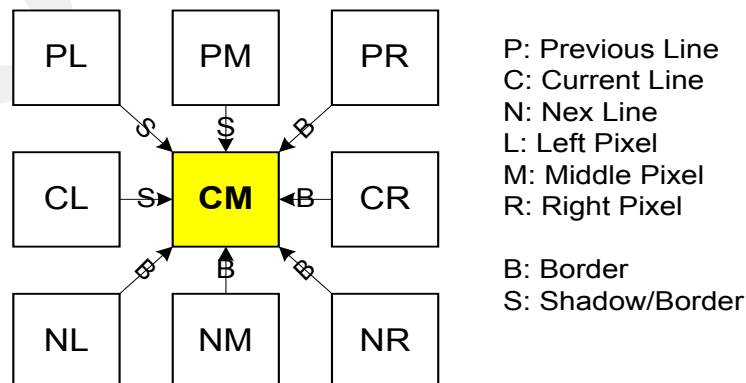


Figure 2-15 OSD Border/Shadow

2.10.5.7 OSD Programming Examples

2.10.5.7.1 Configuring OSD Function

To access OSD configuration registers, write register index to port A0h, and read/write data from port A1h. For example, set :

```
IOW  A0h, 1Dh      ; point to Cfg_1Dh (revision ID register).
IOR   A1h;          ; get Revision ID.
IOW  A0h, 06h      ; point to Cfg_06h (Character Border / Shadow register).
IOW  A1h, C4;       ; Set Shadow height 2 lines, width 1 line.
```

2.10.5.7.2 Fill LUT RAM

LUT RAM size is 16 (address) x 12 (width). For example, need to fill LUT RAM as:

LUT_RAM[0] = 123h, LUT_RAM[1]=F5Ah, ...LUT_RAM[15]=EF0h

```
IOW  A0h, 0Eh      ; point to Cfg_0Eh (LUT RAM Data port), this will let LUT RAM be
                    ; access-able and pointer starts from 0h of LUT RAM.
IOW  A1h, 23h;      ; fill Green = 0010b and Blue = 0011h in LUT_RAM[0].
IOW  A1h, 01h;      ; fill Red = 0001b in LUT_RAM[0].
                    ; after this write, h/w will increase LUT RAM address to 1 automatically
IOW  A1h, 5Ah;      ; fill Green = 0101b and Blue = 1010h in LUT_RAM[1].
IOW  A1h, 0Fh;      ; fill Red = 1111b in LUT_RAM[1].
                    ; after this write, h/w will increase LUT RAM address to 2 automatically
.....
IOW  A1h, F0h;      ; fill Green = 1111b and Blue = 0000h in LUT_RAM[15].
IOW  A1h, 0Eh;      ; fill Red = 1110b in LUT_RAM[15].
                    ; after this write, h/w will increase LUT RAM address to 0 automatically
IOW  A0h, non-0Eh   ; Disable LUT RAM programming.
```

2.10.5.7.3 Load Fonts to OSD RAM

OSD RAM size is 3K (address: 000h ~ BFFh) x 16 (width). Fonts storing starts from address 000h. For example, loading some fonts to OSD RAM as:

Font[0] is a space (all zero), Font[1] is a character 2 with box, Font[14] is a graphic,...

```
IOW  A2h, 00h      ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW  A3h, 00h;      ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8])
                    ; then the OSD RAM address pointer is set to 000h.
IOW  A4h, 00h;      ; low byte of first row of Font[0].
IOW  A4h, 00h;      ; high byte of first row of Font[0], after this write, h/w will increase OSD
                    ; RAM address to 1 automatically
IOW  A4h, 00h;      ; low byte of 2nd row of Font[0].
IOW  A4h, 00h;      ; high byte of 2nd row of Font[0], after this write, h/w will increase OSD
                    ; RAM address to 2 automatically
..... (for example, programmed font size is 18 (height) x 12 (width)
IOW  A4h, 00h;      ; low byte of 18th (last) row of Font[0].
IOW  A4h, 00h;      ; high byte of 18th row of Font[0], after this write, h/w will increase OSD
                    ; RAM address to 012h automatically
IOW  A4h, F0h;      ; low byte of first row of Font[0]. (since font width is 12, the low byte bit[3:0]
                    ; is no use)
IOW  A4h, FFh;      ; high byte of first row of Font[0], after this write, h/w will increase OSD
                    ; RAM address to 013h automatically
.....
IOW  A2h, 68h      ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW  A3h, 01h;      ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8]),
                    ; then the OSD RAM address pointer is set to 168h = 14d * 18d.
IOW  A4h, 40h;      ; low byte of first row of Font[14].
IOW  A4h, A3h;      ; high byte of first row of Font[14],
.....
```

2.10.5.7.4 Assign Characters and its color to OSD RAM

Use the same way like load fonts

2.11 TCON

2.11.1 LCD Panel Pin Assignment

In this section, we illustrate those pins connected to AU 7" TFT-LCD panel module in a T101 video system.

Table 2-31 T101 Rotation Control and LCD Panel Scanning Direction

L/R	U/D	STH	STV	Reg 0xE1	Scanning Direction
1	1	STH2	STV1	0xBC	Down-to-up, left-to-right
1	0	STH2	STV2	0xF4	Up-to-down, left-to-right
0	1	STH1	STV1	0xA8	Down-to-up, right-to-left
0	0	STH1	STV2	0xE0	Up-to-down, right-to-left

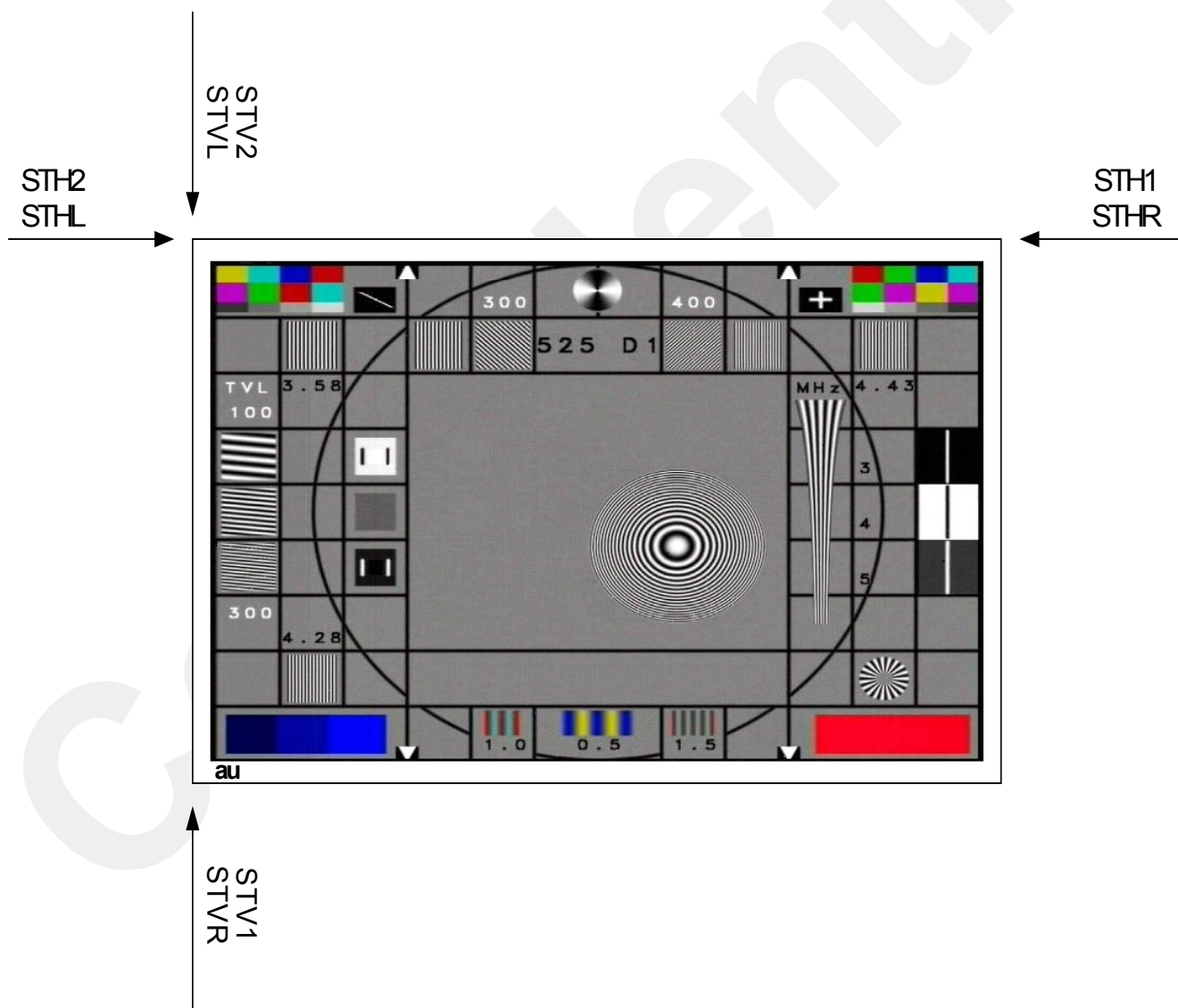


Figure 2-16 Scanning Direction of AU 7" panel

2.11.2 TCON Timing

T101 is designed for Digital LCD panel. The table 2-32 shows a typical setting for AU 7" panel with 10-Mhz operation clock.

Table 2-32 T101 TCON Register Set (C8 =1Bh, C9=03, CA=03h)

Reg	Reg value	Operation
0x20	0x21	Line-inverted Control
0x21	0x79	Polarity Control
0x23,0x22	0x022D	Placement of OEH
0x24	0x0C	Duration of OEH
0x26,0x25	0x024B	Placement of POL
0x28,0x27	0x021C	Placement of GCLK
0x2A,0x29	0x0029	Duration of GCLK
0x2B	0x01	Placement of STH
0x30	0x01	Enable Placement of STV
0x32,0x31	0x01FB	Placement of GOE
0x34,0x33	0x0037	Duration of GOE
0x35	0x06	Placement of STV

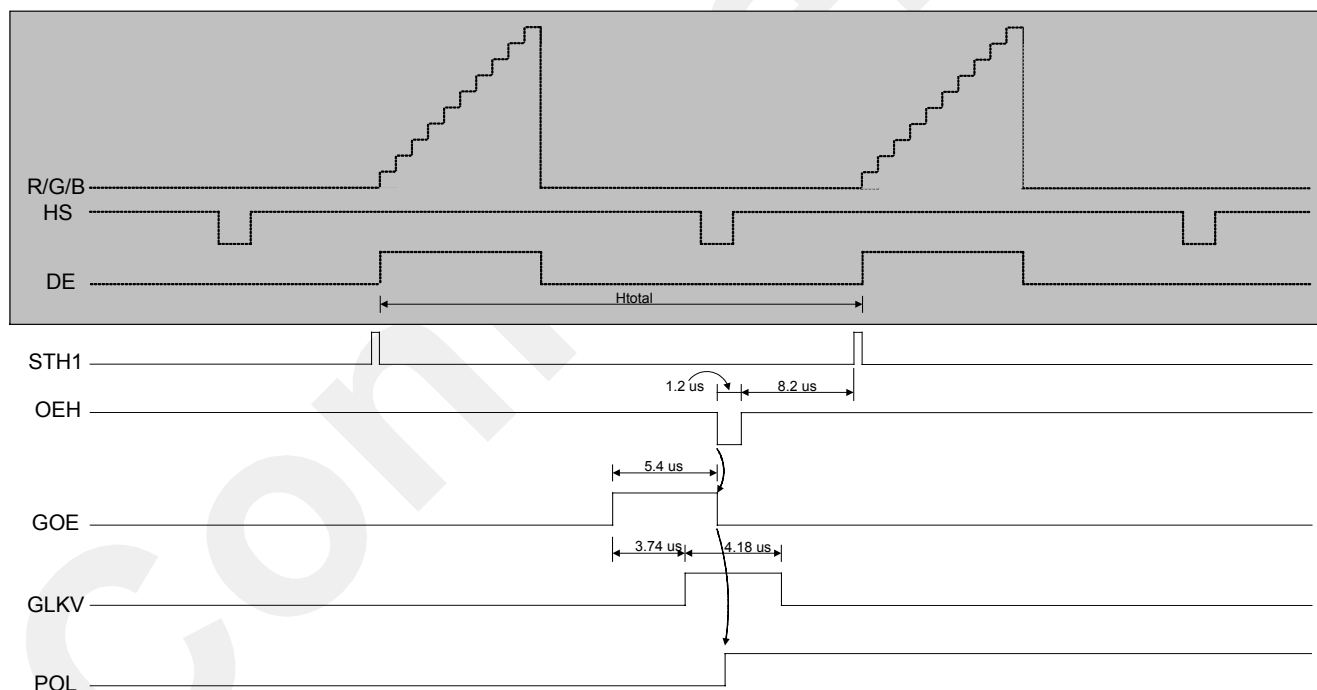


Figure 2-17 AU 7" TCON Timing Spec

The waveforms shown below illustrate TCON location counting. Each TCON signal's placement and duration are allowed to program as alike as analog LCD panels require. On the figure 2-18, the pulse placement starts counting at the leading edge of DE. After placement counter meets the value we give to {P1_27h,P1_28h}, the duration counter starts to count until the duration meets {P1_29h,P1_2Ah}. All of location counting use LLCK as counter clock.

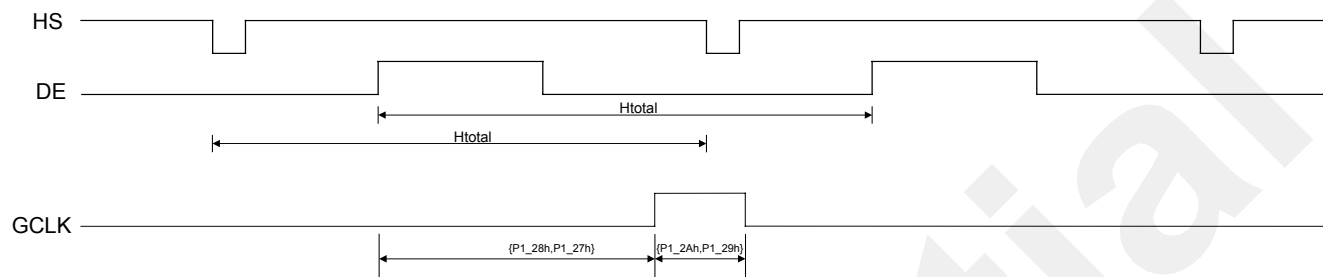


Figure 2-18 Location Counting of GCLK

3 Register Description

Serial Bus Register Set Page 0

3.1 ADC Register Set

3.1.1 RESERVED

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.1.2 RESERVED

Address Offset: 01h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.1.3 RESERVED

Address Offset: 02h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.1.4 ADC Clamping Pulse Placement and Duration

Address Offset: 04h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	STIPCLPL	Clamping pulse placement
[4:0]	R/W	STIPCLDU	Clamping pulse duration

3.1.5 ADC Channel 0 Static Gain

Address Offset: 07h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCRSG	This register can set a fixed gain for ADC channel 0 when static gain control is enabled

3.1.6 ADC Channel 1 Static Gain

Address Offset: 08h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCGSG	This register can set a fixed gain for ADC channel 1 when static gain control is enabled

3.1.7 ADC Channel 2 Static Gain

Address Offset: 09h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCBSG	This register can set a fixed gain for ADC channel 2 when static gain control is enabled

3.1.8 ADC ACR Channel Offset

Address Offset: 0Ah Access: Read/Write
 Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_ROFF	ADC Channel 0 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.9 ADC AY Channel Offset

Address Offset: 0Bh Access: Read/Write
 Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_GOFF	ADC Channel 1 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.10 ADC ACB Channel Offset Configuration Register

Address Offset: 0Ch Access: Read/Write
 Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_BOFF	ADC Channel 2 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.11 ADC General Control Configuration Register

Address Offset: 0Dh Access: Read/Write
 Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	CLPMD	Clamping mode
			Mode Type
			0 Fixed window
			1 Locked Window
			2 Reserved
			3 Reserved
[5]	R/W	DCEN	DC Clamping Enable
[4]	R/W	DCSEL	Clamping Source Selection
[3]	R/W	RESERVED	
[2]	R/W	DC_CAL_RDY	DC Calibration Ready
[1]	R/W	DC_CALEN	DC Calibration Enable

[0]	R/W	DC_CALMD	DC Calibration Mode	
			Mode	Type
			0	minimum
			1	average

3.1.12 ADC Power Down Control

Address Offset: 0Fh
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	PD2	1: Power down 0: Power up
[5]	R/W	PD1	1: Power down 0: Power up
[4]	R/W	PD0	1: Power down 0: Power up
[3:0]	R/W	RESERVED	

3.1.13 Reserved

Address Offset: 10h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.1.14 YPbPr Clamping Control Register

Address Offset: 11h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description						
[7]	R/W	RESERVED							
[6]	R/W	Bmidsel	0: Midscale volt from I/O pad, 1:Auto midscale volt						
[5]	R/W	Gmidsel	0: Midscale volt from I/O pad, 1:Auto midscale volt						
[4]	R/W	Rmidsel	0: Midscale volt from I/O pad, 1:Auto midscale volt						
[3]	R/W	RESERVED							
[2]	R/W	BSCALE	ADC Channel 2 Clamping Mode <table><tr><th>Mode</th><th>Select</th></tr><tr><td>0</td><td>Clamp to ground</td></tr><tr><td>1</td><td>Clamp to midscale</td></tr></table>	Mode	Select	0	Clamp to ground	1	Clamp to midscale
Mode	Select								
0	Clamp to ground								
1	Clamp to midscale								
[1]	R/W	GSCALE	ADC Channel 1 Clamping Mode <table><tr><th>Mode</th><th>Select</th></tr><tr><td>0</td><td>Clamp to ground</td></tr><tr><td>1</td><td>Clamp to midscale</td></tr></table>	Mode	Select	0	Clamp to ground	1	Clamp to midscale
Mode	Select								
0	Clamp to ground								
1	Clamp to midscale								

[0]	R/W	RSCALE	ADC Channel 0 Clamping Mode	
			Mode	Type
			0	Clamp to ground
			1	Clamp to midscale

3.1.15 Analog Source MUX Selection

Address Offset: 18h
Default Value: 00h

Access: Read/Write
Size: 8 bits

	Access	Symbol	Description										
[7:6]	R/W	RESERVED											
[5:4]	R/W	AI2SEL	Analog mux selection for ADC channel 1 <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ACB1</td></tr><tr><td>1</td><td>ACB0</td></tr><tr><td>2</td><td>ACB2</td></tr><tr><td>3</td><td>ACB2</td></tr></table>	Mode	Type	0	ACB1	1	ACB0	2	ACB2	3	ACB2
Mode	Type												
0	ACB1												
1	ACB0												
2	ACB2												
3	ACB2												
[3:2]	R/W	AI1SEL	Analog mux selection for ADC channel 1 <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>AY1</td></tr><tr><td>1</td><td>AY0</td></tr><tr><td>2</td><td>AY2</td></tr><tr><td>3</td><td>AY2</td></tr></table>	Mode	Type	0	AY1	1	AY0	2	AY2	3	AY2
Mode	Type												
0	AY1												
1	AY0												
2	AY2												
3	AY2												
[1:0]	R/W	AI0SEL	Analog mux selection for ADC channel 0 <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ACR1</td></tr><tr><td>1</td><td>ACR0</td></tr><tr><td>2</td><td>ACR2</td></tr><tr><td>3</td><td>ACR2</td></tr></table>	Mode	Type	0	ACR1	1	ACR0	2	ACR2	3	ACR2
Mode	Type												
0	ACR1												
1	ACR0												
2	ACR2												
3	ACR2												

3.1.16 Y/Cb/Cr Data Switching Control

Address Offset: 19h
Default Value: 07h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description										
[7:6]	R/W	RESERVED											
[5:4]	R/W	CBINSEL	The digitized CB or Chroma data can be taken from one of 3 ADCs according to following table <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr><tr><td>2</td><td>ADC Ch2</td></tr><tr><td>3</td><td>ADC Ch2</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1	2	ADC Ch2	3	ADC Ch2
Mode	Type												
0	ADC Ch0												
1	ADC Ch1												
2	ADC Ch2												
3	ADC Ch2												

Bit	Access	Symbol	Description										
[3:2]	R/W	YINSEL	<div>The digitized Y or Composite data can be taken from one of 3 ADCs according to following table</div> <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr><tr><td>2</td><td>ADC Ch2</td></tr><tr><td>3</td><td>ADC Ch2</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1	2	ADC Ch2	3	ADC Ch2
Mode	Type												
0	ADC Ch0												
1	ADC Ch1												
2	ADC Ch2												
3	ADC Ch2												
[1:0]	R/W	CRINSEL	<div>The digitized CR or Chroma data can be taken from one of 3 ADCs according to following table</div> <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr><tr><td>2</td><td>ADC Ch2</td></tr><tr><td>3</td><td>ADC Ch2</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1	2	ADC Ch2	3	ADC Ch2
Mode	Type												
0	ADC Ch0												
1	ADC Ch1												
2	ADC Ch2												
3	ADC Ch2												

3.1.17 ADC Analog AGC Selection

Address Offset: 1Ah
Default Value: 42h

Access: Read/Write
Size: 8 bits

	Access	Symbol	Description	
[7:6]	R/W	AGC_GAINMD		
			Mode	Type
			0	Positive gain
			1	Positive gain 1x~2x
			2	Negative gain 1x~2x
			3	Negative gain
[5:3]	R/W	RESERVED		
[2]	R/W	CB_AGC_SEL	If 0, refer to ADCBSG	
			Mode	Type
			0	Static gain
			1	Dynamic gain
[1]	R/W	Y_AGC_SEL	If 0, refer to ADCGSG	
			Mode	Type
			0	Static gain
			1	Dynamic gain
[0]	R/W	CR_AGC_SEL	If 0, refer to ADCRSB	
			Mode	Type
			0	Static gain
			1	Dynamic gain

3.1.18 Blank Sync Level

Address Offset: 1Ch
Default Value: C0h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLANK_SL	

3.1.19 ADC Read-back Selection

Address Offset: 1Dh
Default Value: 80h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	RBK_SEL	1: Read Max of ADC data 0: Read Min of ADC data or Average of ADC data

3.1.20 ADC Read-back Data

Address Offset: 1Eh
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RBK_ADC[7:0]	

3.1.21 ADC Read-back Data

Address Offset: 1Fh
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R	RESERVED	
[1:0]	R	RBK_ADC[9:0]	

3.1.22 De-Interlaced Process & Vertical Shadow Control Register

Address Offset: 30h
Default Value: 82h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CBCR_INTERP	1: Enable CbCr interpolation 0: Disable
[6]	R/W	BLANK_LF_PR SVC	1: When Left Cropping and this bit are enabled, the original YCbCr are preserved on blank interval. 0: When Left Cropping, the original YCbCr are reset as blank color
[5]	R/W	VST_CHGSEL	1: Vsync timing change determined by 8*# of XCLK 0: Vsync timing change determined by # of hsync # can be assigned at Reg 0x3A
[4]	R/W	INT_EDGE	Interrupt polarity 1: positive 0: negative
[3]	R/W	LB_SIZE_FIXED	This bit control capture size for Scaler. 1: Hsize and Vsize are assigned by 54h ~57h 0: sizes assigned by input sources.

[2]	R/W	ENQKHS	Set 0 for normal operation
[1]	R/W	ITLCPRO	Set 1 for interlaced video Set 0 for non-interlaced video
[0]	R/W	ENSHDW	

3.1.23 Source Select Register

Address Offset: 31h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[5]	R/W	INP_D565_SEL	1:select digital RGB565 input 0:ITU656 or analog input
[4]	R/W	INP_SRC_SEL	1: select digital ITU656 input 0: select analog input
[3:0]	R/W	RESERVED	

3.1.24 Interrupt Status Register

Address Offset: 32h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R	ITLCFLM	Indicates incoming video signal is interlaced
[5:0]	R/W	INTSTS	

3.1.25 Interrupt Mask Register

Address Offset: 33h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	INTMASK	

3.1.26 Lower 8-bit Timer Counter Register

Address Offset: 35h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_L [7:0]	Lower byte of the number of XCLK's in 1ms.

3.1.27 Upper 8-bit Timer Counter Register

Address Offset: 36h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_H [15:8]	Higher byte of the number of XCLK's in 1ms.

3.1.28 VSYNC Missing Counter Register

Address Offset: 37h Access: Read/Write

Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_MISS_CNT	

3.1.29 Lower 8-bit HSYNC Missing Counter RegisterAddress Offset: 38h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[7:0]	

3.1.30 Upper 8-bit HSYNC Missing Counter RegisterAddress Offset: 39h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[15:8]	

3.1.31 VSYNC Delta Difference Result RegisterAddress Offset: 3Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSYNC_DLT[7:0]	

3.1.32 HSYNC Delta Difference Result RegisterAddress Offset: 3Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSYNC_DLT[7:0]	

3.1.33 Input Sync Signal Detection RegisterAddress Offset: 3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HSTLSPVS	1:use trailing edge of hsync to sample 0:use leading edge of hsync to sample
[6]	R/W	AUTOVSD6	When the edges of vsync and hsync are too close, input detection circuit can delay vsync 6 cycle of XCLK to avoid unstable detection 1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true. 0:Dealy 6 cycles of XCLK if FCVSD6 is true
[5]	R/W	FCVSD6	AUTOVSD6 FCSVSD6T 1 x Autmatically delay VSync 6 XCLK if CFSEEDGE is true 0 1 Force to delay VSync 6 XCLK 0 0 No Vsync Dealy
[4]	R	CFSEEDGE	VS and HS edges are to close.
[3:2]	R/W	RESERVED	

[1]	R/W	VsHs_Sync_Edge	1: leading edge of Vsi 0: falling edge of Hsi
[0]	R/W	VsHS_Sync_En	1:leading edge of Vsi starts at leading edge of Hsi 0:leading edge of Vsi starts at mid of Hsi

3.1.34 Left Border Cropping

Address Offset: 40h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	CROP_LEFTTB	Remove noisy pixels appearing on left border. 1LSB =1 pixel

3.1.35 RGB565 Input Configuration

Address Offset: 47h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6:4]	R/W	DRGBI_SWAP	0:RGB 1:RBG 2:GBR 3:GRB 4:BRG 5:BGR 6:BRG 7:BGR
[3]	R/W	RESERVED	
[2]	R/W	DVSIN_POL	1: Positive sync tip 0:Negative sync tip
[1]	R/W	DATIN_NEG	1:Inverted data 0:Non-inverted data
[0]	R/W	DEIN_POL	1:Positive DE 0:Negative DE

3.1.36 VSYNC Timing Measurement Register

Address Offset: 50h
Default Value: 00h

Access: **Read Only**
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	HSPMD	Register 0x5c and 0x5d can be HS pulse width or hsync period 1:Period in # of pixel clock. 0:Hsync pulse width in # of pixel clock.
[5]	R	DONE_FRMXCLKCNT	When EN_FRAMEXCLKCNT is enabled, a whole frame time can be obtained through XCLK counting. See registers 0x51, 0x52 and 0x53. After this bit read back as 1, then clear EN_FRAMEXCLKCNT first before reading 0x51~0x53 values.