



***Terawins, Inc.***

***Advanced Information  
Version 0.2***

*Mar., 14, 2006*

# **T112 Video Display Controller**

Confidential

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# 1 Introduction

## 1.1 Features

### ■ Cost Effective Highly Integrated Triple ADC + 2D Video Decoder + OSD + Scaler + TCON

- Integrates 9-bit Analog to Digital Converters (ADC) & Phase Locked Loop (PLL)
- Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ratio.
- Requires no external Frame Buffer Memory for deinterlacer.
- Advanced On Screen Display (OSD) function
- Programmable Timing Controller (Tcon) for Car TV applications
- Multi-standard color decoder with 2D adaptive comb filter
- Innovative and flexible design to reduce total system cost

### Triple 9-bit Analog to Digital Converters (ADC)

#### ■ 27 MSPS Conversion Rate

- Built-in Pre-amp, mid-level & ground clamp circuit
- Automatic Clamp Control for CVBS, Y and C
- Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
- Max Input configuration up to 4xCVBS or 2xS-video

### Digital Video Enhancement

#### ■ Separate Luminance and Chroma Enhancer

- Y Supports Luminance Peaking, DLTi, Black Level Expansion, Contrast and Brightness adjustment
- C Supports DCTi, Saturation and Hue adjustment.

### Advanced Scaling Engine

#### ■ Two Dimensions FIR Scaler

- Coefficient based sharpness filters
- 2-D edge enhancement
- Independent vertical and horizontal scaling ratio
- 16:9 Non-linear Aspect ratio

#### ■ LCD Interface

- Provides Gamma correction for panel compensation
- Supports image pan functions
- Programmable Timing Controller

- RGB Triple DAC output

#### ■ Color Management

- Coef Programmable YCbCr-to-RGB Color Space Converter
- RGB Gamma Correction

#### ■ Built-in On Screen Display Engine

- 1K-word OSD SRAM memory
- Supports font or bitmap modes
- Supports character blinking, overlay, shadow and border functions
- Fully programmable character mapping
- Supports alpha blending & Zoom-in/Zoom-out function
- Optional fonts can be stored in off-chip serial EEPROM

#### ■ Versatile VBI Data Decoder

- Supports Close Caption, Wide Screen Signalling and Teletext

#### ■ Crystal Oscillator Circuit

- Direct interface to a (27.0MHz) Crystal
- Also provide a buffered clock output for external Micro-controller

#### ■ Digital Test Pattern Generator

- Programmable standard & special panel burn-in test patterns
- Support special border frame blocking mode

#### ■ Independent Display Phase Lock Loop

- Generates pixel clock output to panel
- Supports free run OSD mode

#### ■ Serial Bus Interface

- Supports 2-wire (normal speed)

#### ■ Pulse Width Modulation Outputs

#### ■ Design For Testability

- Scan chain insertion
- Separated analog & digital test modes

■ Power Supply: +2.5V & +3.3V

■ Package: 64-pin LQFP

## 1.2 General Description

The T112 is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T112 has built-in high performance dual ADCs, TCON, Triple DACs, Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative integrated

“Frame-Buffer-Less” De-interlacer can significantly reduce system cost. The T112 also integrates On Screen Display engine with 1K-word of font RAM. The device can interface to an external micro-controller through 2-wire serial bus interface.

## 1.3 Applications

1. 4-inch to 10-inch portable DVD or in-car TV
2. Progressive CRT TV

## 1.4 System Architecture

T112 Block Diagram

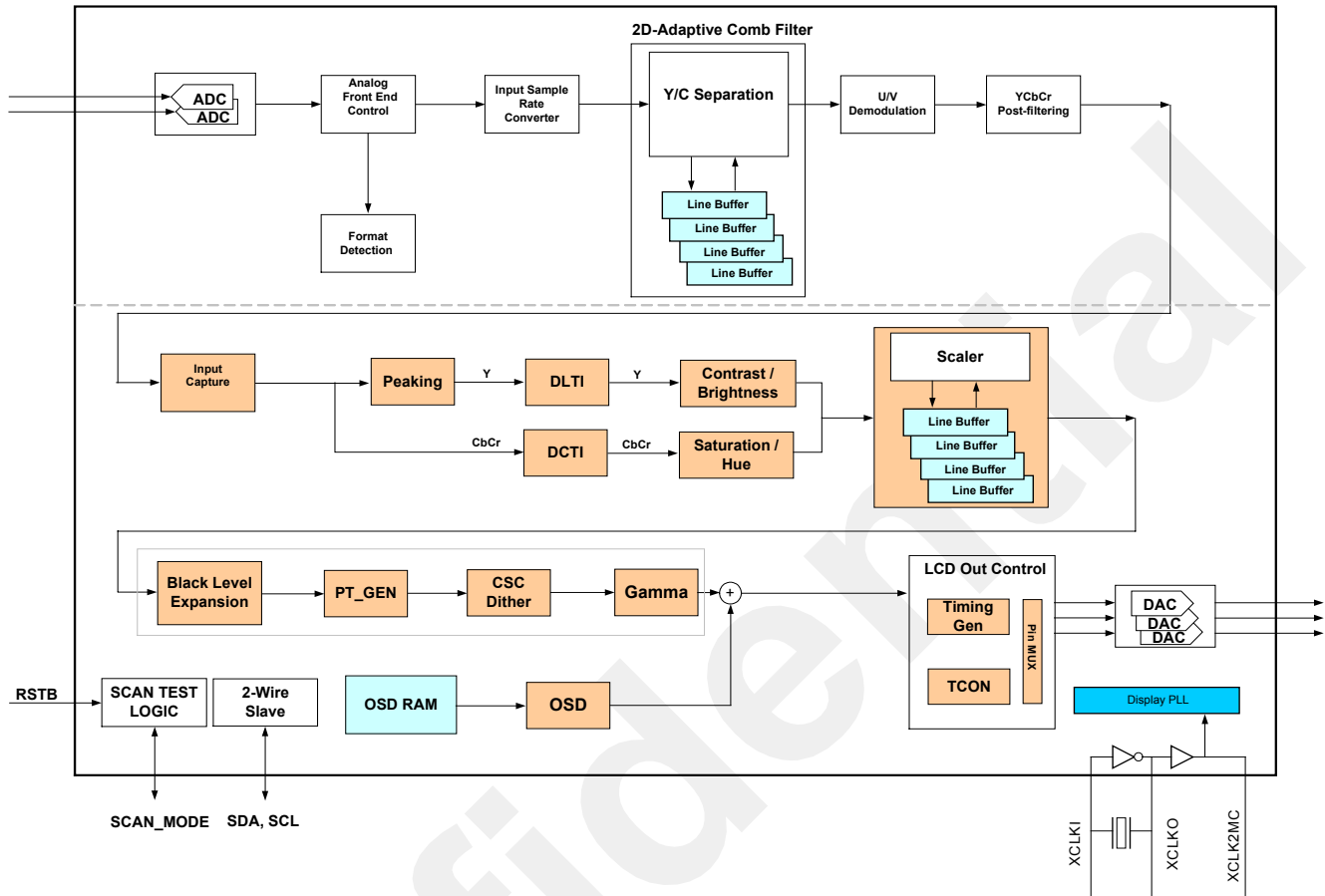


Figure 1-1 System Architecture

## 1.5 System Configurations

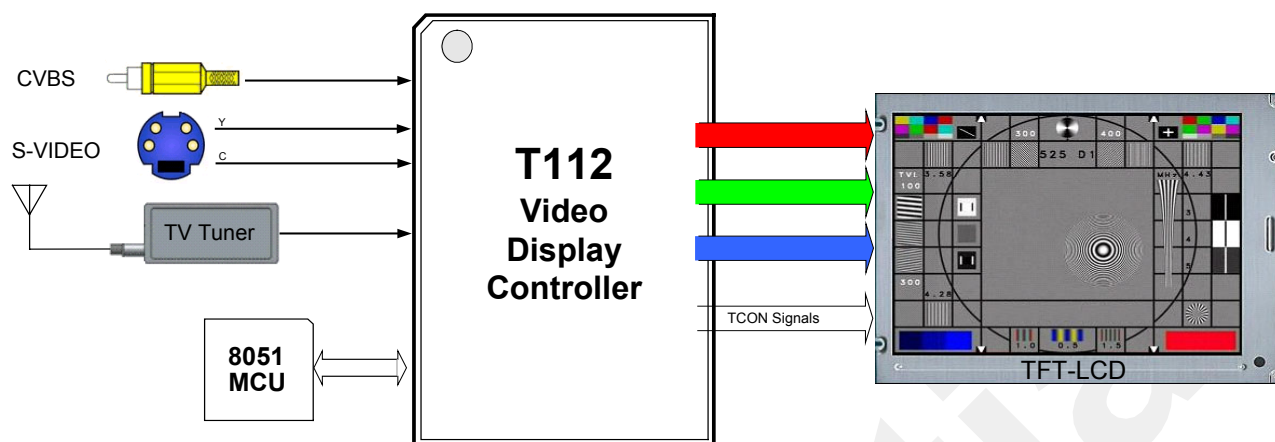


Figure 1-2 System Configuration

## 1.6 Pinout Diagram

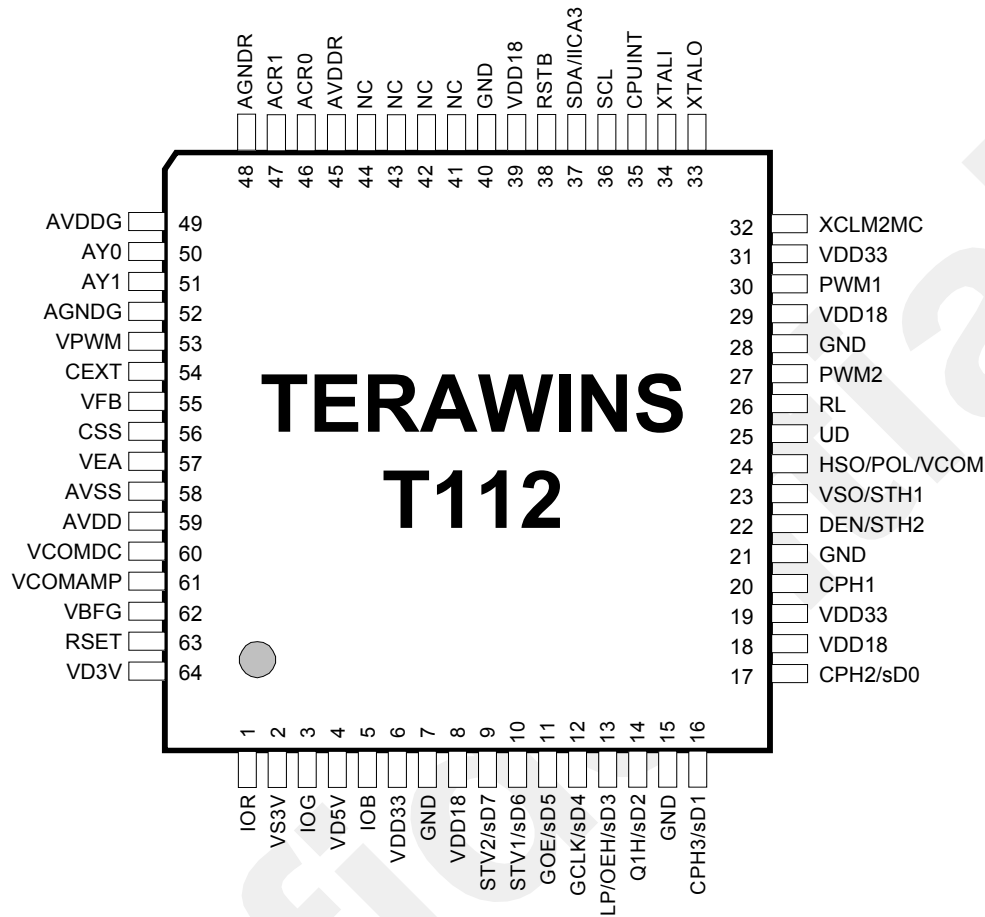


Figure 1-3 Pinout Diagram

## 1.7 Pin Description

Table 1-1 Pin Description

Symbol	Pin #	Type	Description
<b>Power Supplies</b>			
VDD18	8,18,29,39	PWR	+1.8V digital core power supply
VDD33	6,19,31	PWR	+3.3V digital output power supply
AVDDG	49	PWR	+3.3V analog power supply for ADC channel 1
AVDDR	45	PWR	+3.3V analog power supply for ADC channel 0
GND	7,15,21,28,40	GND	Digital ground
AGNDG	52	GND	Analog ground for ADC channel 1
AGNDR	48	GND	Analog ground for ADC channel 0
VD5V	4	PWR	+5.0V analog power supply for DAC
VD3V	64	PWR	+3.3V analog power supply for VCOM and DAC
AVDD	59	PWR	+1.8V Analog Power Supply for DAC
VS3V	2	GND	Analog ground for DAC
AVSS	58	GND	Analog ground for DAC
<b>Output Interface Signals</b>			
RSET	63	AO	DAC reference current adjustment
VBFG	62	AO	Voltage reference output
IOR	1	AO	Channel R current output
IOG	3	AO	Channel G current output
IOB	5	AO	Channel B current output
CPH1	20	DO	Output data clock
CPH2/sD0	17	DO	Output data clock/the bit 0 of serial interfaced panel
CPH3/sD1	16	DO	Output data clock/the bit 1 of serial interfaced panel
VSO/STH1	23	DO	Vertical synchronization output signal.
HSO/POL	24	DO	Horizontal synchronization output signal.
DEN/STH2	22	DO	Horizontal data enable
<b>Timing Controller Interface Signals</b>			
Q1H/sD2	14	DO	Source Driver Q1H/the bit 2 of serial interfaced panel
LP/sD3	13	DO	Latch pulse for source driver/the bit 3 of serial interfaced panel
GCLK/sD4	12	DO	Gate driver clock/the bit 4 of serial interfaced panel
GOE/sD5	11	DO	Gate driver output enable/the bit 5 of serial interfaced panel
STV1/sD6	10	DO	Gate Driver start pulse/the bit 6 of serial interfaced panel
STV2/sD7	9	DO	Gate Driver start pulse/the bit 7 of serial interfaced panel
VCOMAMP	61	DO	Analog VCOM amplitude
VCOMDC	60	DO	Analog VCOM DC offset
<b>2-wire serial bus Interface Signals</b>			
SCL	36	DI	2-wire serial bus clock. Power down does not affect SCL.
SDA/IICA3	37	I/O	2-wire serial bus data. Power down does not affect SDA.
<b>Configuration interface Signals</b>			
CPUINT	35	I/O	Internal Interrupt.
RSTB	38	DI	Whole chip reset. (Internal Pull-up)
<b>ADC Interface</b>			
AY1	51	AI	Analog input 1 of channel 1
AY0	50	AI	Analog input 0 of channel 1



Symbol	Pin #	Type	Description
ACR1	47	AI	Analog input 1 of channel 0
ACR0	46	AI	Analog input 0 of channel 0
<b>PLL Reference Clock</b>			
XTALI	34	DI	Output PLL reference clock input
XTALO	33	DO	Output PLL reference clock output
XCLK2MC	32	DO	Buffered XTALI for external microprocessor.
<b>Power Management Interface Signals</b>			
PWM1	30	DO	Pulse Width Modulation for volume/backlight control.
PWM2	27	DO	Pulse Width Modulation for volume/backlight control.

## 2 Theory of Operations

### 2.1 I<sup>2</sup>C Command Protocol

Before your tester writes I<sup>2</sup>C commands to T112, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. SDA(A3) can affect slave address. Set low for 40h. Set high for 50h.

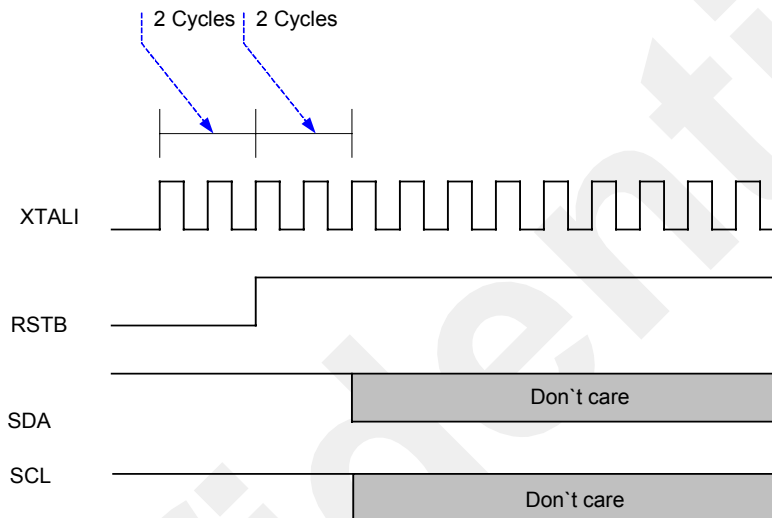


Figure 2-1 Power-up initialization

When tester issues commands to the T112, the only way the user can program the T112 is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. **The frequency of SCL can be from 50 KHz up to 1 Mhz.**

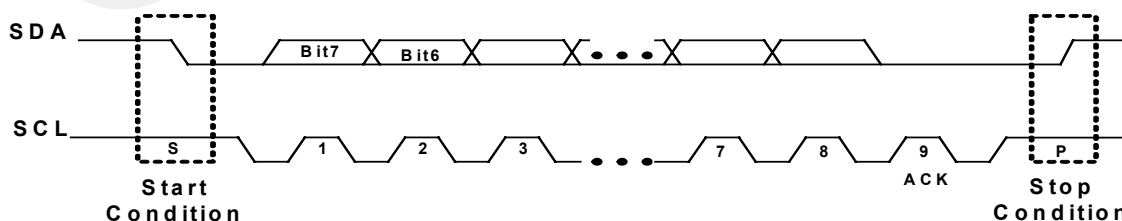


Figure 2-2 2-wire serial bus Protocol

The timing below shows a typical T112 IIC single byte write command,

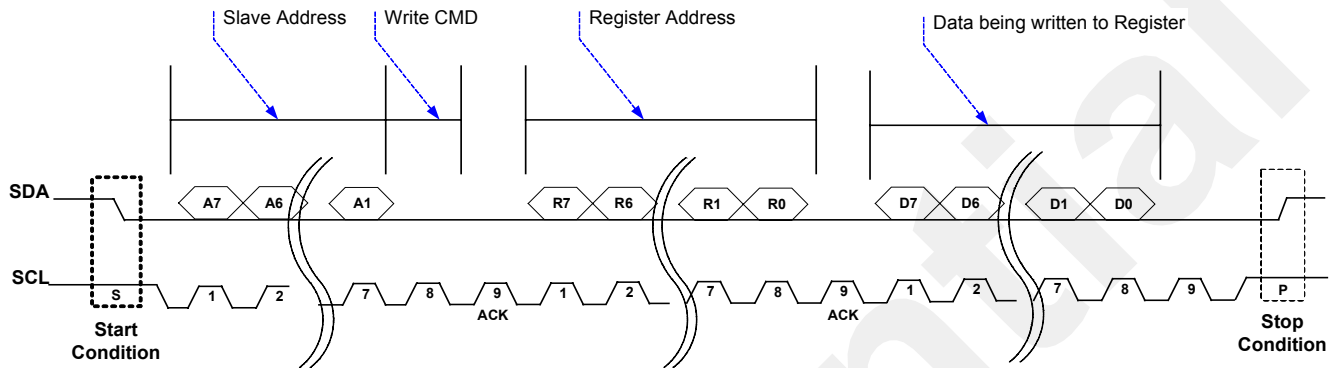


Figure 2-3 T112 IIC single byte write command

The timing below shows a typical T112 IIC single byte read command,

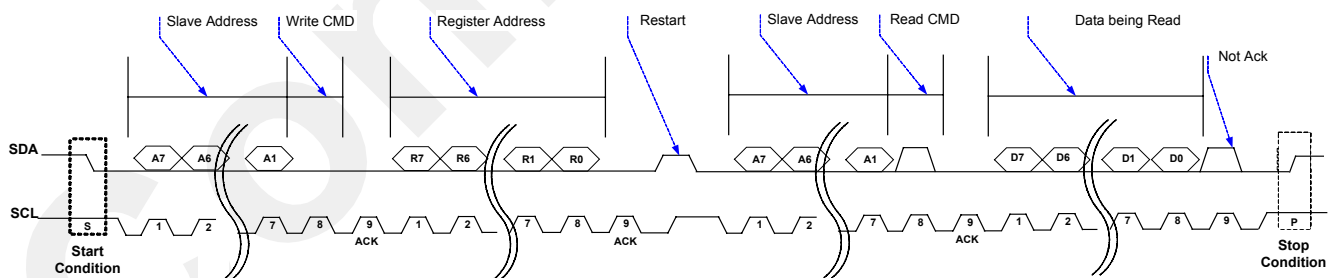


Figure 2-4 T112 IIC single byte read command

## 2.2 Analog Front End

T112 contains 2 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV signals from analog to digital. The figure shown below can describe how to select a SDTV signal from 2 inputs prior to ADCs.

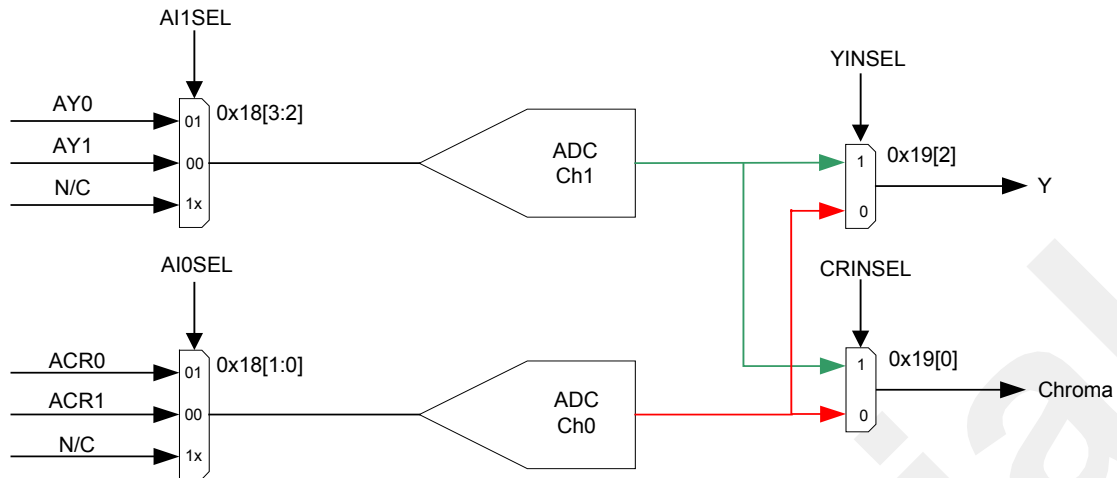


Figure 2-5 Analog Front End

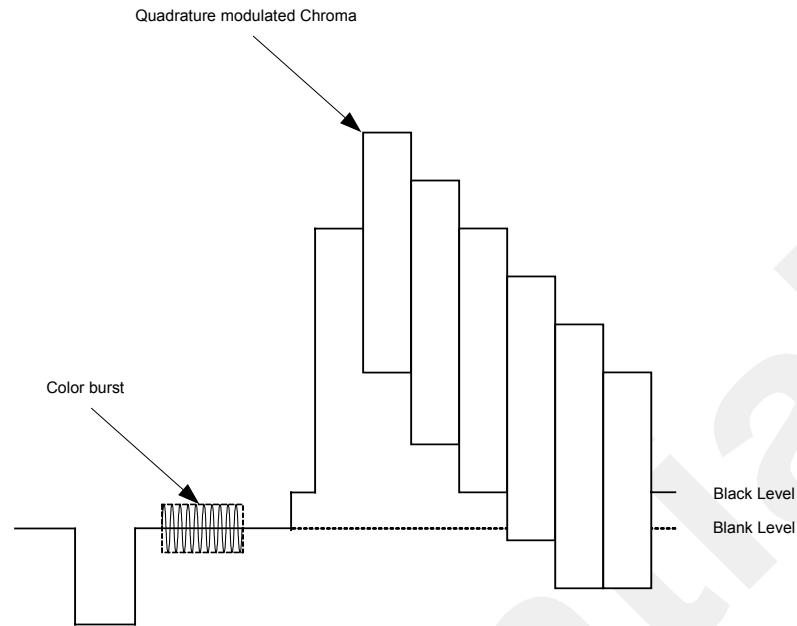
### 2.3 Y/C Separation and Chroma Decoder

A composite video has luma(Y) and chroma(C) information mixed in the same video signal. This video signal can also be represented by the equation below,

$$CVBS = Y + U * \sin(wt) + V * \cos(wt)$$

Where  $w = 2\pi f_{SC}$ ,  $f_{SC} = 3.58\text{Mhz}$  if NTSC,  $f_{SC} = 4.43\text{Mhz}$  if PAL

The figure below shows a typical composite signal. The 2-D adaptive comb filter inside T112 is designed to separate Y and C from a composite video signal.



**Figure 2-6 Typical Color SDTV Signal**

. The conventional 3-line comb filter fails to separate Y and C if there is a vertical transition. The 2-D adaptive comb filter is based on equally weighting factors that color changes along vertical and horizontal edges. Let the amount of color change along vertical and horizontal direction  $DC_v$  and  $DCh$ , the weighting factor can be expressed as following equations,

$$W_h = \frac{DC_v}{DC_v + DCh}$$

$$W_v = \frac{DCh}{DC_v + DCh}$$

By employing adaptive method, chroma can be recovered by following equation,

$$C = Ch * W_h + C_v * W_v$$

After Y/C separation, Y and C should look like waveforms shown as in following figure. Y only contains low frequency part, while C contains high frequency part which is centered around sub-carrier  $f_{sc}$ .

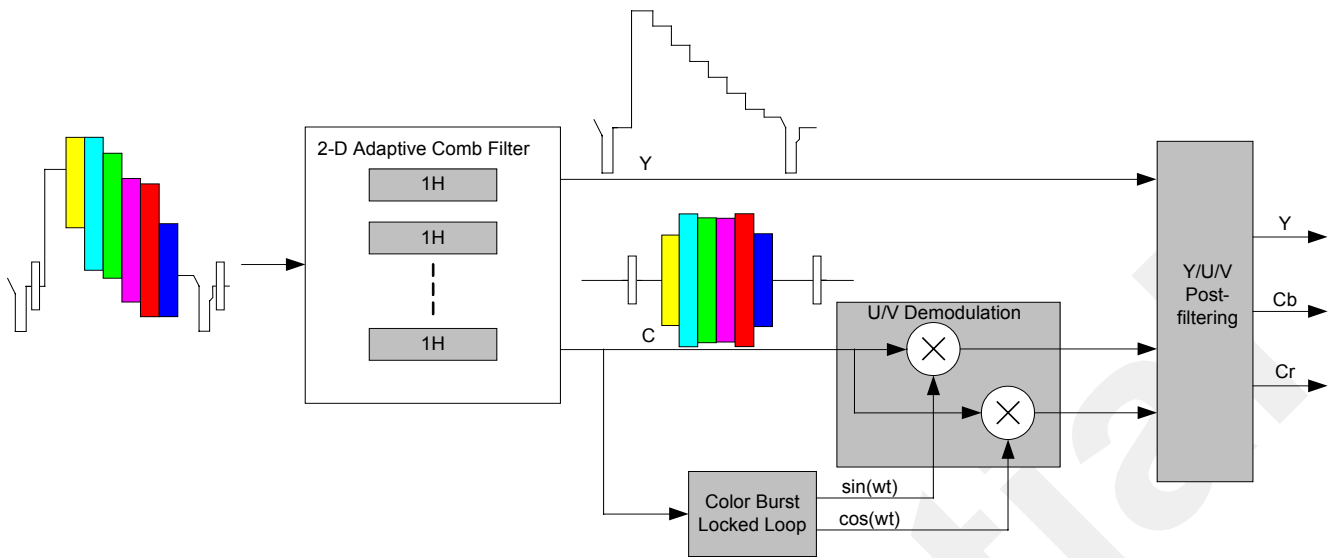


Figure 2-7 Video Decoding Flow

## 2.4 Digital Color Transient Improvement (DCTI)

Usually, a composite or S-video SDTV signal may have bandwidth limitation that causes the loss chroma detail around two different color bars. Two pictures shown below illustrate the result before and after DCTI block. Without DCTI (the upper picture), we may see color transient wider than several pixels. A slow transient edge usually blurs image. T112 DCTI algorithm can sharpen those color transient edges. The lower picture shows that chroma data is enhanced by increasing the slope of edge transient without introducing the ring effects.



Figure 2-8 Comparison of DCTI

## 2.5 Digital Luminance Transient Improvement (DLTI)

The Digital Luminance Transient Improvement is intended to sharpen luminance edge transient. The figure shown below is DLTI transfer function. DLTI doesn't increase peak-to-peak amplitude; rather it turns sloped waveforms into rectangular waveforms.

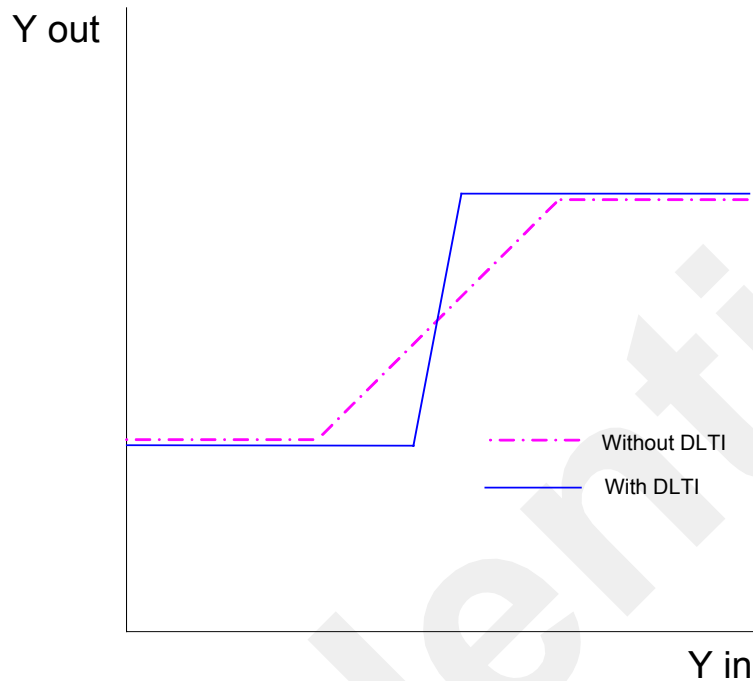


Figure 2-9 DLTI Transfer Curve

## 2.6 FIR Scaler

FIR Scaler can scale input H/V sizes to fit any LCD panel resolution. The flexible and independent H/V scalers allow users to program display area in 16:9 Full mode, 16:9 non-linear wide mode and 4:3 mode. FIR scaler also provides coefficient-based 2-D sharpness that can sharpen detail of picture.

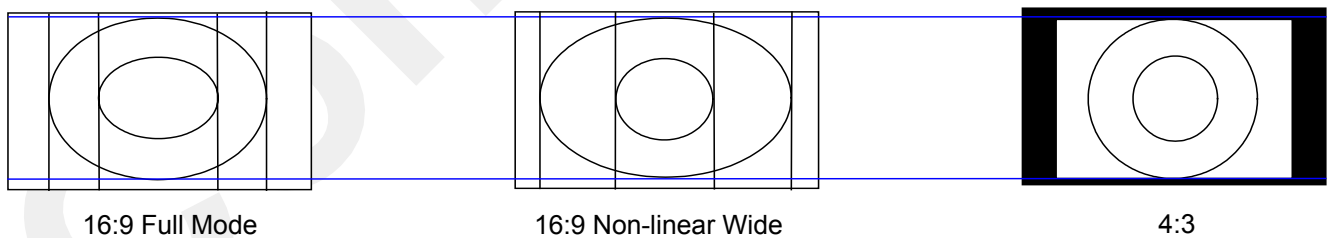


Figure 2-10 Practical Applications of FIR Scaler

## 2.7 Black-Level Extension (BLE)

Black Level Expansion (BLE) can enhance image contrast that makes dark regions of image darker, while bright regions remain unchanged. The figure shown below is BLE transfer function.

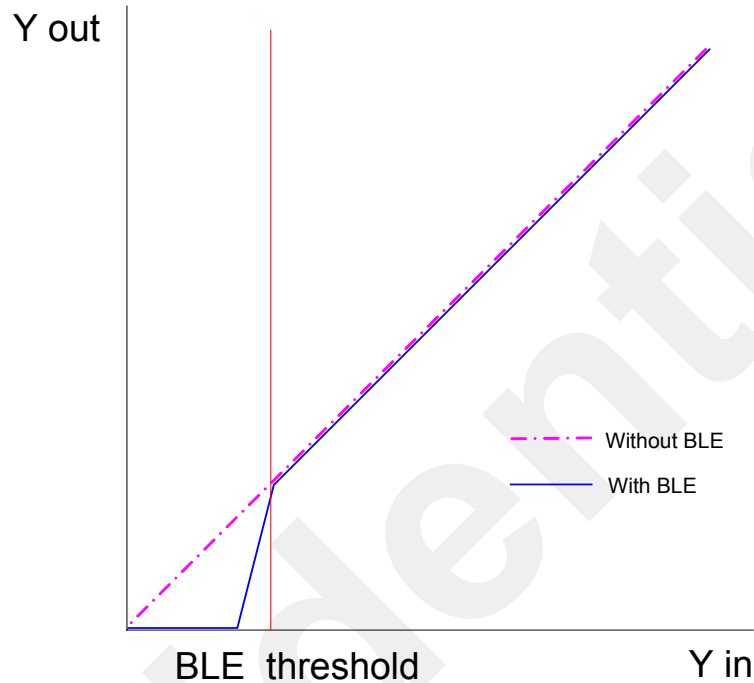


Figure 2-11 BLE Transfer Curve

$$Y_{out} = Y_{in} - (Y_{offset} - Y_{in}) * BLE\_Gain / 16$$

Where  $Y_{offset}$  and  $BLE\_Gain$  can be programmed by register P0\_96h.

## 2.8 Color Space Converter

A pixel in YCbCr color space can be converted to RGB color space by using following equations,

$$R = YCoefCSC * (Y - 16) + CrCoef\_R * (Cr - 128)$$

$$G = YCoefCSC * (Y - 16) - CrCoef\_G * (Cr - 128) - CbCoef\_G * (Cb - 128)$$

$$B = YCoefCSC * (Y - 16) + CbCoef\_B * (Cb - 128)$$

Where  $YCoefCSC$  is in 1.7-bit fixed point with default 1.164.  $CrCoef\_R$  in 1.7-bit fixed point with default 1.596.  $CrCoef\_G$  in 0.8-bit fixed point with default 0.813.  $CbCoef\_G$  in 0.8-bit fixed point with default 0.392.  $CbCoef\_B$  in 2.6-bit fixed point with default 2.017

The equations shown as below correspond to a typical YCbCr-to-RGB converter. In T101, we make those coefficients adjustable.



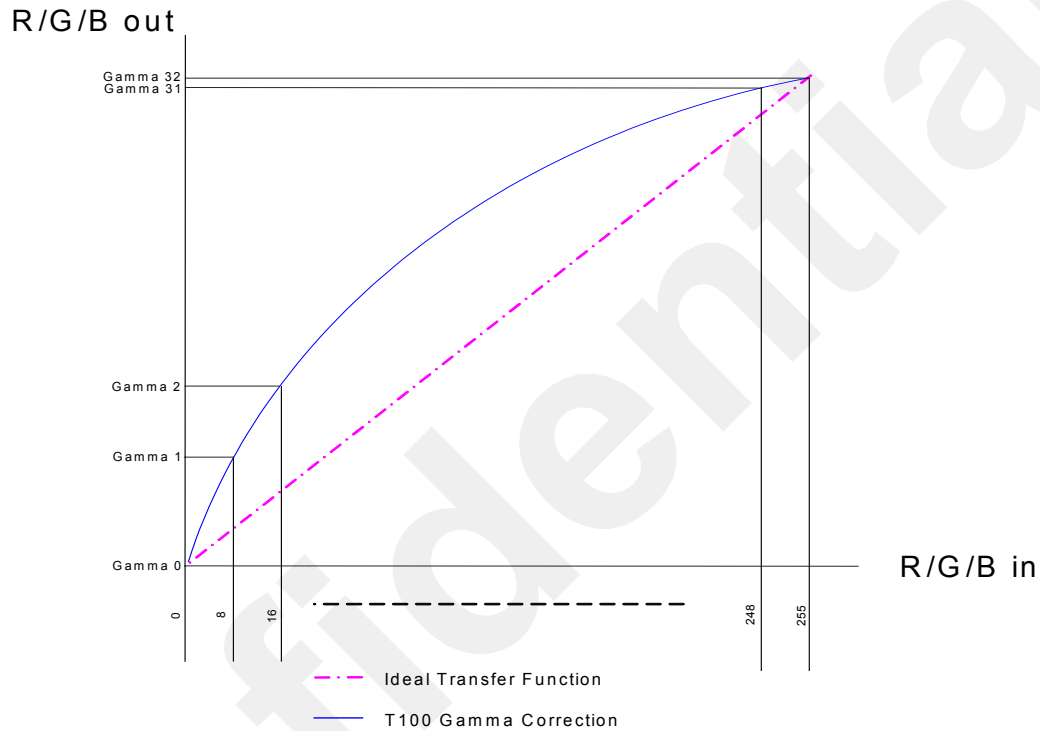
$$R = 1.164 * (Y - 16) + 1.596 * (Cr - 128)$$

$$G = 1.164 * (Y - 16) - 0.813 * (Cr - 128) - 0.392 * (Cb - 128)$$

$$B = 1.164 * (Y - 16) + 2.017 * (Cb - 128)$$

## 2.9 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,



**Figure 2-12 Gamma Transfer Curve**

T112 uses 33-point piece-wise linear interpolation instead of RAM-based LUTs. Each point can be programmed via register at P0\_93h and P0\_94h.

## 2.10 OSD

### 2.10.1 OSD Access

Table 2-1 OSD Access

I/O Port	Index	Default	Description
A0h – OSD_Index A1h – OSD_Data	00h	00h	OSD Control Register
	01h	00h	Character Delay_1
	02h	10h	Character Delay_2
	03h	08h	Character Delay_3
	04h	00h	Alpha Blending Control
	05h	38h	Char_RAM Base Address
	06h	40h	Char_RAM Stop Address
	07h	00h	Reserved
	08h	00h	Reserved
	09h	0Ah	Blinking Control
	0Ah	00h	Bit_Map Window Size : Height Upper Bits and BMP Enlarge Control
	0Bh	0Ah	Bit_Map Window Size : Width
	0Ch	66h	Bit_Map Window Size : Height
	0Dh	00h	Reserved
	0Eh	-	OSD LUT RAM data port (Write Only)
	0Fh	00h	Char Control Register
A2h – ORAM_AL		00h	OSD RAM Low Address Port of Starting Access
A3h – ORAM_AH		00h	OSD RAM High Address Port of Starting Access
A4h – ORAM_D		00h	OSD RAM Data Port (Low Byte first, then High Byte). After two Writes, the address will be increased by 1.

### 1Kx16 bits (=2KByte) OSD RAM Partition



### 2.10.3 Character RAM format

In Character Mode (contrast to Bit\_Map Mode), the Characters displayed on OSD can be grouped to few rows; each row has its own row attribute which defines the behavior of current character row. And, there is maximum 30 characters in one row, each character has 1~2 bytes to define its character font number and its colors. Due to providing more flexible menu programming, T102 supports three character modes:

**Table 2-2 Character Index Modes (Char\_idx\_Mode)**

#### Char\_idx\_Mode = 0

Char_Index_Mode															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				FG[3:0]				Index (Char_0)							
				FG[3:0]				Index (Char_1)							
				FG[3:0]				Index (Char_2)							

XXX-XXX0-0000

XXX-XXX0-0001

XXX-XXX0-0010

32 words

				FG[3:0]				Index (Char_29)							
				0000b				Index to Blank Char							
low Bit	Row Gap					CHS	CWS								

XXX-XXX1-1101

XXX-XXX1-1110

XXX-XXX1-1111

#### Char\_idx\_Mode = 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
			Index (Char_1)					BG	FG	Index (Char_0)						XXX-XXXX-0000
			Index (Char_3)					BG	FG	Index (Char_2)						XXX-XXXX-0001
			Index (Char_27)					BG	FG	Index (Char_26)						XXX-XXXX-1101
			Index (Char_29)					BG	FG	Index (Char_28)						XXX-XXXX-1110
low_Bt							CHS	CWS	BG_C[2:0]			FG_C[3:0]				XXX-XXXX-1111

16 words

#### Char\_idx\_Mode = 2

Char_15_0								Char_7_0								Char_3_0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
BG	FG[1:0]		Index (Char_1)					BG	FG[1:0]		Index (Char_0)					XXX-XXXX-0000							
BG	FG[1:0]		Index (Char_3)					BG	FG[1:0]		Index (Char_2)					XXX-XXXX-0001							
																} 16 words							
BG	FG[1:0]		Index (Char_27)					BG	FG[1:0]		Index (Char_26)						XXX-XXXX-1101						
BG	FG[1:0]		Index (Char_29)					BG	FG[1:0]		Index (Char_28)						XXX-XXXX-1110						
low Bt	Row Gap					CHS	CWS	BG C[2:0]				=> LUT[0]~[3]			XXX-XXXX-1111								

And the Word #1E<sub>h</sub> in Char\_idx\_Mode=0 is reserved, which must be filled with transparent color and pointed to blank font.

**2.10.3.1 Character Index Data (Address to Font Select)**

Address Offset: no (part of menu char) Access: Write Only  
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	WO	00 or BG/FG	Depends on Char_idx_Mode
[4:0]	WO	CHRA[5:0]	Character Address (Index), selects the character font (i.e., 0,1,2,... A,B,C, a,b,c,\$,%,...). If the value is number N, then it selects the N <sup>th</sup> font, and that font starting address is (N x Font_Height). The Font_Height is defined in OSD_0Fh<5>.

In Char\_idx\_Mode=0, this Index is 8 bits, and selecting one of total 256 fonts (but OSD RAM is small, for 64 fonts maximum)

In Char\_idx\_Mode=1, this Index is 6 bits, and selecting one of total 64 fonts

In Char\_idx\_Mode=2, this Index is 5 bits, and selecting one of total 32 fonts

**2.10.3.2 Character Attribute**

Address Offset: no (part of menu char) Access: Write Only  
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	WO	BG_R, BG_G, BG_B	Background R/G/B Color (Intensity=0). If all 0, then no background, i.e. transparent.
[4]	WO	Blink	Enable this Character display with blinking feature. Refer to section 2.10.4.8 for detail blinking control.
[3:0]	WO	FG_R, FG_G, FG_B, FG_I	Foreground R/G/B/Intensity Color. If the value is set as 0000b, then there will be no foreground, i.e. transparent.

**2.10.3.3 Row Attribute**

Address Offset: no (part of menu char) Access: Write Only  
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7]	WO	RGAP_BG	Color Select of Row Gap. Set 1 for selecting the same color of background of current row character, 0 for selecting transparent color.
[6:2]	WO	RGAP[4:0]	Row Gap (=Row Space). Inserted range is 4 x (31 <sub>d</sub> ~0) scan lines before current Row.
[1]	WO	CHS	Character Height Select. Set 1 for double height, 0 for single height.
[0]	WO	CWS	Character Width Select. Set 1 for double width, 0 for single width. When set to 1, only the even numbered characters will be shown, odd numbered characters are skipped.

## 2.10.4 OSD Configuration Register

### 2.10.4.1 Cfg\_00h – OSD Control Register

Address Offset: OSD\_00h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	OSD_En	Enabling the OSD function. Set 1 for enabling, 0 for disabling OSD
[6]	R/W	Bit_Map	Select Bit Mapped OSD display mode. Set 1 for Bit_Map Mode, 0 for Character Mode.
[5]	R/W	Bit2PP	Two bits per Pixel for Bit_Map mode. Set 1 for 2 Bits/Pixel, 0 for 1 Bit/Pixel.
[4]	RO	Reserved	
[3]	R/W	Font_Hx2	Character mode, fonts height double.
[2]	R/W	Early_hDE	let OSD a little shift left.
[1:0]	R/W	Font_WxN	Character mode, fonts width enlarge. Value 0~3 = x1, x2, x3, x4

### 2.10.4.2 Cfg\_01h – Character Delay\_1

Address Offset: OSD\_01h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	VERTD[10:8]	Vertical Starting Position (Upper bits) of Character displaying. These bits with Cfg_03h, total 11 bits, become 2048 steps, with an increment one pixel per step for each field.
[3]	RO	Reserved	
[2:0]	R/W	HORD[10:8]	Horizontal Starting Position (Upper bits) of Character displaying. These bits with Cfg_02h, total 11 bits, become 2048 steps, with an increment one pixel per step.

### 2.10.4.3 Cfg\_02h – Character Delay\_2

Address Offset: OSD\_02h      Access: Read/Write  
Default Value: 10h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HORD[7:0]	Horizontal Starting Position (Lower bits) of Character displaying. These bits with Cfg_01h<2:0>, total 11 bits, become 2048 steps, with an increment one pixel per step.

### 2.10.4.4 Cfg\_03h – Character Delay\_3

Address Offset: OSD\_03h      Access: Read/Write  
Default Value: 08h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VERTD[7:0]	Vertical Starting Position (Lower bits) of Character displaying. This register with Cfg_01h<6:4>, total 11 bits become 2048 steps, with an increment one line per step for each field.

**2.10.4.5 Cfg\_04h – Alpha Blending Control**

Address Offset: OSD\_04h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	FG_NoAB	OSD Character ForeGround portion will be exclusive to be blended if set to one. Default is 0 as no matter the current displayed pixels are in Character foreground or border/shadow or background or in OSD window, all will be alpha blended with original Video source.
[6:3]	RO	Reserved	
[2:0]	R/W	AB_Set[2:0]	Alpha Blending percentage (n/8). If set 000b, alpha blending is disabled ( $0/8 * \text{Original Video Source} + 8/8 * \text{OSD display}$ ); If set 001b, blending as $1/8 * \text{Original Video Source} + 7/8 * \text{OSD display}$ ; ... If set N, blending as $N/8 * \text{Original Video Source} + (8-N)/8 * \text{OSD display}$ ;

**2.10.4.6 Cfg\_05h – Char\_RAM Base Address**

Address Offset: OSD\_05h  
Default Value: 38h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	CharBA[6:0]	Programmable Character RAM Base Address. Those 7 bits become 128 steps, each step is 32 Bytes (one Character Row include Char_Index, Char_Attr, Row_Attr; i.e. 30 column maximum for each Row). The actual address will be 0RR-RRRX-XXXX (in Char_idx_Mode=0 and the CharBA[0] should be 0), or 0RR-RRRR-XXXX (for Char_idx_mode=1 or 2). The RR-RRRR means the value of CharBA[6:0]; the X-XXXX is the nth Char Column. For trading off Font number and Character number in a single RAM (this version is 1Kx16 bits), user should carefully setting this register.

**2.10.4.7 Cfg\_06h – Char\_RAM Stop Address**

Address Offset: OSD\_06h  
Default Value: 40h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	CharEA[6:0]	Programmable Character RAM Stop/End Address (Available if Revision ID $\geq 0h$ ). Those 7 bits become 128 steps, each step is 32 bytes. The actual stop address will be 0RR-RRRX-XXXX (The RRRR-RRR means the value of CharEA[6:0]; the X-XXXX is the nth Char Column. and OSD will be displayed for Character Row $\geq$ CharBA and $<$ CharEA.

**2.10.4.8 Cfg\_09h – Blinking Control**

Address Offset: OSD\_09h  
Default Value: 0Ah

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_Global_Blink	Enable whole OSD Characters blinking if set to 1.
[6:4]	RO	Reserved	
[3:2]	R/W	BCLK[1:0]	Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.
[1:0]	R/W	Duty[1:0]	For adjusting the blinking duty cycle, Set: 00b for Global Blink Off, i.e., 0% Background, 100% OSD. 01b for 25% Background, 75% OSD. 10b for 50% Background, 50% OSD. 11b for 75% Background, 25% OSD.

**2.10.4.9 Cfg\_0Ah – Bit\_Map Window Size: Height Upper Bits**

Address Offset: OSD\_0Ah  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	BMH[9:8]	Bit Map Window Height Upper bits (only available in Bit_Map mode). Please refer to OSD_0Ch for detail. User must be careful of the OSD RAM size limitation.
[3:2]	R/W	BMP_Height_xN [1:0]	Bit Map Window Vertical Enlarge (only available in Bit_Map mode). Set 00b for 1 line per dot, 01b for 2 lines per dot, 10b for 3 lines per dot, 11b for 4 lines per dot.
[1:0]	R/W	BMP_Width_xN[1:0]	Bit Map Window Horizontal Enlarge (only available in Bit_Map mode). Set 00b for 1 pixel per dot, 01b for 2 pixels per dot, 10b for 3 pixels per dot, 11b for 4 pixels per dot.

**2.10.4.10 Cfg\_0Bh – Bit\_Map Window Size: Width**

Address Offset: OSD\_0Bh  
Default Value: 0Ah

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMW[7:0]	Bit Map Window Width Lower bits (only available in Bit_Map mode). This register has 8 bits, i.e., 256 steps (value 00h is not valid), each step is 16 or 8 dots depends on Bit2PP (OSD_00h<5>) setting. When Bit2PP=0 (i.e., 1 bit/pixel), each step is 16 dots. When Bit2PP=1 (i.e., 2 bits/pixel), each step is 8 dots. User must be careful of the OSD RAM size limitation.

**2.10.4.11 Cfg\_0Ch – Bit\_Map Window Size: Height**

Address Offset: OSD\_0Ch  
Default Value: 66h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMH[7:0]	Bit Map Window Height Lower bits (only available in Bit_Map mode). This register combined with OSD_0Ah<5:4> and become 10 bits, i.e. 1024 height step: all 0 for reserved, 10'h001 for 1 line, 10'h3FF for 1023 lines. User must be careful of the OSD RAM size limitation.



**2.10.4.12 Cfg\_0Dh – Bit\_Map Window Size: Height**

Address Offset: OSD\_0Dh      Access: Read/Write  
 Default Value: 86h      Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	FontH[4:0]	Font Height. Value >=1
[2:0]	R/W	FontW[3:1]	Font WeighX2. Value 3~7 = width 6, 8, ..., 14; others = width 16

**2.10.4.13 Cfg\_0Eh – OSD Color LUT RAM Data Port**

Address Offset: OSD\_0Eh      Access: Write Only  
 Default Value: XXh      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LUT_D[7:0]	The data will be written to (or read from) OSD Color LUT RAM. After each Read or Write access to LUT RAM, then the LUT address will be increased automatically.

Note: Whenever the Configuration Index is programmed from other index value to 0Eh, the OSD Color LUT RAM becomes access capable and the address pointer is reset to 1 (the starting byte). In other words, whenever the index value is programmed to non-0Eh value, the OSD Color LUT RAM can not be access, and the pointer always kept at 1.

Note: The order to fill LUT RAM is:

1. LUT[1]\_Green/Blue
2. LUT[1]\_0000b/Red
3. LUT[2]\_Green/Blue
4. LUT[2]\_0000b/Red
5. LUT[3]\_Green/Blue
6. ----
29. LUT[15]\_Green/Blue
30. LUT[15]\_0000b/Red
31. LUT[0]\_Green/Blue (wrap to beginning)
32. LUT[0]\_0000b/Red
33. LUT[1]\_Green/Blue
34. LUT[1]\_0000b/Red
- 

**2.10.4.14 Cfg\_0Fh – OSD Color LUT RAM Data Port**

Address Offset: OSD\_0Fh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	FontW_Byte	When font width = 6 or 8 (and only), this bit is optional for the font RAM utilization. When clear to 0, fonts stored in RAM as font width >=10. When set to 1, fonts stored in RAM: Even-indexed fonts put at the high byte in RAM, and Odd-indexed fonts put at the low byte in RAM.
[5:4]	RO	Reserved	
[3:2]	R/W	Char_idx_Mode[1:0]	Character attribute/Index coding modes, 0 for original 2 bytes (256 index) mode, 1 for 1-byte (64 index) mode, 2 for 1-byte (32 index) mode, 3 for reserved.
[1:0]	R/W	CRAM_ByteAccess[1:0]	OSD RAM access pointer behavior: 0X: Word (2-bytes) R/W; (Fonts, BMP, Character Menu) 10: Low byte only; 11: High byte only; (Character Menu)

## 2.10.5 Functional Description

### 2.10.5.1 Host Access OSD RAM

#### 2.10.5.1.1 Writing Data

The OSD RAM size is 1Kx16, i.e., 1K word with each word is 2 bytes. The host interface is 8-bit data width, so whenever the host writes 2 times (one for data low byte, the other for data high byte) then it becomes one write with 16-bit data to OSD RAM.

The ORAM\_D (OSD module base address + 04h) port when writing in the 1<sup>st</sup>/3<sup>rd</sup>/5<sup>th</sup>/7<sup>th</sup>...times, it will latch lower byte of OSD RAM writing data when the host want to program Font or Character, Attribute, BMP values; and when writing 2<sup>nd</sup>/4<sup>th</sup>/6<sup>th</sup>/8<sup>th</sup>... times, it will use this 8bits data as high byte and write both two bytes to OSD RAM.

#### 2.10.5.1.2 Reading Data

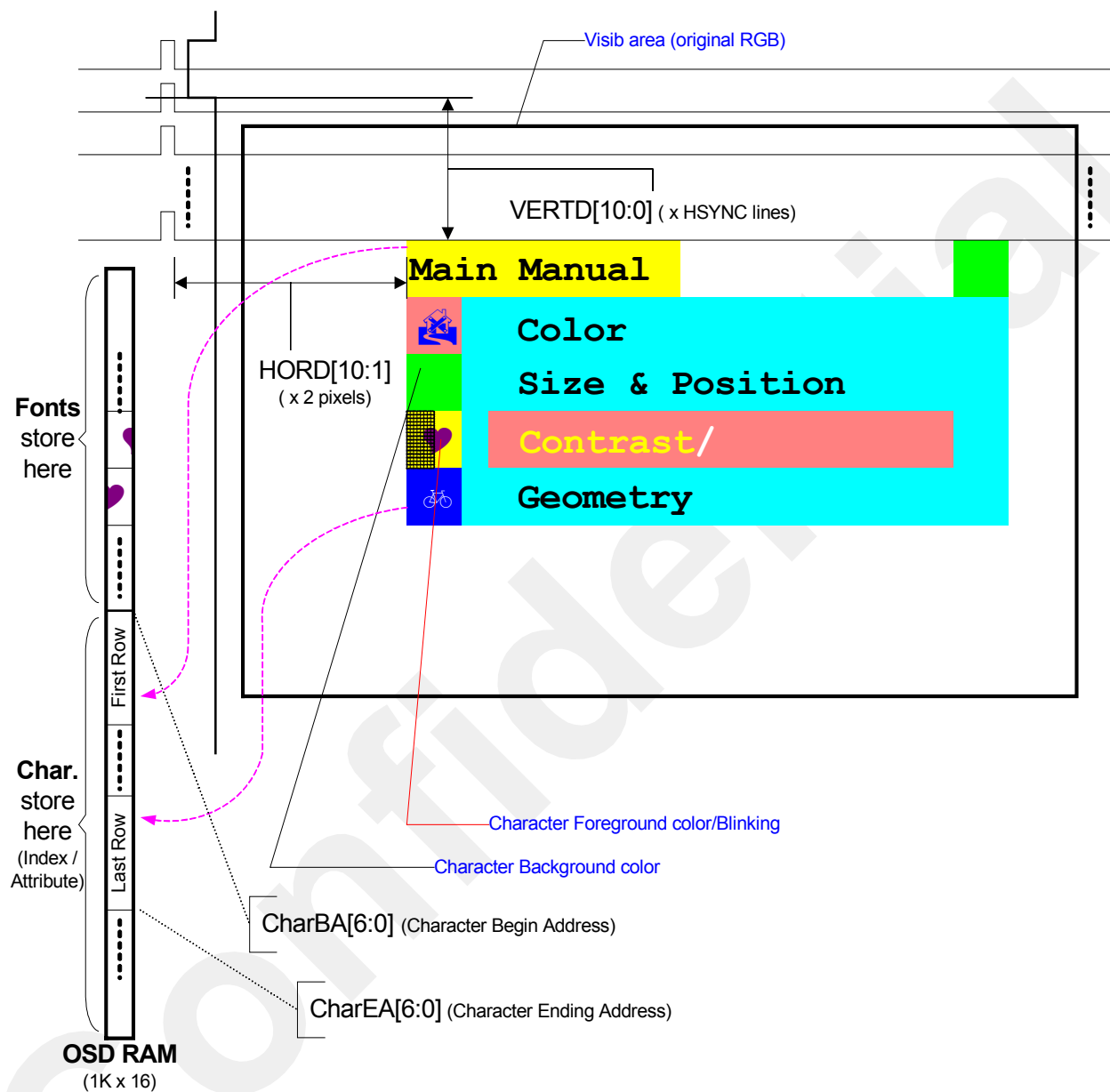
Read back data in OSD RAM is disabled.

#### 2.10.5.1.3 Access Address

The OSD RAM access pointer is programmed by the host write access to ORAM\_AL and ORAM\_AH ports. The OSD RAM size is 1Kx16, so the pointer is required to cover 1K words, i.e., 11 address lines => A[10:0]. When the host read these ORAM\_AL/ORAM\_AH ports, the pointer value reflects the current OSD RAM accessing pointer.

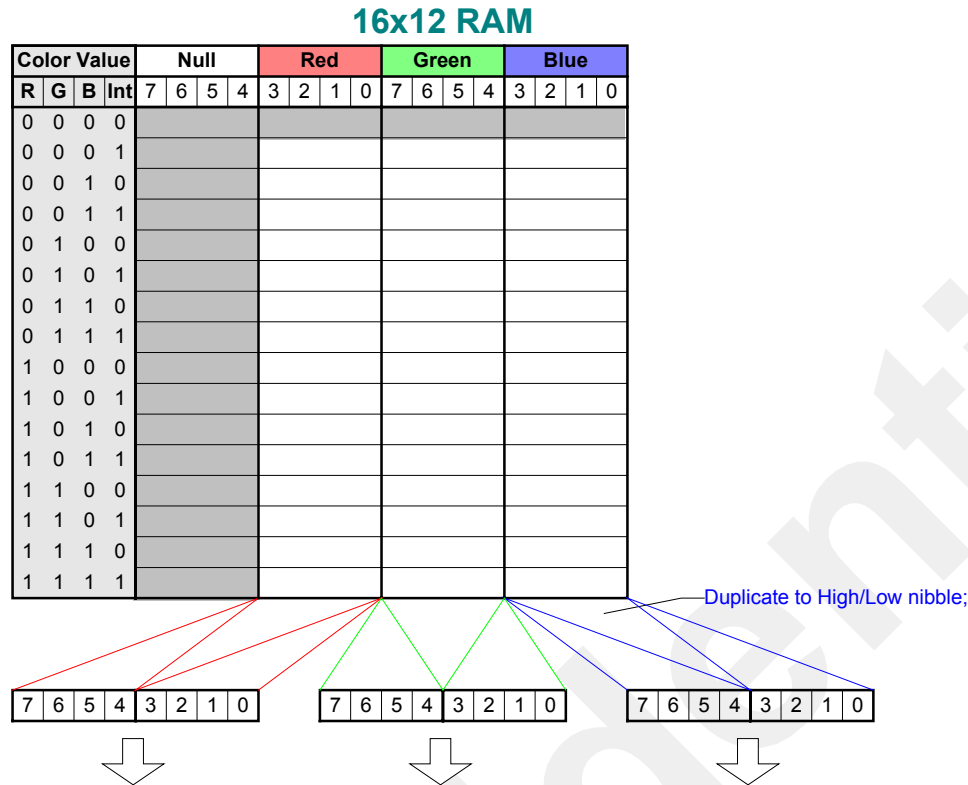
### 2.10.5.2 OSD Displaying in Character Mode

## Character Mode



### Figure 2-14 OSD Character Mode

### 2.10.5.3 OSD LUT Color Mapping



#### 1. Character Mode

1. Char\_idx\_Mode=0, FG[3:0] as Color\_0= transparent; Color\_1~15= LUT[1..15]  
BG[2:0] as Color\_0= transparent; Color\_1~7= LUT[2,4,..14]
2. Char\_idx\_Mode=1, FG as Color\_0= transparent; Color\_1= depends on its Row\_Attribute FG\_C[3:0], then redirect to transparent or LUT[1..15]  
BG as Color\_0= transparent; Color\_1= depends on its Row\_Attribute BG\_C[2:0], then redirect to transparent or LUT[2,4,..14]
3. Char\_idx\_Mode=2, FG[1:0] as Color\_0= transparent; Color\_1~3= LUT[1..3]  
BG as Color\_0= transparent; Color\_1= depends on its Row\_Attribute BG\_C[2:0], then redirect to transparent or LUT[2,4,..14]

#### 2. Bit\_Map Mode

- 1 Bit/Pixel mode: Color\_0= transparent; Color\_1= LUT[1]
- 2 Bits/Pixel mode: Color\_0= transparent; Color\_1~3= LUT[1..3]

Figure 2-15 OSD Color Look Up Table

## 2.10.5.4 Programming Examples

### 2.10.5.4.1 Configuring OSD Function

To access OSD configuration registers, write register index to port A0h, and read/write data from port A1h. For example, set :

```
IOW    A0h, 05h      ; point to OSD_05h (Char Base Address register).
IOR     A1h;          ; get Char Base Address.
IOW     A0h, 06h      ; point to OSD_06h (Char Stop Address register).
IOW     A1h, 3Eh;      ; Set Char Stop Address of current menu.
```

### 2.10.5.4.2 Fill LUT RAM

LUT RAM size is 16 (address) x 12 (width). For example, need to fill LUT RAM as:

LUT\_RAM[1]=F5Ah, ...LUT\_RAM[15]=EF0h

```
IOW     A0h, 0Eh      ; point to OSD_0Eh (LUT RAM Data port), this will let LUT RAM be
                      ; access-able and pointer starts from 0h of LUT RAM.
IOW     A1h, 5Ah;      ; fill Green = 0101b and Blue = 1010h in LUT_RAM[1].
IOW     A1h, 0Fh;      ; fill Red = 1111b in LUT_RAM[1].
                      ; after this write, h/w will increase LUT RAM address to 2 automatically
.....
IOW     A1h, F0h;      ; fill Green = 1111b and Blue = 0000h in LUT_RAM[15].
IOW     A1h, 0Eh;      ; fill Red = 1110b in LUT_RAM[15].
                      ; after this write, h/w will increase LUT RAM address to 0 automatically
IOW     A0h, non-0Eh   ; Disable LUT RAM programming.
```

### 2.10.5.4.3 Load Fonts to OSD RAM

OSD RAM size is 1K (address: 000h ~ 3FFh) x 16 (width). Fonts storing starts from address 000h. For example, loading some fonts to OSD RAM as:

Font[0] is a space (all zero), Font[1] is a character 2 with box, Font[14] is a graphic,...

```
IOW     A2h, 00h      ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW     A3h, 00h;      ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8])
                      ; then the OSD RAM address pointer is set to 000h.
IOW     A4h, 00h;      ; low byte of first row of Font[0].
IOW     A4h, 00h;      ; high byte of first row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 1 automatically
IOW     A4h, 00h;      ; low byte of 2nd row of Font[0].
IOW     A4h, 00h;      ; high byte of 2nd row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 2 automatically
..... (for example, programmed font size is 18 (height) x 12 (width)
IOW     A4h, 00h;      ; low byte of 18th (last) row of Font[0].
IOW     A4h, 00h;      ; high byte of 18th row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 012h automatically
IOW     A4h, F0h;      ; low byte of first row of Font[0]. (since font width is 12, the low byte bit[3:0]
                      ; is no use)
IOW     A4h, FFh;      ; high byte of first row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 013h automatically
.....
IOW     A2h, 68h      ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW     A3h, 01h;      ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8]),
                      ; then the OSD RAM address pointer is set to 168h = 14d * 18d.
IOW     A4h, 40h;      ; low byte of first row of Font[14].
IOW     A4h, A3h;      ; high byte of first row of Font[14],
```

## 2.11 TCON

### 2.11.1 LCD Panel Pin Assignment

In this section, we illustrate those pins connected to AU 7" TFT-LCD panel module in a T112 video system.

Table 2-3 T112 Rotation Control and LCD Panel Scanning Direction

L/R	U/D	STH	STV	Reg 0xE1	Scanning Direction
1	1	STH2	STV1	0xBC	Down-to-up, left-to-right
1	0	STH2	STV2	0xF4	Up-to-down, left-to-right
0	1	STH1	STV1	0xA8	Down-to-up, right-to-left
0	0	STH1	STV2	0xE0	Up-to-down, right-to-left

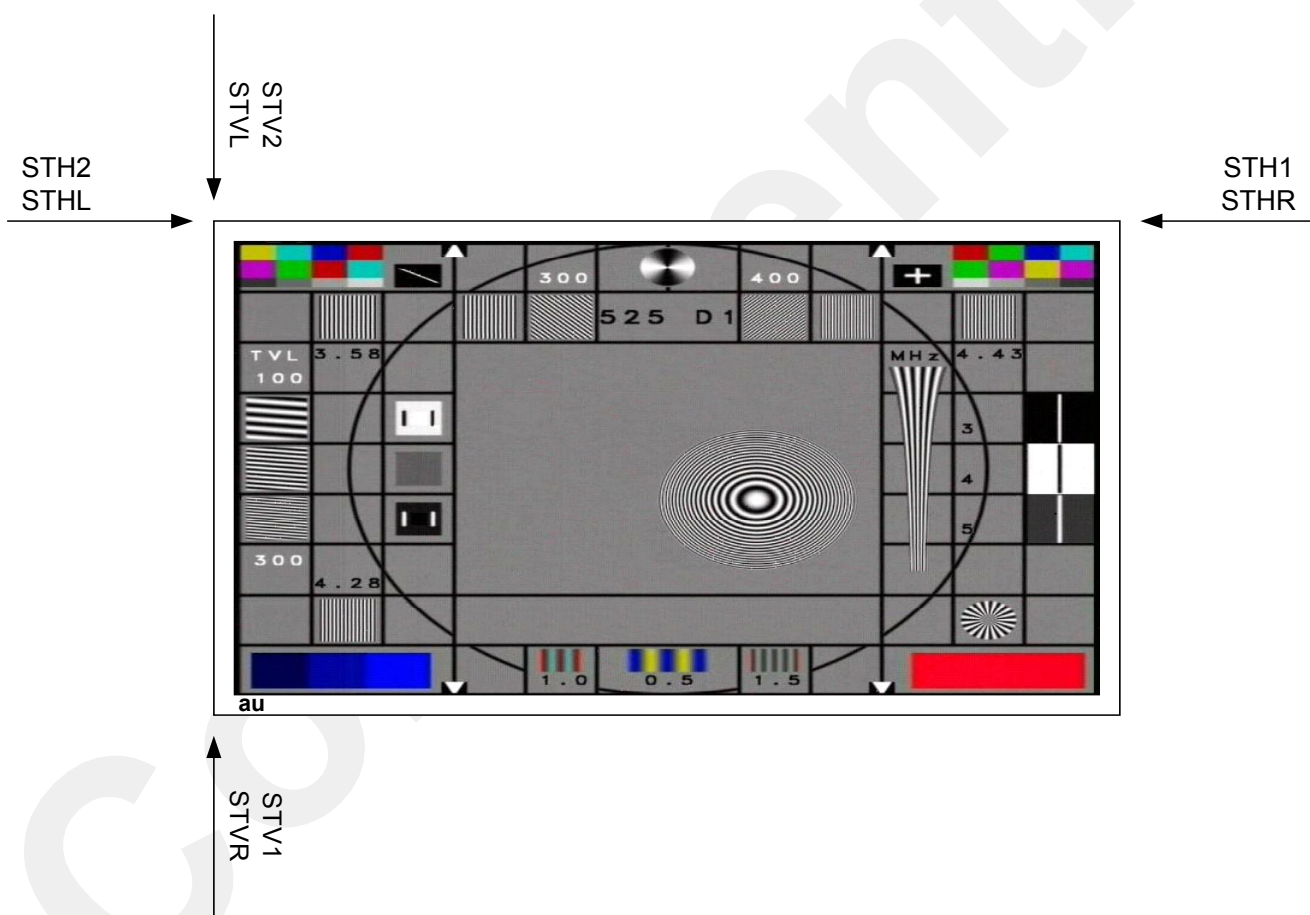


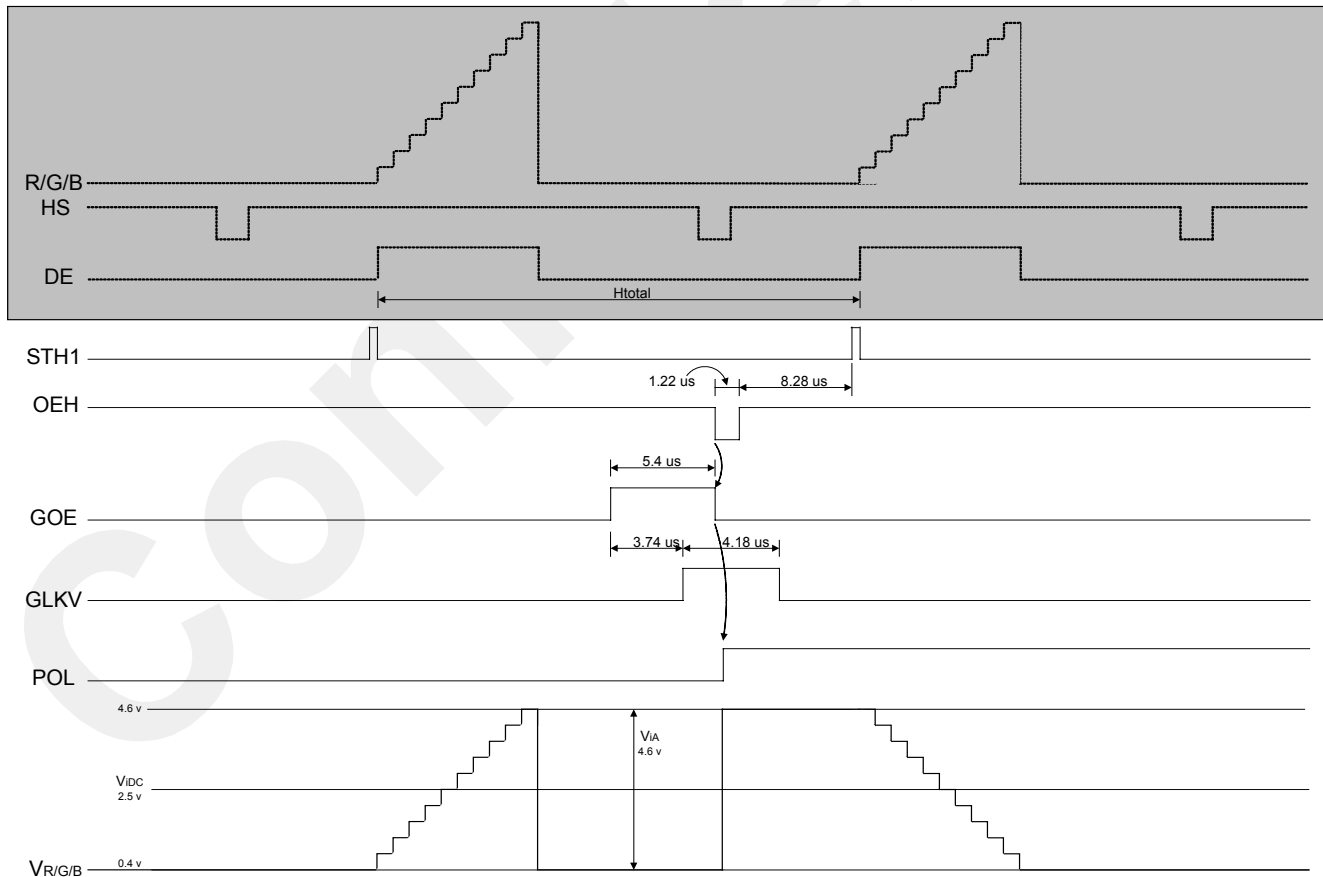
Figure 2-16 Scanning Direction of AU 7" panel

### 2.11.2 TCON Timing

T112 is designed for analog LCD panel. Each 24-bit color pixel must be converted into analog voltage via built-in triple DACs. The table 2-1 shows a typical setting for AU 7" panel with 10-Mhz operation clock.

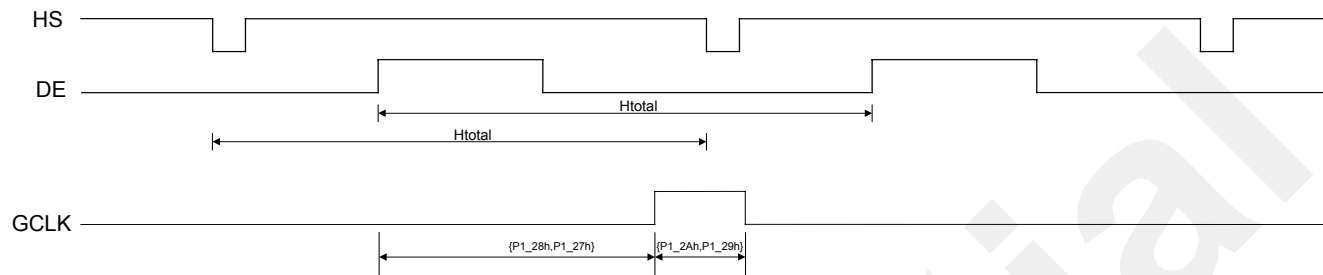
**Table 2-4 T112 TCON Register Set (C8 =1Bh, C9=03, CA=03h)**

Reg	Reg value	Operation
0x20	0x21	Line-inverted Control
0x21	0x79	Polarity Control
0x23,0x22	0x022D	Placement of OEH
0x24	0x0C	Duration of OEH
0x26,0x25	0x024B	Placement of POL
0x28,0x27	0x021C	Placement of GCLK
0x2A,0x29	0x0029	Duration of GCLK
0x2B	0x01	Placement of STH
0x30	0x01	Enable Placement of STV
0x32,0x31	0x01FB	Placement of GOE
0x34,0x33	0x0037	Duration of GOE
0x35	0x06	Placement of STV



**Figure 2-17 AU 7" TCON Timing Spec**

The waveforms shown below illustrate TCON location counting. Each TCON signal's placement and duration are allowed to program as alike as analog LCD panels require. On the figure 2-2, the pulse placement starts counting at the leading edge of DE. After placement counter meets the value we give to {P1\_27h,P1\_28h}, the duration counter starts to count until the duration meets {P1\_29h,P1\_2Ah}. All of location counting use LLCK as counter clock.



**Figure 2-18 Location Counting of GCLK**



### 3 Register Description

## Serial Bus Register Set Page 0

#### 3.1 ADC Register Set

##### 3.1.1 ADC Clamping Pulse Placement and Duration

Address Offset: 04h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	STIPCLPL	Clamping pulse placement
[4:0]	R/W	STIPCLDU	Clamping pulse duration

##### 3.1.2 ADC Channel 0 Static Gain

Address Offset: 07h      Access: Read/Write  
Default Value: 80h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCRSG	This register can set a fixed gain for ADC channel 0 when static gain control is enabled

##### 3.1.3 ADC Channel 1 Static Gain

Address Offset: 08h      Access: Read/Write  
Default Value: 80h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCGSG	This register can set a fixed gain for ADC channel 1 when static gain control is enabled

##### 3.1.4 ADC ACR Channel Offset

Address Offset: 0Ah      Access: Read/Write  
Default Value: 60h      Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_ROFF	ADC Channel 0 DC Offset Control
[1:0]	R/W	RESERVED	

##### 3.1.5 ADC AY Channel Offset

Address Offset: 0Bh      Access: Read/Write  
Default Value: 60h      Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_GOFF	ADC Channel 1 DC Offset Control
[1:0]	R/W	RESERVED	

##### 3.1.6 ADC General Control Configuration Register

Address Offset: 0Dh      Access: Read/Write  
Default Value: 20h      Size: 8 bits

Bit	Access	Symbol	Description
-----	--------	--------	-------------

[7:6]	R/W	CLPMD	Clamping mode	
			Mode	Type
			0	Fixed window
			1	Locked Window
			2	Reserved
			3	Reserved
[5]	R/W	DCEN	DC Clamping Enable	
[4]	R/W	DCSEL	Clamping Source Selection	
[3]	R/W	RESERVED		
[2]	R/W	DC_CAL_RDY	DC Calibration Ready	
[1]	R/W	DC_CALEN	DC Calibration Enable	
[0]	R/W	DC_CALMD	DC Calibration Mode	
			Mode	Type
			0	minimum
			1	average

### 3.1.7 ADC Power Down Control

Address Offset: 0Fh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	PD1	1: Power down 0: Power up
[4]	R/W	PD0	1: Power down 0: Power up
[3:0]	R/W	RESERVED	

### 3.1.8 YPbPr Clamping Control Register

Address Offset: 11h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description						
[7:6]	R/W	RESERVED							
[5]	R/W	Gmidsel	0: Midscale volt from internal ground, 1:Auto midscale volt set by CSG						
[4]	R/W	Rmidsel	0: Midscale volt from internal ground, 1:Auto midscale volt set by CSR						
[3:2]	R/W	RESERVED							
[1]	R/W	GSCALE	ADC Channel 1 Clamping Mode <table><tr><th>Mode</th><th>Select</th></tr><tr><td>0</td><td>Clamp to ground</td></tr><tr><td>1</td><td>Clamp to midscale</td></tr></table>	Mode	Select	0	Clamp to ground	1	Clamp to midscale
Mode	Select								
0	Clamp to ground								
1	Clamp to midscale								

[0]	R/W	RSCALE	ADC Channel 0 Clamping Mode	
			Mode	Type
			0	Clamp to ground
			1	Clamp to midscale

### 3.1.9 Mid-level Clamping Voltage Selection

Address Offset: 12h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

	Access	Symbol	Description	
[7:4]	R/W	RESERVED		
[3:2]	R/W	CSG	Clamping Voltage	
			Mode	Voltage Type
			0	Adaptiv Voltage
			1	0.65*Ref
			2	0.5*Ref
			3	0.35*Ref
[1:0]	R/W	CSR	Clamping Voltage	
			Mode	Voltage Type
			0	Adaptiv Voltage
			1	0.65*Ref
			2	0.5*Ref
			3	0.35*Ref

### 3.1.10 Analog Source MUX Selection

Address Offset: 18h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

	Access	Symbol	Description	
[7:4]	R/W	RESERVED		
[3:2]	R/W	AI1SEL	Analog mux selection for ADC channel 1	
			Mode	Type
			0	AY1
			1	AY0
			2	RESERVED
			3	RESERVED
[1:0]	R/W	AI0SEL	Analog mux selection for ADC channel 0	
			Mode	Type
			0	ACR1
			1	ACR0
			2	RESERVED
			3	RESERVED

### 3.1.11 Y/Cb/Cr Data Switching Control

Address Offset: 19h      Access: Read/Write  
 Default Value: 07h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	

Bit	Access	Symbol	Description										
[3:2]	R/W	YINSEL	<div>The digitized Y or composite data can be taken from one of 2 ADCs according to following table</div> <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr><tr><td>2</td><td>RESERVED</td></tr><tr><td>3</td><td>RESERVED</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1	2	RESERVED	3	RESERVED
Mode	Type												
0	ADC Ch0												
1	ADC Ch1												
2	RESERVED												
3	RESERVED												
[1:0]	R/W	CRINSEL	<div>The digitized chroma or composite data can be taken from one of 2 ADCs according to following table</div> <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr><tr><td>2</td><td>RESERVED</td></tr><tr><td>3</td><td>RESERVED</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1	2	RESERVED	3	RESERVED
Mode	Type												
0	ADC Ch0												
1	ADC Ch1												
2	RESERVED												
3	RESERVED												

### 3.1.12 ADC Analog AGC Selection

Address Offset: 1Ah  
Default Value: 42h

Access: Read/Write  
Size: 8 bits

	Access	Symbol	Description	
[7:6]	R/W	AGC_GAINMD		
			Mode	Type
			0	Positive gain
			1	Positive gain 1x~2x
			2	Negative gain 1x~2x
			3	Negative gain
[5]	R/W	AGC_FreeMM	1: release dynamic gain control whenever no signal is present 0: allow dynamic gain control	
[4:2]	R/W	RESERVED		
[1]	R/W	Y_AGC_SEL	If 0, refer to ADCGSG	
			Mode	Type
			0	Static gain
			1	Dynamic gain
[0]	R/W	CR_AGC_SEL	If 0, refer to ADCRSG	
			Mode	Type
			0	Static gain
			1	Dynamic gain

### 3.1.13 Blank Sync Level

Address Offset: 1Ch  
Default Value: C0h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLANK_SL	

### 3.1.14 ADC Read-back Selection

Address Offset: 1Dh  
Default Value: 80h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	RBK_SEL	1: Read Max of ADC data 0: Read Min of ADC data or Average of ADC data

### 3.1.15 ADC Read-back Data

Address Offset: 1Eh      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RBK_ADC[7:0]	

### 3.1.16 ADC Read-back Data

Address Offset: 1Fh      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R	RESERVED	
[1:0]	R	RBK_ADC[9:0]	

### 3.1.17 De-Interlaced Process & Vertical Shadow Control Register

Address Offset: 30h      Access: Read/Write  
Default Value: 82h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CBCR_INTERP	1: Enable CbCr interpolation 0: Disable
[6]	R/W	BLANK_LF_PR SVC	1: When Left Cropping and this bit are enabled, the original YCbCr are preserved on blank interval. 0: When Left Cropping, the original YCbCr are reset as blank color
[5]	R/W	VST_CHGSEL	1: Vsync timing change determined by 8*# of XCLK 0: Vsync timing change determined by # of hsync # can be assigned at Reg 0x3A
[4]	R/W	INT_EDGE	Interrupt polarity 1: positive 0: negative
[3]	R/W	LB_SIZE_FIXED	This bit control capture size for Scaler. 1: Hsize and Vsize are assigned by 54h ~57h 0: sizes assigned by input sources.
[2]	R/W	ENQKHS	Set 0 for normal operation
[1]	R/W	ITLCPRO	Set 1 for interlaced video Set 0 for non-interlaced video
[0]	R/W	RESERVED	

### 3.1.18 Source Select Register

Address Offset: 31h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	

[4]	R/W	RESERVED	
[3:0]	R/W	RESERVED	

### 3.1.19 Interrupt Status Register

Address Offset: 32h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R	ITLCFLM	Indicates incoming video signal is interlaced
[5:0]	R/W	INTSTS	

### 3.1.20 Interrupt Mask Register

Address Offset: 33h      Access: Read/Write  
 Default Value: FFh      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	INTMASK	

### 3.1.21 Lower 8-bit Timer Counter Register

Address Offset: 35h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_L [7:0]	Lower byte of the number of XCLK's in 1ms.

### 3.1.22 Upper 8-bit Timer Counter Register

Address Offset: 36h      Access: Read/Write  
 Default Value: 10h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_H [15:8]	Higher byte of the number of XCLK's in 1ms.

### 3.1.23 VSYNC Missing Counter Register

Address Offset: 37h      Access: Read/Write  
 Default Value: 40h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_MISS_CNT	

### 3.1.24 Lower 8-bit HSYNC Missing Counter Register

Address Offset: 38h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L [7:0]	

### 3.1.25 Upper 8-bit HSYNC Missing Counter Register

Address Offset: 39h      Access: Read/Write  
 Default Value: 10h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[15:8]	

### 3.1.26 VSYNC Delta Difference Result Register

Address Offset: 3Ah      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSYNC_DLT[7:0]	

### 3.1.27 HSYNC Delta Difference Result Register

Address Offset: 3Bh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSYNC_DLT[7:0]	

### 3.1.28 Input Sync Signal Detection Register

Address Offset: 3Fh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

	Access	Symbol	Description
[7]	R/W	HSTLSPVS	1:use trailing edge of sync to sample 0:use leading edge of sync to sample
[6]	R/W	AUTOVSD6	When the edge of vsync and hsync are too close, input detection circuit can delay 6 cycles of XCLK to avoid unstable detection  1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true. 0:Dealy 6 cycles of XCLK if FCVSD6 is true
[5]	R/W	FCVSD6	<b>AUTOVSD6 FCSVSD6T</b> 1      x      Automatically delay VSync 6 XCLK if CFSEEDGE is true 0      1      Force to delay VSync 6 XCLK 0      0      No Vsync Dealy
[4]	R	CFSEEDGE	VS and HS edges are to close.
[3:2]	R/W	RESERVED	
[1]	R/W	VsHs_Sync_Edge	1: leading edge of Vsi 0: falling edge of Hsi
[0]	R/W	VsHS_Sync_En	1:leading edge of Vsi starts at leading edge of Hsi 0:leading edge of Vsi starts at mid of Hsi

### 3.1.29 Left Border Cropping

Address Offset: 40h      Access: Read/Write  
 Default Value: 00h      Table 3-35 Left Border Cropping

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	CROP_LEFTB	Remove noisy pixels appearing on left border. 1LSB =1 pixel

**3.1.30 VSYNC Timing Measurement Register**

Address Offset: 50h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	HSPMD	Register 0x5c and 0x5d can be HS pulse width or hsync period 1:Period in # of pixel clock. 0:Hsync pulse width in # of pixel clock.
[5]	R	DONE_FRMXCLKCNT	When EN_FRAMEXCLKCNT is enabled, a whole frame time can be obtained through XCLK counting. See registers 0x51, 0x52 and 0x53.  After this bit read back as 1, then clear EN_FRAMEXCLKCNT first before reading 0x51~0x53 values.
[4]	R/W	EN_FRAMEXCLKCNT	When input VSync changes, enable this bit to start measurement on VSync using XCLK.
[3:0]	R/W	RESERVED	

**3.1.31 VSYNC Measurement Counter L Register**

Address Offset: 51h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[7:0]	

**3.1.32 VSYNC Measurement Counter M Register**

Address Offset: 52h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[15:8]	

**3.1.33 VSYNC Measurement Counter H Register**

Address Offset: 53h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[23:16]	

**3.1.34 Hsize**

Address Offset: 54h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HSIZE[7:0]	

**3.1.35 Hsize**

Address Offset: 55h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	



[3:0]	R	HSIZE[11:8]	
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**3.1.36 Vsize**

Address Offset: 56h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VSIZE[7:0]	

**3.1.37 Vsize**

Address Offset: 57h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	VSIZE[11:8]	

**3.1.38 HSYNC Period LSB Register**

Address Offset: 58h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HS_PERIOD[7:0]	HSYNC period counted by XCLK

**3.1.39 HSYNC Period MSB Register**

Address Offset: 59h      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HS_PERIOD[15:8]	HSYNC period counted by XCLK

**3.1.40 VSYNC Period LSB Register**

Address Offset: 5Ah      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VS_PERIOD[7:0]	VSYNC period counted by input HSYNC

**3.1.41 VSYNC Period MSB Register**

Address Offset: 5Bh      Access: **Read Only**  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	VS_PERIOD[11:8]	VSYNC period counted by input HSYNC

**3.1.42 HSYNC Pulse Width LSB Register**

Address Offset: 5Ch

Access: **Read Only**

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HS_WIDTH[7:0]	HSYNC pulse width or period counted by dot clock See HSPMD for detail.  Note: dot clock speed is in 1-pixel-per-clock mode

**3.1.43 HSYNC Pulse Width MSB Register**

Address Offset: 5Dh

Access: **Read Only**

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R	RESERVED	
[3:0]	R	HS_WIDTH[11:8]	HSYNC pulse width or period counted by dot clock

**3.1.44 VSYNC Pulse Width LSB Register**

Address Offset: 5Eh

Access: **Read Only**

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VS_WIDTH[7:0]	VSYNC pulse width counted by input HSYNC

**3.1.45 VSYNC Pulse Width MSB Register**

Address Offset: 5Fh

Access: **Read Only**

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R	RESERVED	
[3:0]	R	VS_WIDTH[11:8]	VSYNC pulse width counted by input HSYNC

## 3.2 Picture Enhancement Register Set

### 3.2.1 Bandwidth of Digital Color Transient Improvement

Address Offset: 60h      Access:  
Default Value: 02h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	DCTI_EC	DCTI Error Correction
[6:1]	R/W	RESERVED	
[0]	R/W	DCTI_BW	0: high bandwidth 1: low bandwidth

### 3.2.2 Luma Peaking Control

Address Offset: 61h      Access:  
Default Value: 08h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PeakingEN	
[6]	R/W	HoldLR_PIX	When this bit is enabled, the peaking doesn't affect pixels appearing at Left/Right borders.
[5:0]	R/W	PeakingCo	

### 3.2.3 Bandpass Peaking Coef

Address Offset: 62h      Access:  
Default Value: 04h      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4:0]	R/W	BP_COEF	

### 3.2.4 Highpass Peaking Coef

Address Offset: 63h      Access:  
Default Value: 04h      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4:0]	R/W	HP_COEF	

### 3.2.5 Lowpass Peaking Coef

Address Offset: 64h      Access:  
Default Value: 02h      Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	LP_COEF	

### 3.2.6 Gain and Coring of DLTI

Address Offset: 65h      Access:  
Default Value: 08h      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	DLTI_GAIN	
[4:0]	R/W	DLTI_CO	

**3.2.7 Gain and Coring of DCTI**

Address Offset: 66h

Access:

Default Value: 08h

Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	DCTI_GAIN	
[4:0]	R/W	DCTI_CO	

**3.2.8 Contrast Adjust**

Address Offset: 68h

Access:

Default Value: 80h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LumaCON	

**3.2.9 Brightness Adjust**

Address Offset: 69h

Access:

Default Value: 80h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LumaBRI	

**3.2.10 Hue Sin Adjust**

Address Offset: 6Ah

Access:

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HueSin	

**3.2.11 Hue Cos Adjust**

Address Offset: 6Bh

Access:

Default Value: 7Fh

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HueCos	

**3.2.12 Chroma Saturation Adjust**

Address Offset: 6Ch

Access:

Default Value: 80h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ChromSat	

### 3.3 Scaling Register Set

#### 3.3.1 Scaling General Control Register

Address Offset: 70h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	Inv_VideoF	Inv_VideoF: Reverse input odd field control for intra field scaling, only take action when ITLCPRO is set to 1.
[4]	R/W	Dclki_is_Faster	Software need to turn this bit on when the freq of input pixel clock is higher than output pixel clock.
[3]	R/W	Reserved	
[2]	R/W	Reserved	
[0]	R/W	C16_Pointer_RST	Reset coef table. 1: Reset write pointer to 0x00. 0: Don't Care

#### 3.3.2 Scaling Coefficient Data Port Register

Address Offset: 71h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Coef_Data_Port	

#### 3.3.3 Horizontal Scale Step LSB Register

Address Offset: 72h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [7:0]	

#### 3.3.4 Horizontal Scale Step MSB Register

Address Offset: 73h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [15:8]	

#### 3.3.5 Vertical Scale Step LSB Register

Address Offset: 74h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [7:0]	

#### 3.3.6 Vertical Scale Step MSB Register

Address Offset: 75h      Access: Read/Write

Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [15:8]	

### 3.3.7 Horizontal Aspect Ratio Register

Address Offset: 76h                      Access: Read/Write  
 Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HASPR[7:0]	

### 3.3.8 Horizontal Aspect Ratio Register

Address Offset: 77h                      Access: Read/Write  
 Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HASPEN	
[6]	R/W	HASP_C_ELG	
[5:0]	R/W	HASPR[13:8]	

### 3.3.9 Antialiasing Filtering

Address Offset: 78h                      Access: Read/Write  
 Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:4]	R/W	LPF_AVE	3: LPF ==[0.25 0.25 0.25 0.25] 2: LPF ==[0.25 0.5 0.25] 0/1:LPF ==[0 1 0]
[3]	R/W	LPF_BND_DUP	Padding starting and ending pixels at starting and ending position.
[2]	R/W	RESERVED	
[1:0]	R/W	LPF_SHPIX	Pipelined alignment for antialiasing LPF

### 3.3.10 Half Sampling and Luma High Boost

Address Offset: 79h                      Access: Read/Write  
 Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	En_Half_Input	Half Sampling by pixel reduction. When this bit is enabled, P0_30h[7] must be disabled.
[4]	R/W	RESERVED	
[3:0]	R/W	LumaHB[3:0]	Luma High Boost Coef

### 3.3.11 Chroma High Boost

Address Offset: 7Ah                      Access: Read/Write  
 Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	ChromaHB[3:0]	Chroma High Boost Coef

**3.3.12 Luma High Boost**

Address Offset: 7Bh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	YDrTh	Edge threshold value for 2 <sup>nd</sup> derivative of Luma

**3.3.13 Chroma High Boost**

Address Offset: 7Ch  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDrTh	Edge threshold value for 2 <sup>nd</sup> derivative of Chroma

**3.3.14 Scaler Frame Color Y**

Address Offset: 7Dh  
Default Value: 10h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SCFR_Y	

**3.3.15 Scaler Frame Color Cb**

Address Offset: 7Eh  
Default Value: 80h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SCFR_Cb	

**3.3.16 Scaler Frame Color Cr**

Address Offset: 7Fh  
Default Value: 80h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SCFR_Cr	

**3.3.17 Input Vsync Leading Edge to DE Time Counter 1/3 Register**

Address Offset: 81h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	TVIBLK[7:0]	Timing counter can measure the time interval between leading edge of input vsync and first valid input pixel. This time interval is TVIBLK * (1/XCLK)

**3.3.18 Input Vsync Leading Edge to DE Time Counter 2/3 Register**

Address Offset: 82h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	TVIBLK [15:8]	

**3.3.19 Input Vsync Leading Edge to DE Time Counter 3/3 Register**

Address Offset: 83h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TVIBLK[23:16]	

**3.3.20 Line Buffer Configuration LSB Register**

Address Offset: 84h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[7:0]	LBPRFL can cause a time delay in XCLK count between the leading edge of input Vsync and leading edge of output Vsync.

**3.3.21 Line Buffer Configuration MSB Register**

Address Offset: 85h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[15:8]	

**3.3.22 Output Hsync Vibration Step Register**

Address Offset: 86h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSVIB	Output HSync re-map factor in vertical Active period.

**3.3.23 Output Vsync Front Porch Remapping Register**

Address Offset: 87h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSFPRMP	Output HSync remap amount in vertical front porch period.

**3.3.24 Left Display Border Configuration Register**

Address Offset: 88h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HLDSPLB[7:0]	When Output pixel's index is less than HRDSPLB, output pixel value is assigned as left display border {FMCLRDE, FMCLRGRN, FMCLRBLU}

**3.3.25 Left Display Border Configuration Register**

Address Offset: 89h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HDSPLB_INV	Horizontal border is on if HDSPLB_INV is set as follows 1: HLDSPLB < Horizontal border < HRDSPLB 0: Horizontal border < HLDSPLB or HRDSPLB < Horizontal border



[6]	R/w	VDSPLB_INV	Vertical border is on if VDSPLB_INV is set as follows 1: VTDSPLB < VBDSPLB 0: Vertical border < VTDSPLB or VBDSPLB < Vertical border
[5]	R/W	HDSPLB_STY	Border style 1: mesh 0: solid
[4]	R/W	VDSPLB_STY	Border style 1: mesh 0: solid
[3:0]	R/W	HLDSPLB[11:8]	

### 3.3.26 Right Display Border Configuration LSB Register

Address Offset: 8Ah      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HRDSPLB[7:0]	When Output pixel's index is greater than HRDSPLB, output pixel value is assigned as right display border {FMCLRRDE, FMCLRGRN, FMCLRBLU}

### 3.3.27 Right Display Border Configuration MSB Register

Address Offset: 8Bh      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HRDSPLB[11:8]	

### 3.3.28 Top Display Border Configuration LSB Register

Address Offset: 8Ch      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VTDSPLB[7:0]	

### 3.3.29 Top Display Border Configuration MSB Register

Address Offset: 8Dh      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	HDSPLB_GRID[1:0]	H grip precision, 00b: 1 pixel 01b: 4 pixels 10b: 16 pixels 11b: 32 pixels
[5:4]	R/W	VDSPLB_GRID[1:0]	V grip precision 00b: 1 line 01b: 4 lines 10b: 16 lines 11b: 32 lines
[3:0]	R/W	VTDSPLB[11:8]	

**3.3.30 Bottom Display Border Configuration LSB Register**

Address Offset: 8Eh

Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VBDSPLB[7:0]	

**3.3.31 Bottom Display Border Configuration MSB Register**

Address Offset: 8Fh

Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VBDSPLB[11:8]	

### 3.4 Color Space Converter Register Set

#### 3.4.1 Image Function Control Register

Address Offset: 90h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description	
[7:6]	R/W	GATS[1:0]	Gamma Table Select. Default=2'b00.	
			GATS[1:0]	Polarity
			2'b11	Gamma Table R
			2'b10	Gamma Table G
			2'b01	Gamma Table B
			2'b00	All 3
[5]	R/W	RESERVED		
[4]	R/W	RESERVED	Reserved	
[3]	R/W	RESERVED	Reserved	
[2]	R/W	EN_CSC	Enable CSC	
[1]	R/W	EN_GAMMA	Enable Gamma.	
[0]	R/W	EN_DITHER	Enable Dithering.	

#### 3.4.2 Built-in Pattern Generator Control Register

Address Offset: 91h      Access: Read/Write  
 Default Value: 0Ch      Size: 8 bits

	Access	Symbol	Description										
[7]	R/W	EFMCLR	Enable Frame background color Turn on this bit may disable Scaler's color and show user-defined color on LCD panel. See 0x9D, 0x9E and 0x9F for user-defined color.										
[6]	R/W	ESLDSW	This bit may enable pattern generator shows 9 patterns sequentially. <table><tr><td>EFMCLR, ESLDSW</td><td>Output</td></tr><tr><td>2'b00</td><td>Normal Color</td></tr><tr><td>2'b01</td><td>Normal Color</td></tr><tr><td>2'b10</td><td>Still pattern</td></tr><tr><td>2'b11</td><td>Motion patterns</td></tr></table>	EFMCLR, ESLDSW	Output	2'b00	Normal Color	2'b01	Normal Color	2'b10	Still pattern	2'b11	Motion patterns
EFMCLR, ESLDSW	Output												
2'b00	Normal Color												
2'b01	Normal Color												
2'b10	Still pattern												
2'b11	Motion patterns												
[5]	R/W	VBAR	1: indicate vertical gray bars 0: indicate horizontal gray bars										
[4]	R/W	PLBIT	1: indicate 8-bit patterns 0:indicate 6-bit patterns										
[3:0]	R/W	PTN	Show nth pattern on LCD panel when EFMCLR is enabled When Both EFMCLR and ESLDSW are enabled, pattern generator may show 0, 1 ,2 ...up to PTNth. There are 12 parrerns we can show on LCD panel.										

#### 3.4.3 GAMMA Table Address Port Register

Address Offset: 93h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_ADR	Gamma coefficient table address. The Index range is 00h~20h

**3.4.4 GAMMA Table Write Data Port Register**

Address Offset: 94h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_WR_D	Gamma coefficient write data port.

**3.4.5 Black Level Expansion Threshold**

Address Offset: 95h      Access: Read/Write  
 Default Value: 10h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLE_TH	

**3.4.6**

Address Offset: 96h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	BLE_GAIN	
[3:2]	R/W	RESERVED	
[1:0]	R/W	BLE_OFFSET	

**3.4.7 CSC Y Coef**

Address Offset: 97h      Access: Read/Write  
 Default Value: 95h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	YCoefCSC	1.7-bit fixed point

**3.4.8 CSC Red Coef of Cr**

Address Offset: 98h      Access: Read/Write  
 Default Value: CCh      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_R	1.7-bit fixed point

**3.4.9 CSC Green Coef of Cb**

Address Offset: 99h      Access: Read/Write  
 Default Value: 64h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_G	0.8-bit fixed point

**3.4.10 CSC Green Coef of Cr**

Address Offset: 9Ah      Access: Read/Write  
 Default Value: D0h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_G	0.8-bit fixed point

**3.4.11 CSC Blue Coef of Cb**

Address Offset: 9Bh  
Default Value: 81h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_B	2.6-bit fixed point

**3.4.12 Pattern Color Gradient & Dithering Mode Register**

Address Offset: 9Ch  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description										
[7:4]	R/W	CLRGRDT[3:0]	When both ESLDSW and EFMCLR are enabled, CLRGRDT may set color gradient at pattern 2, 3 ,4, 5										
[3:2]	R/W	RESERVED											
[1:0]	R/W	DITHER_MD	Dithering mode. It is enabled by register 90h. <table><tr><th>DITHER_MD</th><th>Output</th></tr><tr><td>2'b00</td><td>4-bit output</td></tr><tr><td>2'b01</td><td>5-bit output</td></tr><tr><td>2'b10</td><td>6-bit output</td></tr><tr><td>2'b11</td><td>7-bit output</td></tr></table>	DITHER_MD	Output	2'b00	4-bit output	2'b01	5-bit output	2'b10	6-bit output	2'b11	7-bit output
DITHER_MD	Output												
2'b00	4-bit output												
2'b01	5-bit output												
2'b10	6-bit output												
2'b11	7-bit output												

**3.4.13**

Address Offset: 9Dh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRRDE	8 bits of red color depth for frame color.

**3.4.14 Frame Color Green Configuration Register**

Address Offset: 9Eh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRGRN	8 bits of green color depth for frame color.

**3.4.15 Frame Color Blue Configuration Register**

Address Offset: 9Fh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRBLU	8 bits of blue color depth for frame color.

### 3.5 OSD Register Set

(For detail OSD description, please refer to 2 Theory of Operation--OSD section.)

#### 3.5.1 OSD Configuration Index Port Register

Address Offset: A0h                      Access: Write Only  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	W	OSD_CFG_INDEX	OSD Configuration Address Port

#### 3.5.2 OSD Configuration Data Port Register

Address Offset: A1h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_CFG_DATA	OSD Configuration Data Port

#### 3.5.3 OSD RAM Address Port LSB Register

Address Offset: A2h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_AL	OSD RAM Address Port LSB

#### 3.5.4 OSD RAM Address Port MSB Register

Address Offset: A3h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_AH	OSD RAM Address Port MSB

#### 3.5.5

Address Offset: A4h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_D	OSD RAM Data Port

#### 3.5.6 Reserved

Address Offset: A5h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

### 3.6 LCD Output Control Register Set

#### 3.6.1 Display Window Horizontal Start LSB Register

Address Offset: B0h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

	Access	Symbol	Description
[7:0]	R/W	DWHS_L	Horizontal back porch.

#### 3.6.2 Display Window Horizontal Start MSB Register

Address Offset: B1h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWHS_H	Horizontal back porch

#### 3.6.3 Display Window Vertical Start LSB Register

Address Offset: B2h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWVS_L	Vertical back porch.

#### 3.6.4 Display Window Vertical Start MSB Register

Address Offset: B3h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWVS_H	Vertical back porch

#### 3.6.5 Display Window Horizontal Width LSB Register

Address Offset: B4h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

	Access	Symbol	Description
[7:0]	R/W	DWHSZ_L	Horizontal Active.

#### 3.6.6 Display Window Horizontal Width MSB Register

Address Offset: B5h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit		Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWHSZ_H	Horizontal Active.

#### 3.6.7 Display Window Vertical Width LSB Register

Address Offset: B6h                      Access: Read/Write  
Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWVSZ_L	Vertical Active.

### 3.6.8 Display Window Vertical Width MSB Register

Address Offset: B7h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWVSZ_H	

### 3.6.9 Display Panel Horizontal Total Dots per Scan Line LSB Register

Address Offset: B8h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PH_TOT_L	Output horizontal total dots

### 3.6.10 Display Panel Horizontal Total Dots per Scan Line MSB Register

Address Offset: B9h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PH_TOT_H	

### 3.6.11 Display Panel Vertical Total Lines per Frame LSB Register

Address Offset: BAh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PV_TOT_L	Output vertical total lines

### 3.6.12 Display Panel Vertical Total Lines per Frame MSB Register

Address Offset: BBh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PV_TOT_H	

### 3.6.13 Display Panel HSYNC Width LSB Register

Address Offset: BCh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PH_PW_L	

### 3.6.14 Display Panel HSYNC Width MSB Register

Address Offset: BDh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	



[3:0]	R/W	PH_PW_H	
-------	-----	---------	--

### 3.6.15 Display Panel VSYNC Width LSB Register

Address Offset: BEh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PV_PW_L	

### 3.6.16 Display Panel VSYNC Width MSB Register

Address Offset: BFh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PV_PW_H	

### 3.6.17 Panel Output Signal Control 1 Register

Address Offset: C0h      Access: Read/Write  
 Default Value: 01h      Size: 8 bits

Bit	Access	Symbol	Description						
[7:6]	R/W	RESERVED							
[5]	R/W	EN_SPANEL	Enable Serial RGB panel interface						
[4]	R/W	RESERVED							
[3]	R/W	DAT_NEG	1:Negative RGB Data 0:Positive RGB Data						
[2]	R/W	POUT_CTL1[2]	PHSYNC Polarity. Default=0. <table><tr><td>POUT_CTL1[2]</td><td>Polarity</td></tr><tr><td>0</td><td>ACTIVE LOW</td></tr><tr><td>1</td><td>ACTIVE HIGH</td></tr></table>	POUT_CTL1[2]	Polarity	0	ACTIVE LOW	1	ACTIVE HIGH
POUT_CTL1[2]	Polarity								
0	ACTIVE LOW								
1	ACTIVE HIGH								
[1]	R/W	POUT_CTL1[1]	PVSYNC Polarity. Default=0. <table><tr><td>POUT_CTL1[1]</td><td>Polarity</td></tr><tr><td>0</td><td>ACTIVE LOW</td></tr><tr><td>1</td><td>ACTIVE HIGH</td></tr></table>	POUT_CTL1[1]	Polarity	0	ACTIVE LOW	1	ACTIVE HIGH
POUT_CTL1[1]	Polarity								
0	ACTIVE LOW								
1	ACTIVE HIGH								
[0]	R/W	POUT_CTL1[0]	PDE polarity. Default=0. <table><tr><td>POUT_CTL1[0]</td><td>Polarity</td></tr><tr><td>0</td><td>ACTIVE LOW</td></tr><tr><td>1</td><td>ACTIVE HIGH</td></tr></table>	POUT_CTL1[0]	Polarity	0	ACTIVE LOW	1	ACTIVE HIGH
POUT_CTL1[0]	Polarity								
0	ACTIVE LOW								
1	ACTIVE HIGH								

### 3.6.18 Panel Output Signal Control 3 Register

Address Offset: C1h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description	
[7:5]	R/W	RESERVED		
[3]	R/W	DCLK_INV	DCLK Polarity. Default=0.	
			DCLK_INV	Mode
			0	Normal
			1	Inverted
[2:1]	R/W	RESERVED		

Bit	Access	Symbol	Description
[0]	R/W	DDR_SDRV	1:DDR source driver 0:SDR source driver

### 3.6.19 Panel VSYNC Frame Delay Control Register

Address Offset: C2h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	VO_INTERLACE	Convert interlaced input timing for Output timing generation.
[6:5]	R/W	HSO_to_VSO_DLY	0= 0-pixel clocks behind HSO 1=2-pixel clocks behind HSO 2=4-pixel clocks behind HSO 3=6-pixel clocks behind HSO
[4]	R/W	PSYNC_STR	1:Block input vsync triggering on output vsync 0: Allow input vsync to trigger output vsync
[3]	R/W	ELASTPHS	0= Short line, i.e., last hsync is less than 1.0 line 1= Long line, i.e., last hsync is greater than 1.0 line
[2]	R/W	EN_SAVE_REC	Save recovery mode
[1]	R/W	IGNORE_VSYNC	Ignore the input VSYNC. This can be used for output free run when input VSYN is not available
[0]	R/W	Reserved	

### 3.6.20 Panel VSYNC Frame Delay Line Count LSB Register

Address Offset: C3h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PV_DELAY_L	

### 3.6.21 Panel VSYNC Frame Delay Line Count MSB Register

Address Offset: C4h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PV_DELAY_H	Delay last stage VSync output, in the unit of output HSync leading edge.

### 3.6.22 Serial RGB Output Interface

Address Offset: C5h      Access: Read/Write  
Default Value: 22h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	SPL_VS_1T	For Serial RGB interface, Vsync pulse width can be programmed as 1 or more cycles wide, 1:1 cycle wide 0:see P0_BEh,P0_BFh
[5]	R/W	SPL_HS_1T	For Serial RGB interface, Hsync pulse width can be programmed as 1 or more cycles wide, 1:1 cycle wide 0:see P0_BCh,P0_BDh

[4:2]	R/W	RESERVED	
[1:0]	R/W	SPL_SYNC PH	Sync tip can appears at position 0,1 or 2, Where 2 stands for B, 1 for G, 0 for R 3 is not allowed.

### 3.6.23 Output RGB Reordering Register

Address Offset: C7h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description																		
[7]	R/W	RGB3XSEQ	Serial RGB output sequence 1:210-210-210 0:012-012-012, where 2 stands for B, 1 for G, 0 for R																		
[6]	R/W	RGB_CFRT	Shift Right/Left RGB 1: GBR 0: BRG																		
[5]	R/W	RGB_CFLT	Color Filter Line Toggling 1:Odd line,i.e.,1,3,5... 0:Even line, ie, 2, 4, 6...																		
[4]	R/W	RGB_CFMD	Color Filter Type 1:Delta 0:Strip																		
[3]	R/W	BIGENDIANE	0: Ro/Go/Bo[7:0] 1: Ro/Go/Bo[0:7]																		
[2:0]	R/W	RGBSWAPE	<table><tr><th>RGBSWAPE</th><th>Ro Go Bo</th></tr><tr><td>0</td><td>Ri Gi Bi</td></tr><tr><td>1</td><td>Ri Bi Gi</td></tr><tr><td>2</td><td>Gi Bi Ri</td></tr><tr><td>3</td><td>Gi Ri Bi</td></tr><tr><td>4</td><td>Bi Ri Gi</td></tr><tr><td>5</td><td>Bi Gi Ri</td></tr><tr><td>6</td><td>Bi Ri Gi</td></tr><tr><td>7</td><td>Bi Gi Ri</td></tr></table>	RGBSWAPE	Ro Go Bo	0	Ri Gi Bi	1	Ri Bi Gi	2	Gi Bi Ri	3	Gi Ri Bi	4	Bi Ri Gi	5	Bi Gi Ri	6	Bi Ri Gi	7	Bi Gi Ri
RGBSWAPE	Ro Go Bo																				
0	Ri Gi Bi																				
1	Ri Bi Gi																				
2	Gi Bi Ri																				
3	Gi Ri Bi																				
4	Bi Ri Gi																				
5	Bi Gi Ri																				
6	Bi Ri Gi																				
7	Bi Gi Ri																				

### 3.6.24 Output PLL Divider 1 Register

Address Offset: C8h      Access: Read/Write  
Default Value: 15h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Reserved	
[6:0]	R/W	PLLDIV_F	PLL feedback divider. Default=21.

### 3.6.25 Output PLL Divider 2 Register

Address Offset: C9h      Access: Read/Write  
Default Value: 02h      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	PLLDIV_I	PLL Input Divider. Default=2.

**3.6.26 Output PLL Divider 3 Register**

Address Offset: CAh  
Default Value: 03h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	PLLMX	PLL MUX Function Select
			PLL MX Mode
			2'b00 PLLCLK
			2'b01 Bypass PLL
			2'b10 Keep High
			2'b11 Keep High
[5]	R/W	PLLPD	Power down Display PLL . high active
[4]	R/W	PLLDIV2	0:PLLDIV_O=PLLDIV_O+0 1:PLLDIV_O=PLLDIV_O+1
[3:2]	R/W	DPLL_EXDIV	PLL additional divider 0: divided by 2, only valid when Serial RGB is enabled 1: divided by 4, only valid when Serial RGB is enabled 2: reserved 3: reserved
[1:0]	R/W	PLLDIV_O	PLL Output Divider. Default=1.

**3.6.27**

Address Offset: CBh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	PHASE_1	Phase of CPH1
[3:0]	R/W	DIVN	

**3.6.28 Digital Phase Delay**

Address Offset: CCh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	PHASE_3	Phase of CPH3
[3:0]	R/W	PHASE_2	Phase of CPH2

**3.6.29 Horizontal Main Display Start**

Address Offset: D8h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

	Access	Symbol	Description
[7:0]	R/W	HMDISP_STR	

**3.6.30 Horizontal Main Display Start**

Address Offset: D9h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HMDISP_STR	

**3.6.31 Vertical Main Display Start**

Address Offset: DAh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_STR	

**3.6.32 Vertical Main Display Start**

Address Offset: DBh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VMDISP_STR	

**3.6.33 Horizontal Main Display Size**

Address Offset: DCh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_SIZE	

**3.6.34 Horizontal Main Display Size**

Address Offset: DDh  
Default Value: 05h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HMDISP_SIZE	

**3.6.35 Vertical Main Display Size**

Address Offset: DEh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_SIZE	

**3.6.36 Vertical Main Display Size**

Address Offset: DFh  
Default Value: 04h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VMDISP_SIZE	

**3.6.37 Power Management Control Register**

Address Offset: E0h  
Default Value: 1Ch

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	TPDB	Default=1. When writing 0 to this bit, power down output pads except CPH1, CPH2 and CPH3
[6:5]	R/W	RESERVED	

Bit	Access	Symbol	Description
[4]	R/W	PDC_B	Power Down Comb Video Decoder. For internal software test. Low active.
[3]	R/W	CPH3_OEN	CPH3 Output enable. Low active
[2]	R/W	CPH2_OEN	CPH2 Output enable. Low active
[1]	R/W	CPH1_OEN	CPH1 Output enable. Low active
[0]	R/W	PWDNTC	Power Down DC Interface. Low active.

### 3.6.38 Output Pin Configuration

Address Offset: E1h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

	Access	Symbol	Description
[7:6]	R/W	RowSTV_Sel	RowSTV_Sel
			Mode
			2'b00 Pin STV2 = ColDrvRst, STV1=STV
			2'b01 Pin STV2 = ColDrvRst, STV1=STV
			2'b10 Output STV1, STV2 Tri-stated
			2'b11 Output STV2, STV1 Tri-stated
[5:4]	R/W	ColSTH_Sel	ColSTH_Sel
			Mode
			2'b00 Pin STH2=INVO, Pin STH1=STH
			2'b01 Pin STH2=INVO, Pin STH1=STH
			2'b10 Output STH1, STH2 Tri-stated
			2'b11 Output STH2, STH1 Tri-stated
[3]	R/W	UD_SEL	Panel Up/Down control
[2]	R/W	LR_SEL	Panel Right/Left control
[1]	R/W	Ext_POLC_sel	1: Takes external POL through LP. 0: Internal POL
[0]	R/W	PTsync_sel	Pin VSO and HSO have two functions under TCON mode, 1: Output VSO and HSO. 0: Output TCON signals

### 3.6.39 Shadow Control

Address Offset: E2h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4]	R/W	Shadow_enable	
[3:1]	R/W	Reserved	
[0]	R/W	Shadow_update_set	

### 3.6.40 DAC Power Management

Address Offset: E3h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

[3]	R/W	SL	1:Power Down DAC RGB 0:Power on DAC RGB
[2]	R/W	SLR	1:Power Down DAC R 0:Power on DAC R
[1]	R/W	SLG	1:Power Down DAC G 0:Power on DAC G
[0]	R/W	SLB	1:Power Down DAC B 0:Power on DAC B

### 3.6.41 DAC Amplitude Control

Address Offset: E4h  
Default Value: 0Fh

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4:0]	R/W	DACAMP	Fine-tune IOR/IOG/IOB amplitude

### 3.6.42 VCOM Amplitude Control

Address Offset: E5h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PDVCOM	1:Power down VCOM 0:Enable VCOM
[6:5]	R/W	RESERVED	
[4:0]	R/W	VCOMA	32-step VCOM amplitude control 0.5vpp ~1.0vpp

### 3.6.43 VCOM DC Control

Address Offset: E6h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4:0]	R/W	VCOMDC	32-step VCOM DC control 0.0v ~2.0v

### 3.6.44 OSC Clock Buffering Control

Address Offset: E7h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	XCLTO_OEN	This bit can enable/disable pin 17 0: Enable output 1: Disable output
[6:0]	R/W	RESERVED	

### 3.6.45 PWM General Control Register

Address Offset: E8h  
Default Value: 07h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4]	R/W	VPWME	Enable Volume PWM

[3]	R/W	RESERVED	
[2:0]	R/W	VPWM_FREQ_SEL	This register allow base clock has 7 types of clock freqs divided from XCLK .  000 = XCLK/2 <sup>3</sup> 001 = XCLK/2 <sup>5</sup> 010 = XCLK/2 <sup>7</sup> 011 =XCLK/2 <sup>9</sup> 100 =XCLK/2 <sup>11</sup> 101= XCLK/2 <sup>13</sup> 110=XCLK/2 <sup>15</sup> 111=XCLK/2 <sup>17</sup>

### 3.6.46 PWM Active High Time Counter Register

Address Offset: E9h      Access: Read/Write  
Default Value: 80h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VPWM_HIGH	This register may allow volume PWM high time counted by base clock The based clock is divide from XCLK , see 0xE8[2:0]

### 3.6.47 PWM2 General Control Register

Address Offset: EAh      Access: Read/Write  
Default Value: 07h      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	PWM2inSyncVS	1:sync with output vsync 0:Free run
[4]	R/W	VPWME2	Enable PWM2
[3]	R/W	RESERVED	
[2:0]	R/W	VPWM_FREQ_SEL2	This register allow base clock has 7 types of clock freqs divided from XCLK .  000 = XCLK/2 <sup>3</sup> 001 = XCLK/2 <sup>5</sup> 010 = XCLK/2 <sup>7</sup> 011 =XCLK/2 <sup>9</sup> 100 =XCLK/2 <sup>11</sup> 101= XCLK/2 <sup>13</sup> 110=XCLK/2 <sup>15</sup> 111=XCLK/2 <sup>17</sup>

### 3.6.48 PWM2 Active High Time Counter Register

Address Offset: EBh      Access: Read/Write  
Default Value: 80h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VPWM2_HIGH	This register may allow volume PWM high time counted by base clock The based clock is divide from XCLK , see 0xEA[2:0]

### 3.6.49 Serial Bus Slave Device Address Register

Address Offset: F0h      Access: Read/Write  
Default Value: 40h      Size: 8 bits



Bit	Access	Symbol	Description
[7:4]	R/W	SDADDR	
[3:0]	R/W	Reserved	

### 3.6.50 2-wire/4-wire Serial Bus Select Register

Address Offset: F1h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

	Access	Symbol	Description						
[7:4]	R/W	RESERVED							
[3]	R/w	RESERVED							
[2]	R/W	I2CATINCADR	Enable 2-wire serial bus automatic address increment. Access mode. Default=1'b1. <table><tr><td>Mode</td><td>INC</td></tr><tr><td>1'b0</td><td>Stop INC</td></tr><tr><td>1'b1</td><td>Auto INC</td></tr></table>	Mode	INC	1'b0	Stop INC	1'b1	Auto INC
Mode	INC								
1'b0	Stop INC								
1'b1	Auto INC								
[1:0]	R/W	RESERVED							

### 3.6.51 Vendor ID 1 Register

Address Offset: F3h      Access: **Read Only**  
 Default Value: 54h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VID_L	Reading this register obtains ASCII code "T". Hex value is 54h

### 3.6.52 Vendor ID 2 Register

Address Offset: F4h      Access: **Read Only**  
 Default Value: 57h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VID_H	Reading this register obtains ASCII code "W".

### 3.6.53 Device ID Register

Address Offset: F5h      Access: **Read Only**  
 Default Value: D2h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	DID	This field puts a part number in Hex "D2".

### 3.6.54 Revision ID Register

Address Offset: F6h      Access: **Read Only**  
 Default Value: A0h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	RID	This field puts a revision number in Hex "A0".

### 3.6.55 Page Selection Register

Address Offset: FFh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	

[2:0]	R/W	PAGE[2:0]	
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Confidential

## Serial Bus Register Set Page 1

### 3.7 TCON Register Set

#### 3.7.1 Timing Controller (TCON) Control Register

Address Offset: 20h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	RESERVED	
[5]	R/W	GTOE	Enable gate driver output Mode 0      Type 1      Shutdown output Enable output
[4]	R/W	DBS_Cedge	Clocking edge of STV When DBS_STV15 is enabled, DBS_Cedge can control STV alignment with falling edge or rising edge of GCLK Mode 0      Type 1      Falling edge of GCLK Rising edge of GCLK
[3]	R/W	DBS_STV15	STV 1.5-line wide Mode 0      Type 1      1 line wide 1.5 line wide
[2]	R/W	DBSCAN	Gate driver Scanning control Mode 0      Type 1      1 line/GCLK 2 lines/GCLK
[1]	R/W	Q1HPL	Q1H polarity Mode 0      Type 1      Negative Positive
[0]	R/W	PNINV	Enable line-inverted function.

#### 3.7.2 Timing Protocol & Polarity Control Register

Address Offset: 21h      Access: Read/Write  
Default Value: 7Fh      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	DRVRSTPL	Source Driver Reset Polarity When P0_E1[7:6] is not 3, Pin STV2 becomes the reset of source driver.
[6]	R/W	GTOEPL	This bit can control GOE polarity Mode 0      Type 1      Low-active Highactive

[5]	R/W	STVPL	Row Driver start pulse polarity Mode 0 1 Type Negative Positive
[4]	R/W	CLKVPL	CLKV Polarity Mode 0 1 Type Negative Positive
[3]	R/W	RESERVED	
[2]	R/W	POLPL	Source Driver POL inversion polarity Mode 0 1 Type Negative Positive
[1]	R/W	LPPL	Source Driver Latch Pulse polarity Mode 0 1 Type Negative Positive
[0]	R/W	STHPL	Source Driver Start Pulse polarity Mode 0 1 Type Negative Positive

### 3.7.3 Source Driver Latch Pulse Placement LSB Register

Address Offset: 22h      Access: Read/Write  
Default Value: 03h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPPLM[7:0]	This register allows LP to place in between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

### 3.7.4 Source Driver Latch Pulse Placement MSB Register

Address Offset: 23h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CDLPPLM[11:8]	This register allows LP to place in between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

### 3.7.5 Source Driver Latch Pulse Duration Control Register

Address Offset: 24h      Access: Read/Write  
Default Value: 21h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPDU[7:0]	This register allows LP duration programmable. counted by LLCK dot clock.

### 3.7.6 POL Placement LSB Register

Address Offset: 25h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	POLPLM[7:0]	The reference point is the leading edge of DE.

### 3.7.7 POL Placement MSB Register

Address Offset: 26h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	POLPLM[11:8]	The reference point is the leading edge of DE.

### 3.7.8 CLKV Placement LSB Register

Address Offset: 27h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVPLM[7:0]	The reference point is the leading edge of DE

### 3.7.9 CLKV Placement MSB Register

Address Offset: 28h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CLKVPLM[11:8]	The reference point is the leading edge of DE

### 3.7.10 CLKV Duration LSB Register

Address Offset: 29h      Access: Read/Write  
 Default Value: 0Fh      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVDU[7:0]	The reference point is leading edge of DE

### 3.7.11 CLKV Duration MSB Register

Address Offset: 2Ah      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CLKVDU[11:8]	The reference point is the leading edge of DE

### 3.7.12 STH Position Placement Register

Address Offset: 2Bh      Access: Read/Write  
 Default Value: 01h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	

[6:4]	R/W	STHWTH	The width of STH 000=1 CLKH wide 001=2 CLKHs wide ... 111= 8 CLKHs wide
[3]	R/W	RESERVED	
[2:0]	R/W	STHPLM[2:0]	This register allows STH to lead DE -3~3 CLKHs 011= 3 CLKHs 010= 2 CLKHs ... 111= -3 CLKHs

**3.7.13 Reserved**

Address Offset: 2Ch      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

**3.7.14 Gate Driver Predriving**

Address Offset: 2Dh      Access: Read/Write  
Default Value: 05h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GDPReDu	

**3.7.15 Second CLKV Placement LSB Register**

Address Offset: 2Eh      Access: Read/Write  
Default Value: 68h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DBCLKVPLM[7:0]	The reference point is the leading edge of DE

**3.7.16 Second CLKV Placement MSB Register**

Address Offset: 2Fh      Access: Read/Write  
Default Value: 01h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	DBCLKVPLM[11:8]	The reference point is the leading edge of DE

**3.7.17 Gate Driver Configuration Register**

Address Offset: 30h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	ESTVOFFSET	1: allow STV offset 0: STV appears 1 <sup>st</sup> DE

**3.7.18 Gate Driver OE Pulse Position Placement LSB Register**

Address Offset: 31h      Access: Read/Write  
Default Value: 0Fh      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GOEPL[7:0]	

### 3.7.19 Gate Driver OE Pulse Position Placement MSB Register

Address Offset: 32h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	GOEPL[11:8]	

### 3.7.20 Gate Driver OE Pulse Duration LSB Register

Address Offset: 33h      Access: Read/Write  
 Default Value: 0Fh      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GOEDU[7:0]	

### 3.7.21 Gate Driver OE Pulse Duration MSB Register

Address Offset: 34h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	GOEDU[11:8]	

### 3.7.22 STV Offset Register

Address Offset: 35h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	STVOFF[7:0]	

### 3.8 ITU - 656 Decoder Register Set

#### 3.8.1 ITU-656 Decoder HS Delay

Address Offset: D0h      Access: Read/Write  
Default Value: 30h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HS_DELAY656[7:0]	Unit: Cycles of Half VCLK

#### 3.8.2 ITU-656 Decoder HS Delay

Address Offset: D1h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	HS_DELAY656[11:8]	

#### 3.8.3 ITU-656 Decoder HS Pulse Width

Address Offset: D2h      Access: Read/Write  
Default Value: 20h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HS_WIDTH656[7:0]	Unit: Cycles of Half VCLK

#### 3.8.4 ITU-656 Decoder VS Delay

Address Offset: D3h      Access: Read/Write  
Default Value: 01h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VS_DELAY656[7:0]	Unit: HS

#### 3.8.5 ITU-656 Decoder VS Pulse Width

Address Offset: D4h      Access: Read/Write  
Default Value: 01h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	VS_WIDTH656[3:0]	Unit: HS

#### 3.8.6 ITU-656 Decoder HDE Start

Address Offset: D5h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSTART656[7:0]	Unit: Pixel



**3.8.7 ITU-656 Decoder HDE Start**

Address Offset: D6h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HSTART656[11:8]	Unit: Pixel

**3.8.8 ITU-656 Decoder HDE Size**

Address Offset: D7h      Access: Read/Write  
 Default Value: D0h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSIZE656[7:0]	Unit: Pixel

**3.8.9 ITU-656 Decoder HDE Size**

Address Offset: D8h      Access: Read/Write  
 Default Value: 02h      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HSIZE656[11:8]	Unit: Pixel

**3.8.10 ITU-656 Decoder Odd Field VDE Start**

Address Offset: D9h      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OVSTART656[7:0]	Unit: HS

**3.8.11 ITU-656 Decoder Odd/Even Field VDE Start**

Address Offset: DAh      Access: Read/Write  
 Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	EVPluse1	Even Filed VDE Start 1: EVSTART656=OVSTART + 1 0: EVSTART656=OVSTART
[6:4]	R/W	RESERVED	
[3:0]	R/W	OVSTART656[11:8]	Odd Filed VDE Start Unit: HS

**3.8.12 ITU-656 Decoder VDE Size**

Address Offset: DBh      Access: Read/Write  
 Default Value: F0h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSIZE656[7:0]	Unit: HS

**3.8.13 ITU-656 Decoder VDE Size**

Address Offset: DCh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VSIZE656[11:8]	Unit: HS

**3.8.14 ITU-656 Decoder VCLK Tuning**

Address Offset: DEh  
Default Value: 02h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	RESERVED	
[1]	R/W	VCLK_INV	
[0]	R/W	VCLK_DLY	Unit: 2ns

**3.8.15 ITU-656 Decoder Format Control**

Address Offset: DFh  
Default Value: 4Ch

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	ODDF_INV	Filed flag indicator 0: 1 <sup>st</sup> field =0, 2 <sup>nd</sup> field=1 1: 1 <sup>st</sup> filed =1, 2 <sup>nd</sup> field=0
[5:4]	R/W	RESERVED	
[3]	R/W	UV_ALN	UV Align
[2]	R/W	UV_INTPL	422-444 UV Interpolation
[1]	R/W	SIZE_DET	Read back Size of HDE and VDE 1:Enable 0:Disable
[0]	R/W	URBK_DET	1:Keep previous detection 0:Update current detection

## Serial Bus Register Set Page 2

### 3.9 Y/C Separation and Chroma Decoder Register Set

#### 3.9.1 Video Source Selection of Comb Filter

Address Offset: 00h      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	HPIX	Pixels per scan line. 0: 858 pixels 1: 864 pixels
[4]	R/W	VSLine_625	The number of scan lines per frame. 0 = 525 1 = 625
[3:1]	R/W	STD_MD	These bits select Standard Definition TV video mode. 000 = NTSC 001 = PAL (I,B,G,H,D,N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM
[0]	R/W	YC_SEL	This selects input video format. 0 = CVBS composite 1 = S-Video

#### 3.9.2 Bandwidth Control

Address Offset: 01h      Access: Read/Write  
Default Value: 09h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CMPV_INV	Specify analog input multiplexing mode during component video mode. 0 = non-inverted 1 = inverted
[6]	R/W	CMPV_SEL	0= S-video or CVBS 1 =YPbPr compoent video input
[5:4]	R/W	LUMA_NOTCH_BW	luma notch filter bandwidth 00 = none 01 = narrow 10 = medium 11 = wide
[3:2]	R/W	CHROMA_LP_BW	Chroma low pass filter bandwidth 0 = narrow 1 = wide 2 = extra wide 3 = extra wide
[1]	R/W	CHROMA_BST5OR10	This bit selects the burst gate width 0 = 5 subcarrier clock cycles 1 = 10 subcarrier clock cycles
[0]	R/W	PedBlk	Blank-to-black pedestal enable. 0 = no pedestal subtraction 1 = pedestal subtraction

**3.9.3 Y/C AGC Enable**

Address Offset: 02h  
Default Value: 4Fh

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	GAIN_UPDATE	Gain updating mode. 0 = per line 1 = per field
[6]	R/W	MV_LAGC_MD	Set 1 to allow the gain reduced ( P2_04) by 25% when macro-vision encoded signal is detected 0 = Disable 1 = Enable
[5:4]	R/W	DC_CLAMP_MD	DC clamping position 00 = auto 01 = backporch only 10 = syncip only 11 = off
[3]	R/W	DGAIN_EN	Enable coarse digital AGC. 0 = Disable 1 = Enable
[2]	R/W	RESERVED	
[1]	R/W	C_AGC_EN	Enable adaptive chroma AGC 0 = Disable 1 = Enable
[0]	R/W	L_AGC_EN	Enable adaptive luma AGC 0 = Disable 1 = Enable

**3.9.4 Comb Filtering Mode**

Address Offset: 03h  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/W	Color_Trap	Notch filter at the luma path after the comb filter. 0 = Disabled 1 = Enabled
[2:0]	R/W	COMB_MD	000 = 2-D adaptive comb filter 010 = 5-tap adaptive comb filter (PAL mode only) 011 = must be used for S-Video 110 = 5-tap hybrid adaptive comb filter (PAL mode only) others = reserved.

**3.9.5 Luma AGC Target Value**

Address Offset: 04h  
Default Value: DDh

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
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[7:0]	R/W	AGC_LEVEL	Luma AGC target value Note that if a MacroVision signal is detected P2_02[6] is set, then this value is automatically reduced by 25%.														
			<table><tr><th>Standard</th><th>Programming Value</th></tr><tr><td>NTSC M</td><td>DDh (221d)</td></tr><tr><td>NTSC J</td><td>CDh (205d)</td></tr><tr><td>PAL B,D,G,H,I, CN, SECAM</td><td>DCh (220d)</td></tr><tr><td>PAL M,N</td><td>DDh (221d)</td></tr><tr><td>NTSC M (MACROVISION)</td><td>A6h (166d)</td></tr><tr><td>PAL B,D,G,H,I, CN (MACROVISION)</td><td>A6h (174d)</td></tr></table>	Standard	Programming Value	NTSC M	DDh (221d)	NTSC J	CDh (205d)	PAL B,D,G,H,I, CN, SECAM	DCh (220d)	PAL M,N	DDh (221d)	NTSC M (MACROVISION)	A6h (166d)	PAL B,D,G,H,I, CN (MACROVISION)	A6h (174d)
Standard	Programming Value																
NTSC M	DDh (221d)																
NTSC J	CDh (205d)																
PAL B,D,G,H,I, CN, SECAM	DCh (220d)																
PAL M,N	DDh (221d)																
NTSC M (MACROVISION)	A6h (166d)																
PAL B,D,G,H,I, CN (MACROVISION)	A6h (174d)																

### 3.9.6 Noise Threshold

Address Offset: 05h  
Default Value: 32h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Noise_Thold	This register sets the noise value for the circuit to consider a signal noisy. The detected noise value can be read back through register P2_7Fh. If the detected noise value is greater than Noise_Thold, then register P2_3C[3] is set.

### 3.9.7 Y/C Output Control

Address Offset: 07h  
Default Value: 20h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[6]	R/W	RESERVED	
[5:4]	R/W	BLUE_SCREEN	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto 11 = Reserved
[3:0]	R/W	YC_DELAY	The range is [-5,7]

### 3.9.8 Luma Contrast

Address Offset: 08h  
Default Value: 80h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CONTRAST	$Luma_{out} = Luma_{in} * CONTRAST$ where CONTRAST is a 1.7-bit fixed point value.

### 3.9.9 Luma Brightness

Address Offset: 09h  
Default Value: 20h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BRIGHTNESS	$Luma_{out} = Luma_{in} + BRIGHTNESS - 32$

### 3.9.10 Chroma Saturation

Address Offset: 0Ah  
Default Value: 80h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SATURATION	$Chroma\_out = Chroma\_in * SATURATION$ where SATURATION is a 1.7-bit fixed point value

### 3.9.11 Chroma Hue Phase

Address Offset: 0Bh  
Default Value: 00h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HUE	$U\_out = U\_in * \cos(HUE/256*360) + V\_in * \sin(HUE/256*360)$ $V\_out = V\_in * \cos(HUE/256*360) - U\_in * \sin(HUE/256*360)$

### 3.9.12 Chroma AGC

Address Offset: 0Ch  
Default Value: 8Ah

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CHROMA_AGC	Chroma AGC target.

### 3.9.13 Chroma Kill

Address Offset: 0Dh  
Default Value: 07h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	Ckill_MD	0= uses auto hardware chroma kill 1= forces chroma kill on 2= forces chroma kill off
[5]	R/W	VBI_Ckill	1: chroma is killed during VBI 0: None
[4]	R/W	HLock_Ckill	Chroma is killed whenever horizontal locking is lost
[3:0]	R/W	LVL_Ckill	The chroma kill level

### 3.9.14 AGC Peak Nomial

Address Offset: 10h  
Default Value: 0Ah

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6:0]	R/W	AGC_PEAK	Luma peak white value For internal detection, H/W takes $4*(Agc\_peak+128)$

### 3.9.15 AGC Peak and Gate Control

Address Offset: 11h  
Default Value: A9h

Access: Read/Write  
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	AGC_Gt_Coarse_Vs	Coarse synctip and backporch gates are forced to be used during vsync when VCR signal is detected
[6]	R/W	AGC_Gt_Stip_Vs	Synctip clamping is enabled during vsync
[5:4]	R/W	AGC_GT_KillMD	Synctip and backporch gates can be suppressed by 00 = off 01 = enabled, if synctip gate is killed, kill backporch gate 10 = enabled, if synctip gate is killed, kill backporch gate, except during vsync 11 = enabled, if synctip gate is killed, do not kill backporch gate
[3]	R/W	AGC_Peak_En	Enable AGC peak white detector

[2:0]	R/W	AGC_Peak_CST	Time constant for the AGC peak white detector
-------	-----	--------------	---

### 3.9.16 Chroma DTO Incremental 0

Address Offset: 18h      Access: Read/Write  
 Default Value: 21h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CHROMA_FREQ_FIX	Fixed chroma frequency. 0: disable 1: enable
[6]		RESERVED	
[5:0]	R/W	C_FREQ[29:24]	Bits 29:24 of the 30-bit-wide chroma frequency increment.

### 3.9.17 Chroma DTO Incremental 1

Address Offset: 19h      Access: Read/Write  
 Default Value: F0h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[23:16]	Bits 23:16 of the 30-bit-wide chroma frequency increment.

### 3.9.18 Chroma DTO Incremental 2

Address Offset: 1Ah      Access: Read/Write  
 Default Value: 7Ch      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[15:8]	Bits 15:8 of the 30-bit-wide chroma frequency increment.

### 3.9.19 Chroma DTO Incremental 3

Address Offset: 1Bh      Access: Read/Write  
 Default Value: 0Fh      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[7:0]	Bits 7:0 of the 30-bit-wide chroma frequency increment.

### 3.9.20 Chroma Burst Gate Start Time

Address Offset: 2Ch      Access: Read/Write  
 Default Value: 23h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BST_GT_STR	The start of the burst gate window

### 3.9.21 Chroma Burst Gate End Time

Address Offset: 2Dh      Access: Read/Write  
 Default Value: 64h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BST_GT_END	the end of the burst gate window

### 3.9.22 Active Video Horizontal Start Time

Address Offset: 2Eh      Access: Read/Write

Default Value: 82h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_START	Active video horizontal start position

### 3.9.23 Active Video Horizontal Width

Address Offset: 2Fh                      Access: Read/Write  
 Default Value: 50h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_WIDTH	Active video horizontal pixel counts. An offset 640 is added to this register Default is (640+80)

### 3.9.24 Active Video Vertical Start

Address Offset: 30h                      Access: Read/Write  
 Default Value: 22h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_START	Active video vertical line start position. The number of half lines from the start of a field.

### 3.9.25 Active Video Vertical Height

Address Offset: 31h                      Access: Read/Write  
 Default Value: 61h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_HEIGHT	Active video vertical line counts. An offset 384 is added to this register. Default is (384+97) 481 half lines

### 3.9.26 Vsync Time Constant

Address Offset: 39h                      Access: Read/Write  
 Default Value: 0Ah                      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	FLD_POL	Set field polarity during decoding 0 : 1 for odd fields, 0 for even fields 1 : 0 for odd fields, 1 for even fields
[6]	R/W	FLIP_FLD	Flips even/odd fields during decoding
[5]	R/W	Even_DetDLY	Delay detection of even fields by 1 vertical line
[4]	R/W	Odd_DetDLY	Delay detection of odd fields by 1 vertical line
[3:2]	R/W	RESERVED	Set 2 for normal operation
[1:0]	R/W	VLoop_TCST	Vertical PLL time constant 0 = fast 1 = moderate 2 = slow 3 = very slow

### 3.9.27 Comb Video Status Register 1

Address Offset: 3Ah                      Access: Read only  
 Default Value: 00h                      Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R	MV_CLR_STP	Macrovision color stripes detected. MV_CLR_STP indicates the number of color stripe lines in each group



[4]	R	MV_VBI_DET	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Not Found
[3]	R	ChromaLock	Chroma PLL locked to color burst 1 = Locked 0 = Unlocked
[2]	R	Vlock	Vertical lock 1 = Locked 0 = Unlocked
[1]	R	Hlock	Horizontal line locked 1 = Locked 0 = Unlocked
[0]	R	No_signal	No signal detected 1 = No Signal 0 = Signal Detected

### 3.9.28 Comb Video Status Register 2

Address Offset: 3Bh      Access: Read only  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:3]		RESERVED	
[2]	R	CKILLON	1:chroma is being killed 0:no chroma is being killed
[1]	R	WeakChroma	1:indicates incoming signal contains weak color burst 0:no weak color burst amplitude is present
[0]	R	Proscan_detected	Progressive Scan Video Detected

### 3.9.29 Comb Video Status Register 3

Address Offset: 3Ch      Access: Read only  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7]	R	VCRrew	VCR Rewind Detected
[6]	R	VCRff	VCR Fast-Forward Detected
[5]	R	VCRtrk	VCR Trick-Mode Detected
[4]	R	VCRin	VCR Detected
[3]	R	Noisy	Noisy Signal Detected. This bit is set when the detected noise value (status register P2_7Fh) is greater than the value programmed into register ( P2_05h).
[2]	R	Vline625_present	625 Scan Lines present
[1]	R	SECAM_present	SECAM color mode present
[0]	R	PAL_present	PAL color mode present

### 3.9.30 Soft Reset

Address Offset: 3Fh      Access: Read/Write  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	Soft_Reset	Soft Reset: Write 1 to reset initial values for comb filter

### 3.9.31 Comb Filter Noise Status

Address Offset: 7Fh      Access: Read only  
Default Value: 00h      Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	CombF_Noise	Noise indicator. Larger values indicate noisier signals. CombF_Noise can be used with P2_05h and P2_3C[3]

### 3.9.32 Luminance Peaking Control

Address Offset: 80h      Access: Read/Write  
Default Value: 04h      Size: 8 bits

Bit	Access		Description
[7:6]	R/W	RESERVED	
[5:4]	R/W	PEAK_RANGE	Luma peaking enhancement during decoding  PEAK_RANGE[1:0]Peak Range Value 01 12 24 38  $Y_{peak} = Y + YH * (peak\_gain/peak\_range)$ , where Y is the luma and YH is the high frequency luma only
[3:1]	R/W	PEAK_GAIN	The gain of peaking filter
[0]	R/W	PEAK_EN	Luma peaking control enable. 0 = Disable 1 = Enable

### 3.9.33 Comb Filter Configuration

Address Offset: 82h      Access: Read/Write  
Default Value: 42h      Size: 8 bits

	Access	Symbol	Description
[7]		RESERVED	
[6]	R/W	PAL_ERR	Reduce phase error artifacts in the comb filter's luma path. Set for VCR signals
[5]	R/W	PERR_AUTO_EN	1: Turn on PAL_PERR when VCR input is detected 0: None
[4]	R/W	COMB_PAL_WBAND	The bandpass filter used in the comb-filter when input is PAL
[3:2]		RESERVED	
[1:0]	R/W	PAL_SW_LEVEL	PAL switch level. Higher level for noisy signals.

### 3.9.34 Chroma Lock Configuration

Address Offset: 83h      Access: Read/Write  
Default Value: 6Fh      Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	Lose_Chroma_LkCnt	The time period to adjust Chromakill, Higher values are more sensitive to losing lock
[3:1]	R/W	Lose_Chroma_level	Level of Chromakill.
[0]	R/W	Lose_C_Ckill	1: When ChromaLock is lost, Chromakill takes action 0: None

## 4 Electrical Characteristics

### 4.1 Digital I/O Pad Operation Condition

**Table 4-1 Digital I/O Operation Condition**

	Parameter	Min	Typ	Max
VDD25	Digital Core Power Supply	2.25V	2.50V	2.75V
VD33	Digital I/O Power Supply	3.0V	3.3V	3.6V
V <sub>IL</sub>	Input Low Voltage	-0.3V		0.8V
V <sub>IH</sub>	Input High Voltage	2.0V		5.0V
V <sub>T+</sub>	Schmitt Trigger Low-to-High Threshold	1.44V	1.58V	1.71V
V <sub>T+</sub>	Schmitt Trigger High-to-Low Threshold	1.09V	1.19V	1.31V
I <sub>I</sub>	Input Leakage Current@ V <sub>I</sub> =3.3V or 0V			±1μ A
I <sub>OZ</sub>	Tri-state Output Leakage Current@ V <sub>O</sub> =3.3V or 0V			±1μ A
I <sub>OL</sub>	Low level Output Current@ V <sub>OL</sub> =0.4V			
	2mA	2.1mA	3.4mA	4.2mA
	4mA	4.2mA	6.9mA	8.6mA
	8mA	8.4mA	13.9mA	17.2mA
	12mA	12.5mA	20.8mA	25.8mA
I <sub>OH</sub>	High level Output Current@ V <sub>OH</sub> =2.4V			
	2mA	3.0mA	6.2mA	10.0mA
	4mA	5.7mA	11.6mA	18.6mA
	8mA	9.5mA	19.4mA	30.9mA
	12mA	13.3mA	27.1mA	43.3mA
R <sub>PD</sub>	Pull-up resistor	74KΩ	104KΩ	177KΩ
R <sub>PD</sub>	Pull-down resistor	62KΩ	90KΩ	176KΩ

Note: R<sub>PD</sub> and R<sub>PD</sub> are always present no matter normal operation or power down mode is enabled. A typical 30~40μ A false leakage current which is resulted from R<sub>PD</sub> and R<sub>PD</sub> when a tester forces I/O to 3.3V or 0.0 V.

## 4.2 DC Characteristics

( DVDD=AVDD=2.5V; AVD33R=AVD33G=AVD33B=3.3V; VREFIN=1.235V; RL=37.5ohm, CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted )

**Table 4-2 DAC Operation Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	AVD33R AVD33G AVD33B	3.0	3.3	3.6	V	
Operating voltage range	AVDD	2.25	2.5	2.75	V	
Operating voltage range	DVDD	2.25	2.5	2.75	V	
AVD33R supply current	IAVD33R	--	35	--	mA	SL=0, SLR=0
AVD33G supply current	IAVD33G	--	35	--	mA	SL=0, SLG=0
AVD33B supply current	IAVD33B	--	35	--	mA	SL=0, SLB=0
AVDD supply current	IAVD33	--	1	--	mA	SL=0
VDD supply current	IDVDD	--	TBD	--	mA	
Full scale current	IOFS	2.00	34.08	--	mA	Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. $RSET(ohm)=VREFIN(V)*10.66/IOFS(A)$ ,where IOFS is full-scale output current.
Output voltage range	V(IO)	--	1.28	--	V	.
DAC resolution	--	--	10	--	bits	.
Integral non-linearity error	INL	--	0.5	+2	LSB	.
Differential non-linearity error	DNL	--	0.5	+1	LSB	.
Gain error	--	--	--	TBD	%	.
DAC to DAC matching	--	--	TBD	TBD	%	.

### 4.3 AC Characteristics

(DVDD=AVDD=2.5V; AVD33R=AVD33G=AVD33B=3.3V; VREFIN=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp =75oC, unless otherwise noted)

**Table 4-3 DAC Parameters**

Parameter	Sym	Min	Typ	Max	Unit	Condition
CK period	Tck	5	--	--	Ns	
CK to valid output	Tdelay	--	--	0.5*Tck+2	Ns	
Output rise time	Tr	--	--	4	Ns	10% to 90% IOFS; assume no package inductance.
Output fall time	Tf	--	--	4	Ns	90% to 10% IOFS; assume no package inductance.
Output settling time	Tsettle	--	--	TBD	Ns	assume no package inductance
Glitch energy	--	--	--	--	pvs	assume no package inductance
DAC to DAC crosstalk	--	--	TBD	--	Db	.

### 4.4 Analog Processing and A/D Converters

**Table 4-4 ADC Parameters**

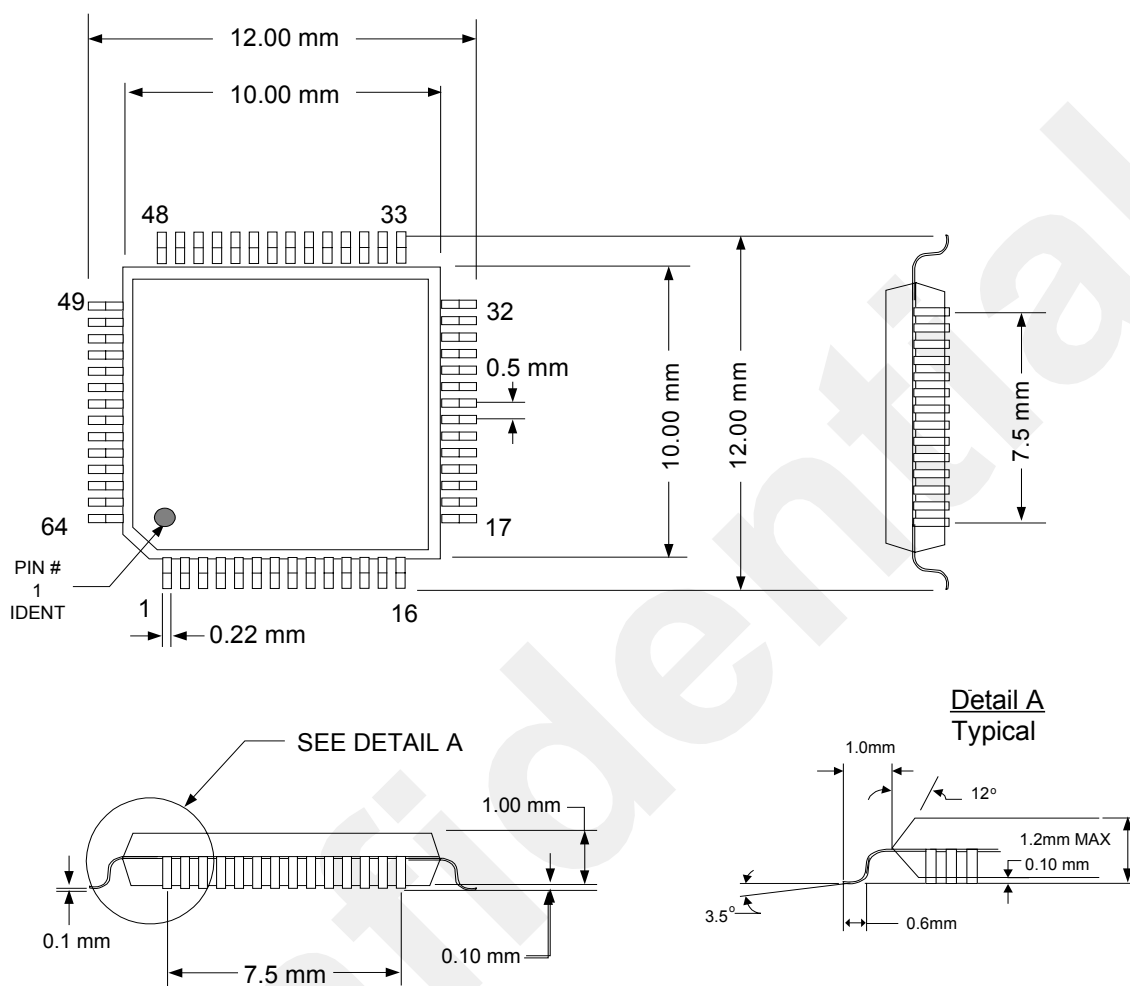
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Zi</b> Input impedance, analog video inputs	By design		500		kΩ
<b>Ci</b> Input capacitance, analog video inputs	By design		10		pF
<b>Vi(pp)</b> Input voltage range†	Ccoupling = 0.1μF	<b>0</b>		<b>0.75</b>	V
<b>ΔG</b> Gain control range		<b>0</b>		<b>12</b>	dB
<b>DNL</b> DC differential nonlinearity	A/D only		±0.5		LSB
<b>INL</b> DC integral nonlinearity	A/D only		±1		LSB
<b>Fr</b> Frequency response	6 MHz		-0.9	-3	dB
<b>SNR</b> Signal-to-noise ratio	6 MHz, 1.0 Vp-p		50		dB
<b>NS</b> Noise spectrum	50% flat field		50		dB
<b>DP</b> Differential phase			1.5		
<b>DG</b> Differential gain			0.5%		

### 4.5 Absolute Maximum Rating

**Table 4-5 Min AND Max Temperature**

Parameter	Min	Max	Unit
Topr Operation Temperature	-20	+85	°C
Tstg Storage Temperature	-65	+150	°C

## 5 Package Dimensions



**64 LQFP 10 X 10 X 1.0 mm**

**Figure 5-1**

## 6 Ordering Information

**Table 6-1**

Part No.	Package
T112	64 LQFP

## 7 Revisions Note

Table 7-1

Revisions	Description of changes	Date	Note
0.1	First draft	AUG. 25, 2005	
0.2	Enhanced DAC	JAN. 06, 2006	

## 8 General Disclaimer

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