

# PWM-FF IC

ICE2AS01/S01G

ICE2BS01/S01G

Off-Line SMPS Current Mode  
Controller

Power Management & Supply



Never stop thinking.

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**ICE2AS01/G**  
**ICE2BS01/G****Revision History: 2002-02-01****Datasheet**

Previous Version:

Page	Subjects (major changes since last revision)

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## Off-Line SMPS Current Mode Controller

### Product Highlights

- **Enhanced Protection Functions all with Auto Restart**
- **Lowest Standby Power Dissipation**
- **Very Accurate Current Limiting**



P-DIP-8-4



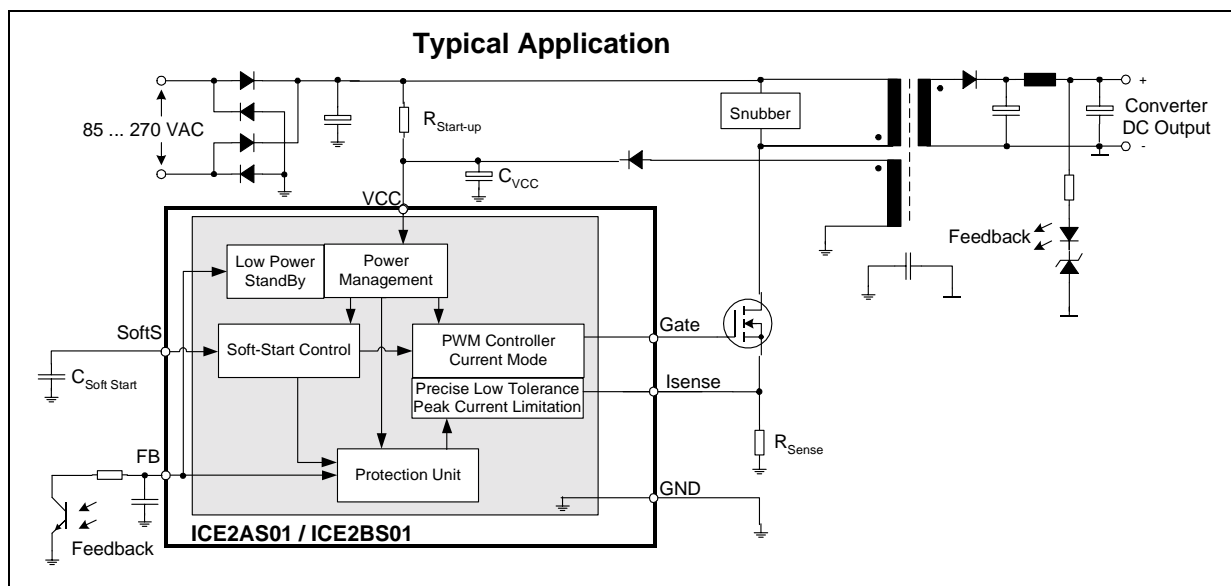
P-DSO-8-3

### Features

- Only few external Components required
- Input Undervoltage Lockout
- 67kHz/100kHz fixed Switching Frequency
- Max Duty Cycle 72%
- Low Power Standby Mode to support "Blue Angle" Norm
- Latched Thermal Shut Down
- Overload and Open Loop Protection
- Overvoltage Protection during Auto Restart
- Adjustable Peak Current Limitation via External Resistor
- Overall Tolerance of Current Limiting  $< \pm 5\%$
- Internal Leading Edge Blanking
- Soft Start
- Soft Switching for Low EMI

### Description

This stand alone controller provides several special enhancements to satisfy the needs for low power standby and protection features. In standby mode frequency reduction is used to lower the power consumption and provide a stable output voltage in this mode. The frequency reduction is limited to 20kHz / 21.5 kHz (typ.) to avoid audible noise. In case of failure modes like open loop, overvoltage or overload due to short circuit the device switches in Auto Restart Mode which is controlled by the internal protection unit. By means of the internal precise peak current limitation the dimension of the transformer and the secondary diode can be lower which leads to more cost efficiency.



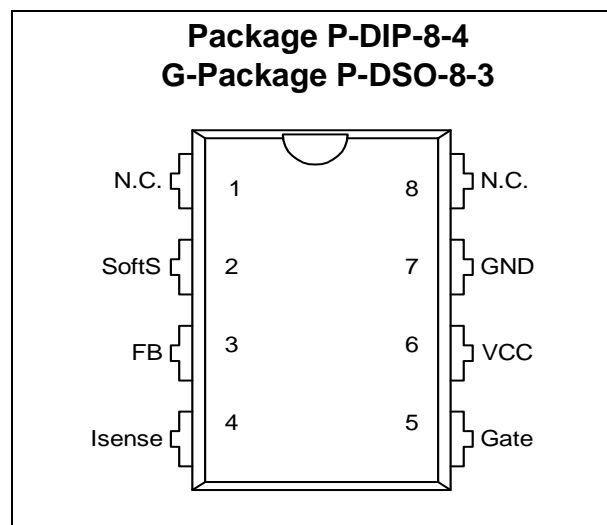
Type	Ordering Code	Frequency	Package
ICE2AS01	Q67040-S4472	100kHz	P-DIP-8-4
ICE2AS01G	Q67040-S4473	100kHz	P-DSO-8-3
ICE2BS01	Q67040-S4475	67kHz	P-DIP-8-4
ICE2BS01G	Q67040-S4476	67kHz	P-DSO-8-3

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# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration

Pin	Symbol	Function
1	N.C.	Not connected
2	SoftS	Soft Start & Auto Restart Control
3	FB	Regulation Feedback
4	Isense	Controller Current Sense Input
5	Gate	Driver Output
6	VCC	Controller Supply Voltage
7	GND	Controller Ground
8	N.C.	Not connected



**Figure 1** Pin Configuration (top view)

## 1.2 Pin Functionality

### SoftS (Soft Start & Auto Restart Control)

This pin combines the function of Soft Start in case of Start Up and Auto Restart Mode and the controlling of the Auto Restart Mode in case of an error detection.

### FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle.

### Isense (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the external Power Switch. When Isense reaches the internal threshold of the Current Limit Comparator, the Driver output is disabled. By this mean the Over Current Detection is realized.

Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

### Gate (Driver Output)

The current and slew rate capability of this pin are suited to drive Power MOSFETs.

### VCC (Power supply)

This pin is the positiv supply of the IC. The operating range is between 8.5V and 21V.

To provide overvoltage protection the driver gets disabled when the voltage becomes higher than 16.5V during Start up Phase.

### GND (Ground)

This pin is the ground of the primary side of the SMPS.

## 2 Representative Blockdiagram

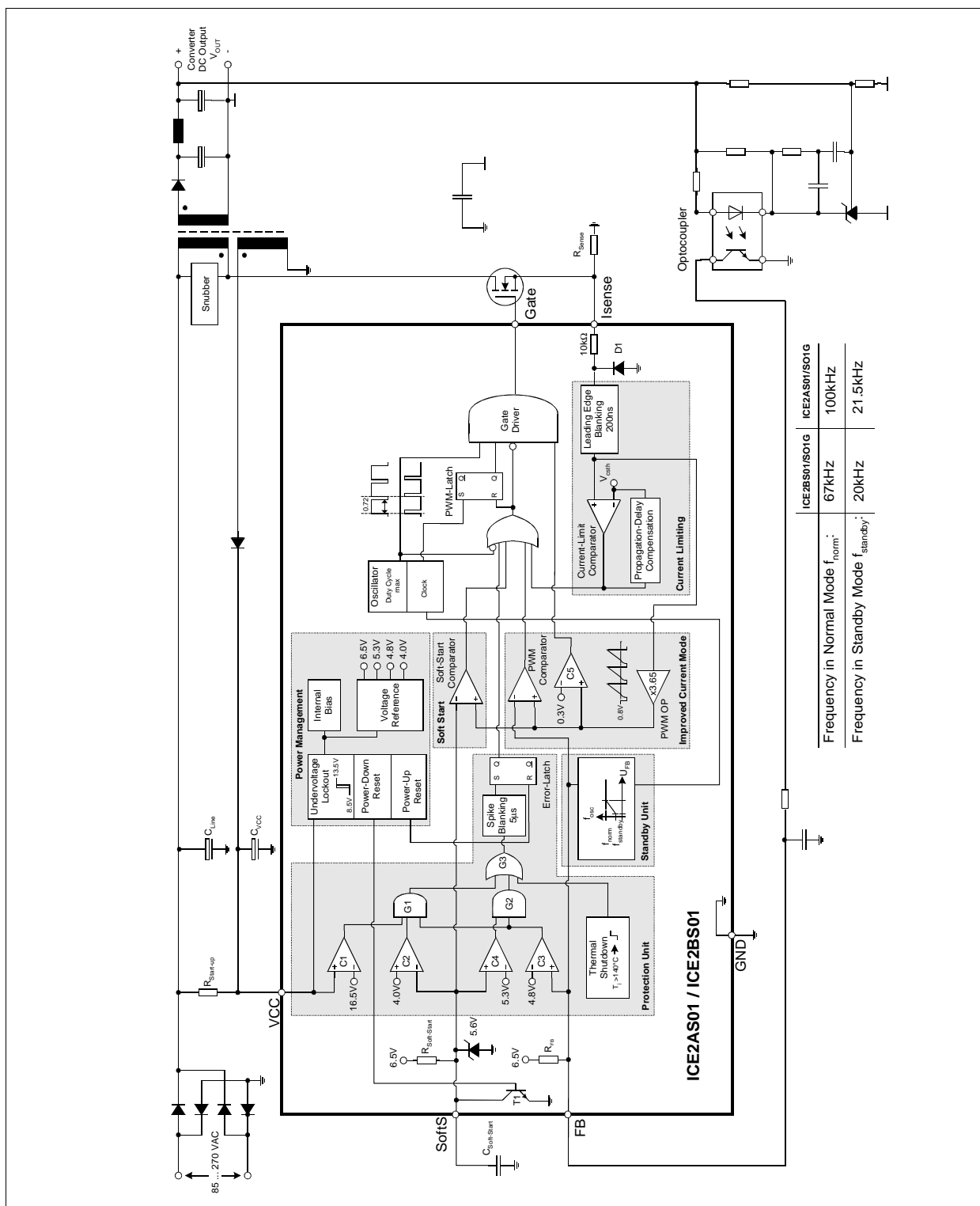
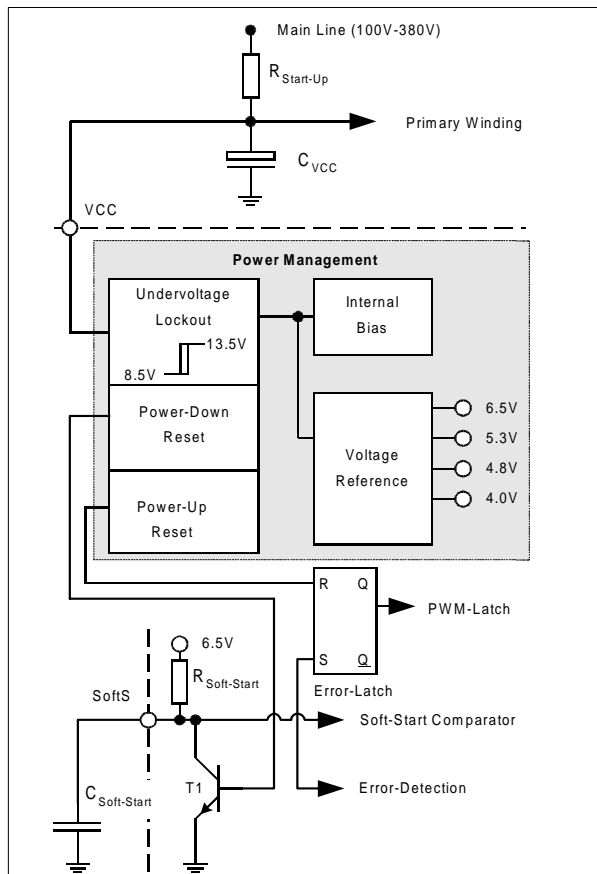


Figure 2

## 3 Functional Description

### 3.1 Power Management



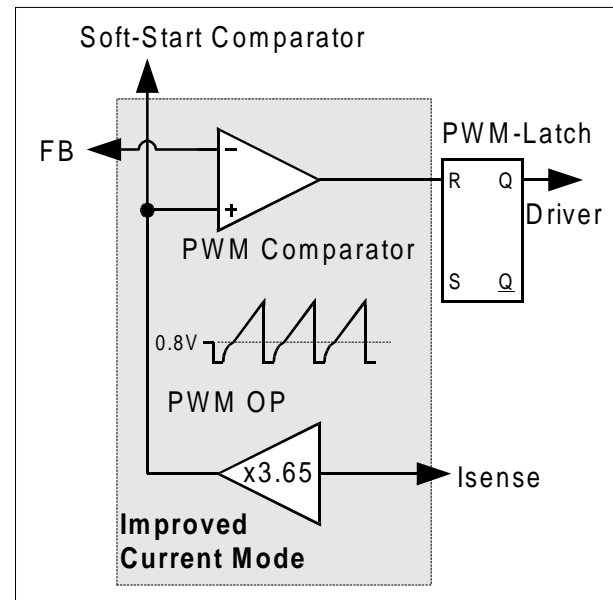
**Figure 3** Power Management

The Undervoltage Lockout monitors the external supply voltage  $V_{CC}$ . In case the IC is inactive the current consumption is max.  $55\mu A$ . When the SMPS is plugged to the main line the current through  $R_{Start-Up}$  charges the external Capacitor  $C_{VCC}$ . When  $V_{CC}$  exceeds the on-threshold  $V_{CCon}=13.5V$  the internal bias circuit and the voltage reference are switched on. After it the internal bandgap generates a reference voltage  $V_{REF}=6.5V$  to supply the internal circuits. To avoid uncontrolled ringing at switch-on a hysteresis is implemented which means that switch-off is only after active mode when  $V_{CC}$  falls below  $8.5V$ .

In case of switch-on a Power Up Reset is done by resetting the internal error-latch in the protection unit.

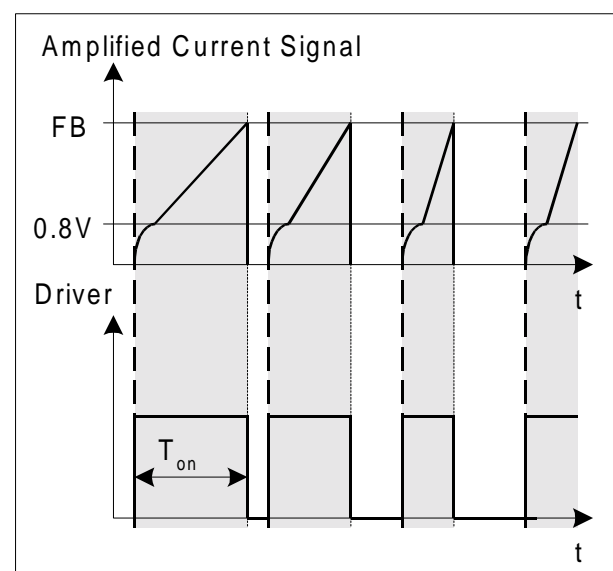
When  $V_{CC}$  falls below the off-threshold  $V_{CCoff}=8.5V$  the internal reference is switched off and the Power Down reset let T1 discharging the soft-start capacitor  $C_{Soft-Start}$  at pin SoftS. Thus it is ensured that at every switch-on the voltage ramp at pin SoftS starts at zero.

### 3.2 Improved Current Mode



**Figure 4** Current Mode

Current Mode means that the duty cycle is controlled by the slope of the primary current. This is done by comparison the FB signal with the amplified current sense signal.



**Figure 5** Pulse Width Modulation

In case the amplified current sense signal exceeds the FB signal the on-time  $T_{on}$  of the driver is finished by resetting the PWM-Latch (see Figure 5).

## Functional Description

The primary current is sensed by the series resistor  $R_{\text{sense}}$  inserted in the source of the external Power Switch. By means of Current Mode the regulation of the secondary voltage is insensitive on line variations. Line variation causes variation of the increasing current slope which controls the duty cycle.

The external  $R_{\text{Sense}}$  allows an individual adjustment of the maximum source current of the external Power Switch.

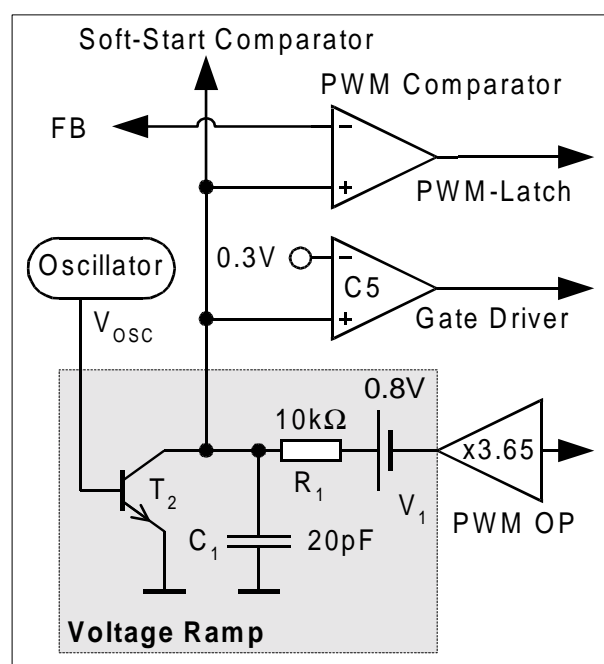
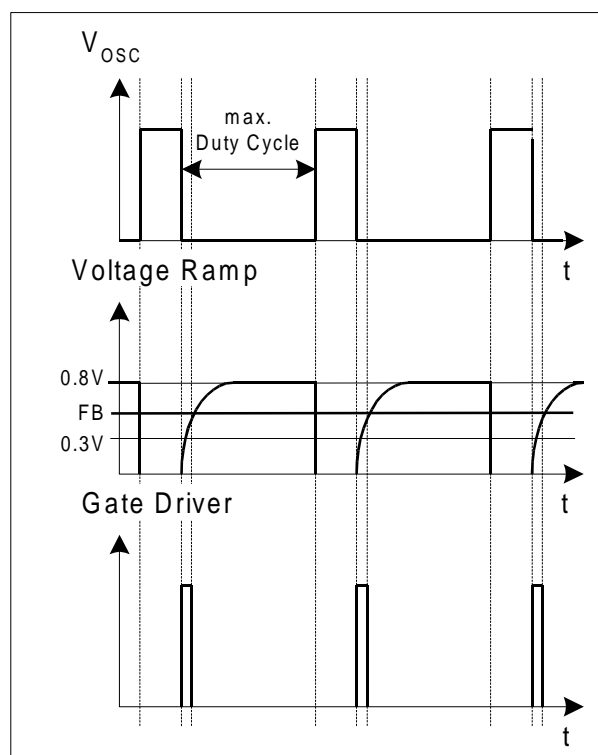


Figure 6 Improved Current Mode

To improve the Current Mode during light load conditions the amplified current ramp of the PWM-OD is superimposed on a voltage ramp, which is built by the switch  $T_2$ , the voltage source  $V_1$  and the 1st order low pass filter composed of  $R_1$  and  $C_1$  (see Figure 6, Figure 7). Every time the oscillator shuts down for max. duty cycle limitation the switch  $T_2$  is closed by  $V_{OSC}$ . When the oscillator triggers the Gate Driver  $T_2$  is opened so that the voltage ramp can start (see Figure 7).

In case of light load the amplified current ramp is too small to ensure a stable regulation. In that case the Voltage Ramp is a well defined signal for the comparison with the FB-signal. The duty cycle is then controlled by the slope of the Voltage Ramp.

By means of the C5 Comparator the Gate Driver is switched-off until the voltage ramp exceeds 0.3V. It allows the duty cycle to be reduced continuously till 0% by decreasing  $V_{FB}$  below that threshold.



*Figure 7 Light Load Conditions*

### 3.2.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor  $R_{\text{Sense}}$  connected to pin ISense.  $R_{\text{Sense}}$  converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.65 by PWM OP. The output of the PWM-OP is connected to the voltage source V1. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM-Comparator, C5 and the Soft-Start-Comparator.

### 3.2.2 PWM-Comparator

The PWM-Comparator compares the sensed current signal of the external Power Switch with the feedback signal  $V_{FB}$  (see Figure 8).  $V_{FB}$  is created by an external optocoupler or external transistor in combination with the internal pullup resistor  $R_{FB}$  and provides the load information of the feedback circuitry. When the amplified current signal of the external Power Switch exceeds the signal  $V_{FB}$  the PWM-Comparator switches off the Gate Driver.



## Functional Description

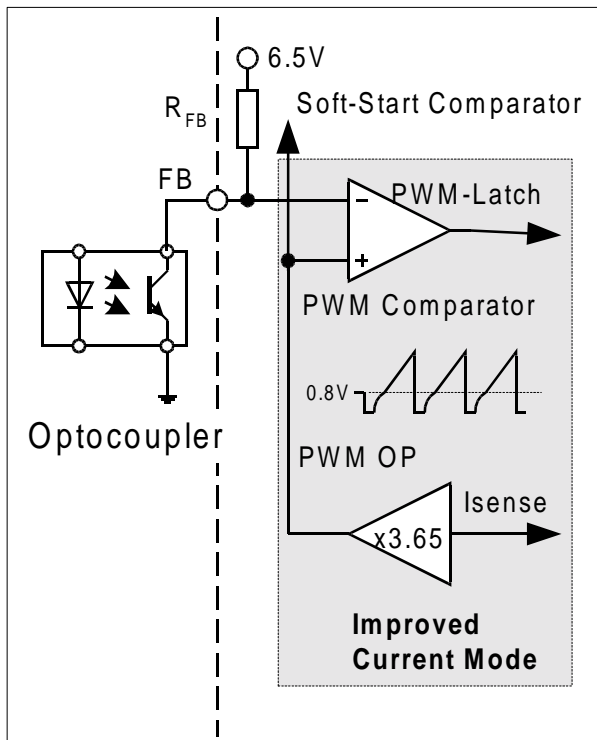


Figure 8 PWM Controlling

### 3.3 Soft-Start

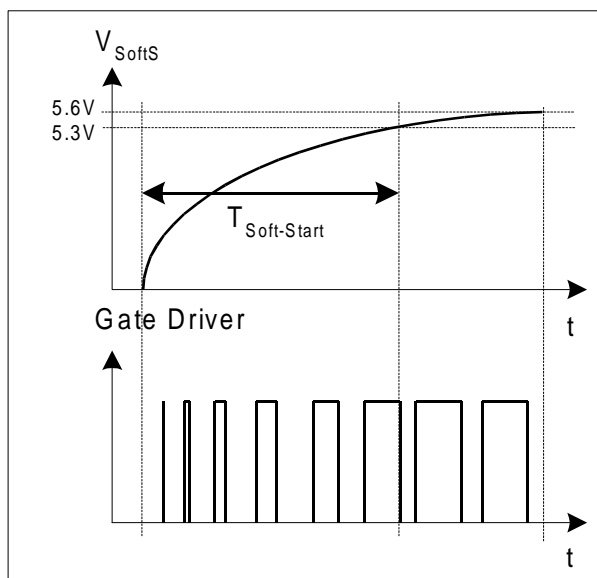


Figure 9 Soft-Start Phase

The Soft-Start is realized by the internal pullup resistor  $R_{Soft-Start}$  and the external Capacitor  $C_{Soft-Start}$  (see Figure 2). The Soft-Start voltage  $V_{SoftS}$  is generated by charging the external capacitor  $C_{Soft-Start}$  by the internal

pullup resistor  $R_{Soft-Start}$ . The Soft-Start-Comparator compares the voltage at pin SoftS at the negative input with the ramp signal of the PWM-OP at the positive input. When Soft-Start voltage  $V_{SoftS}$  is less than Feedback voltage  $V_{FB}$  the Soft-Start-Comparator limits the pulse width by resetting the PWM-Latch (see Figure 9). In addition to Start-Up, Soft-Start is also activated at each restart attempt during Auto Restart. By means of the above mentioned  $C_{Soft-Start}$  the Soft-Start can be defined by the user. The Soft-Start is finished when  $V_{SoftS}$  exceeds 5.3V. At that time the Protection Unit is activated by Comparator C4 and senses the FB by Comparator C3 whether the voltage is below 4.8V which means that the voltage on the secondary side of the SMPS is settled. The internal Zener Diode at SoftS with breakthrough voltage of 5.6V is to prevent the internal circuit from saturation (see Figure 10).

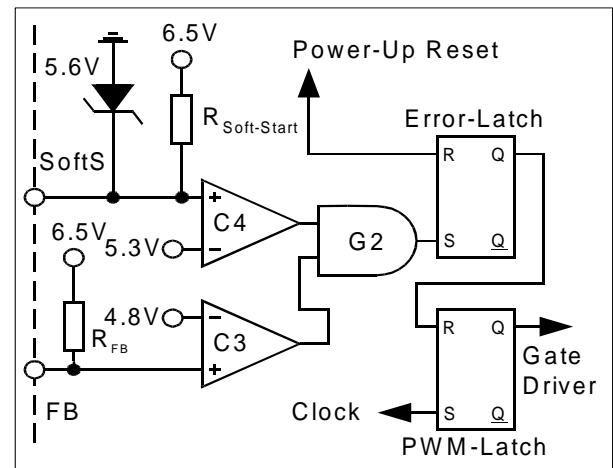


Figure 10 Activation of Protection Unit

The Start-Up time  $T_{Start-Up}$  within the converter output voltage  $V_{OUT}$  is settled must be shorter than the Soft-Start Phase  $T_{Soft-Start}$  (see Figure 11).

$$C_{Soft-Start} = \frac{T_{Soft-Start}}{R_{Soft-Start} \times 1,69}$$

By means of Soft-Start there is an effective minimization of current and voltage stresses on the external Power Switch, the clamp circuit and the output overshoot and prevents saturation of the transformer during Start-Up.

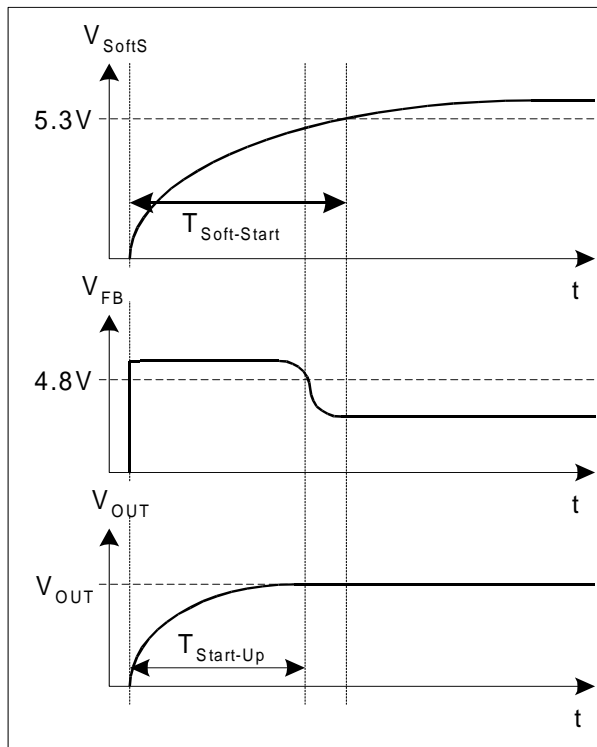


Figure 11 Start Up Phase

### 3.4 Oscillator and Frequency Reduction

#### 3.4.1 Oscillator

The oscillator generates a frequency  $f_{\text{switch}} = 100\text{kHz}$ . A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a max. duty cycle limitation of  $D_{\text{max}}=0.72$ .

#### 3.4.2 Frequency Reduction

The frequency of the oscillator is depending on the voltage at pin FB. The dependence is shown in Figure 12. This feature allows a power supply to operate at lower frequency at light loads thus lowering the switching losses while maintaining good cross regulation performance and low output ripple. In case of low power the power consumption of the whole SMPS can now be reduced very effective. The minimal reachable frequency is limited to 20kHz / 21.5 kHz to avoid audible noise in any case.

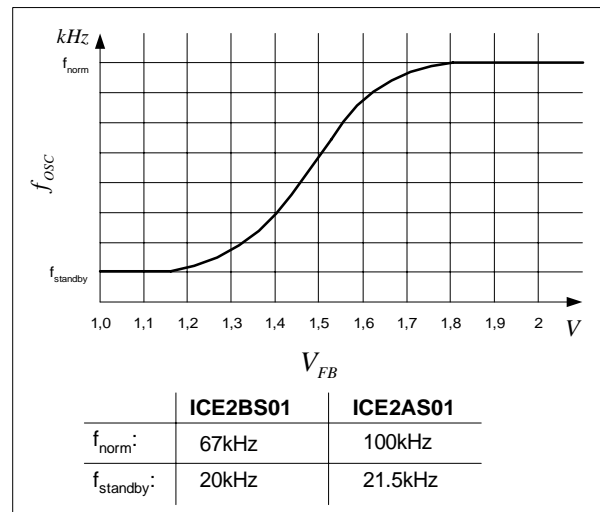


Figure 12 Frequency Dependence

### 3.5 Current Limiting

There is a cycle by cycle current limiting realised by the Current-Limit Comparator to provide an overcurrent detection. The source current of the external Power Switch is sensed via an external sense resistor  $R_{\text{Sense}}$ . By means of  $R_{\text{Sense}}$  the source current is transformed to a sense voltage  $V_{\text{Sense}}$ . When the voltage  $V_{\text{Sense}}$  exceeds the internal threshold voltage  $V_{\text{csth}}$  the Current-Limit-Comparator immediately turns off the gate drive. To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated at the Current Sense. Furthermore a Propagation Delay Compensation is added to support the immediate shut down of the Power Switch in case of overcurrent.

#### 3.5.1 Leading Edge Blanking

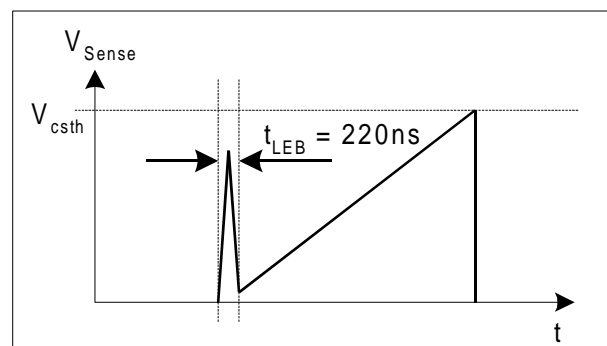


Figure 13 Leading Edge Blanking

Each time when the external Power Switch is switched on a leading spike is generated due to the primary-side capacitances and secondary-side rectifier reverse

## Functional Description

recovery time. To avoid a premature termination of the switching pulse this spike is blanked out with a time constant of  $t_{LEB} = 220\text{ns}$ . During that time the output of the Current-Limit Comparator cannot switch off the gate drive.

### 3.5.2 Propagation Delay Compensation

In case of overcurrent detection the shut down of the external Power Switch is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current  $I_{peak}$  which depends on the ratio of  $dI/dt$  of the peak current (see Figure 14).

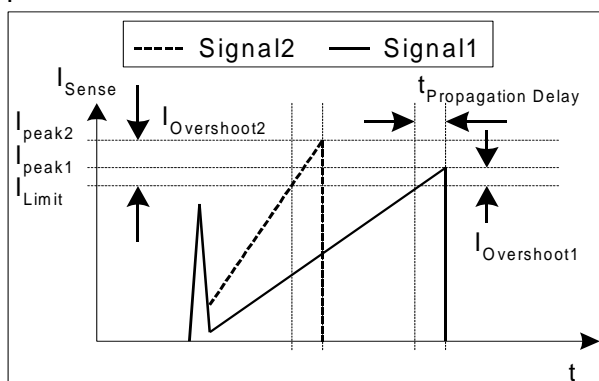


Figure 14 Current Limiting

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform.

A propagation delay compensation is integrated to bound the overshoot dependent on  $dI/dt$  of the rising primary current. That means the propagation delay time between exceeding the current sense threshold  $V_{csth}$  and the switch off of the external Power Switch is compensated over temperature within a range of at least

$$0 \leq R_{Sense} \times \frac{dI_{peak}}{dt} \leq 1 \frac{dV_{Sense}}{dt}$$

So current limiting is now capable in a very accurate way (see Figure 16).

E.g.  $I_{peak} = 0.5\text{A}$  with  $R_{Sense} = 2$ . Without propagation delay compensation the current sense threshold is set to a static voltage level  $V_{csth} = 1\text{V}$ . A current ramp of  $dI/dt = 0.4\text{A}/\mu\text{s}$ , that means  $dV_{Sense}/dt = 0.8\text{V}/\mu\text{s}$ , and a propagation delay time of i.e.  $t_{Propagation Delay} = 180\text{ns}$  leads then to an  $I_{peak}$  overshoot of 12%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 15).

The propagation delay compensation is done by means of a dynamic threshold voltage  $V_{csth}$  (see Figure 15). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

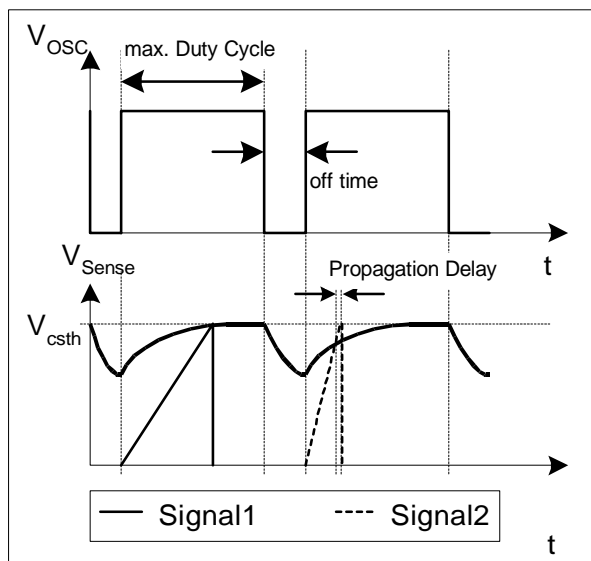


Figure 15 Dynamic Voltage Threshold  $V_{csth}$

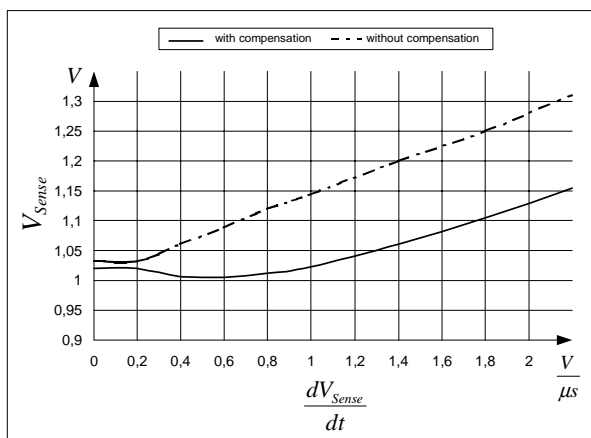


Figure 16 Overcurrent Shutdown

### 3.6 PWM-Latch

The oscillator clock output applies a set pulse to the PWM-Latch when initiating the external Power Switch conduction. After setting the PWM-Latch can be reset by the PWM-OP, the Soft-Start-Comparator, the Current-Limit-Comparator, Comparator C3 or the Error-Latch of the Protection Unit. In case of resetting the driver is shut down immediately.

### 3.7 Driver

The driver is a fast totem pole gate drive, which is designed to avoid cross conduction currents and which is equipped with a Zener diode Z1 (see Figure 17) in order to improve the control of the gate attached power

## Functional Description

transistors as well as to protect them against undesirable gate overvoltages.

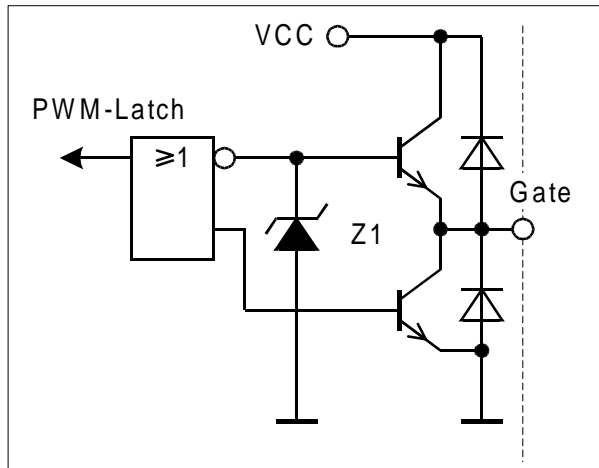


Figure 17 Gate Driver

At voltages below the undervoltage lockout threshold  $V_{VCCoff}$  the gate drive is active low.

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the external Power Switch threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 18).

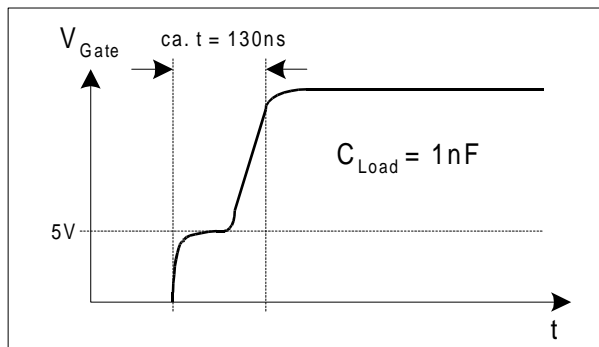


Figure 18 Gate Rising Slope

Thus the leading switch on spike is minimized. When the external Power Switch is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

### 3.8 Protection Unit (Auto Restart Mode)

An overload, open loop and overvoltage detection is integrated within the Protection Unit. These three

failure modes are latched by an Error-Latch. Additional thermal shutdown is latched by the Error-Latch. In case of those failure modes the Error-Latch is set after a blanking time of 5 $\mu$ s and the external Power Switch is shut down. That blanking prevents the Error-Latch from distortions caused by spikes during operation mode.

#### 3.8.1 Overload & Open loop with normal load

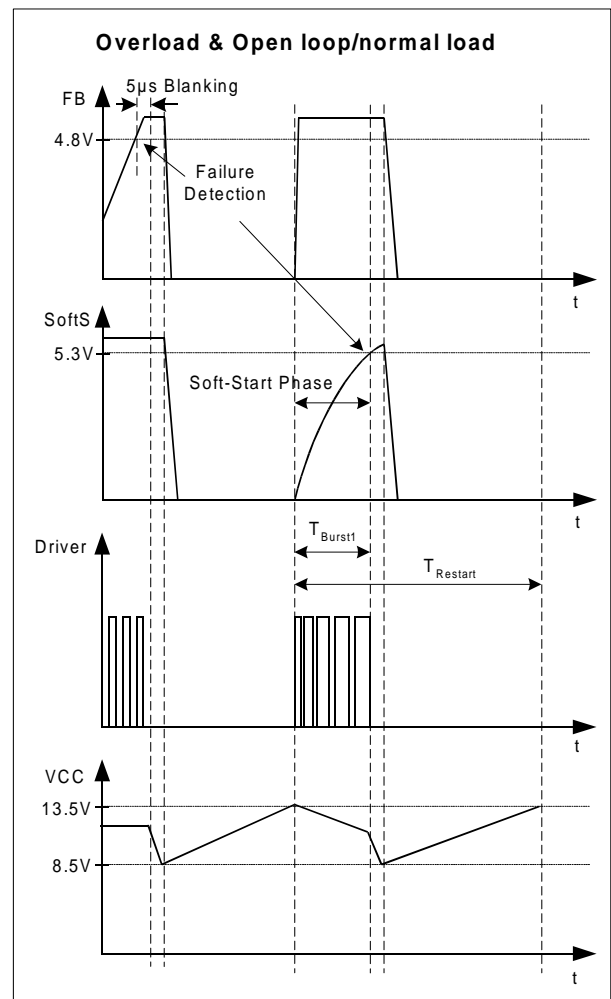


Figure 19 Auto Restart Mode

Figure 19 shows the Auto Restart Mode in case of overload or open loop with normal load. The detection of open loop or overload is provided by the Comparator C3, C4 and the AND-gate G2 (see Figure20).

## Functional Description

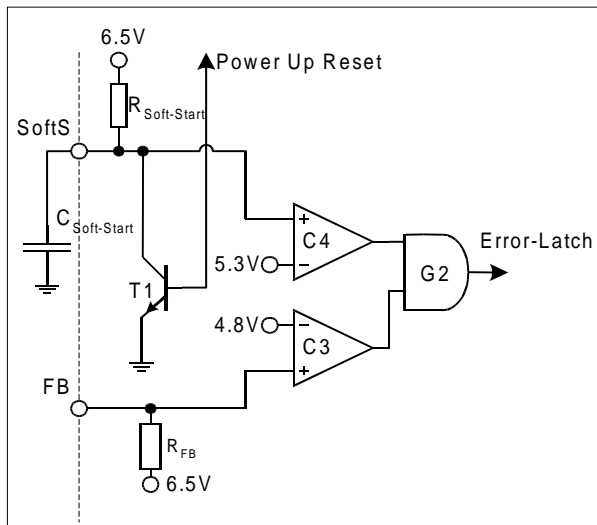


Figure 20 FB-Detection

The detection is activated by C4 when the voltage at pin SoftS exceeds 5.3V. Till this time the IC operates in the Soft-Start Phase. After this phase the comparator C3 can set the Error-Latch in case of open loop or overload which leads the feedback voltage  $V_{FB}$  to exceed the threshold of 4.8V. After latching VCC decreases till 8.5V and inactivates the IC. At this time the external Soft-Start capacitor is discharged by the internal transistor T1 due to Power Down Reset. When the IC is inactive VCC increases till  $V_{CCon} = 13.5V$  by charging the Capacitor  $C_{VCC}$  by means of the Start-Up Resistor  $R_{Start-Up}$ . Then the Error-Latch is reset by Power Up Reset and the external Soft-Start capacitor  $C_{Soft-Start}$  is charged by the internal pullup resistor  $R_{Soft-Start}$ . During the Soft-Start Phase which ends when the voltage at pin SoftS exceeds 5.3V the detection of overload and open loop by C3 and G2 is inactive. In this way the Start Up Phase is not detected as an overload. But the Soft-Start Phase must be finished within the Start Up Phase to force the voltage at pin FB below the failure detection threshold of 4.8V.

### 3.8.2 Overvoltage due to open loop with no load

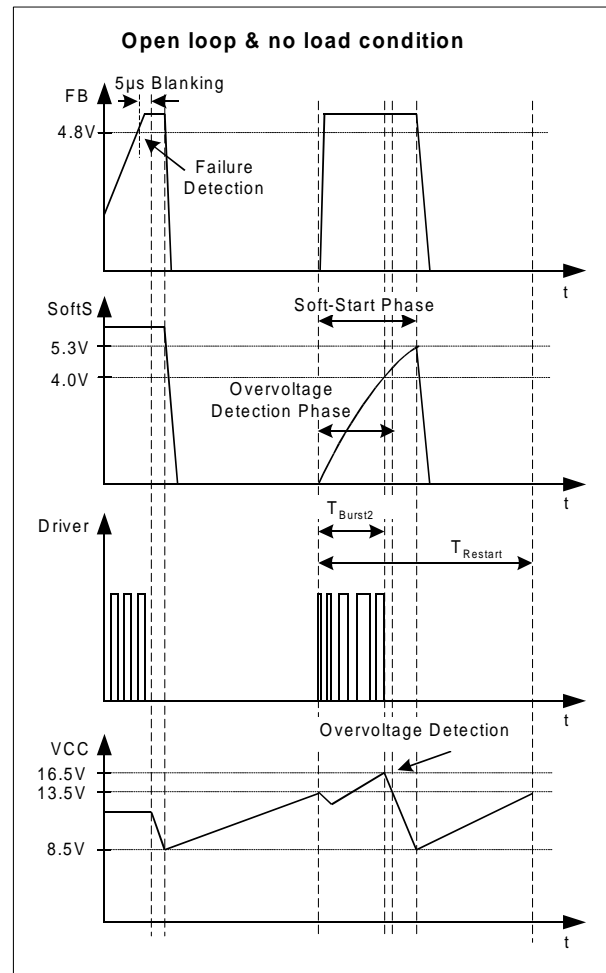


Figure 21 Auto Restart Mode

Figure 21 shows the Auto Restart Mode for open loop and no load condition. In case of this failure mode the converter output voltage increases and also VCC. An additional protection by the comparators C1, C2 and the AND-gate G1 is implemented to consider this failure mode (see Figure 22).

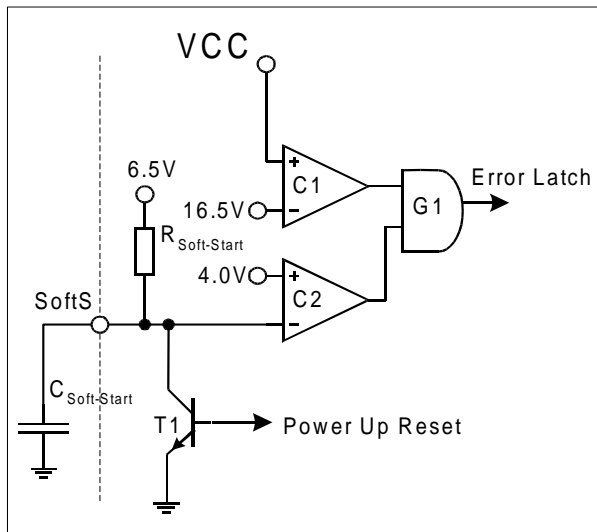


Figure 22 Overvoltage Detection

The overvoltage detection is provided by Comparator C1 only in the first time during the Auto Restart Mode till the Soft-Start voltage exceeds the threshold of the Comparator C2 at 4.0V and the voltage at pin FB is above 4.8V. When VCC exceeds 16.5V during the overvoltage detection phase C1 can set the Error-Latch and the Burst Phase during Auto Restart Mode is finished earlier. In that case  $T_{Burst2}$  is shorter than  $T_{Soft-Start}$ . By means of C2 the normal operation mode is prevented from overvoltage detection due to varying of VCC concerning the regulation of the converter output. When the voltage  $V_{SoftS}$  is above 4.0V the overvoltage detection by C1 is deactivated.

### 3.8.3 Thermal Shut Down

Thermal Shut Down is latched by the Error-Latch when junction temperature  $T_j$  of the pwm controller is exceeding an internal threshold of 140°C. In that case the IC switches in Auto Restart Mode.

*Note: All the values which are mentioned in the functional description are typical. Please refer to Electrical Characteristics for min/max limit values.*

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 6 (V<sub>CC</sub>) is discharged before assembling the application circuit.*

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	-0.3	22	V	
FB Voltage	V <sub>FB</sub>	-0.3	6.5	V	
SoftS Voltage	V <sub>SoftS</sub>	-0.3	6.5	V	
ISense	I <sub>Sense</sub>	-0.3	3	V	
Junction Temperature	T <sub>j</sub>	-40	150	°C	Controller & CoolMOS
Storage Temperature	T <sub>S</sub>	-50	150	°C	
Thermal Resistance Junction-Ambient	R <sub>thJA</sub>	-	90	K/W	P-DIP-8-4
Thermal Resistance Junction-Ambient	R <sub>thJA</sub>	-	185	K/W	P-DSO-8-3
ESD Capability <sup>1)</sup>	V <sub>ESD</sub>	-	2	kV	Human Body Model

<sup>1)</sup> Equivalent to discharging a 100pF capacitor through a 1.5 kΩ series resistor

### 4.2 Operating Range

*Note: Within the operating range the IC operates as described in the functional description.*

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	V <sub>CCoff</sub>	21	V	
Junction Temperature of Controller	T <sub>JCon</sub>	-25	130	°C	limited due to thermal shut down of controller

**Electrical Characteristics**
**4.3 Characteristics**

*Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range  $T_J$  from  $-25^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Typical values represent the median values, which are related to  $25^{\circ}\text{C}$ . If not otherwise stated, a supply voltage of  $V_{CC} = 15\text{ V}$  is assumed.*

**4.3.1 Supply Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCC1}$	-	27	55	$\mu\text{A}$	$V_{CC}=V_{CCon} -0.1\text{V}$
Supply Current with Inactiv Gate	$I_{VCC2}$	-	5.3	7	mA	$V_{SoftS} = 0$ $I_{FB} = 0$
Supply Current with Activ Gate ICE2AS01/G	$I_{VCC3}$	-	6.5	8	mA	$V_{SoftS} = 5\text{V}$ $I_{FB} = 0$ $C_{Gate} = 1\text{nF}$
Supply Current with Activ Gate ICE2BS01/G	$I_{VCC3}$	-	6	7.5	mA	$V_{SoftS} = 5\text{V}$ $I_{FB} = 0$ $C_{Gate} = 1\text{nF}$
VCC Turn-On Threshold	$V_{CCon}$	13	13.5	14	V	
VCC Turn-Off Threshold	$V_{CCoff}$	-	8.5	-	V	
VCC Turn-On/Off Hysteresis	$V_{CHY}$	4.5	5	5.5	V	

**4.3.2 Internal Voltage Reference**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	$V_{REF}$	6.37	6.50	6.63	V	measured at pin FB

**4.3.3 Control Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator Frequency ICE2AS01/G	$f_{OSC1}$	93	100	107	kHz	$V_{FB} = 4\text{V}$
Oscillator Frequency ICE2BS01/G	$f_{OSC3}$	62	67	72	kHz	$V_{FB} = 4\text{V}$
Reduced Osc. Frequency ICE2AS01/G	$f_{OSC2}$	-	21.5	-	kHz	$V_{FB} = 1\text{V}$
Reduced Osc. Frequency ICE2AS01/G	$f_{OSC4}$	-	20	-	kHz	$V_{FB} = 1\text{V}$



**Electrical Characteristics**

Frequency Ratio $f_{osc1}/f_{osc2}$ ICE2AS01/G		4.5	4.65	4.9		
Frequency Ratio $f_{osc3}/f_{osc4}$ ICE2BS01/G		3.18	3.35	3.53		
Max Duty Cycle	$D_{max}$	0.67	0.72	0.77		
Min Duty Cycle	$D_{min}$	0	-	-		$V_{FB} < 0V$
PWM-OP Gain	$A_V$	3.45	3.65	3.85		
Max. Level of Voltage Ramp	$V_{Max-Ramp}$	-	0.85	-	V	
$V_{FB}$ Operating Range Min Level	$V_{FBmin}$	0.3	-	-	V	
$V_{FB}$ Operating Range Max level	$V_{FBmax}$	-	-	4.6	V	
Feedback Resistance	$R_{FB}$	3.0	3.7	4.9	k $\Omega$	
Soft-Start Resistance	$R_{Soft-Start}$	42	50	62	k $\Omega$	

**4.3.4 Protection Unit**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Over Load & Open Loop Detection Limit	$V_{FB2}$	4.65	4.8	4.95	V	$V_{SoftS} > 5.5V$
Activation Limit of Overload & Open Loop Detection	$V_{SoftS1}$	5.15	5.3	5.46	V	$V_{FB} > 5V$
Deactivation Limit of Overvoltage Detection	$V_{SoftS2}$	3.88	4.0	4.12	V	$V_{FB} > 5V$ $V_{CC} > 17.5V$
Overvoltage Detection Limit	$V_{VCC1}$	16	16.5	17.2	V	$V_{SoftS} < 3.8V$ $V_{FB} > 5V$
Latched Thermal Shutdown	$T_{jSD}$	130	140	150	°C	guaranteed by design
Spike Blanking	$t_{Spike}$	-	5	-	$\mu s$	

**4.3.5 Current Limiting**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay Time) (see Figure 7)	$V_{csth}$	0.95	1.00	1.05	V	$dV_{sense}/dt = 0.6V/\mu s$
Leading Edge Blanking	$t_{LEB}$	-	220	-	ns	

**Electrical Characteristics**
**4.3.6 Driver Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	$V_{\text{GATE}}$	-	0.95	1.2	V	$V_{\text{VCC}} = 5 \text{ V}$ $I_{\text{Gate}} = 5 \text{ mA}$
		-	1.0	1.5	V	$V_{\text{VCC}} = 5 \text{ V}$ $I_{\text{Gate}} = 20 \text{ mA}$
		-	0.88	-	V	$I_{\text{Gate}} = 0 \text{ A}$
		-	1.6	2.2	V	$I_{\text{Gate}} = 50 \text{ mA}$
		-0.2	0.2	-	V	$I_{\text{Gate}} = -50 \text{ mA}$
GATE High Voltage	$V_{\text{GATE}}$	-	11.5	-	V	$V_{\text{VCC}} = 20 \text{ V}$ $C_{\text{L}} = 4.7 \text{ nF}$
		-	10	-	V	$V_{\text{VCC}} = 11 \text{ V}$ $C_{\text{L}} = 4.7 \text{ nF}$
		-	7.5	-	V	$V_{\text{VCC}} = V_{\text{VCCoff}} + 0.2 \text{ V}$ $C_{\text{L}} = 4.7 \text{ nF}$
GATE Rise Time	$t_{\text{r}}$	-	160	-	ns	$V_{\text{Gate}} = 2 \text{ V} \dots 9 \text{ V}^{1)}$ $C_{\text{L}} = 4.7 \text{ nF}$
GATE Fall Time	$t_{\text{f}}$	-	65	-	ns	$V_{\text{Gate}} = 9 \text{ V} \dots 2 \text{ V}^{1)}$ $C_{\text{L}} = 4.7 \text{ nF}$
GATE Current, Peak, Rising Edge	$I_{\text{GATE}}$	-0.5	-	-	A	$C_{\text{L}} = 4.7 \text{ nF}^{2)}$
GATE Current, Peak, Falling Edge	$I_{\text{GATE}}$	-	-	0.7	A	$C_{\text{L}} = 4.7 \text{ nF}^{2)}$

<sup>1)</sup> Transient reference value

<sup>2)</sup> Design characteristics (not meant for production testing)

## 5 Typical Performance Characteristics

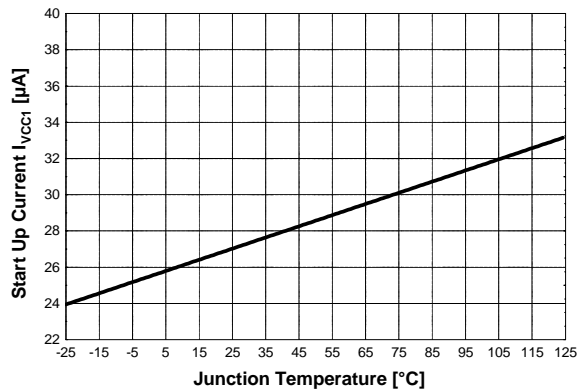


Figure 23 Start Up Current  $I_{VCC1}$  vs.  $T_j$

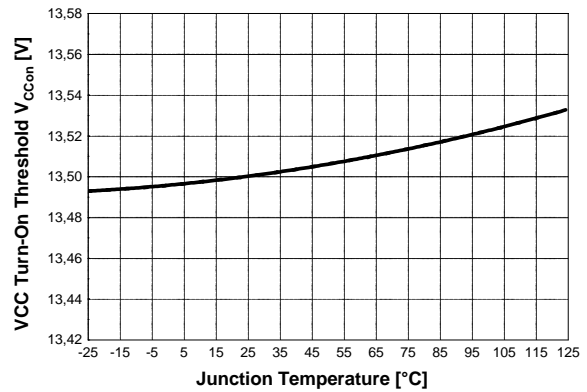


Figure 26 VCC Turn-On Threshold  $V_{VCCon}$  vs.  $T_j$

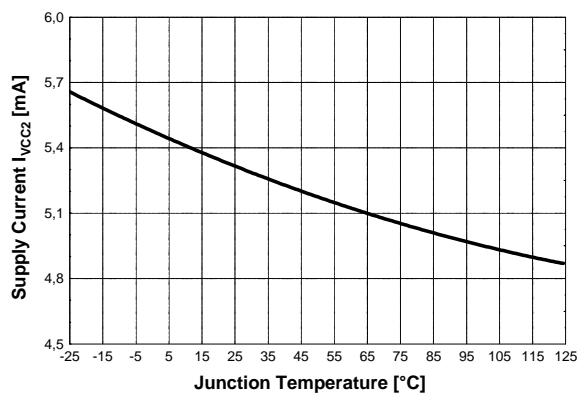


Figure 24 Supply Current  $I_{VCC2}$  vs.  $T_j$

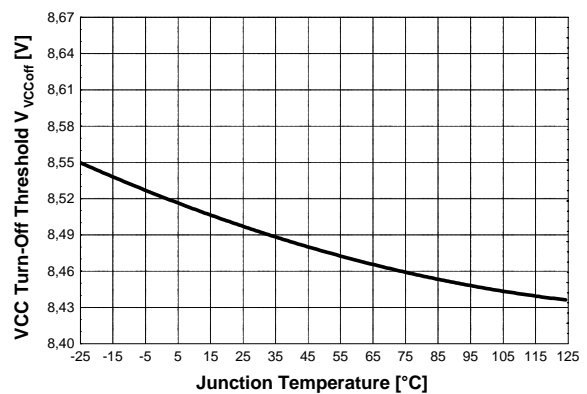


Figure 27 VCC Turn-Off Threshold  $V_{VCCoff}$  vs.  $T_j$

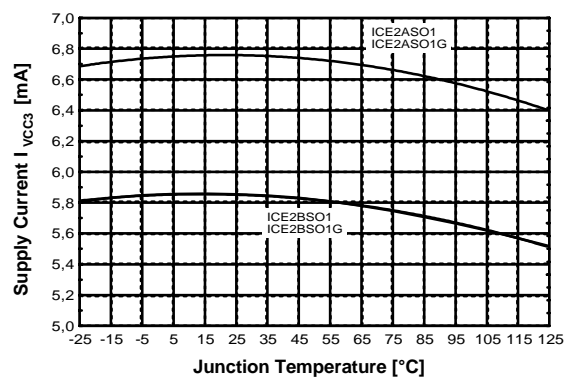


Figure 25 Supply Current  $I_{VCC3}$  vs.  $T_j$

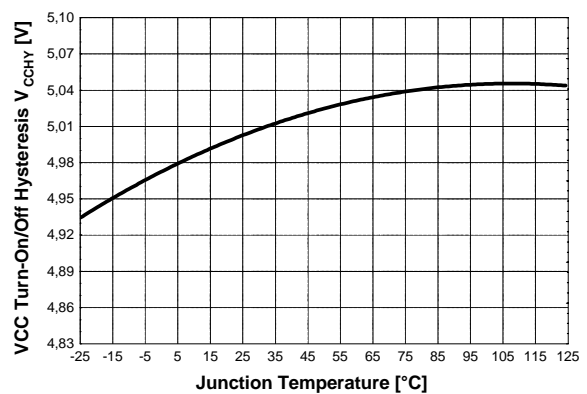


Figure 28 VCC Turn-On/Off Hysteresis  $V_{VCHY}$  vs.  $T_j$

## Typical Performance Characteristics

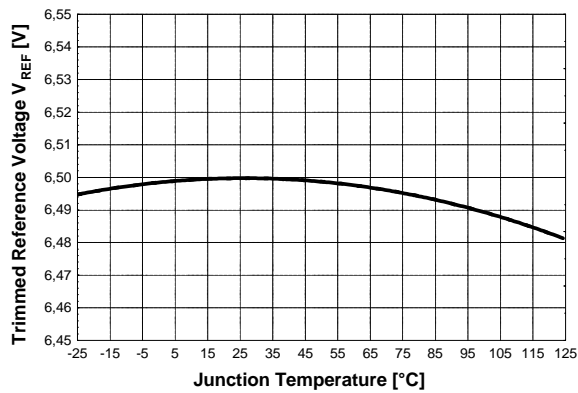


Figure 29 Trimmed Reference  $V_{REF}$  vs.  $T_j$

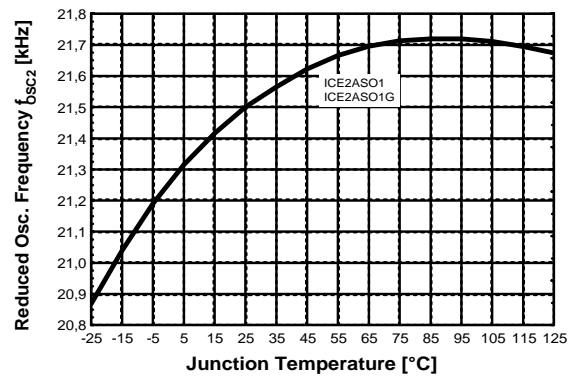


Figure 32 Reduced Osc. Frequency  $f_{OSC2}$  vs.  $T_j$

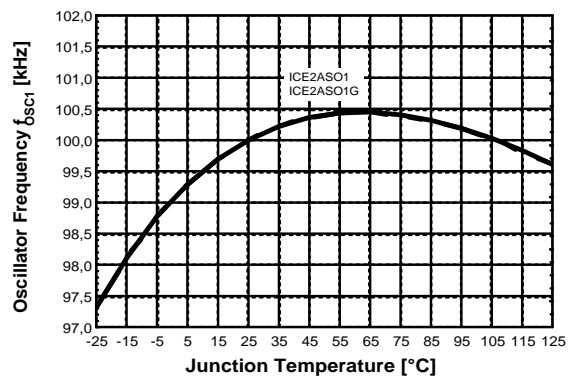


Figure 30 Oscillator Frequency  $f_{OSC1}$  vs.  $T_j$

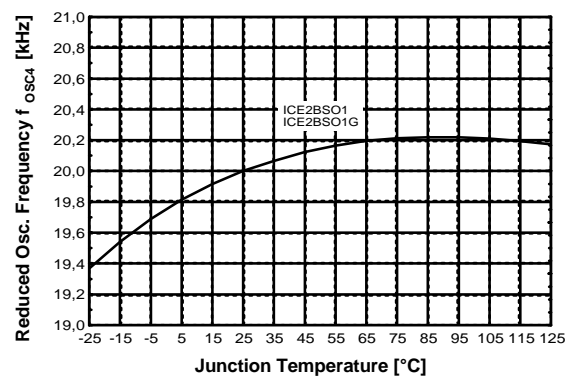


Figure 33 Reduced Osc. Frequency  $f_{OSC4}$  vs.  $T_j$

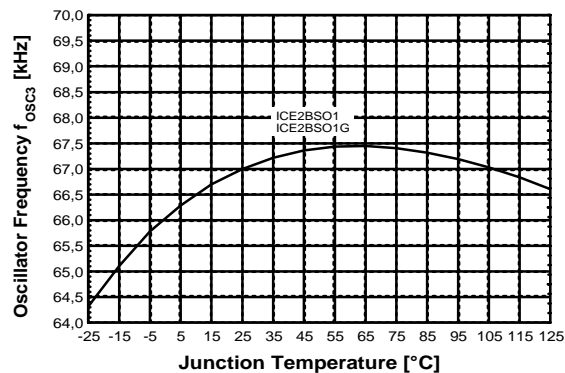


Figure 31 Oscillator Frequency  $f_{OSC3}$  vs.  $T_j$

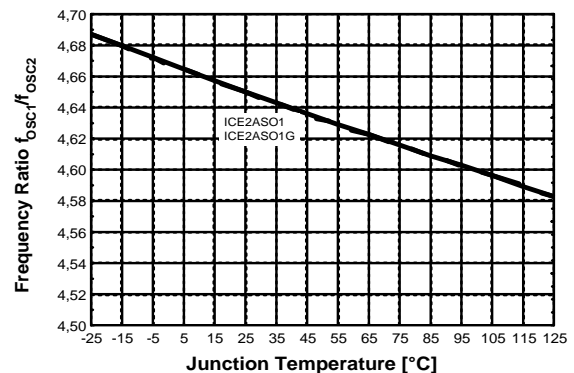


Figure 34 Frequency Ratio  $f_{OSC1} / f_{OSC2}$  vs.  $T_j$

## Typical Performance Characteristics

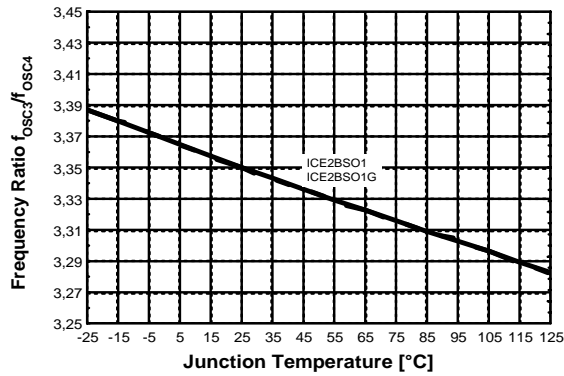


Figure 35 Frequency Ratio  $f_{OSC3} / f_{OSC4}$  vs.  $T_j$

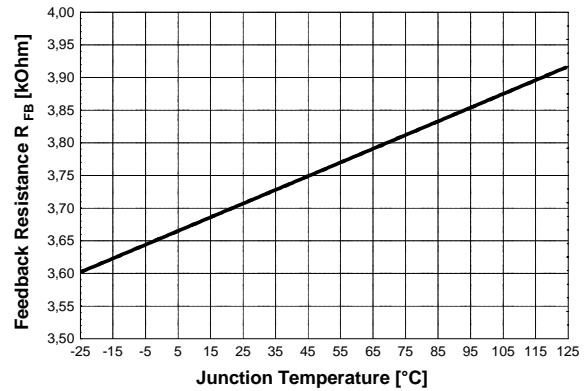


Figure 38 Feedback Resistance  $R_{FB}$  vs.  $T_j$

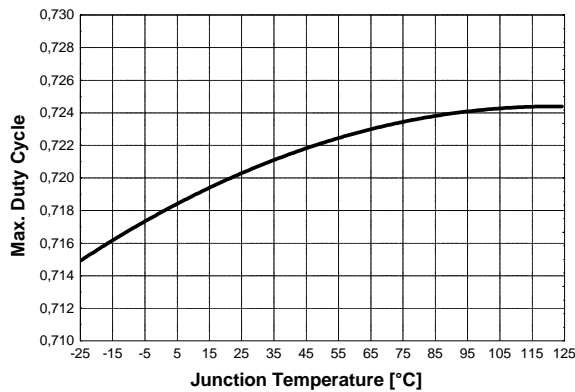


Figure 36 Max. Duty Cycle vs.  $T_j$

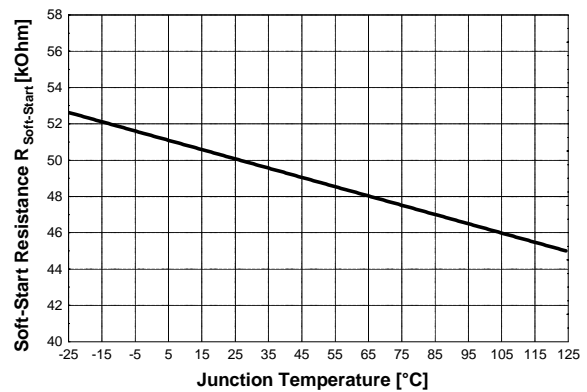


Figure 39 Soft-Start Resistance  $R_{Soft-Start}$  vs.  $T_j$

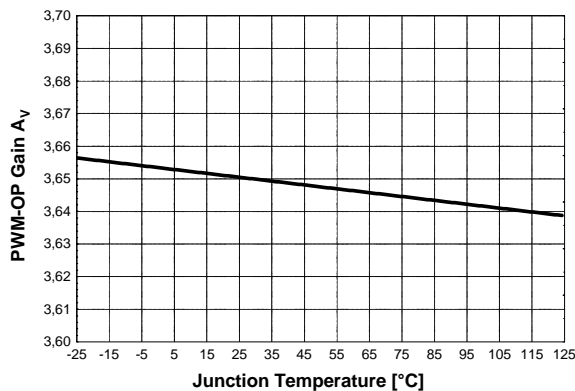


Figure 37 PWM-OP Gain  $A_V$  vs.  $T_j$

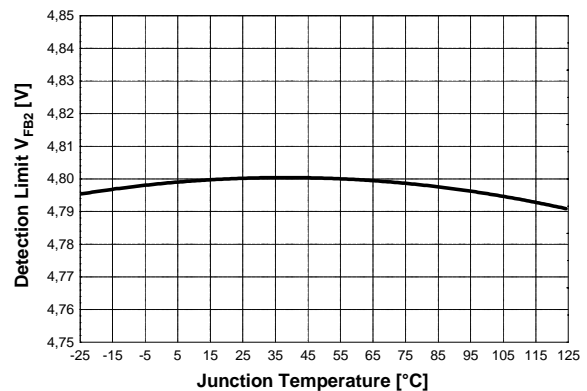


Figure 40 Detection Limit  $V_{FB2}$  vs.  $T_j$

## Typical Performance Characteristics

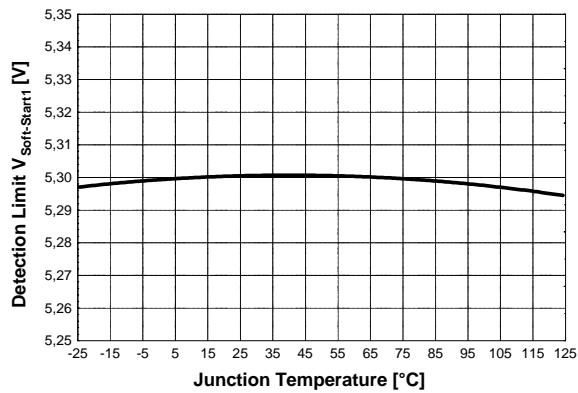


Figure 41 Detection Limit  $V_{Soft-Start1}$  vs.  $T_j$

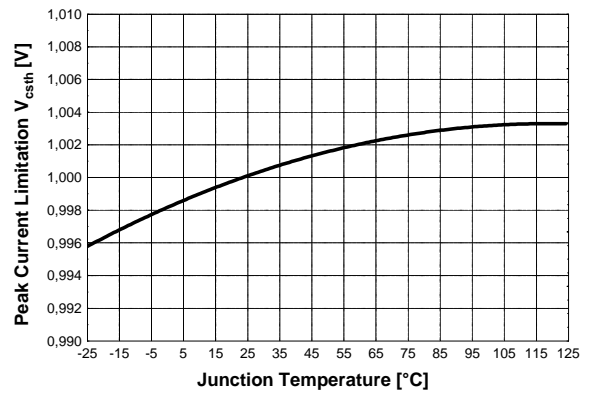


Figure 44 Peak Current Limitation  $V_{csth}$  vs.  $T_j$

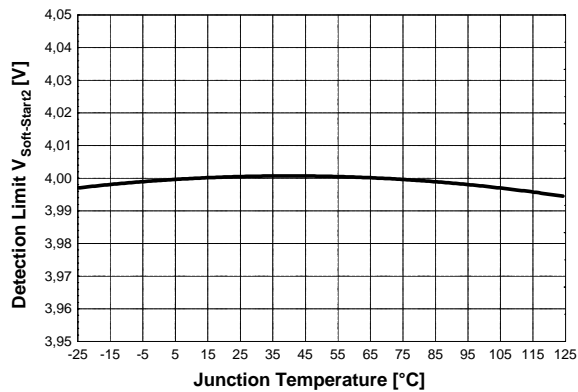


Figure 42 Detection Limit  $V_{Soft-Start2}$  vs.  $T_j$

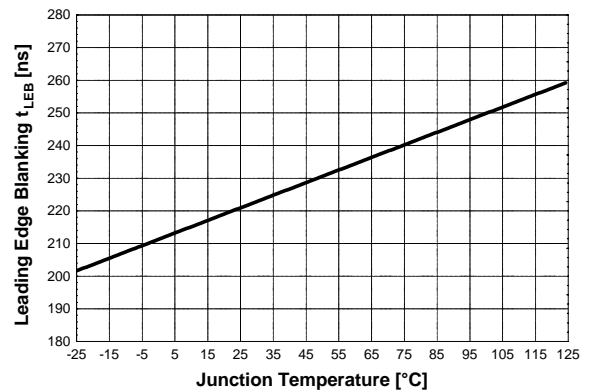


Figure 45 Leading Edge Blanking  $V_{VCC1}$  vs.  $T_j$

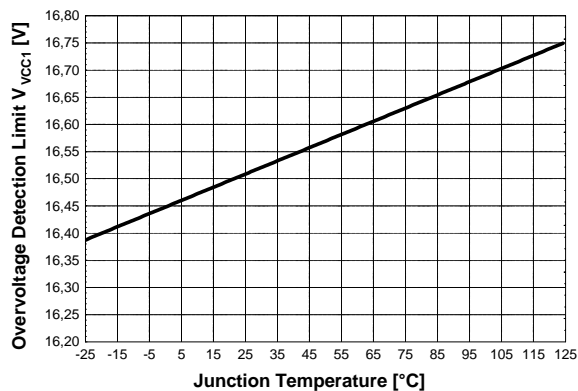
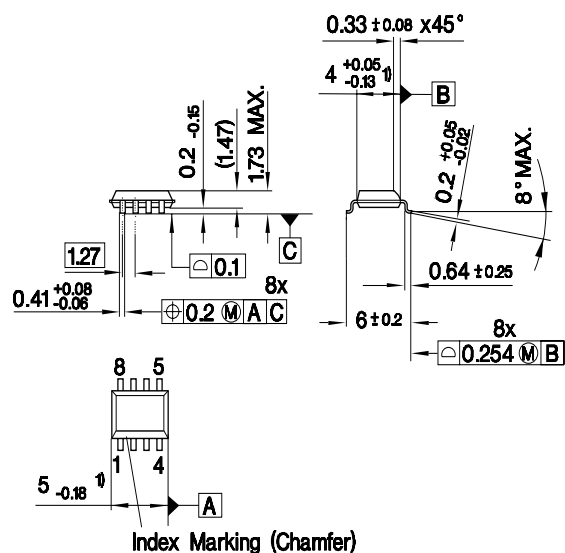


Figure 43 Overvoltage Detection Limit  $V_{VCC1}$  vs.  $T_j$

## 6 Outline Dimension

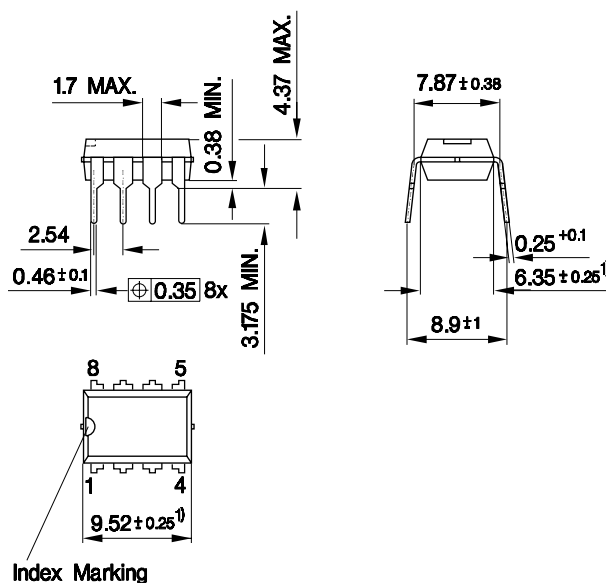
### P-DSO-8-3 (Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 46

### P-DIP-8-4 (Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 47

Dimensions in mm

# Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an all-encompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

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