7512 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0122-0101
Rev.1.01
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DESCRIPTION

The 7512 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7512 Group is designed for battery-pack and includes serial interface functions, 8-bit timer, A/D converter, current integrator and I²C-BUS interface.

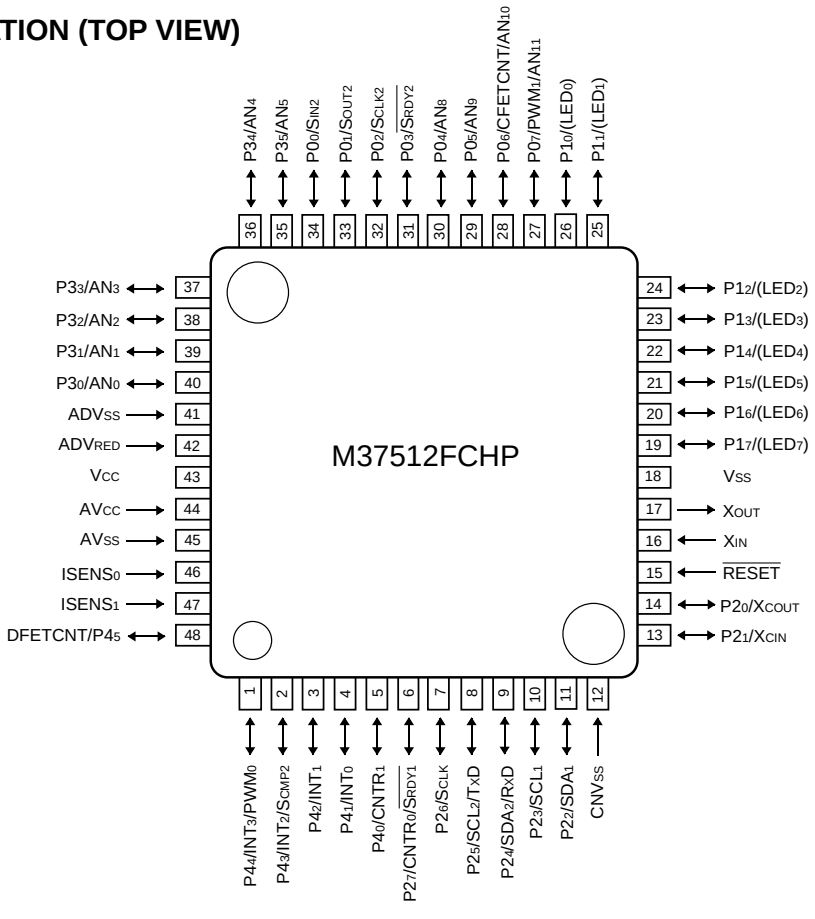
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 1.0 µs
  (at 4 MHz oscillation frequency)
- Memory size
  - Flash memory ..... 36 K to 52 Kbytes
  - RAM ..... 1.0 K to 1.5 Kbytes
- Programmable input/output ports 36
- Interrupts ..... 19 sources, 16 vectors
- Timers ..... 8-bit × 4
- Serial interface
  - Serial I/O1 ..... 8-bit × 1 (UART or Clock-synchronized)
  - Serial I/O2 ..... 8-bit × 1(Clock-synchronized)
- Multi-master I²C-BUS interface (option) ..... 1 channel
- PWM ..... 8-bit × 1
- A/D converter ..... 10-bit × 10 channels
- Current integrator ..... 1 channel
- Over current detector ..... 1 channel
- Easy thermal sensor ..... 1 channel
- Watchdog timer ..... 16-bit × 1
- Clock generating circuit ..... Built-in 4 circuits
  (high-speed RC oscillator and 32kHz RC oscillator, or connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage ..... 2.45 to 2.55 V
- Power dissipation
  - In high-speed mode ..... 3.75 mW
    (at 4 MHz oscillation frequency, at 2.5 V power source voltage)
  - In low-speed mode ..... 1.05 mW
    (at 32 kHz oscillation frequency, at 2.5 V power source voltage)
- Operating temperature range ..... –20 to 85°C

APPLICATION

Battery-Pack, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 48P6Q-A

Fig. 1 M37512FCHP pin configuration

FUNCTIONAL BLOCK

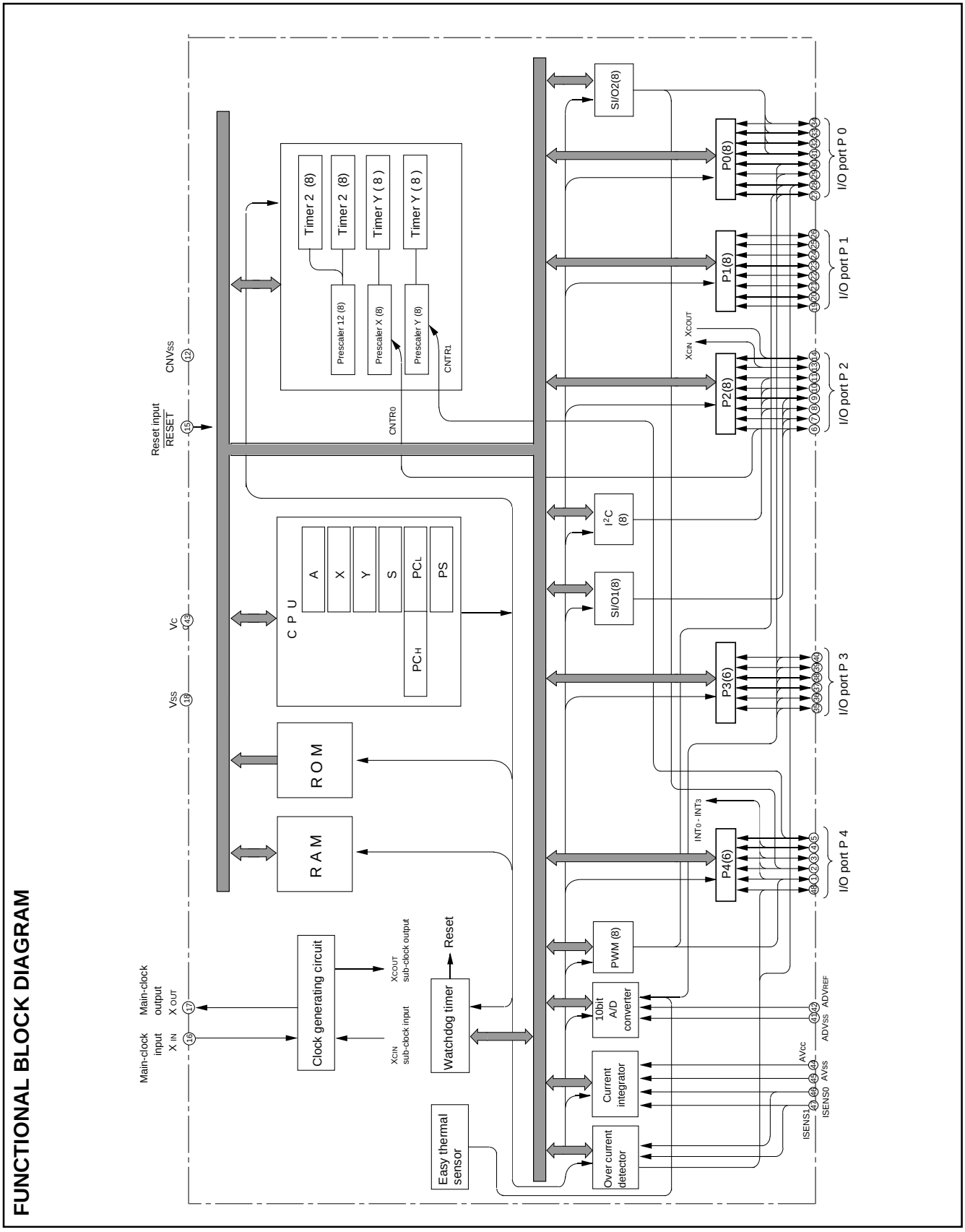


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 2.5V to Vcc, and 0 V to Vss.	
AVCC AVSS ADVSS	Analog power source	•Apply voltage of 2.5V to AVcc, and 0 V to AVss, ADVss.	
ADVREF	Analog reference voltage	•Reference voltage input pin for A/D converters.	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to VSS.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active “L”.	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When a high-speed RC oscillator is used, leave the XIN pin and XOUT pin open. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/$\overline{\text{SRDY2}}$	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •P00 to P07 are CMOS 3-state output structure, and P10 to P17 are N-channel open-drain structure. •P10 to P17 (8 bits) are enabled to output large current for LED drive.	• Serial I/O2 function pin
P04/AN8 P05/AN9			• A/D converter input pin
P06/CFETCNT/ AN10			• A/D converter input pin / Over current detector function pin
P07/AN11/ PWM1			• A/D converter input pin / PWM output pin
P10–P17	I/O port P1		
P20/XCOUT P21/XCIN	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level, but P22 to P25 can be switched between CMOS compatible input level or SMBUS input level in the I^2C-BUS interface function. •P20, P21, P26, P27: CMOS3-state output structure. •P22 to P25: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonat or registor and capacitor)
P22/SDA1 P23/SCL1			• I^2C-BUS interface function pins
P24/SDA2/RxD P25/SCL2/TxD			• I^2C-BUS interface function pins/ Serial I/O1 function pins
P26/SCLK			• Serial I/O1 function pin
P27/$\overline{\text{CNTR0}}$/ $\overline{\text{SRDY1}}$			• Serial I/O1 function pin/ Timer X function pin
P30/AN0– P35/AN5	I/O port P3	•6-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A/D converter input pin
P40/CNTR1	I/O port P4	•6-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •P40 to P42, P45 are CMOS 3-state output structure, and P43 and P44 are N-channel open-drain structure.	• Timer Y function pin
P41/INT0 P42/INT1			• Interrupt input pins
P43/INT2/SCMP2			• Interrupt input pin/SCMP2 output pin
P44/INT3/PWM0			• Interrupt input pin/PWM output pin
P45/DFETCNT			• Over current detector function pin
ISENS0 ISENS1	Analog input pin	•Current integrator and over current detector input pins. •Connect the sense resistor. Normally connect the ISENS0 to GND.	

GROUP EXPANSION

Renesas plans to expand the 7512 group as follows.

Memory Type

Support for flash memory version.

Memory Size

ROM size ..... 36 K to 52 K bytes
RAM size ..... 1024 to 1536 bytes

Packages

48P6Q-A ..... 48-pin plastic molded QFP

Memory Expansion Plan

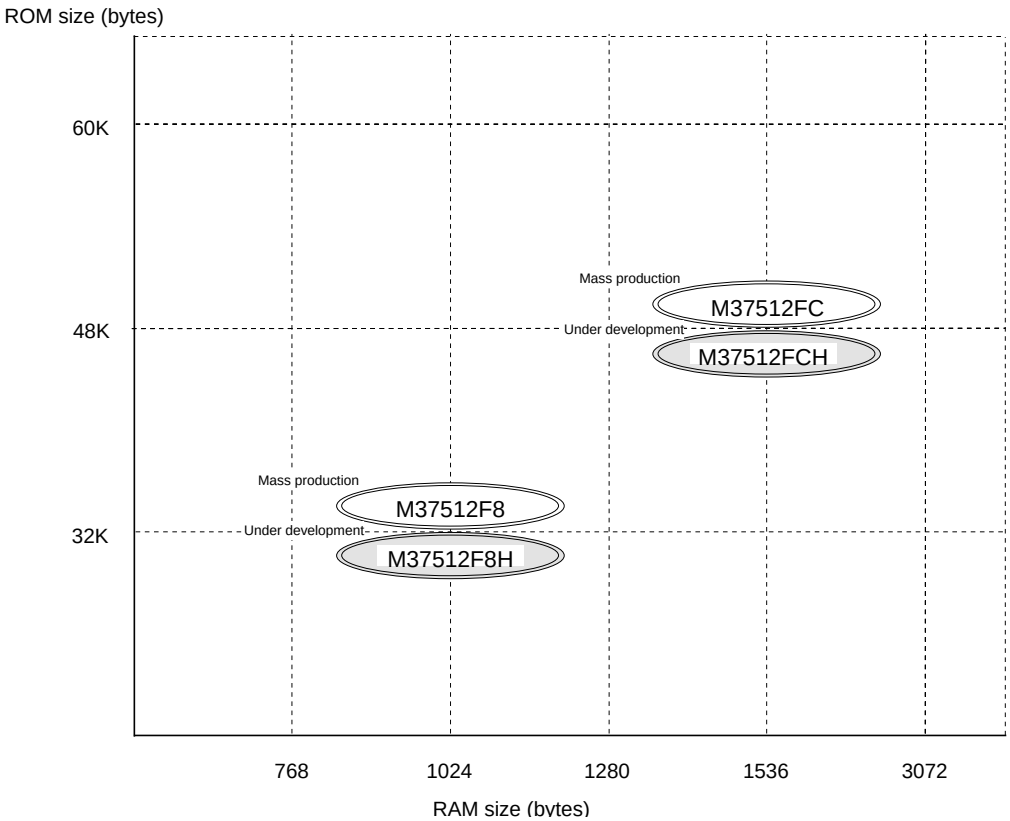


Fig. 3 Memory expansion plan

Currently planning products are listed below.

Table 2 Support products

Product name	ROM size (bytes)	RAM size (bytes)	Package	Remarks
M37512F8HP	32K + 4K	1024	48P6Q-A	
M37512F8-XXXHP				
M37512F8HHP (Note 1)				
M37512F8H-XXXHP (Note 1)				
M37512FCHP	48K + 4K	1536		
M37512FC-XXXHP				
M37512FCHHP (Note 1)				
M37512FCH-XXXHP (Note 1)				

Note 1. The products of which erase/write cycles onto the blocks A and B are maximum 10k are under development.

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 7512 Group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc. are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 5.

Store registers other than those described in Figure 4 with program when the user needs them during interrupts or subroutine calls (see Table 3).

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

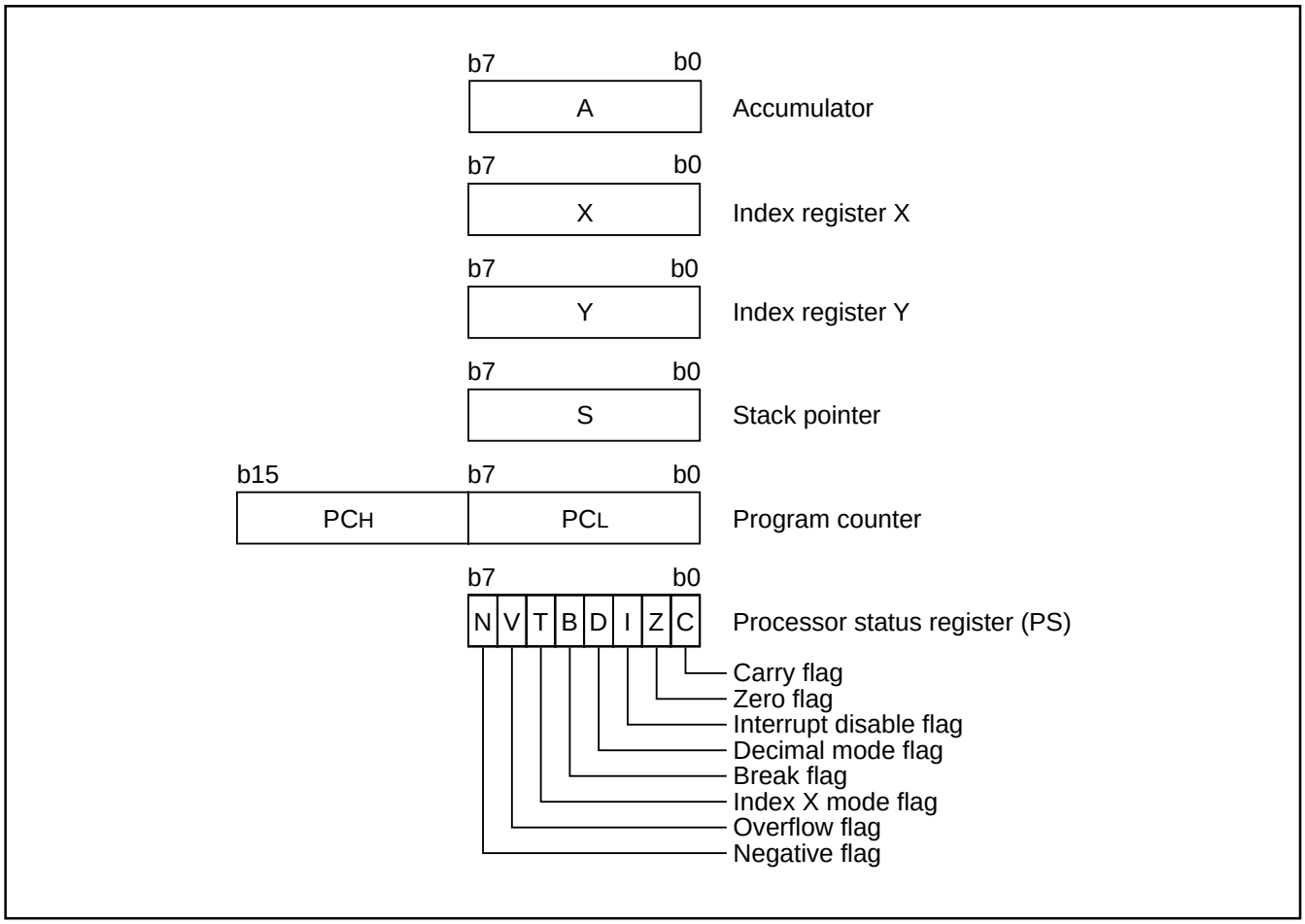


Fig.4 740 Family CPU register structure

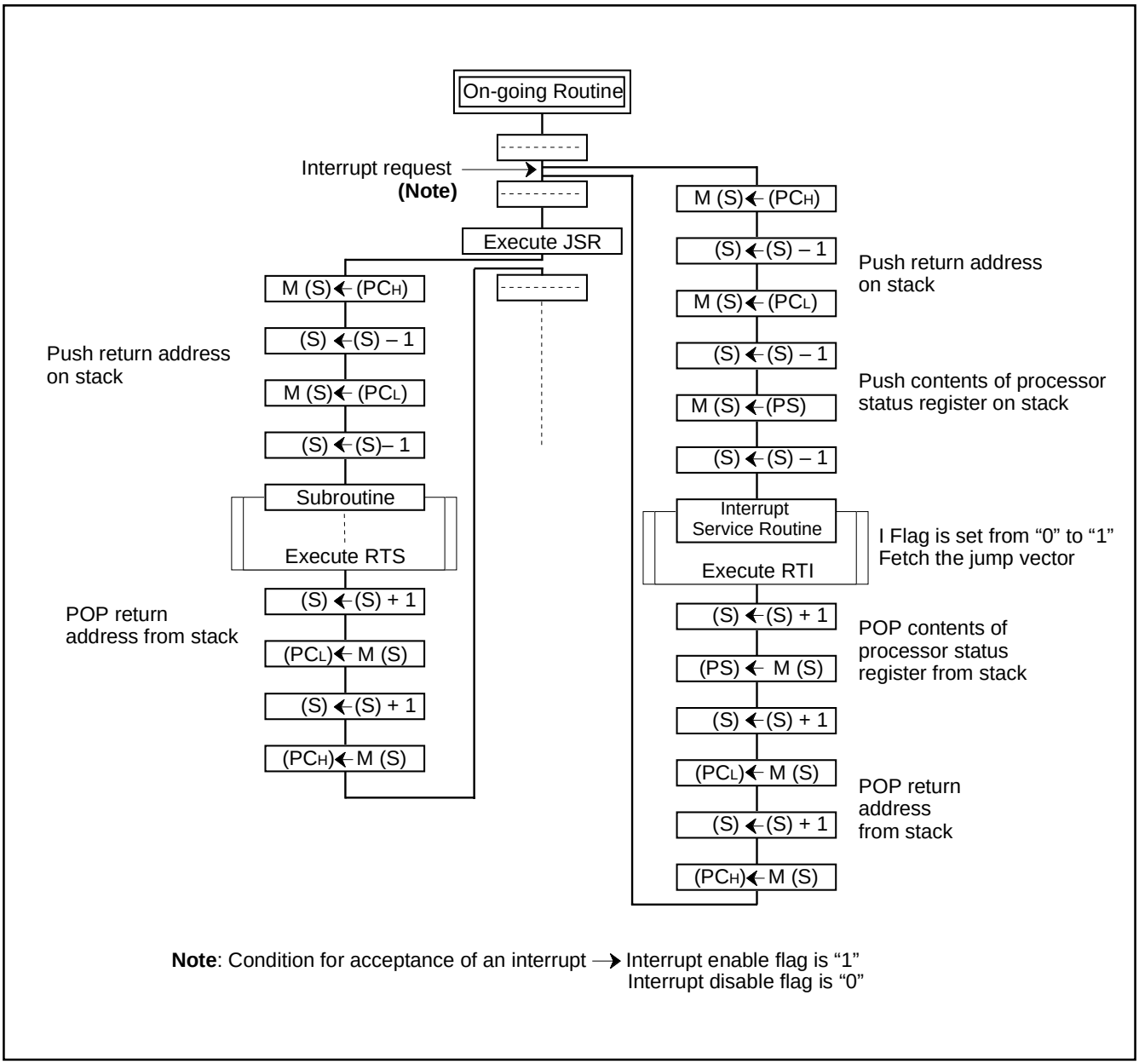


Fig. 5 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can execute decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

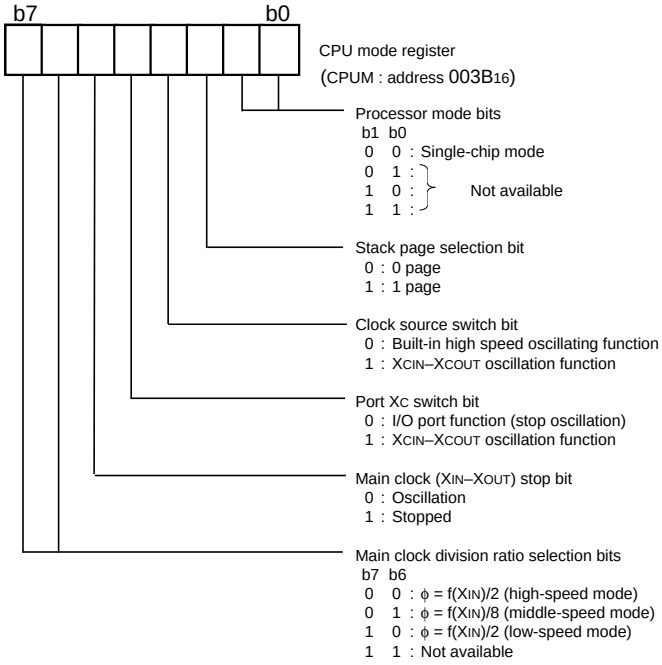
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address 003B16.



Note : All bits in this register are protected by protect mode.

Fig. 6 Structure of CPU mode register

MEMORY
Special Function Register (SFR) Area
The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

Flash Memory
The last 2 bytes of flash memory are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

Zero Page
Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page
Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM size and area

Product name	RAM size (bytes)	Address $XXXX_{16}$
M37512F8HP M37512F8-XXXHP M37512F8HHP M37512F8H-XXXHP	1024	$043F_{16}$
M37512FCHP M37512FC-XXXHP M37512FCHHP M37512FCH-XXXHP	1536	$063F_{16}$

ROM size and area (Except Data block)

Product name	ROM size (bytes)	Address $YYYY_{16}$
M37512F8HP M37512F8-XXXHP M37512F8HHP M37512F8H-XXXHP	32768	8000_{16}
M37512FCHP M37512FC-XXXHP M37512FCHHP M37512FCH-XXXHP	49152	4000_{16}

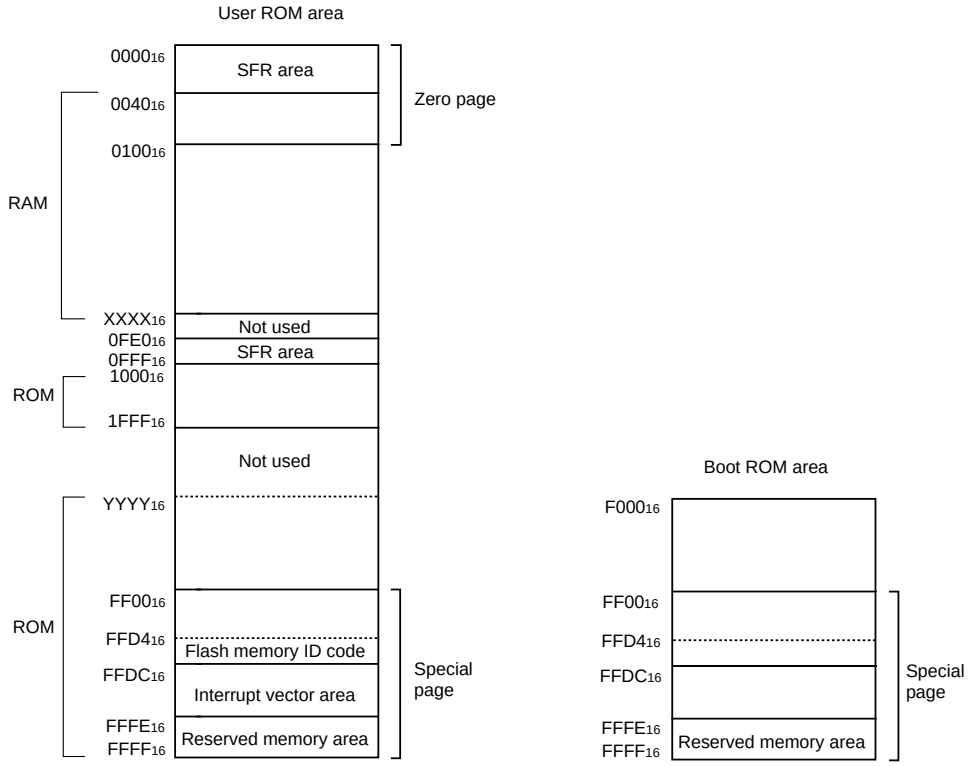


Fig. 7 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Discharge counter latch low-order register (DCHARGEL)
$000B_{16}$	Discharge counter latch high-order register (DCHARGEH)
$000C_{16}$	Charge counter latch low-order register (CHARGEL)
$000D_{16}$	Charge counter latch high-order register (CHARGEH)
$000E_{16}$	Current integrator control register (CINFCON)
$000F_{16}$	Short current detector control register (SCDCON)
0010_{16}	Over current detector control register (OCDCON)
0011_{16}	Current detect time set up register 1 (OCDTIME1)
0012_{16}	Wake up current detector control register1 (WUDCON1)
0013_{16}	Current detect status register (OCDSTS)
0014_{16}	Wake up current detector control register2 (WUDCON2)
0015_{16}	Serial I/O2 control register 1 (SIO2CON1)
0016_{16}	Serial I/O2 control register 2 (SIO2CON2)
0017_{16}	Serial I/O2 register (SIO2)
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O1 status register (SIOSTS)
$001A_{16}$	Serial I/O1 control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	PWM control register (PWMCON)
$001E_{16}$	PWM prescaler (PREPWM)
$001F_{16}$	PWM register (PWM)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Timer count source selection register (TCSS)
0029_{16}	SFR protect control register (PRREG)
$002A_{16}$	
$002B_{16}$	I^2C data shift register (S0)
$002C_{16}$	I^2C address register (S0D)
$002D_{16}$	I^2C status register (S1)
$002E_{16}$	I^2C control register (S1D)
$002F_{16}$	I^2C clock control register (S2)
0030_{16}	I^2C start/stop condition control register (S2D)
0031_{16}	I^2C additional register (S3)
0032_{16}	32kHz RC oscillation control register0 (32KOSCC0)
0033_{16}	32kHz RC oscillation control register1 (32KOSCC1)
0034_{16}	AD control register (ADCON)
0035_{16}	AD conversion low-order register (ADL)
0036_{16}	AD conversion high-order register (ADH)
0037_{16}	MISRG2
0038_{16}	MISRG
0039_{16}	Watchdog timer control register (WDTCON)
$003A_{16}$	Interrupt edge selection register 1 (INTEDGE1)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

$0FE0_{16}$	Flash memory control register 0 (FMCR0)
$0FE1_{16}$	Flash memory control register 1 (FMCR1)
$0FE2_{16}$	Flash memory control register 2 (FMCR2)
$0FE3_{16}$	Reserved *
$0FE4_{16}$	Reserved *
$0FE5_{16}$	Reserved *
$0FE6_{16}$	Reserved *
$0FE7_{16}$	Reserved *
$0FE8_{16}$	Reserved *
$0FE9_{16}$	Reserved *
$0FEA_{16}$	Reserved *
$0FEB_{16}$	Reserved *
$0FEC_{16}$	Reserved *
$0FED_{16}$	Reserved *
$0FEE_{16}$	Reserved *
$0FEF_{16}$	Reserved *

$0FF0_{16}$	Charge over current detector control register (COCDCON)
$0FF1_{16}$	Current detect time set up register 2 (OCDTIME2)
$0FF2_{16}$	High-speed RC oscillator frequency set up register (O4RCFRG)
$0FF3_{16}$	High-speed RC oscillator frequency counter (O4RCFCNT)
$0FF4_{16}$	High-speed RC oscillator control register (O4RCCOT)
$0FF5_{16}$	Interrupt edge selection register 2 (INTEDG2)

* Reserved : Do not write any data to the reserved area.

Fig. 8 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 5 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P0$_0$/SIN$_2$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1)
P0$_1$/SOUT$_2$						(2)
P0$_2$/SCLK$_2$						(3)
P0$_3$/$\overline{\text{SRDY}_2}$						(4)
P0$_4$/AN$_8$				A/D conversion input	AD control register MISRG2	(5)
P0$_5$/AN$_9$						(6)
P0$_6$/CFETCNT/AN$_{10}$				A/D conversion input Over current detector output	AD control register, MISRG2 Charge over current detect control register	(7)
P0$_7$/AN$_{11}$/PWM$_1$				A/D conversion input PWM output	AD control register, MISRG2 PWM control register	(8)
P1$_0$–P1$_7$	Port P1		CMOS compatible input level N-channel open-drain output			(9)
P2$_0$/XCOUT	Port P2		CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit	CPU mode register MISRG2	(10)
P2$_1$/XCIN						(11)
P2$_2$/SDA$_1$			CMOS compatible input level CMOS/SMBUS input level (when selecting I^{2}C-BUS interface function) N-channel open-drain output	I^{2}C-BUS interface function I/O	I^{2}C control register	(12)
P2$_3$/SCL$_1$						(13)
P2$_4$/SDA$_2$/RxD				I^{2}C-BUS interface function I/O Serial I/O1 function I/O	I^{2}C control register Serial I/O1 control register	(14)
P2$_5$/SCL$_2$/TxD						(15)
P2$_6$/SCLK			CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register	(16)
P2$_7$/CNTR$_0$/$\overline{\text{SRDY}_1}$				Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(17)
P3$_0$/AN$_0$–	Port P3			A/D conversion input	AD control register MISRG2	(6)
P3$_5$/AN$_5$						
P4$_0$/CNTR$_1$	Port P4			Timer Y function I/O	Timer XY mode register	(18)
P4$_1$/INT$_0$				External interrupt input	Interrupt edge selection register 1	(19)
P4$_2$/INT$_1$						
P4$_3$/INT$_2$/SCMP$_2$			CMOS compatible input level N-channel open-drain output	External interrupt input SCMP2 output	Interrupt edge selection register 2 Serial I/O2 control register	(20)
P4$_4$/INT$_3$/PWM$_0$				External interrupt input PWM output	Interrupt edge selection register 2 PWM control register	(21)
P4$_5$/DFETCNT			CMOS compatible input level CMOS 3-state output	Over current detector output	Short current detect control register Over current detect control register Wake up current detect control register	(22)

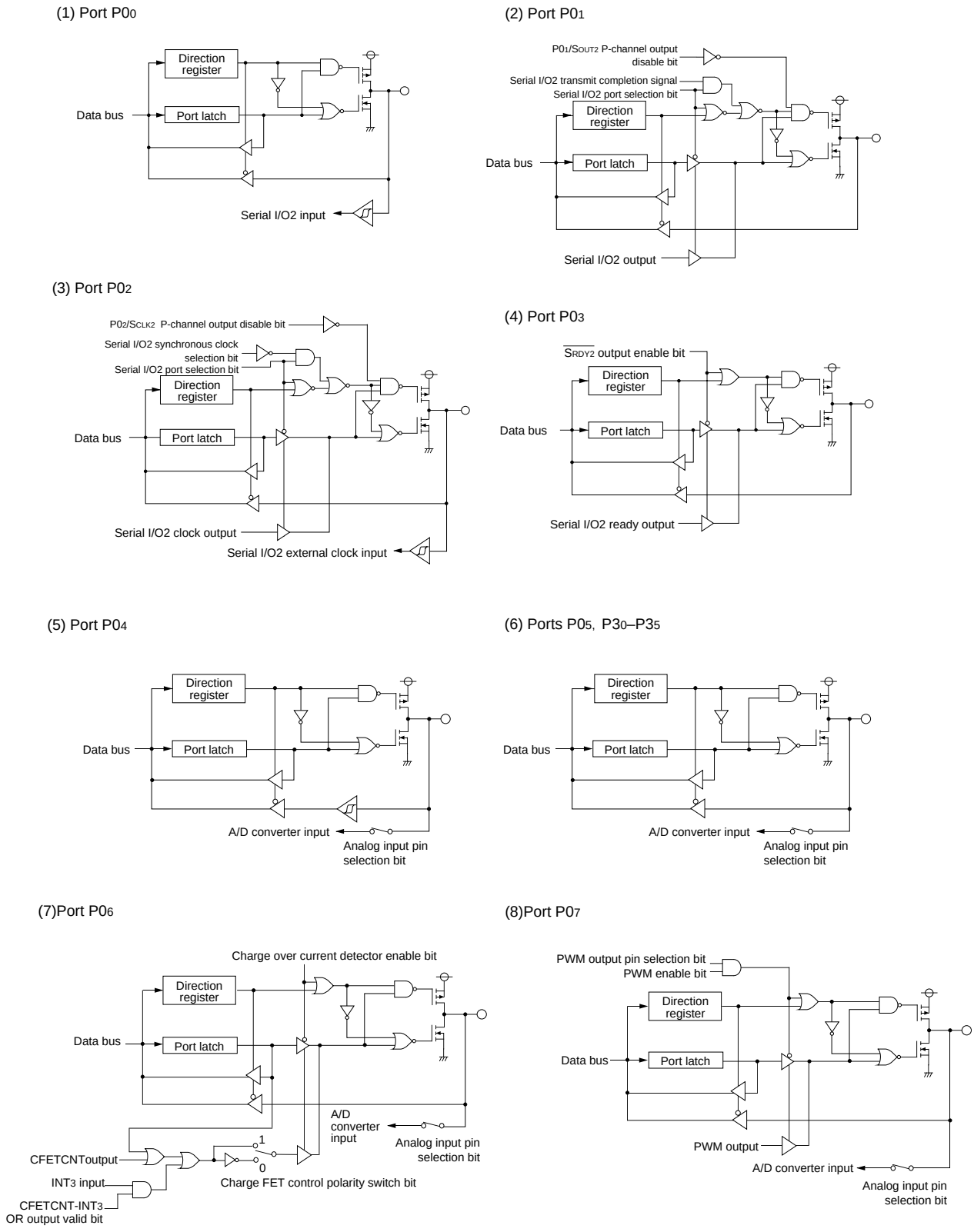
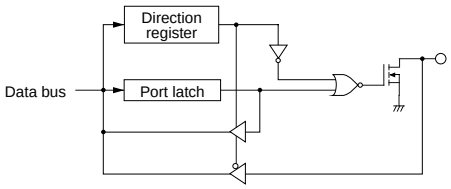
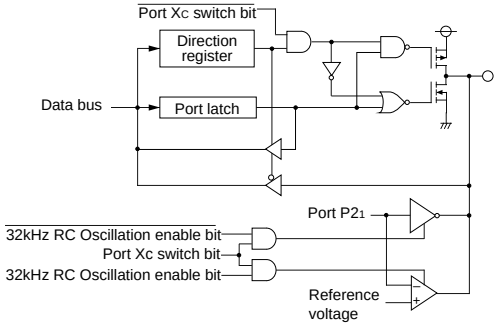


Fig. 9 Port block diagram (1)

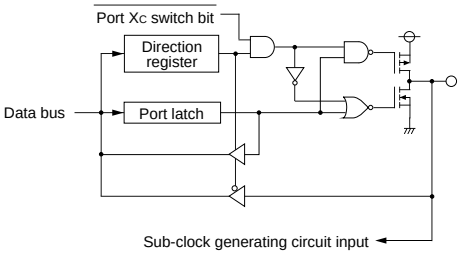
(9) Port P1



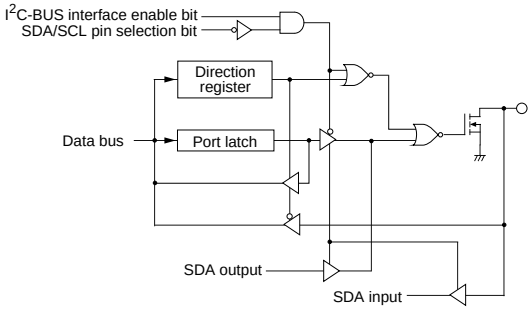
(10) Port P20



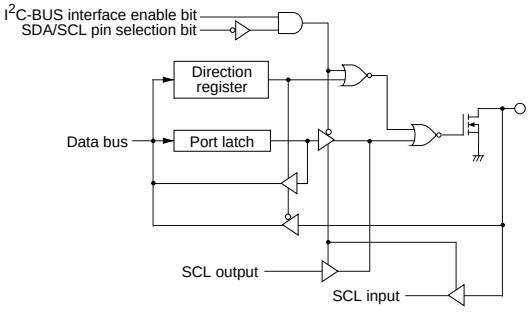
(11) Port P21



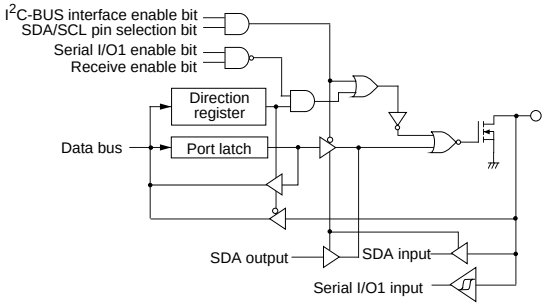
(12) Port P22



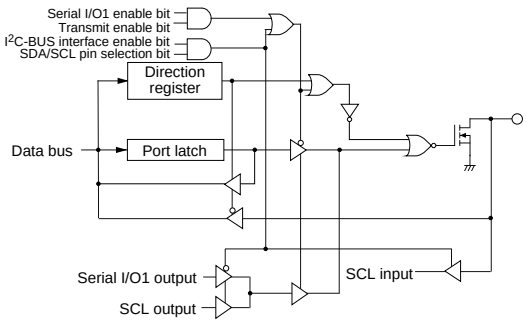
(13) Port P23



(14) Port P24



(15) Port P25



(16) Port P26

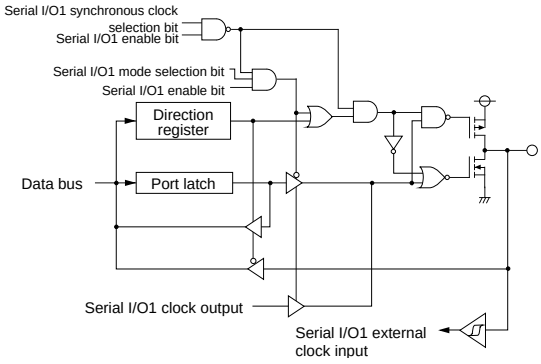


Fig. 10 Port block diagram (2)

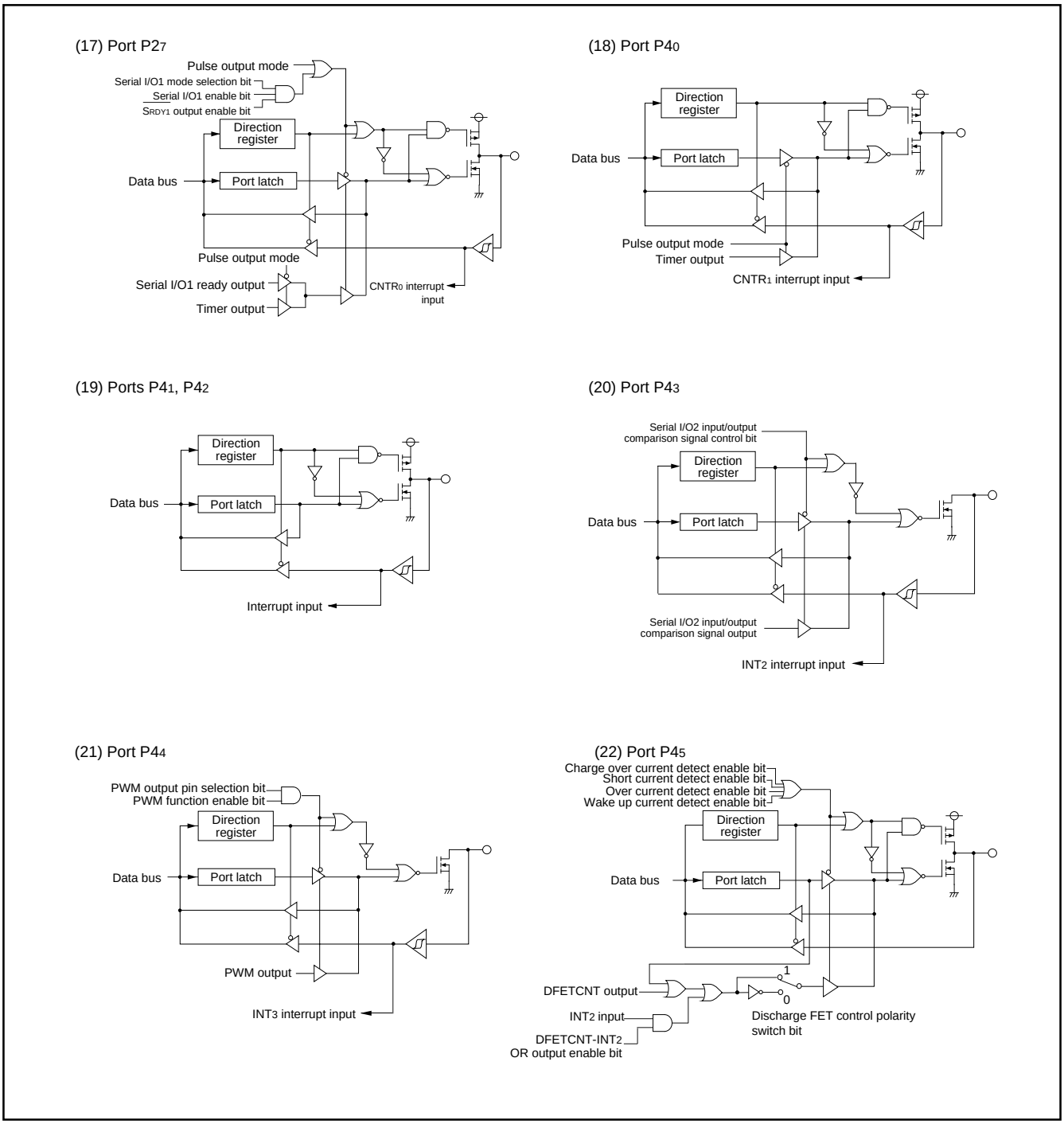


Fig. 11 Port block diagram (3)

INTERRUPTS

Interrupts occur by 16 sources among 20 sources: seven external, twelve internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and the BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the reset and the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When setting the followings, the interrupt request bit may be set to “1”.

•When switching external interrupt active edge
Related register: Interrupt edge selection register 1 (address $003A_{16}$)
I^2C START/STOP condition control register (address 0030_{16})
Timer XY mode register (address 0023_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt edge selection register 1 (address $003A_{16}$)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

(1) Set the corresponding interrupt enable bit to “0” (disabled).
(2) Set the interrupt edge select bit or the interrupt source select bit.
(3) Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to “1” (enabled).

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
SCL, SDA	3	FFF916	FFF816	At detection of either rising or falling edge of SCL or SDA input	External interrupt (active edge selectable)
INT1	4	FFF716	FFF616	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
INT2	5	FFF516	FFF416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	6	FFF316	FFF216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
Serial I/O2				At completion of serial I/O2 data reception / transmission	Valid when serial I/O2 is selected
I2C	7	FFF116	FFF016	At completion of data transfer	
Timer X	8	FFEF16	FFEE16	At timer X underflow	
Timer Y	9	FFED16	FFEC16	At timer Y underflow	
Timer 1	10	FFEB16	FFEA16	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE916	FFE816	At timer 2 underflow	
Serial I/O1 reception	12	FFE716	FFE616	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 Transmission	13	FFE516	FFE416	At completion of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Over current detection				At discharge short current is detected, at discharge over current is detected, at wake up current is detected, or at charge over current is detected.	Valid when discharge short current detector or discharge current detector, or wake up current detector, or charge over current detector is selected.
CNTR0	14	FFE316	FFE216	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	15	FFE116	FFE016	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
A/D converter	16	FFDF16	FFDE16	At completion of A/D conversion	
Current integration				At end of current integration period, or at end of calibration	Valid when current integrator is selected
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

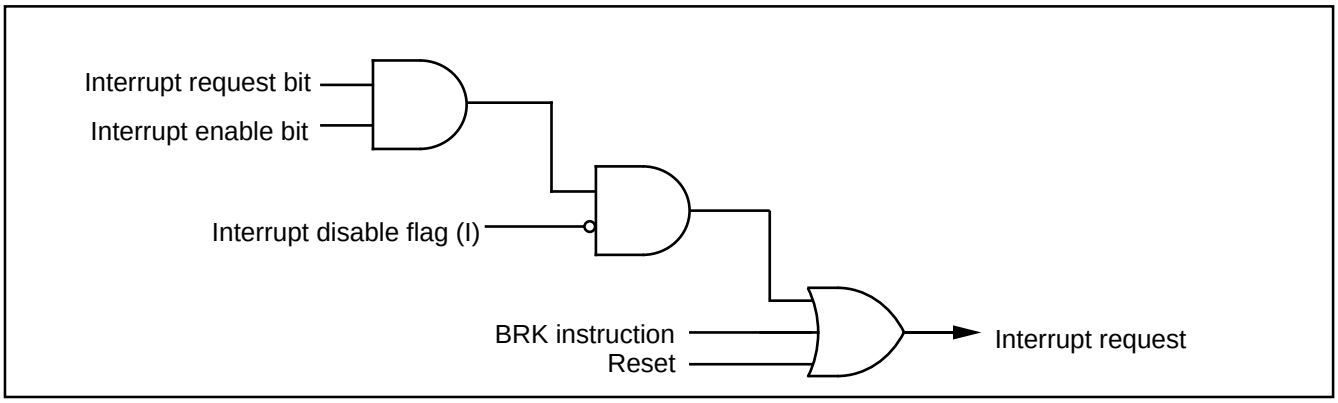


Fig. 12 Interrupt control

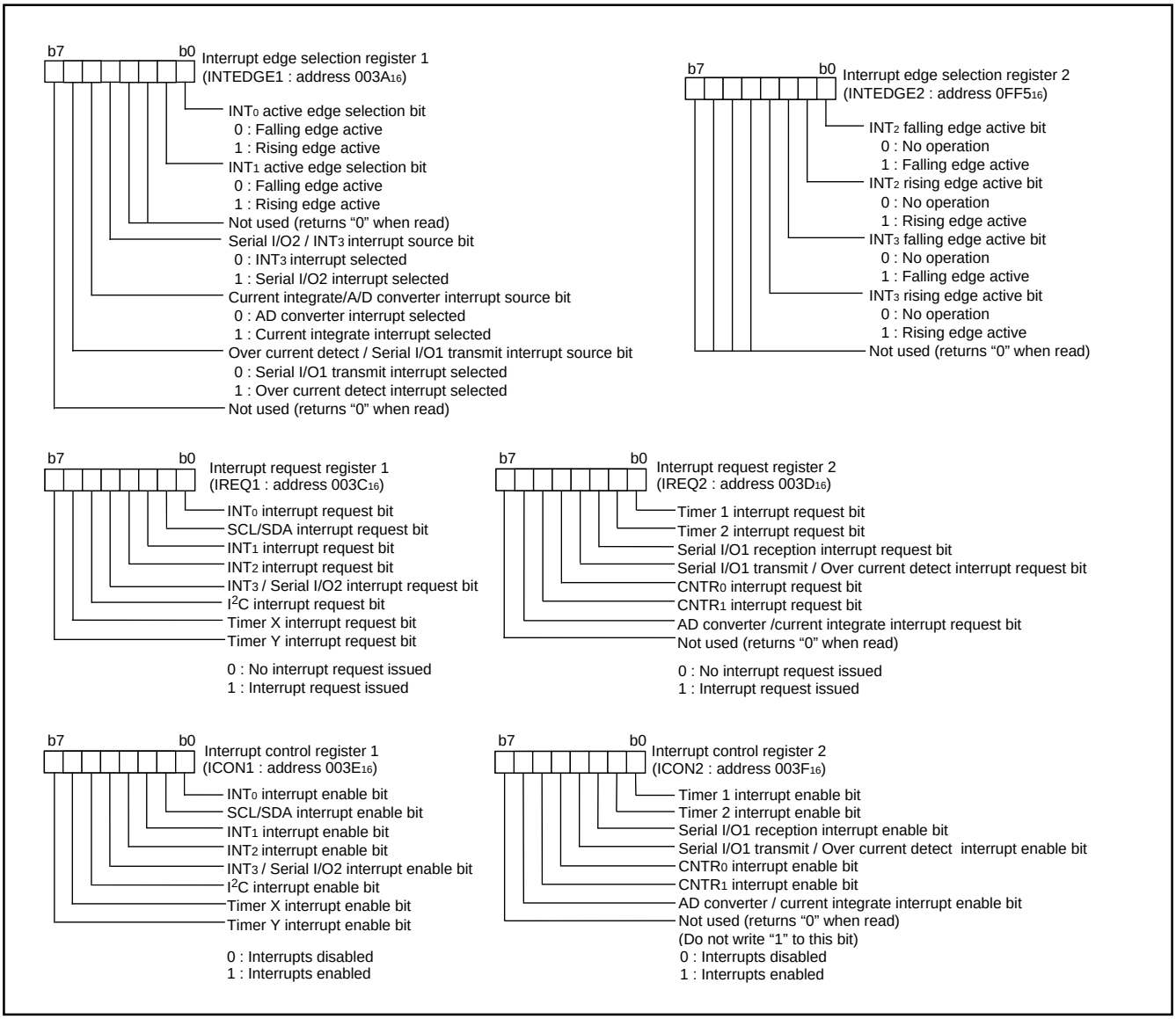


Fig. 13 Structure of interrupt-related registers

TIMERS

The 7512 Group has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

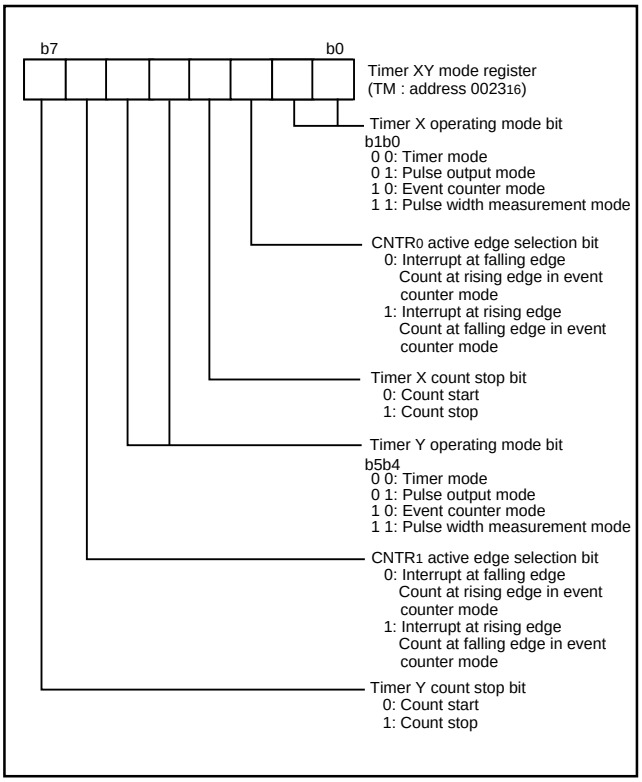


Fig. 14 Structure of timer XY mode register

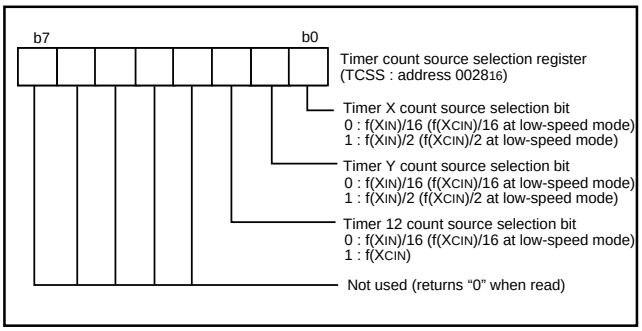


Fig. 15 Structure of timer count source selection register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency which is selected by timer 12 count source selection bit. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P2_7$ (or port $P4_0$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts it while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

■Note

When switching the count source by the timer 12, X and Y count source bit, the value of timer count is altered in inconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

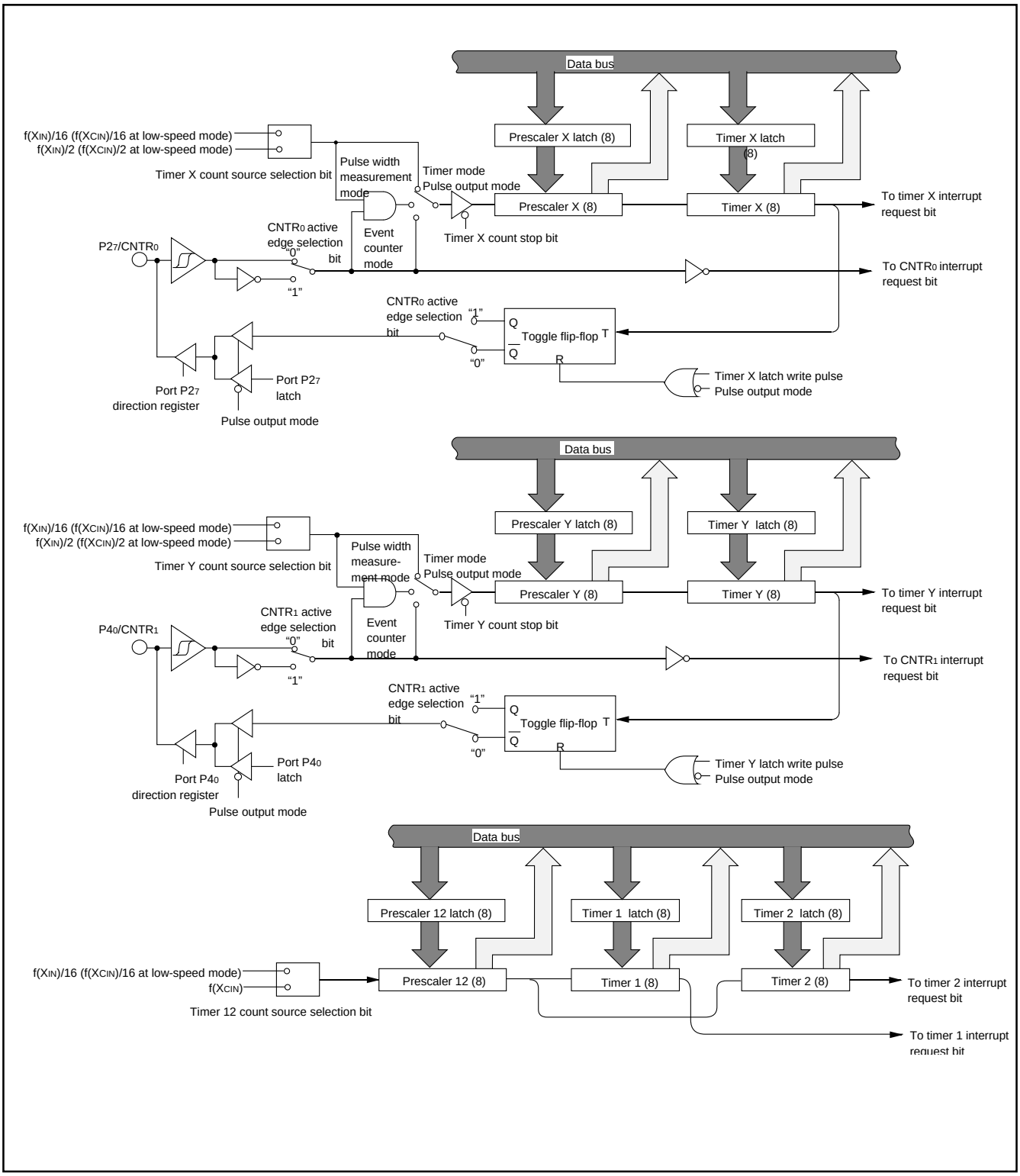


Fig. 16 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O1. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

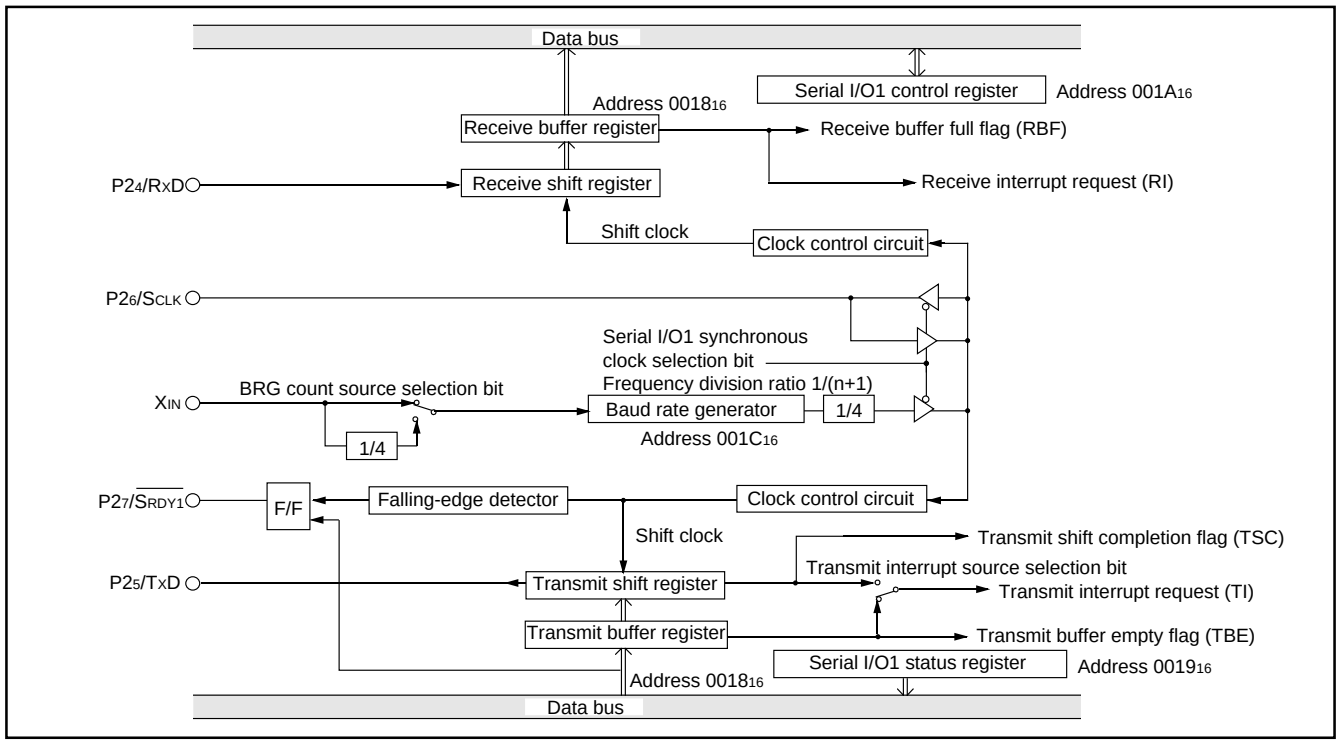
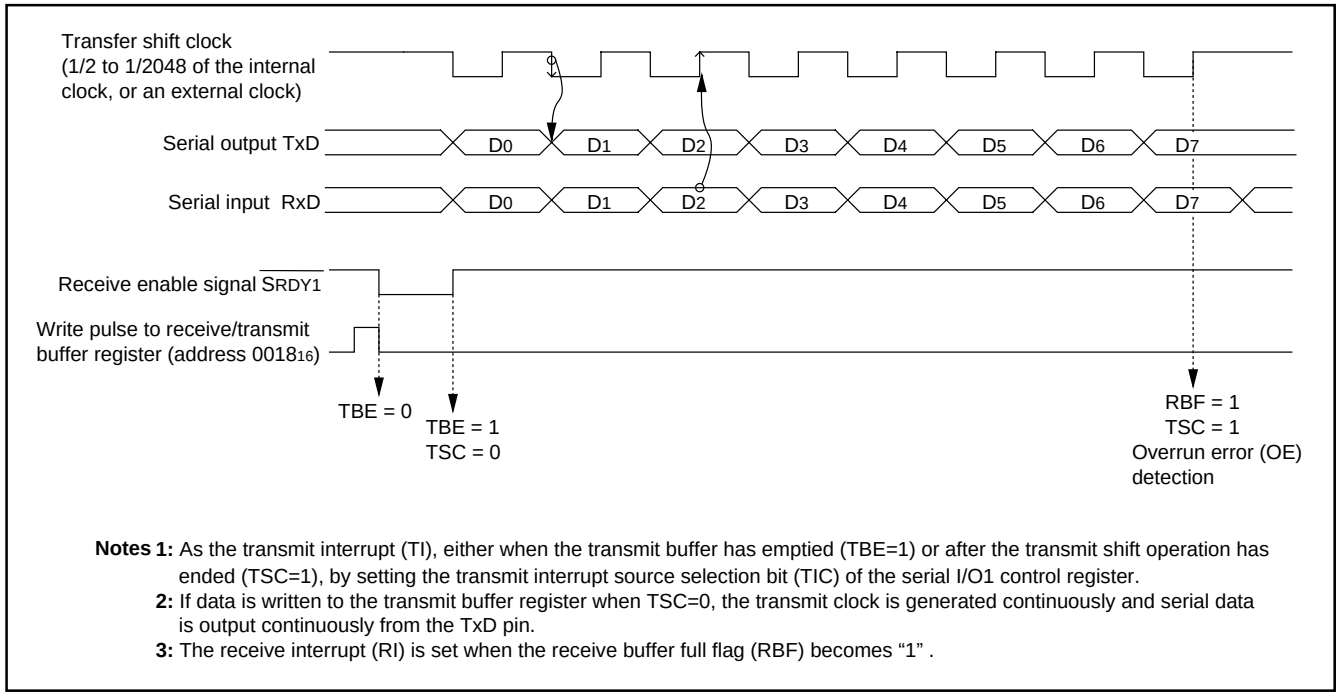


Fig. 17 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 18 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

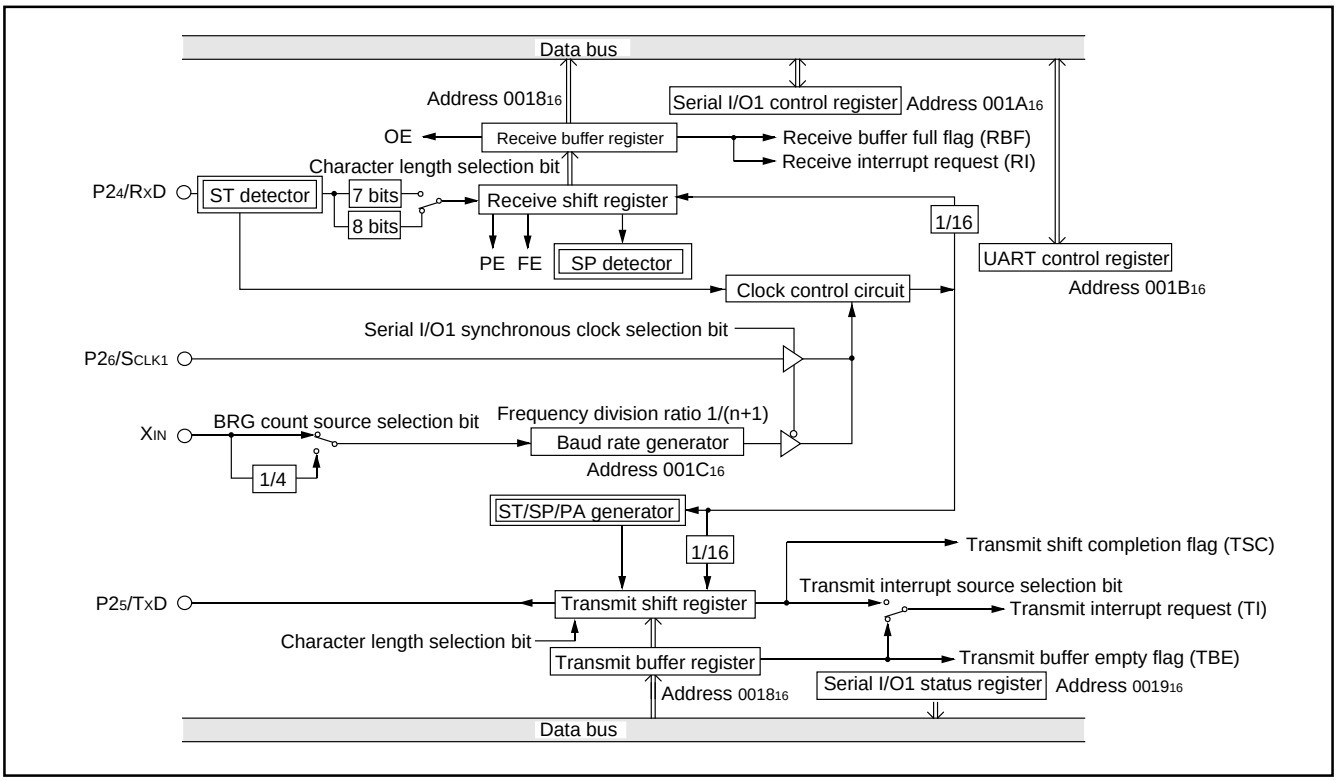
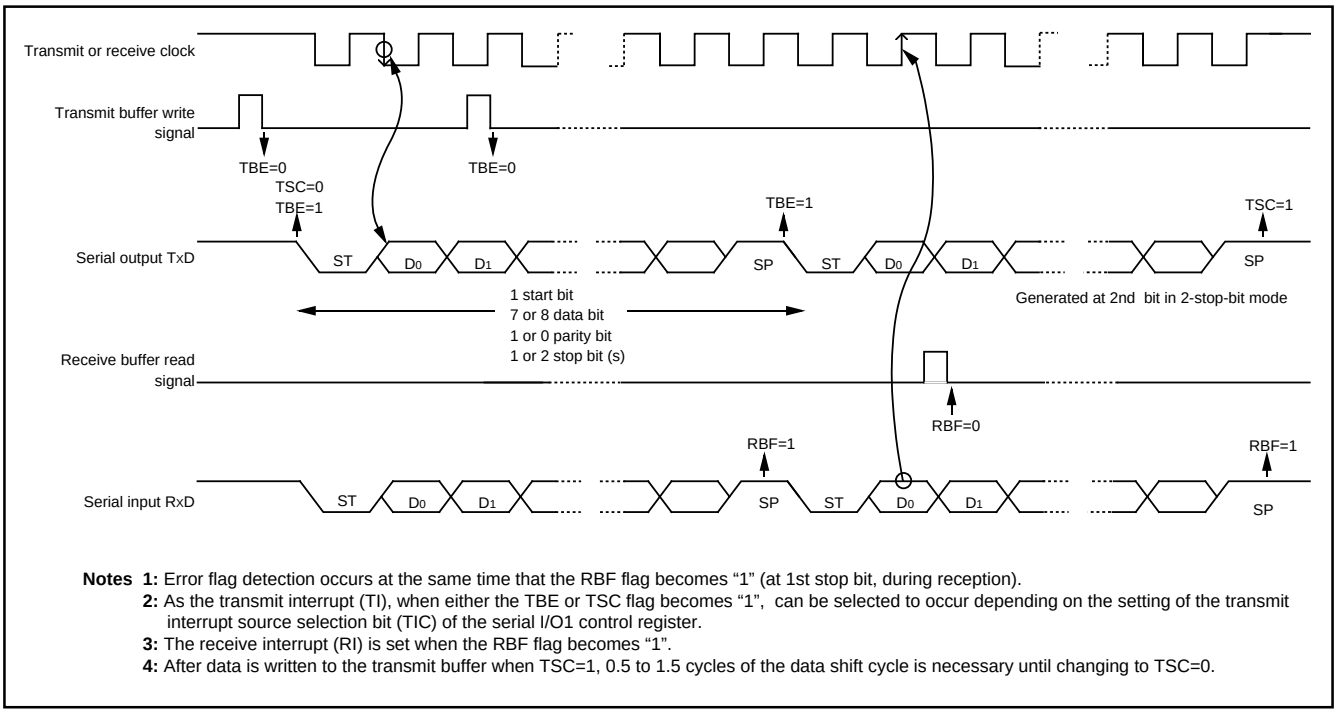


Fig. 19 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1", can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 20 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

Serial I/O1 Control Register (SIOCON)] 001A$_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P25/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Note

When using the serial I/O1, clear the I^2C-BUS interface enable bit to "0" or the SCL/SDA pin selection bit to "0".

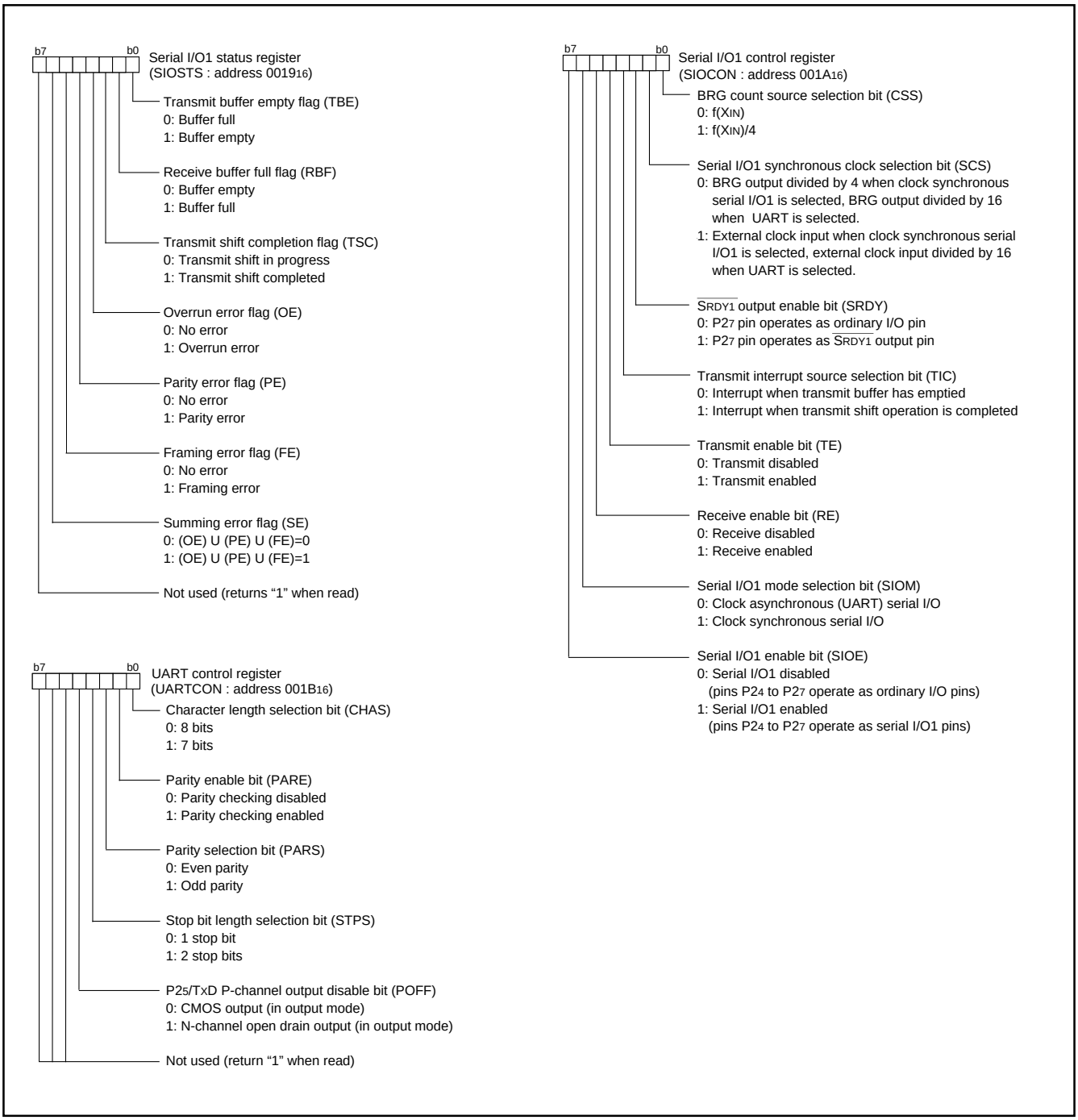


Fig. 21 Structure of serial I/O1 control registers

■Notes

When setting the transmit enable bit to "1", the serial I/O1 transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

(1) Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
(2) Set the transmit enable bit to "1".
(3) Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instructions have been executed.
(4) Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

●Serial I/O2

The serial I/O2 can be operated only as the clock synchronous type. As a synchronous clock for serial transfer, either internal clock or external clock can be selected by the serial I/O2 synchronous clock selection bit (b6) of serial I/O2 control register 1.

The internal clock incorporates a dedicated divider and permits selecting 6 types of clock by the internal synchronous clock selection bits (b2, b1, b0) of serial I/O2 control register 1.

Regarding SOUT2 and SCLK2 being output pins, either CMOS output format or N-channel open-drain output format can be selected by the P01/SOUT2, P02/SCLK2 P-channel output disable bit (b7) of serial I/O2 control register 1.

When the internal clock has been selected, a transfer starts by a write signal to the serial I/O2 register (address 0017$_{16}$). After completion of data transfer, the level of the SOUT2 pin goes to high impedance automatically but bit 7 of the serial I/O2 control register 2 is not set to "1" automatically.

When the external clock has been selected, the contents of the serial I/O2 register is continuously sifted while transfer clocks are input. Accordingly, control the clock externally. Note that the SOUT2 pin does not go to high impedance after completion of data transfer.

To cause the SOUT2 pin to go to high impedance in the case where the external clock is selected, set bit 7 of the serial I/O2 control register 2 to "1" when SCLK2 is "H" after completion of data transfer. After the next data transfer is started (the transfer clock falls), bit 7 of the serial I/O2 control register 2 is set to "0" and the SOUT2 pin is put into the active state.

When the number of bits (1 to 8 bits) selected by the optional transfer bit is transferred regardless of the internal clock to external clock, the serial I/O2 transmission/reception completion flag (Note) is set to "1" and the interrupt request bit is set to "1". The serial I/O2 transmission/reception completion flag is not automatically set to "0", even if the next transmission starts. In case of a fractional number of bits less than 8 bits as the last data, the received data to be stored in the serial I/O2 register becomes a fractional number of bits close to MSB if the transfer direction selection bit of serial I/O2 control register 1 is LSB first, or a fractional number of bits close to LSB if the said bit is MSB first. For the remaining bits, the previously received data is shifted.

At transmit operation using the clock synchronous serial I/O, the SCMP2 signal can be output by comparing the state of the transmit pin SOUT2 with the state of the receive pin SIN2 in synchronization with a rise of the transfer clock. If the output level of the SOUT2 pin is equal to the input level to the SIN2 pin, "L" is output from the SCMP2 pin. If not, "H" is output. At this time, an INT2 interrupt request can also be generated. Select a valid edge by bit 2 of the interrupt edge selection register (address 003A$_{16}$).

Note: After reset is released, the serial I/O2 transmission/reception completion flag is undefined. After the initial setting of serial I/O2 is completed, set this flag to "0".

[Serial I/O2 Control Registers 1, 2] SIO2CON1 / SIO2CON2

The serial I/O2 control registers 1 and 2 are containing various selection bits for serial I/O2 control as shown in Figure 22.

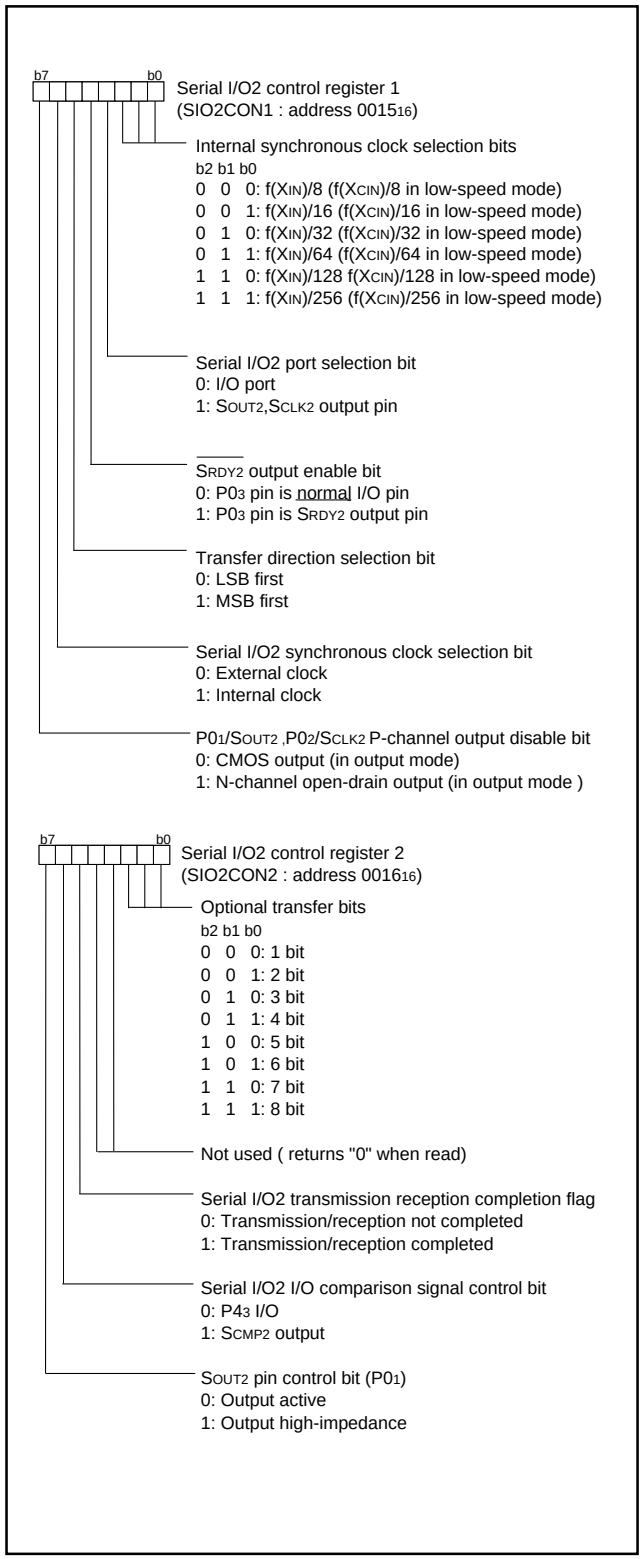
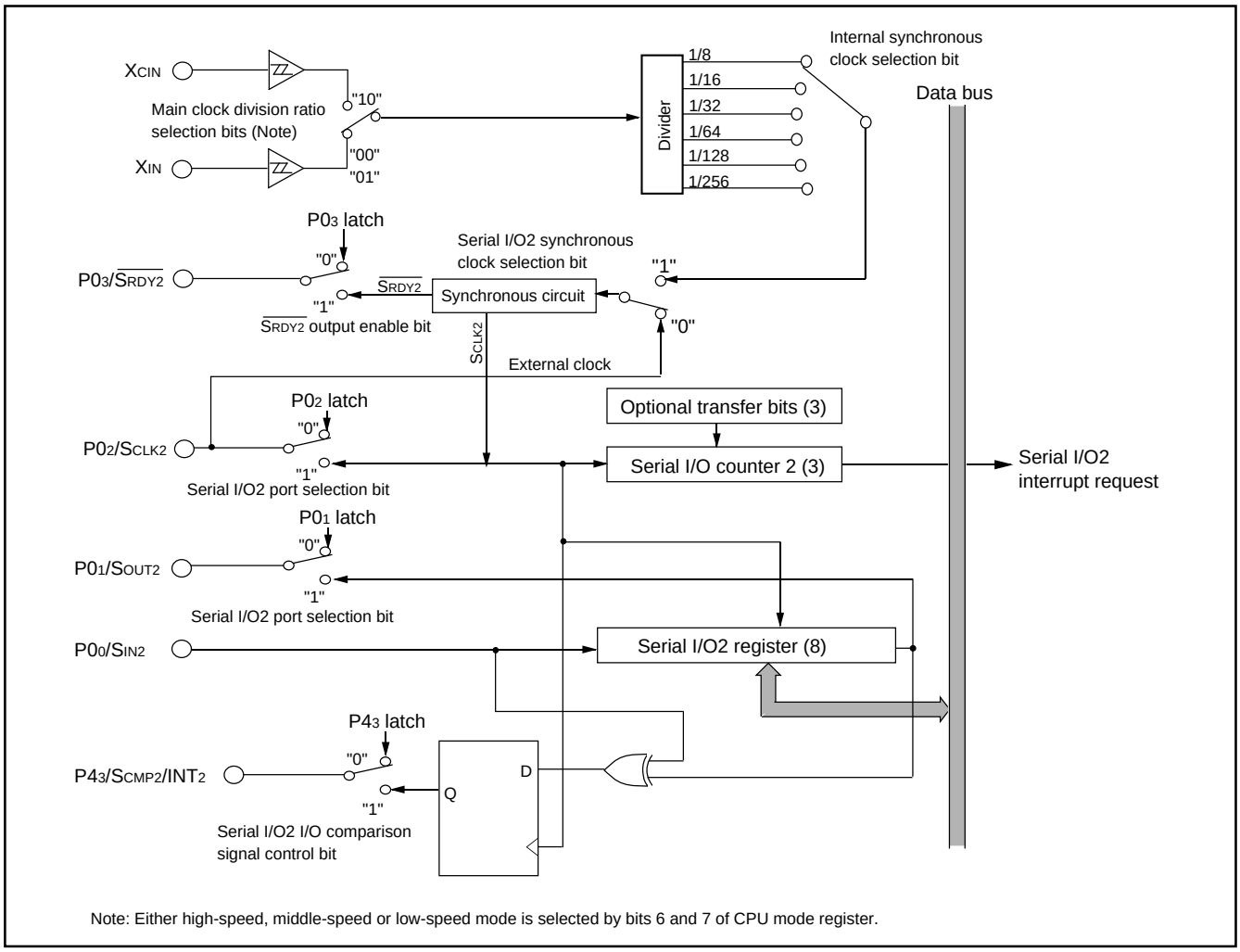
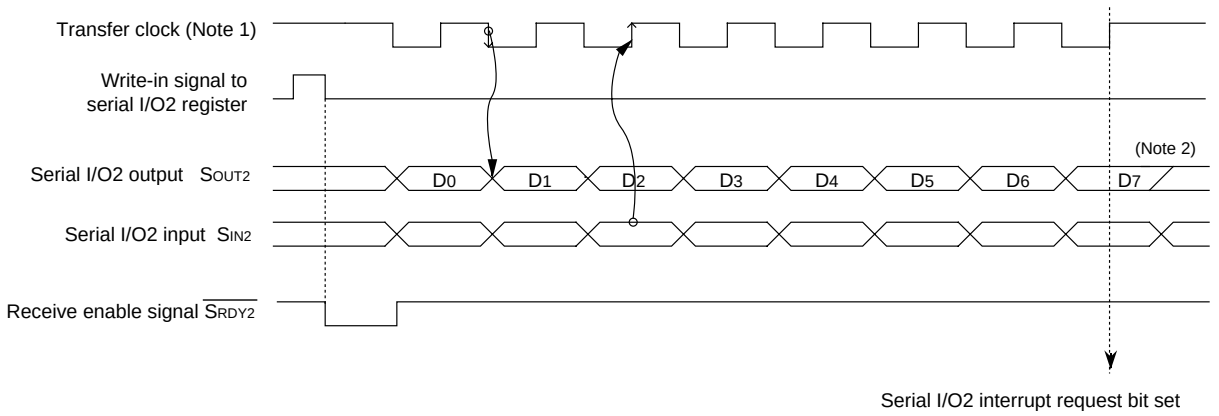


Fig. 22 Structure of Serial I/O2 control registers 1, 2



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 6 and 7 of CPU mode register.

Fig. 23 Block diagram of Serial I/O2



Notes 1: When the internal clock is selected as a transfer clock, the f(XIN) clock division (f(XCIN) in low-speed mode) can be selected by setting bits 0 to 2 of serial I/O2 control register 1.
2: When the internal clock is selected as a transfer clock, the SCOUT2 pin has high impedance after transfer completion.

Fig. 24 Timing chart of Serial I/O2

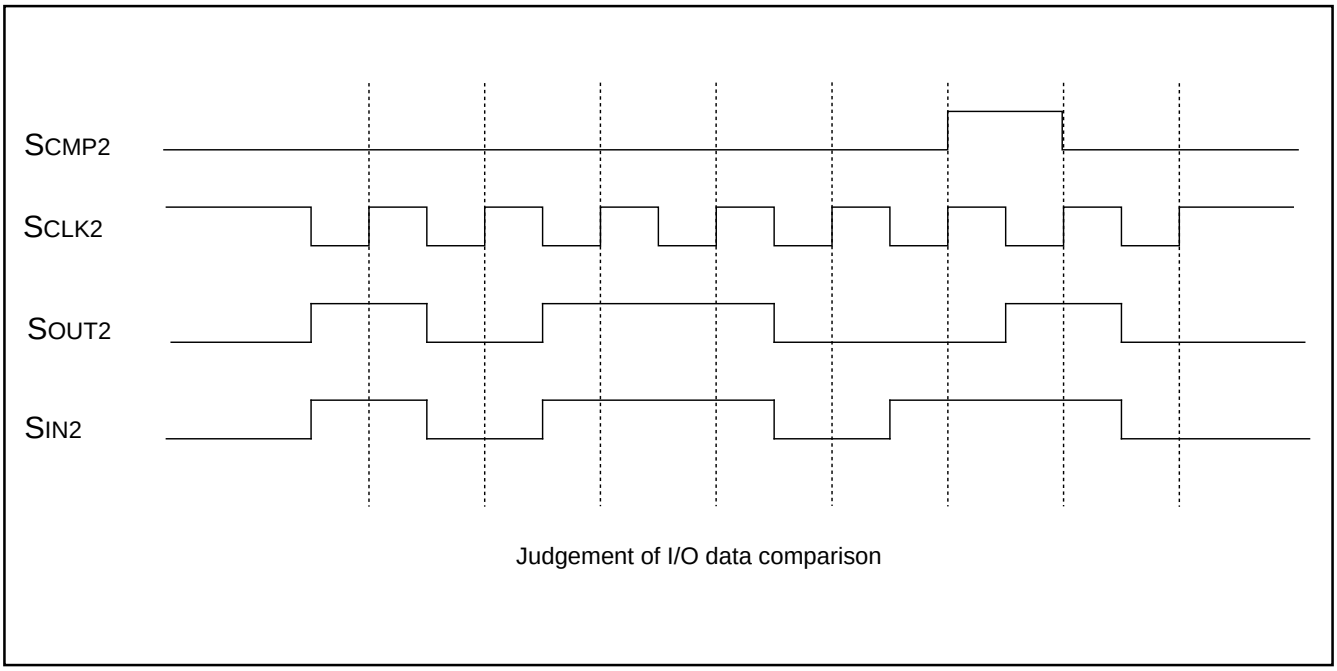


Fig. 25 SCMP2 output operation

MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 26 shows a block diagram of the multi-master I²C-BUS interface and Table 7 lists the multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register, the I²C start/stop condition control register and other control circuits.

When using the multi-master I²C-BUS interface, set 1 MHz or more to ϕ .

Note: Renesas Technology Corporation assumes no responsibility for infringement of any third-party's rights or originating in the use of the connection control function between the I²C-BUS interface and the ports SCL_1, SCL_2, SDA_1 and SDA_2 with the bit 6 of I²C control register ($002E_{16}$).

Table 7 Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ = 4 MHz)

System clock $\phi = f(X_{IN})/2$ (high-speed mode)
$\phi = f(X_{IN})/8$ (middle-speed mode)

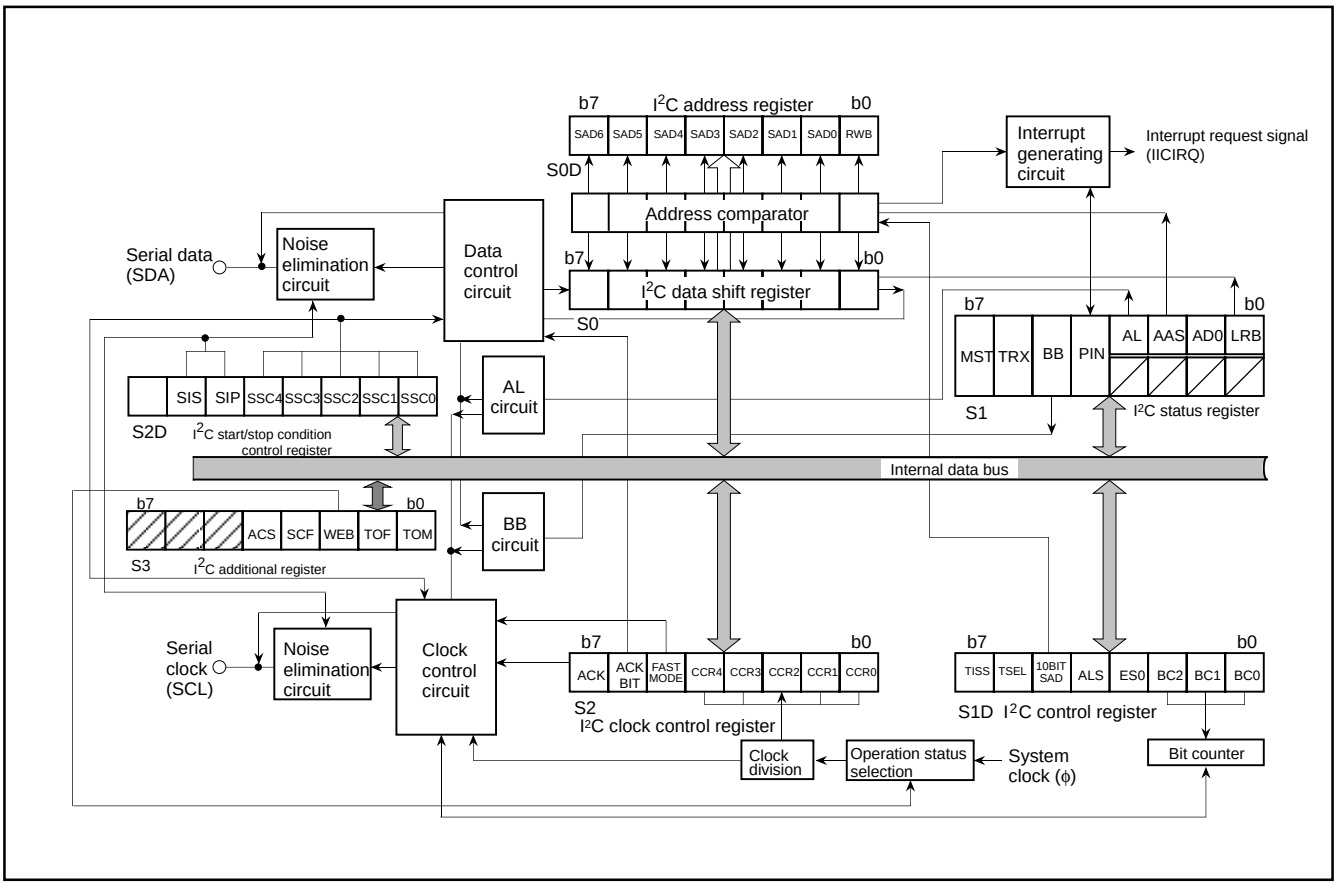


Fig. 26 Block diagram of multi-master I²C-BUS interface

✻ : Purchase of Renesas Technology Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system , provided that the system conforms to the I²C Standard Specification as defined by Philips.

[I²C Data Shift Register (S0)] 002B16

The I²C data shift register (S0 : address 002B16) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 machine cycles are required from the rising of the SCL clock until input to this register.

The I²C data shift register is in a write enable status only when the I²C-BUS interface enable bit (ES0 bit : bit 3 of address 002E16) of the I²C control register is "1". The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (address 002D16) are "1", the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

[I²C Address Register (S0D)] 002C16

The I²C address register (address 002C16) consists of a 7-bit slave address and a read/$\overline{\text{write}}$ bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/$\overline{\text{write}}$ bit (RWB)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RWB) of the I²C address register.

The RWB bit is cleared to "0" automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode or the 10-bit addressing mode, the address data transmitted from the master is compared with these bit's contents.

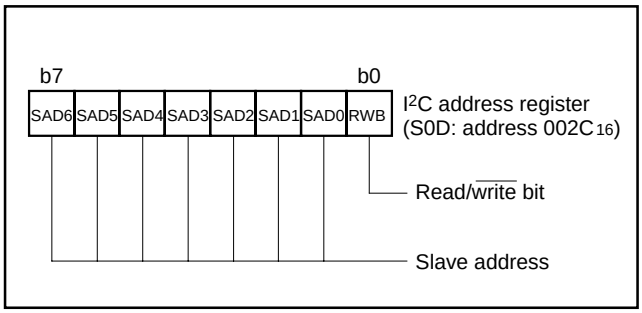


Fig. 27 Structure of I²C address register

[I²C Clock Control Register (S2)] 002F16

The I²C clock control register (address 002F16) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 8.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0", the standard clock mode is selected. When the bit is set to "1", the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C bus standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) and 2 division clock.

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0", the ACK return mode is selected and SDA goes to "L" at the occurrence of an ACK clock. When the bit is set to "1", the ACK non-return mode is selected. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address agree with the address data in the reception of address data at ACK BIT = "0", the SDA is automatically made "L" (ACK is returned). If there is a disagreement between the slave address and the address data, the SDA is automatically made "H" (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to "0", the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to "1", the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

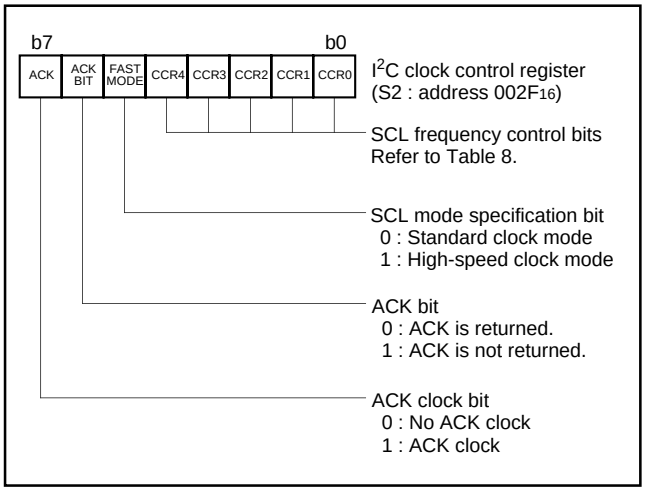


Fig. 28 Structure of I²C clock control register

Table 8 Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at ϕ = 4 MHz, unit : kHz)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	– **(Note 2)**	333
0	0	1	0	0	– **(Note 2)**	250
0	0	1	0	1	100	400 **(Note 3)**
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value **(Note 3)**	1000/CCR value **(Note 3)**
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes 1: Duty of SCL clock output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at ϕ = 4 MHz). "H" duration of the clock fluctuates from –4 to +2 machine cycles in the standard clock mode, and fluctuates from –2 to +2 machine cycles in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because "L" duration is extended instead of "H" duration reduction.
These are value when SCL clock synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at ϕ = 4 MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:
ϕ/(8 × CCR value) Standard clock mode
ϕ/(4 × CCR value) High-speed clock mode (CCR value ≠ 5)
ϕ/(2 × CCR value) High-speed clock mode (CCR value = 5)
Do not set 0 to 2 as CCR value regardless of ϕ frequency.
Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

[I²C Control Register (S1D)] 002E16

The I²C control register (address 002E16) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I²C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK clock bit (bit 7 of address 002F16)) have been transferred, and BC0 to BC2 are returned to "0002".

Also when a START condition is received, these bits become "0002" and the address data is always transmitted and received in 8 bits.

•Bit 3: I²C interface enable bit (ES0)

This bit enables to use the multi-master I²C-BUS interface. When this bit is set to "0", the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to "1", use of the interface is enabled.

When ES0 = "0", the following is performed.

- PIN = "1", BB = "0" and AL = "0" are set (which are bits of the I²C status register at address 002D16).
- Writing data to the I²C data shift register (address 002B16) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0", the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "I²C Status Register", bit 1) is received, transfer processing can be performed. When this bit is set to "1", the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0", the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 002C16) are compared with address data. When this bit is set to "1", the 10-bit addressing format is selected, and all the bits of the I²C address register are compared with address data.

•Bit 6: SDA/SCL pin selection bit

This bit selects the input/output pins of SCL and SDA of the multi-master I²C-BUS interface.

•Bit 7: I²C-BUS interface pin input level selection bit

This bit selects the input level of the SCL and SDA pins of the multi-master I²C-BUS interface.

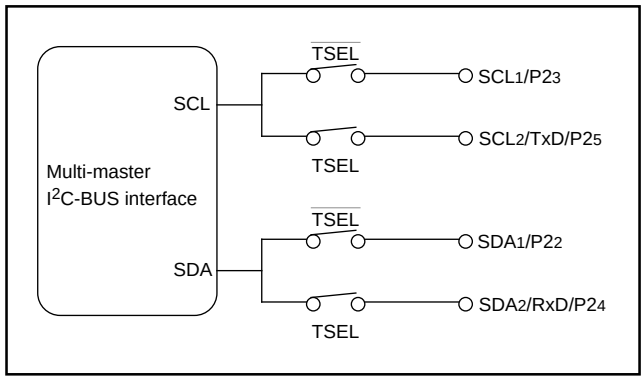


Fig. 29 SDA/SCL pin selection bit

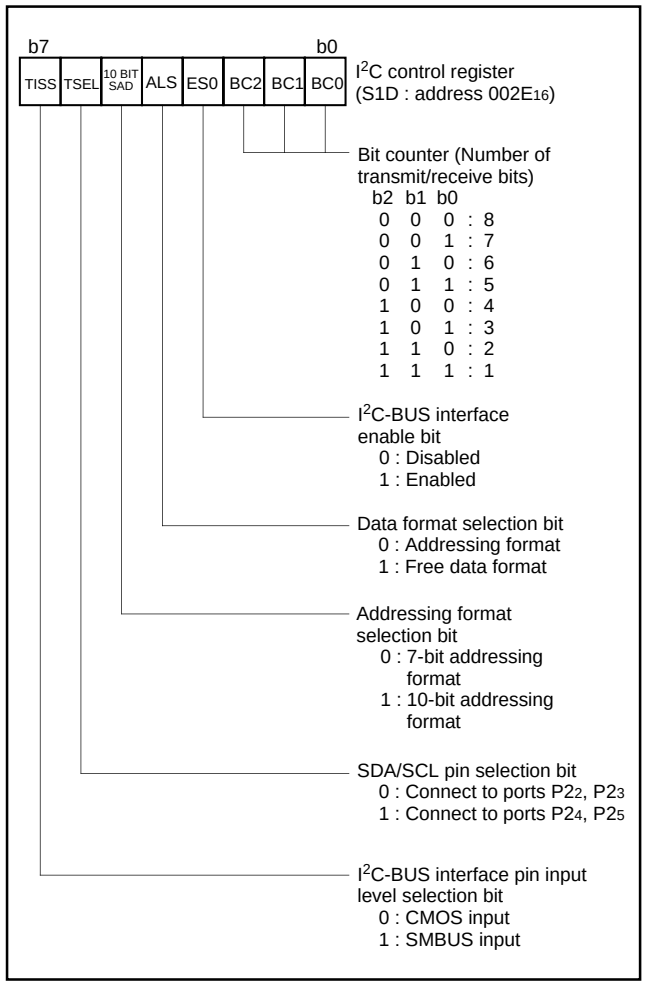


Fig. 30 Structure of I²C control register

[I²C Status Register (S1)] 002D16

The I²C status register (address 002D16) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "0000₂" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0". If ACK is not returned, this bit is set to "1". Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 002B16).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0", this bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

*General call: The master transmits the general call address "00₁₆" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is "0".

(1)In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (address 002C16).
- A general call is received.

(2)In the slave receive mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
- When the address data is compared with the I²C address register (8 bits consisting of slave address and RWB bit), the first bytes agree.

(3)This bit is set to "0" by executing a write instruction to the I²C data shift register (address 002B16) when ES0 is set to "1" or reset.

•Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1". At the same time, the TRX bit is set to "0", so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0". The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

*Arbitration lost : The status in which communication as a master is disabled.

•Bit 4: SCL pin low hold bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to "0". At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0", the SCL is kept in the "0" state and clock generation is disabled. Figure 32 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (address 002B16). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)
- When the ES0 bit is "0"
- At reset
- When writing "1" to the PIN bit by software

The conditions in which the PIN bit is set to "0" are shown below:
- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0", this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to "1" by detecting the start condition, and is set to "0" by detecting the stop condition. The condition of these detecting is set by the start/stop condition setting bits (SSC4–SSC0) of the I²C start/stop condition control register (address 003016). When the ES0 bit of the I²C control register (address 002E16) is "0" or reset, the BB flag is set to "0".

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

•Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is “0”, the reception mode is selected and the data of a transmitting device is received. When the bit is “1”, the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to “1” by hardware when all the following conditions are satisfied:

- When ALS is “0”
- In the slave reception mode or the slave transmission mode
- When the R/$\overline{W}$ bit reception is “1”

This bit is set to “0” in one of the following conditions:

- When arbitration lost is detected.
- When a STOP condition is detected.
- When writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- With MST = “0” and when a START condition is detected.
- With MST = “0” and when ACK non-return is detected.
- At reset

•Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is “0”, the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is “1”, the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to “0” in one of the following conditions.

- Immediately after completion of 1-byte data transfer when arbitration lost is detected
- When a STOP condition is detected.
- Writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- At reset

Note: START condition duplication preventing function
The MST, TRX, and BB bits is set to “1” at the same time after confirming that the BB flag is “0” in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to “1” immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

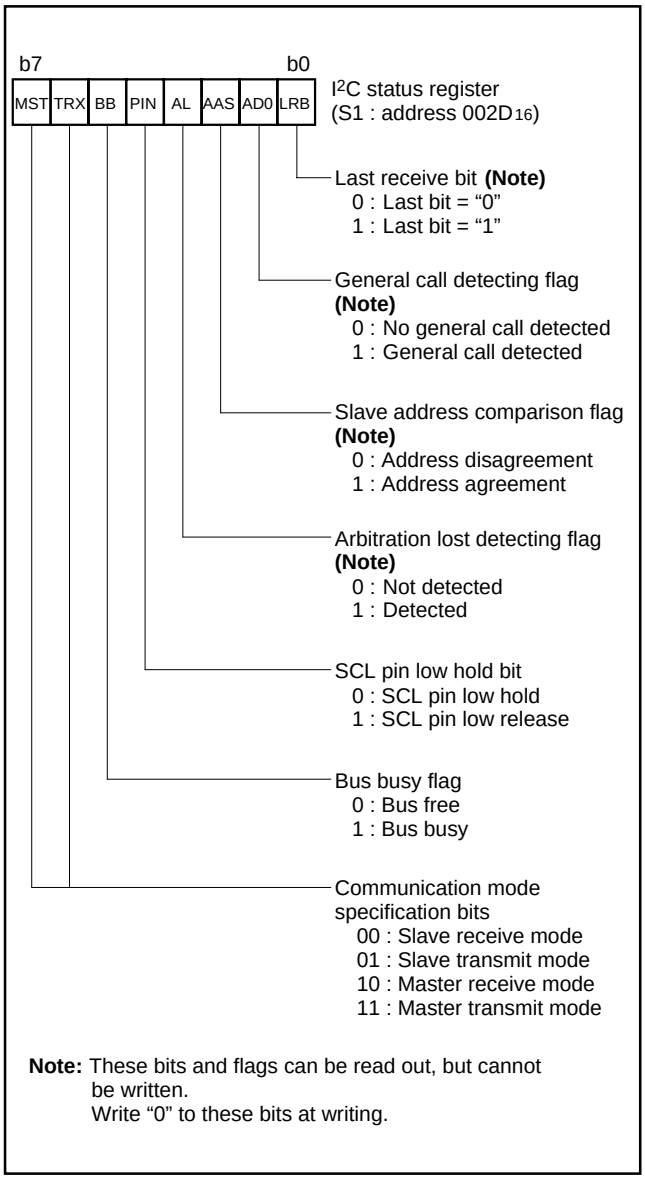


Fig. 31 Structure of I²C status register

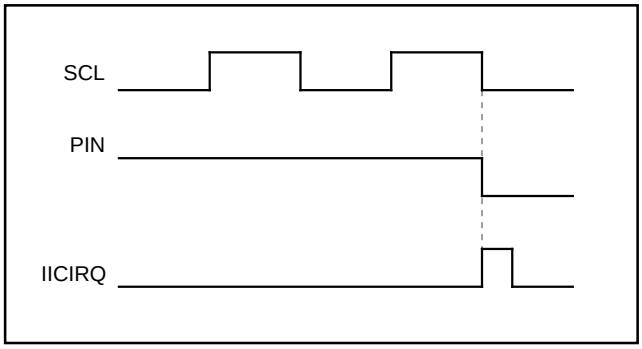


Fig. 32 Interrupt request signal generating timing

START Condition Generating Method

When writing "1" to the MST, TRX, and BB bits of the I²C status register (address 002D16) at the same time after writing the slave address to the I²C data shift register (address 002B16) with the condition in which the ES0 bit of the I²C control register (address 002E16) is "1" and the BB flag is "0", a START condition occurs. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 33, the START condition generating timing diagram, and Table 9, the START condition generating timing table.

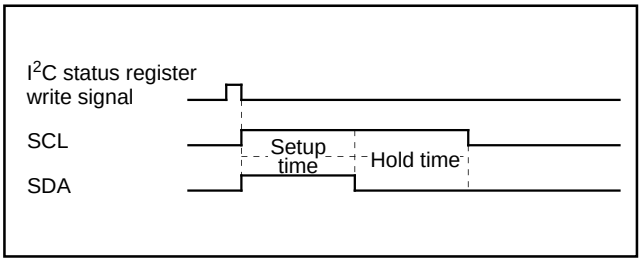


Fig. 33 START condition generating timing diagram

Table 9 START condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (address 002E16) is "1", write "1" to the MST and TRX bits, and write "0" to the BB bit of the I²C status register (address 002D16) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 34, the STOP condition generating timing diagram, and Table 10, the STOP condition generating timing table.

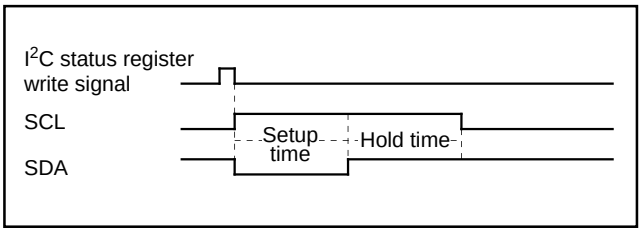


Fig. 34 STOP condition generating timing diagram

Table 10 STOP condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	3.0 µs (12 cycles)
Hold time	4.5 µs (18 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 35, 36, and Table 11. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 11).

The BB flag is set to "1" by detecting the START condition and is reset to "0" by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 11, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" occurs to the CPU.

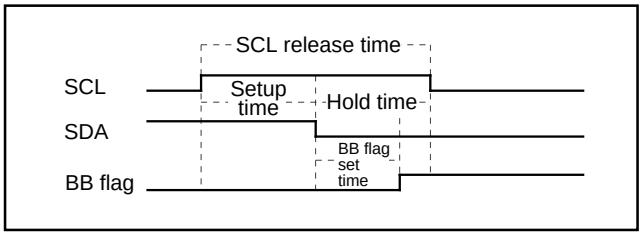


Fig. 35 START condition detecting timing diagram

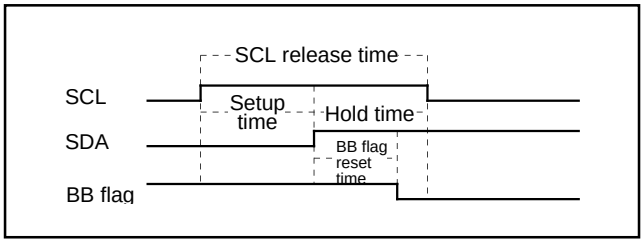


Fig. 36 STOP condition detecting timing diagram

Table 11 START condition/STOP condition detecting conditions

	Standard clock mode	High-speed clock mode
SCL release time	SSC value + 1 cycle (6.25 µs)	4 cycles (1.0 µs)
Setup time	$\frac{\text{SSC value + 1}}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (1.0 µs)
Hold time	$\frac{\text{SSC value + 1}}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (0.5 µs)
BB flag set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles (3.375 µs)	3.5 cycles (0.875 µs)

Note: Unit : Cycle number of system clock ϕ
SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set "0" or an odd number to SSC value. The value in parentheses is an example when the I²C START/STOP condition control register is set to "1816" at ϕ = 4 MHz.

[I²C START/STOP Condition Control Register (S2D)] 0030₁₆

The I²C START/STOP condition control register (address 0030₁₆) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bits (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency f(XIN) because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 11.

Do not set "00000₂" or an odd number to the START/STOP condition set bit (SSC4 to SSC0).

Refer to Table 12, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.

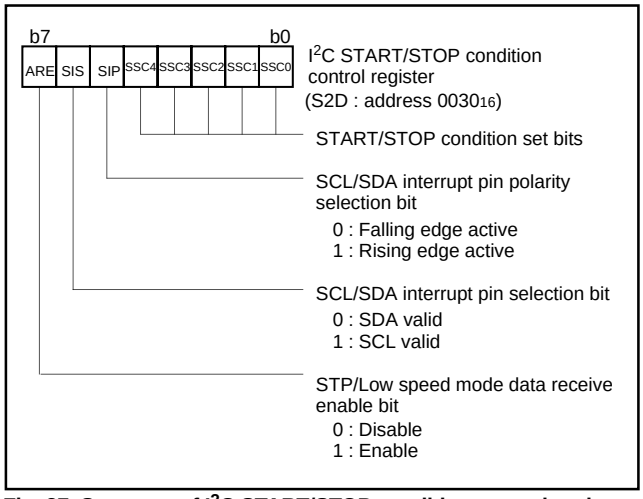


Fig. 37 Structure of I²C START/STOP condition control register

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

•Bit 7: STP/Low speed mode data receive enable bit

Selecting this bit "1" enables I²C to receive the start condition address data even if the CPU is stopping or running at the low speed mode. The detecting the falling edge of the SDA pin, built-in RC oscillator begins oscillation, and receive the start condition address data. After receiving the last bit of address data (in case of ACK clock bit ="1", after receiving ACK bit), SCL/SDA interrupt and I²C interrupt are requested at the same time. And then SCL pin becomes low hold state as a result of becoming SCL pin low hold bit "0". During this state, it is possible to start the Xin oscillation. And after oscillation becomes stable, normal I²C operation begins. If the start condition which is not satisfied the hold time of start condition is input, SCL/SDA interrupt is requested.

In the low-speed mode, when this bit is set to "1", SCL/SDA interrupt which occur by the rising or falling edge of SCL or SDA is disabled.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

Table 12 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

Oscillation frequency f(XIN) (MHz)	Main clock divide ratio	System clock ϕ (MHz)	START/STOP condition control register	SCL release time (μs)	Setup time (μs)	Hold time (μs)
8	2	4	XXX11010	6.75 μs (27 cycles)	3.375 μs (13.5 cycles)	3.375 μs (13.5 cycles)
			XXX11000	6.25 μs (25 cycles)	3.125 μs (12.5 cycles)	3.125 μs (12.5 cycles)
8	8	1	XXX00100	5.0 μs (5 cycles)	2.5 μs (2.5 cycles)	2.5 μs (2.5 cycles)
4	2	2	XXX01100	6.5 μs (13 cycles)	3.25 μs (6.5 cycles)	3.25 μs (6.5 cycles)
			XXX01010	5.5 μs (11 cycles)	2.75 μs (5.5 cycles)	2.75 μs (5.5 cycles)
2	2	1	XXX00100	5.0 μs (5 cycles)	2.5 μs (2.5 cycles)	2.5 μs (2.5 cycles)

Note: Do not set "00000₂" or an odd number to the START/STOP condition set bits (SSC4 to SSC0).

I²C additional register

(1) bit 0: Time-out mode bit (TOM)

Setting the time-out mode bit “1” , continuity of I²C-Bus busy state for about 16ms (f(XIN)=4MHz, high-speed mode) makes time-out flag “1” and time-out interrupt occurs. Check the time-out flag to know which interrupt source of the SCL/SDA interrupt is occurred. When restart condition occurs in the middle of communication, the time-out timer is cleared.

(2) bit 1: Time-out flag (TOF)

Time-out flag becomes “1” when the time-out state occurs. Writing “1” to this bit, time-out timer is reset, and this bit is cleared “0” also.

(3) I²C operation enable bit at WIT mode (WEB)

This bit determines multi-master I²C-BUS interface operation at WIT mode. Setting this bit "0", multi-master I²C interface source clock is not supplied at WIT mode. Setting this bit "1", multi-master I²C interface source clock is supplied even at WIT mode, and it makes possible multi-master I²C interface operation at WIT mode. Do not execute STP instruction at I²C operation enable bit at WIT mode is "1".

(4) Stop condition flag (SCF)

This flag turns to “1”, when the stop condition is generated or detected. This bit is cleared “0” at reset, or when I²C-Bus interface enable bit is “0” or writing this bit “1”. This bit is available only when I²C-Bus interface enable bit is “1”.

(5) ACK clock selection mode bit (ACS)

Setting this bit "1" clears the ACK bit (bit 6 of 002F16) "0" and sets the ACK clock bit (bit 7 of 002F16) "1" automatically, when the stop condition is detected.

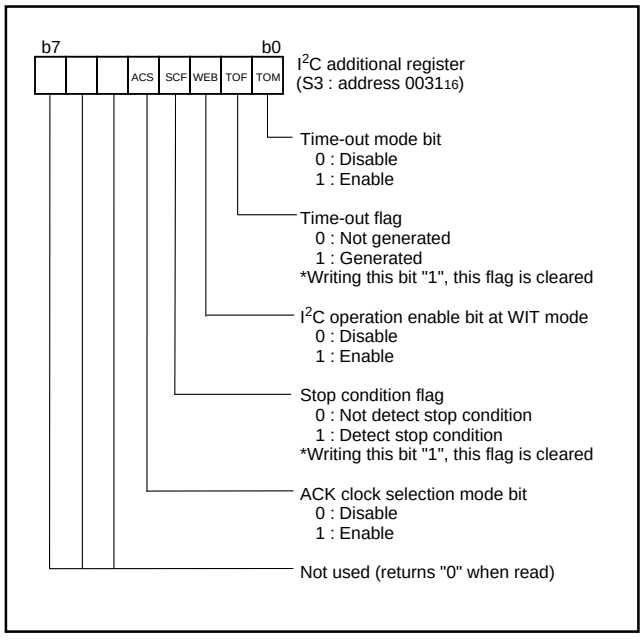


Fig. 38 I²C additional register

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

(1)7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 002E16) to "0". The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 002C16). At the time of this comparison, address comparison of the RWB bit of the I²C address register (address 002C16) is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 39, (1) and (2).

(2)10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 002E16) to "1". An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I²C address register (address 002C16). At the time of this comparison, an address comparison between the RWB bit of the I²C address register (address 002C16) and the R/W bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RWB bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit.

When the first-byte address data agree with the slave address, the AAS bit of the I²C status register (address 002D16) is set to "1". After the second-byte address data is stored into the I²C data shift register (address 002B16), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RWB bit of the I²C address register (address 002C16) to "1" by software. This processing can make the 7-bit slave address and R/W data agree, which are received after a RESTART condition is detected, with the value of the I²C address register (address 002C16). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 39, (3) and (4).

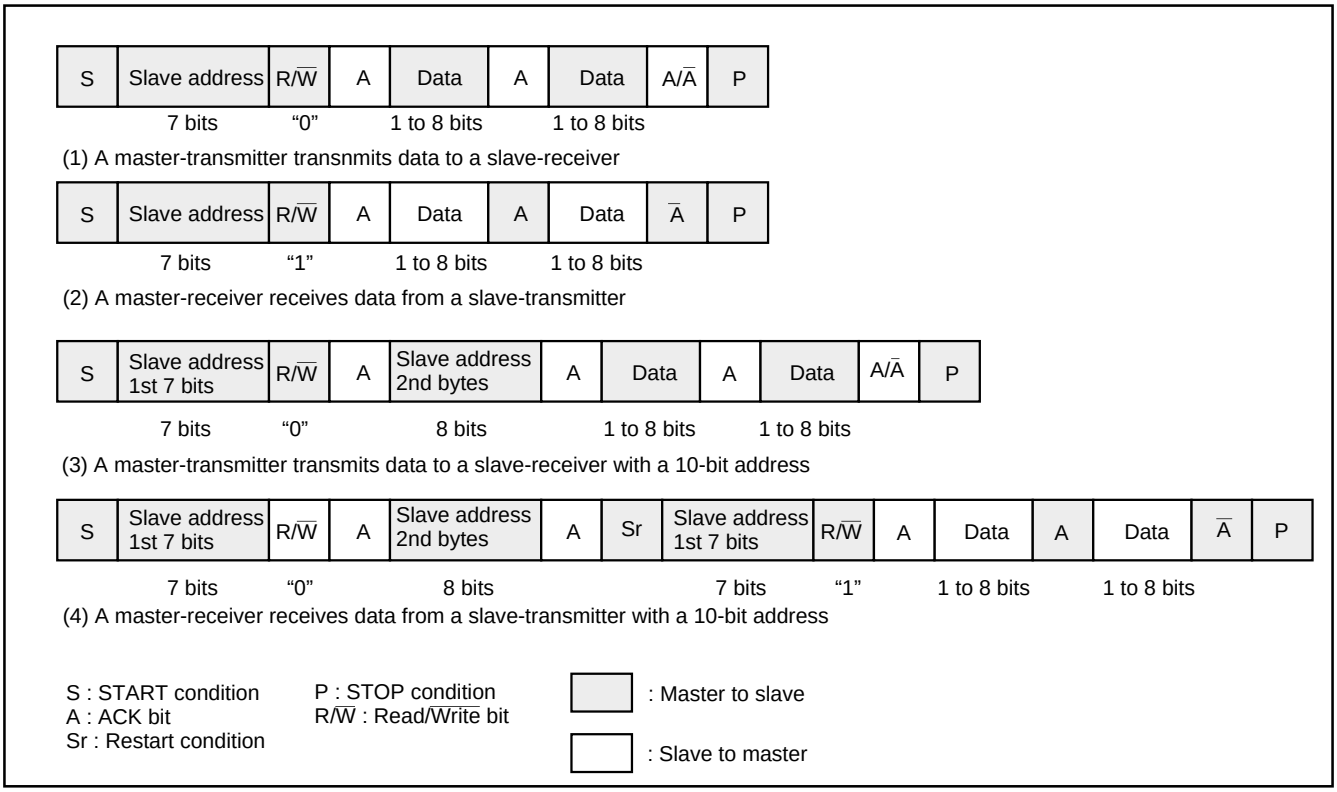


Fig. 39 Address data communication format

Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

(1) Set a slave address in the high-order 7 bits of the I^2C address register (address $002C_{16}$) and "0" into the RWB bit.
(2) Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (address $002F_{16}$).
(3) Set "00_{16}" in the I^2C status register (address $002D_{16}$) so that transmission/reception mode can become initializing condition.
(4) Set a communication enable status by setting "08_{16}" in the I^2C control register (address $002E_{16}$).
(5) Confirm the bus free condition by the BB flag of the I^2C status register (address $002D_{16}$).
(6) Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address $002B_{16}$) and set "0" in the least significant bit.
(7) Set "$F0_{16}$" in the I^2C status register (address $002D_{16}$) to generate a START condition. At this time, a SCL for 1 byte and an ACK clock automatically occur.
(8) Set transmit data in the I^2C data shift register (address $002B_{16}$). At this time, a SCL and an ACK clock automatically occur.
(9) When transmitting control data of more than 1 byte, repeat step (8).
(10) Set "$D0_{16}$" in the I^2C status register (address $002D_{16}$) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

(1) Set a slave address in the high-order 7 bits of the I^2C address register (address $002C_{16}$) and "0" in the RWB bit.
(2) Set the ACK non-return mode and SCL = 400 kHz by setting "25_{16}" in the I^2C clock control register (address $002F_{16}$).
(3) Set "00_{16}" in the I^2C status register (address $002D_{16}$) so that transmission/reception mode can become initializing condition.
(4) Set a communication enable status by setting "08_{16}" in the I^2C control register (address $002E_{16}$).
(5) When a START condition is received, an address comparison is performed.
(6) •When all transmitted addresses are "0" (general call):
AD0 of the I^2C status register (address $002D_{16}$) is set to "1" and an interrupt request signal occurs.
•When the transmitted addresses agree with the address set in (1):
ASS of the I^2C status register (address $002D_{16}$) is set to "1" and an interrupt request signal occurs.
• In the cases other than the above AD0 and AAS of the I^2C status register (address $002D_{16}$) are set to "0" and no interrupt request signal occurs.
(7) Set dummy data in the I^2C data shift register (address $002B_{16}$).
(8) When receiving control data of more than 1 byte, repeat step (7).
(9) When a STOP condition is detected, the communication ends.

■Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

- I²C data shift register (S0: address 002B16)
  When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I²C address register (S0D: address 002C16)
  When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RWB) at the above timing.
- I²C status register (S1: address 002D16)
  Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I²C control register (S1D: address 002E16)
  When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I²C clock control register (S2: address 002F16)
  The read-modify-write instruction can be executed for this register.
- I²C START/STOP condition control register (S2D: address 003016)
  The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 5.

```
    ⋮
  LDA —                 (Taking out of slave address value)
  SEI                   (Interrupt disabled)
  BBS 5, S1, BUSBUSY    (BB flag confirming and branch process)
BUSFREE:
  STA S0                (Writing of slave address value)
  LDM #$F0, S1          (Trigger of START condition generating)
  CLI                   (Interrupt enabled)
    ⋮
BUSBUSY:
  CLI                   (Interrupt enabled)
    ⋮
```

2. Use “Branch on Bit Set” of “BBS 5, $002D, –” for the BB flag confirming and branch process.
3. Use “STA $2B, STX $2B” or “STY $2B” of the zero page addressing instruction for writing the slave address value to the I²C data shift register.
4. Execute the branch instruction of above 2 and the store instruction of above 3 continuously shown the above procedure example.
5. Disable interrupts during the following three process steps:
   - BB flag confirming
   - Writing of slave address value
   - Trigger of START condition generating

   When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 4.)
   Execute the following procedure when the PIN bit is “0”.

```
    ⋮
  LDM #$00, S1          (Select slave receive mode)
  LDA —                 (Taking out of slave address value)
  SEI                   (Interrupt disabled)
  STA S0                (Writing of slave address value)
  LDM #$F0, S1          (Trigger of RESTART condition generating)
  CLI                   (Interrupt enabled)
    ⋮
```

2. Select the slave receive mode when the PIN bit is “0”. Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.
   The TRX bit becomes “0” and the SDA pin is released.
3. The SCL pin is released by writing the slave address value to the I²C data shift register.
4. Disable interrupts during the following two process steps:
   - Writing of slave address value
   - Trigger of RESTART condition generating

(4) Writing to I²C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1”. It is because it may become the same as above.

(5) Process of after STOP condition generating

Do not write data in the I²C data shift register S0 and the I²C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

PULSE WIDTH MODULATION (PWM)

The 7512 Group has a PWM function with an 8-bit resolution, based on a signal that is the clock input XIN or that clock input divided by 2.

Data Setting

The PWM output pin also functions as port P44 or port P07. The PWM output pin can be selected to either port P44/PWM0 or port P07/PWM1 by bit 2 (PWM output pin selectoin bit) of the PWM control register. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 × (n+1) / f(XIN)

= 63.75 × (n+1) µs

(when f(XIN) = 4 MHz)

Output pulse "H" term = PWM period × m / 255

= 0.25 × (n+1) × m µs

(when f(XIN) = 4 MHz)

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

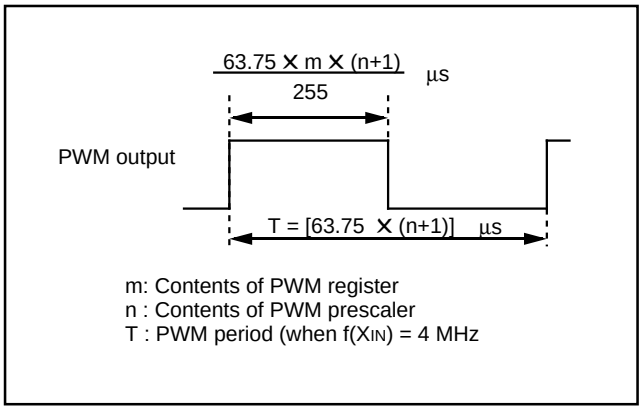


Fig. 40 Timing of PWM period

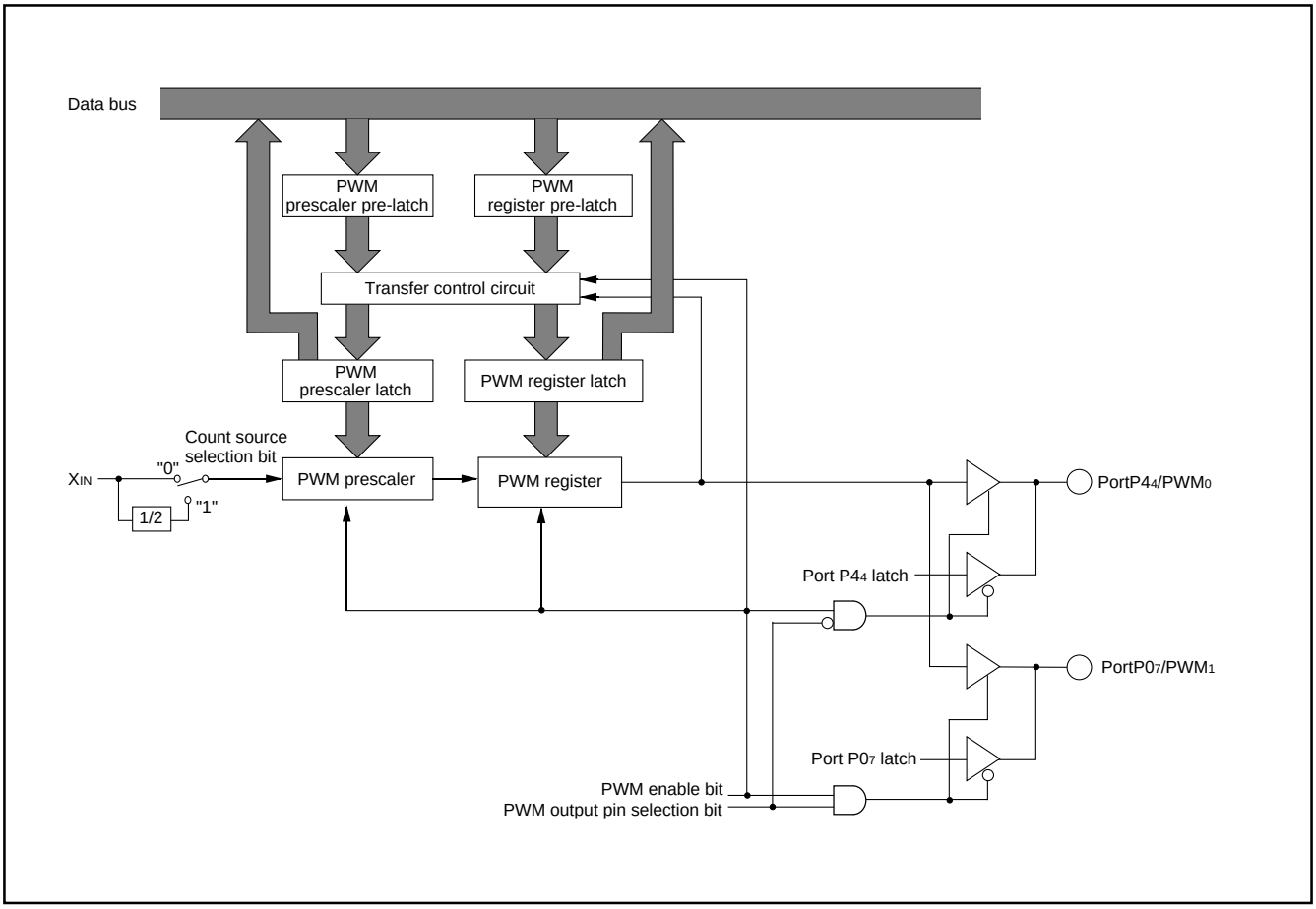


Fig. 41 Block diagram of PWM function

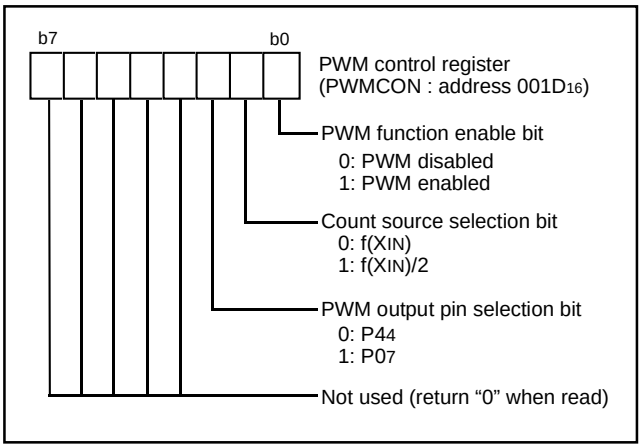


Fig. 42 Structure of PWM control register

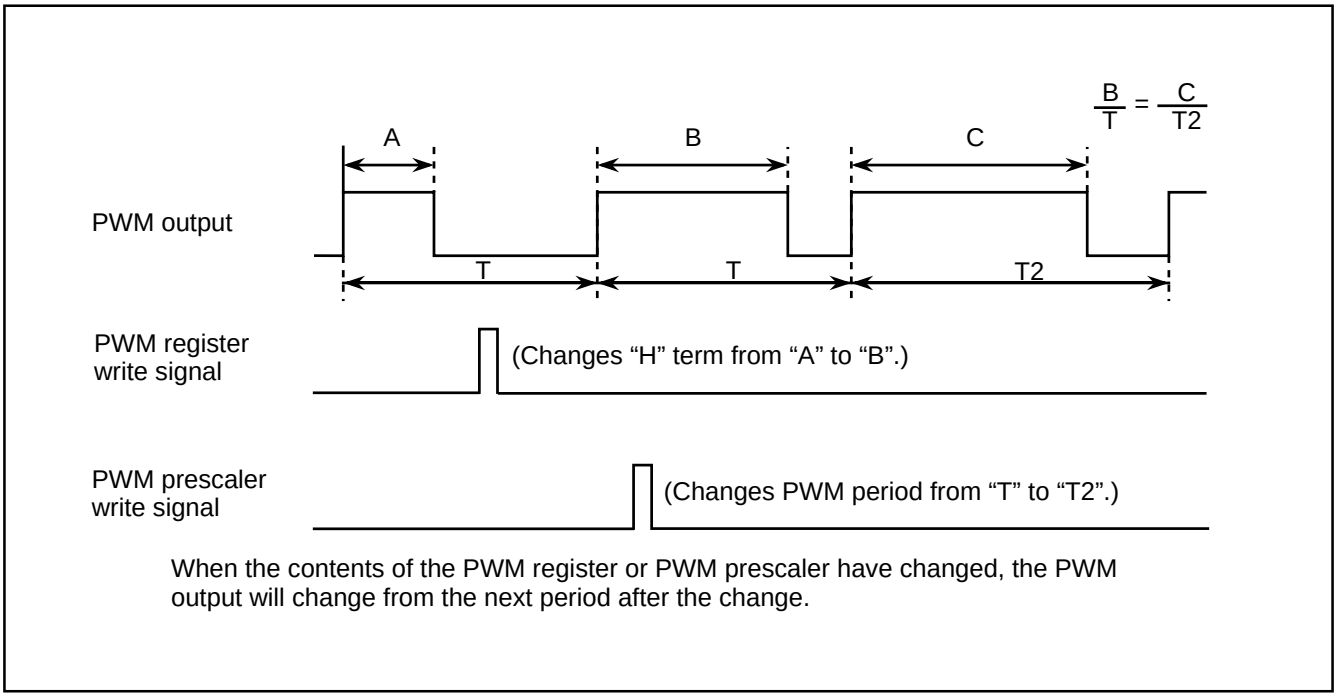


Fig. 43 PWM output timing when PWM register or PWM prescaler is changed

■Note

The PWM starts after the PWM enable bit is set to enable and "L" level is output from the PWM pin.
The length of this "L" level output is as follows:

$\frac{n+1}{2 \cdot f(X_{IN})}$ sec (Count source selection bit = 0, where n is the value set in the prescaler)

$\frac{n+1}{f(X_{IN})}$ sec (Count source selection bit = 1, where n is the value set in the prescaler)

A/D CONVERTER
[AD Conversion Registers (ADL, ADH)] 003516, 003616

The AD conversion registers are read-only registers that store the result of an A/D conversion. Do not read these registers during an A/D conversion

[AD Control Register (ADCON)] 003416

The AD control register controls the A/D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 4 indicates the completion of an A/D conversion. The value of this bit remains at “0” during an A/D conversion and changes to “1” when an A/D conversion ends. Writing “0” to this bit starts the A/D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024 and outputs the divided voltages.

Channel Selector

The channel selector selects one of ports P04/AN8 to P07/AN11 and ports P30/AN0 to P35/AN5 and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the AD conversion registers. When an A/D conversion is completed, the control circuit sets the A/D conversion completion bit and the A/D interrupt request bit to “1”.

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A/D conversion.

When the A/D converter is operated at low-speed mode, f(XIN) and f(XCIN) do not have the lower limit of frequency, because of the A/D converter has a built-in self-oscillation circuit.

Easy thermal sensor

Easy thermal sensor detects voltage change of P-N diordes by thermal difference using A/D converter. Setting the Analog input pin selection additional bit "0" and Analog input pin selection bits "111" starts A/D conversion of thermal sensor.

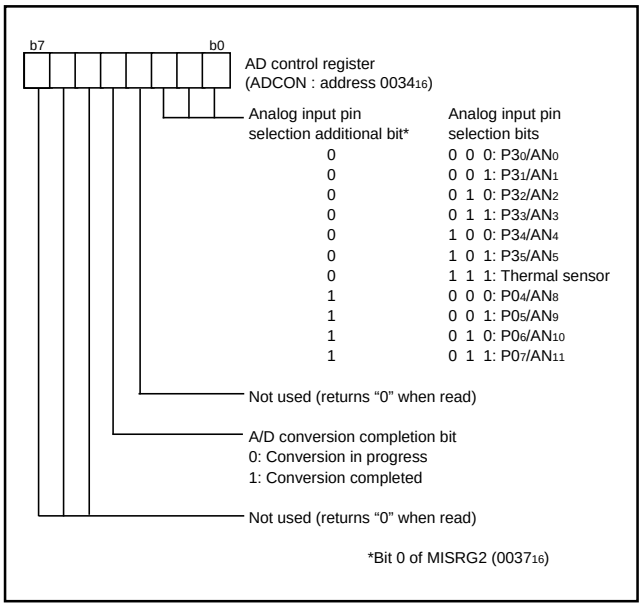


Fig. 44 Structure of AD control register

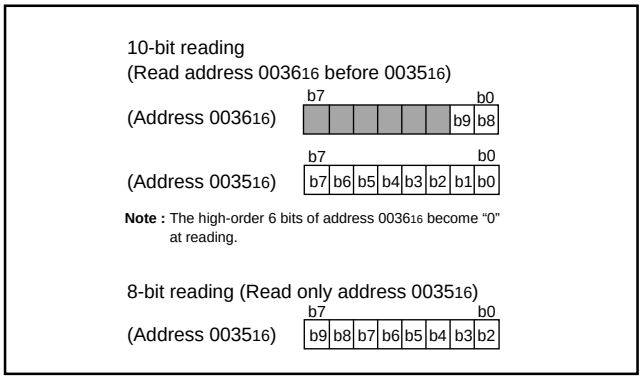


Fig. 45 Structure of AD conversion registers

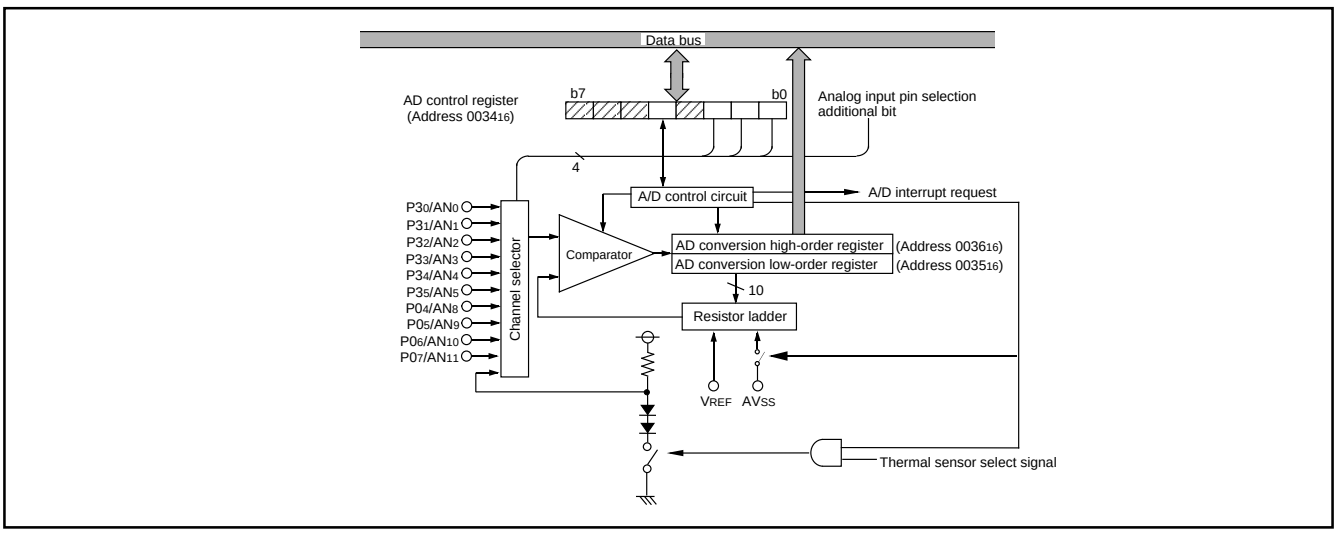


Fig. 46 Block diagram of A/D converter

CURRENT INTEGRATOR

Current integrator integrates the current which flows through sense resistor connected between ISENS0 pin and ISENS1 pin. The current between sense resistor makes electrical potential difference between ISENS0 pin and ISENS1 pin, and it is integrated by the built-in integrator. The output of integrator is connected to comparator, and the integrator and comparator measures about 1mA current in case of using 10 mΩ sense register. And charge/discharge counter counts how many times the integrator overflows.

Setting the current integrate enable bit "1", the current integrator starts the operation.

Current Integrate Mode

Setting the current integrate mode bit "0", input of the V-I converter is connected to the ISENS1 pin and ISENS0 pin, and the current integrator measures the electrical potential difference between ISENS1 pin and ISENS0 pin. The input voltage between ISENS1 and ISENS0 is converted to current by V-I converter, and input to the integrator.

The output of the integrator is connected to the comparator. The integrator integrates input voltage between ISENS1 pin and ISENS0 pin. And when output of the integrator amounts to compared voltage, output of the comparator rises "H", and charge(discharge) counter is increased 1 count. And at the same time, electric charge of the integrator's capacitor is discharged, then the integrator starts next integration. Charge(Dischrage) counter is counting the number of the times "H" output of the comparator during integration period(125msec), and at the end of the period, charge (discharge)counter is latched onto charge(discharge) counter latch. Then charge(discharge) counter is cleared "0", and starts new count. At the end of the period, current integrate interrupt occurs also.

The current integrator has 2 set of comparator and counter for discharge and charge, and only discharge counter counts up in discharge state, and only charge counter counts up in charge state. The integrator and comparator are designed to sense approximate 1mA current, then 1 count of counter means approximate 1mA. Therefore reading the value of counter latch means measuring the total current which flows the sense resistor during integrate period(125msec).

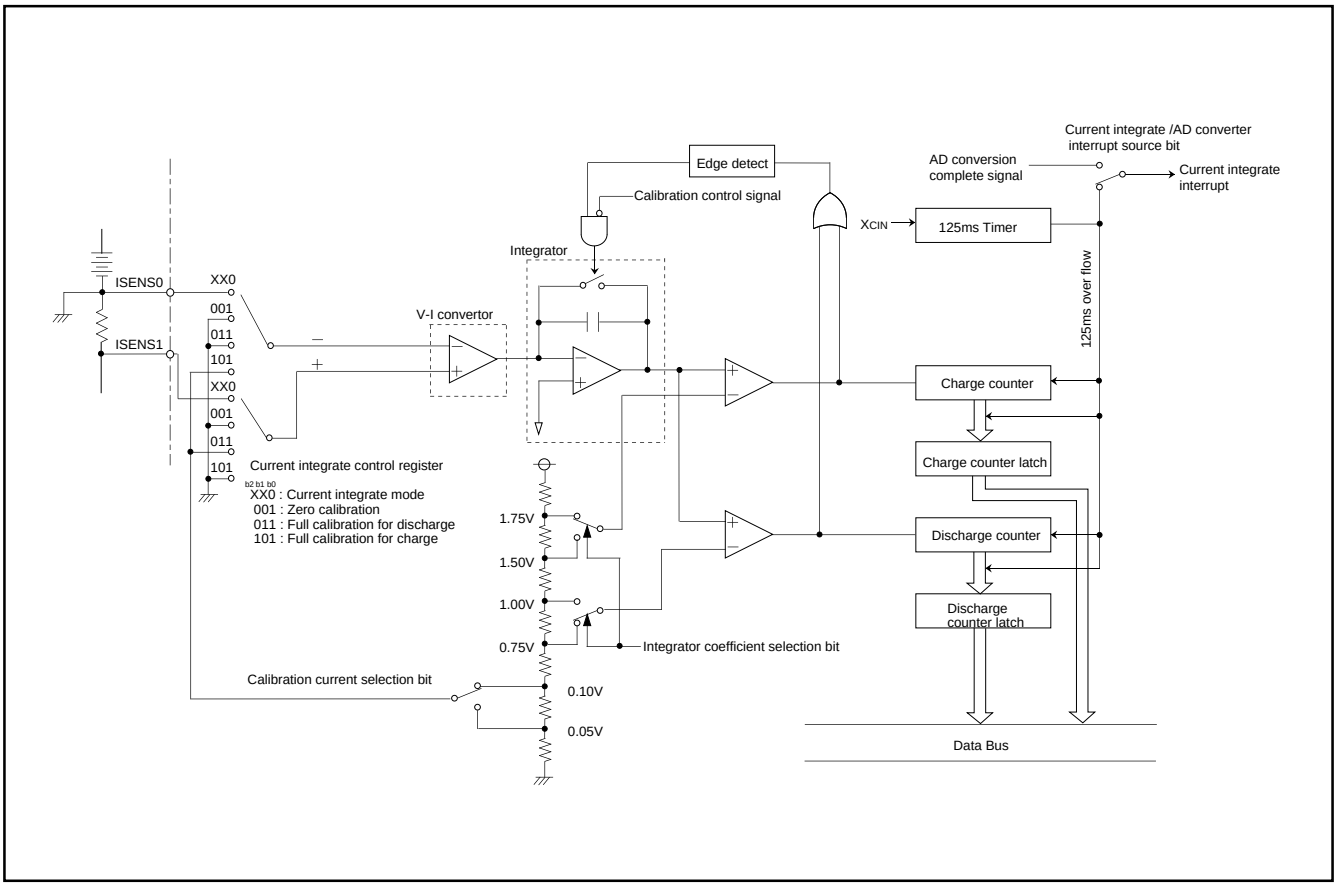


Fig. 47 Block diagram of Current integrator

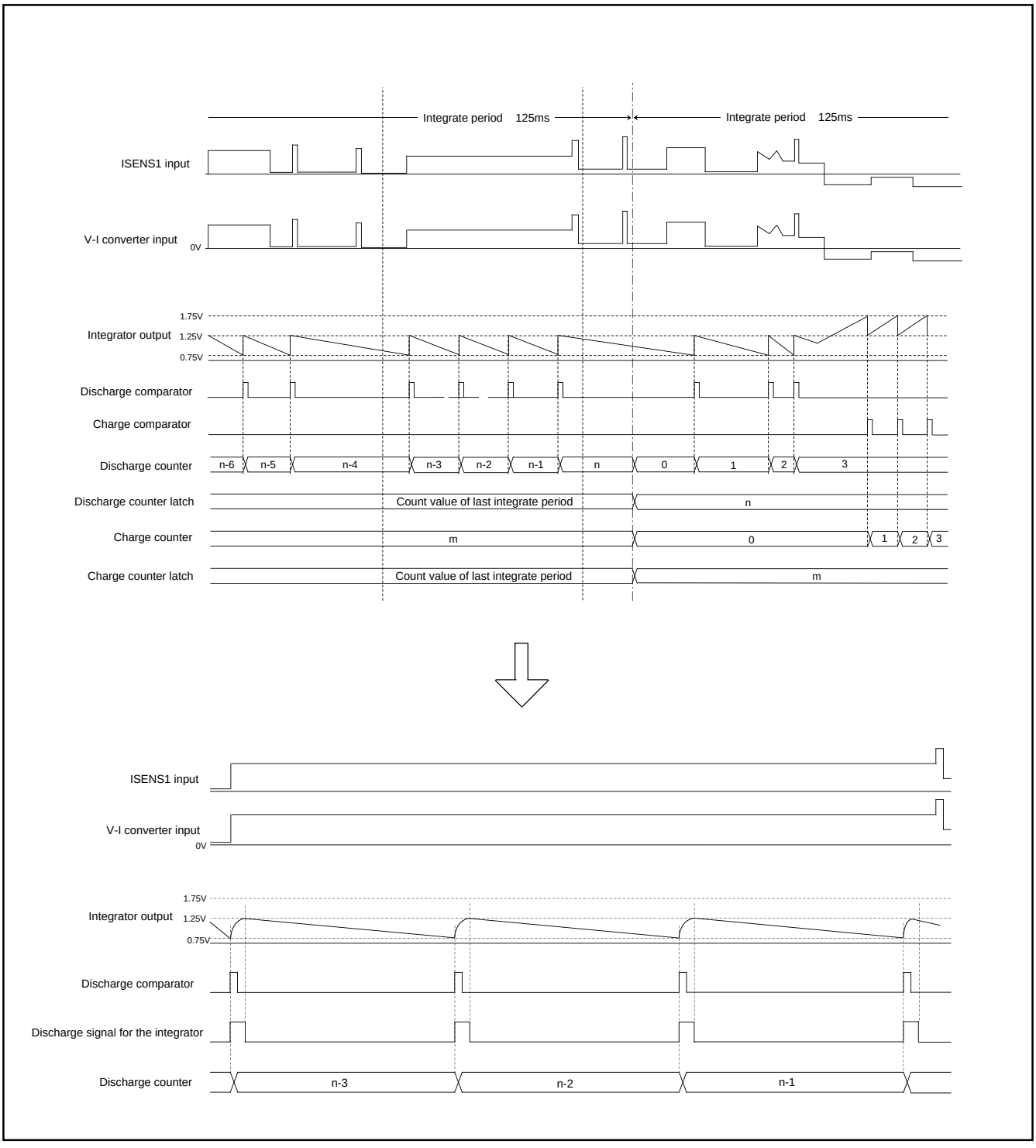


Fig. 48 Current integrator timing diagram

Calibration Mode

Setting the current integrate mode bit “1”, the input of V-I converter is connected to internal AVSS or 0.05V or 0.1V for reference voltage. When the calibration selection bit is “00”, both of plus and minus input of V-I converter are connected to internal AVSS, and zero calibration is operated. When the calibration selection bit is “01”, plus input of V-I converter is connected to internal 0.05V or 0.1V reference voltage, and minus input of V-I converter is connected to internal AVSS, and then full calibration for discharge state is operated. When the calibration selection bit is “10”, plus input of V-I converter is connected to internal AVSS, and minus input of V-I converter is connected to 0.05V or 0.1V reference voltage, and the full calibration for charge state is operated.

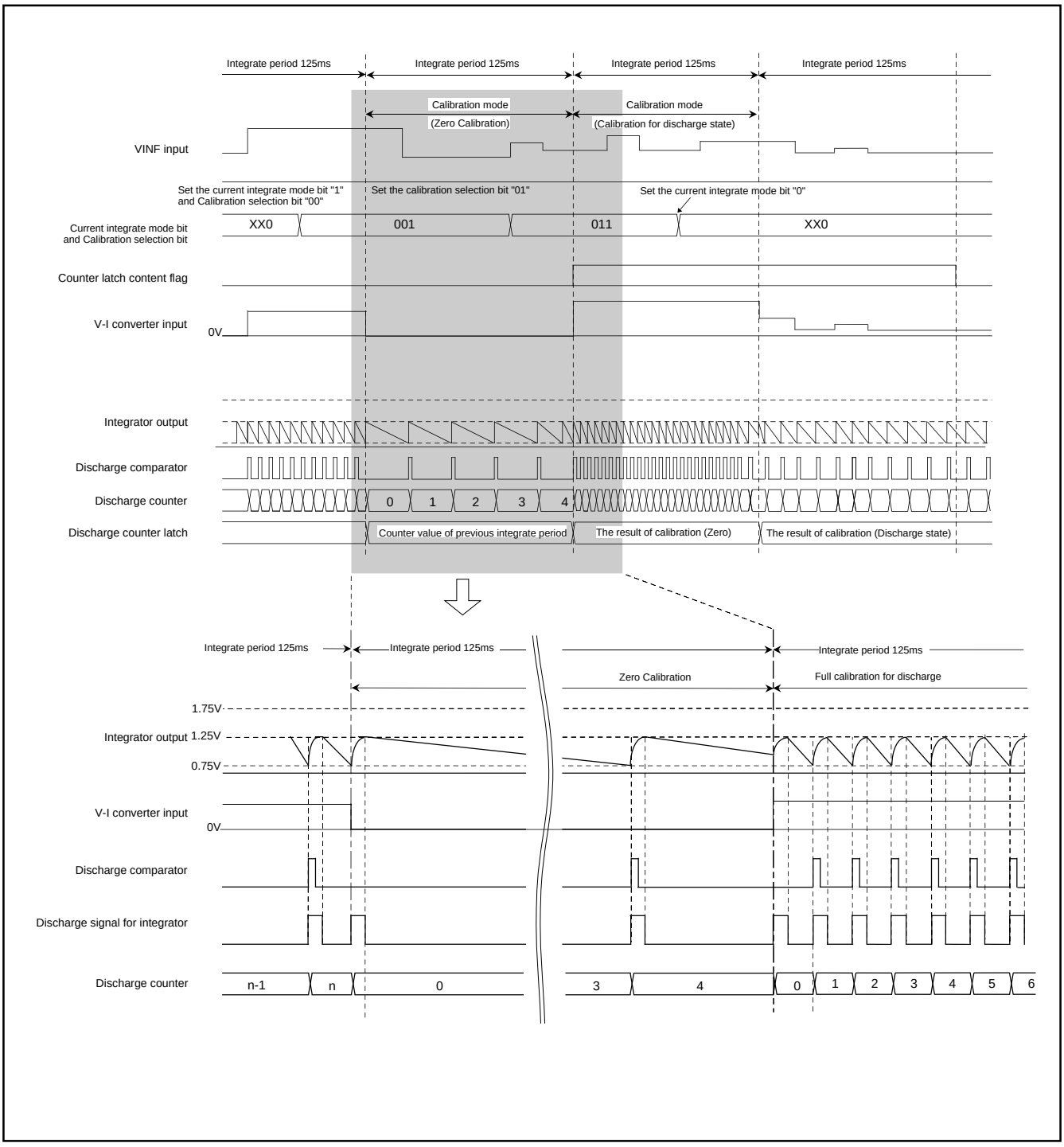


Fig. 49 Calibration timing

The calibration starts current integration for 125 ms, after discharging electric charge which remain in integrator's capacitor. After finished calibration period, value of the discharge(charge) counter is latched to discharge(charge) counter latch. At this time the current integrate interrupt occurs. Which interrupt has occurred current integrate interrupt for current integrate mode or for calibration mode can be judged by reading the counter latch content flag. The counter latch content flag shows the contents of counter latch, value for current integrate mode or value for calibration mode. Note that the contents of the counter latch is updated automatically at the end of next current integration or calibration.
The calibration mode is continued until setting the current integrate mode bit "0".

■Note on using current integrate circuit

Just after setting the current integrate mode bit "1", discharge or charge counter may count up one in surplus, in the first integrate period, because of internal analog circuit still doesn't become stable in the first integrate period. This cause increase of one count on counting up counter or stopping counter in the first integrate period.

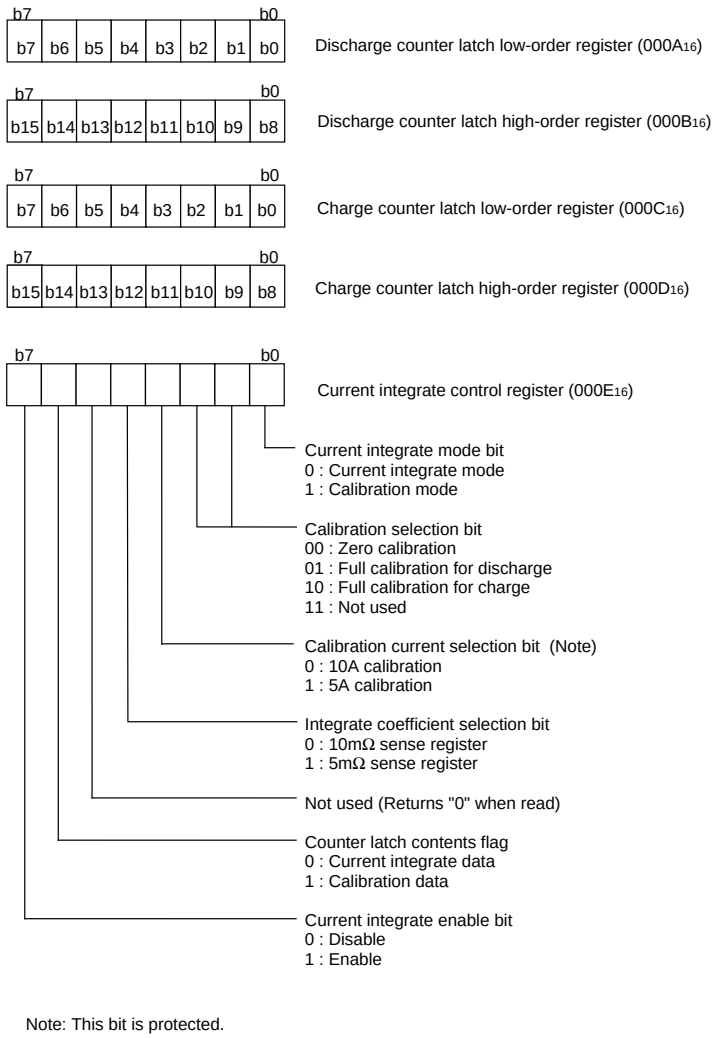


Fig. 50 Current integrator registers

OVER CURRENT DETECTOR

Over current detector detects the over current which flows through the sense resistor connected between ISENS1 pin and ISENS0 pin, and turn off the discharge control FET to stop battery from discharging or charging. In the low power state, and when current integrator disables, wake up current detector which detects approximate 1mA current and generates the interrupt is also built-in.

Discharge Short Current Detector

Discharge short current detector detects the discharge short current(10A-47.5A) with 10mΩ sense resistor. Setting discharge short current detect enable bit of the discharge short current detect control register($000F_{16}$) “1”, discharge short current detector starts the operation. The compare voltage is determined by setting the discharge short current detect voltage select bit of the discharge short current detect control register, and the detect time is determined by setting the discharge short current detect time set up bit of the current detect time set up register 1(0011_{16}).

The potential difference between sense resistor exceeds the compare voltage and continue more than detect time, then discharge short current detect flag(bit 2 of 0013_{16}) becomes “1”, and discharge short current detect interrupt occurs.

Enabling interrupt for discharge short current detect is determined by discharge short current interrupt enable bit(bit 4 of $000F_{16}$). And in case of the FET control enable bit is “1”, The FET control signal is generated from DFETCNT pin with discharge short current interrupt. The polarity of the FET control signal is determined by setting the discharge FET control polarity switch bit(bit 5 of $000F_{16}$).

Setting the discharge short current detect restart bit(bit 6 of 0013_{16}) “1” makes the discharge short current detect state clear.

Discharge Over Current Detector

Discharge over current detector detects the discharge over current(5A-20.5A) with 10mΩ sense resistor. Setting discharge over current detect enable bit of the discharge over current detect control register(0010_{16}) “1”, discharge over current detector starts the operation. The compare voltage is determined by setting the discharge over current detect voltage select bit of the discharge over current detect control register(0010_{16}), and the detect time is determined by setting the discharge over current detect time set up bit of the current detect time set up register 1(0011_{16}).

The potential difference between sense resistor exceeds the compare voltage and continue more than detect time, then discharge over current detect flag(bit 1 of 0013_{16}) becomes “1”, and discharge over current detect interrupt occurs.

Enabling interrupt for discharge over current detect is determined by discharge over current interrupt enable bit. And in case of the discharge FET control enable bit is “1”, the FET control signal is generated from DFETCNT pin with discharge over current interrupt.

Setting the discharge overt current detect restart bit(bit5 of 0013_{16}) “1” makes the discharge over current detect state clear.

Wake Up Current Detector

Wake up current detector detects approximate 1A current with 10mΩ sense resistor. Setting wake up current detect enable bit of the wake up current detect control register 1(0012_{16}) “1”, wake up current detector starts the operation. The sensing voltage is 10 times amplified and compared by the comparator. The comparator is comparing every 3.9msec, and more than 1A current is keeping for about 62msec, wake up current detect flag(bit 0 of 0013_{16}) becomes “1”, and the wake up current detect interrupt occurs. The enabling interrupt for wake up current detect is determined by wake up current detect interrupt enable bit(bit6 of 0012_{16}). Setting the wake up current detect restart bit “1” makes the wake up current detect state clear.

The offset calibration of the amplifier and comparator is able to be adjusted by setting the wake up current compare voltage select bit. Setting the wake up current detect calibration enable bit(bit5 of 0014_{16}) “1”, calibration mode starts. In the calibration mode, input of level shift circuit is connected to internal GND, and it is possible to measure the comparator threshold voltage at 0V input state, with setting wake up current detect compare voltage select bit. Then set the wake up current detect compare voltage select bit the value which is added comparator threshold voltage at 0V state and 0.1V(1A worth voltage).

Charge Over Current Detector

Charge over current detector detects the charge over current (10A-25A) with 10mΩ sense resister. Setting charge over current detect enable bit of the charge over current detect control register ($0FF0_{16}$) "1", charge over current detector starts the operation. The compare voltage is determined by setting the charge over current detect voltage select bit of the charge over current detect control register ($0FF0_{16}$), and the detect time is determined by setting the charge over current detect time set up bit of the current detect time set up register 2 ($0FF1_{16}$).

The potential difference between sense resister exceeds the compare voltage and continue more than detect time, then charge over current detect flag (bit 3 of 0013_{16}) becomes "1", and charge over current detect interrupt occurs.

Enabling interrupt for charge over current detect is determined by charge over current interrupt enable bit. And in case of the charge FET control enable bit is "1", the charge FET control signal is generated from CFETCNT pin with charge over current interrupt. The polarity of the FET control signal is determined by setting the charge FET control polarity switch bit (bit 5 of $0FF0_{16}$).

Setting the charge over current detect restart bit (bit 7 of 0013_{16}) "1" makes the charge over current detect state clear.

SFR Protect Control Register

SFR protect control register(0029_{16}), bit of MISRG2 (0037_{16}) and bit4,5 of MISRG (0038_{16}) protect SFR from changing the contents easily cause of like microcomputer runs away.

When the bit of SFR protect control register bit of MISRG2, bit 4,5 of MISRG is “0”, corresponded bit register is protected. Writing to the protected register, write “1” to the corresponded bit of protect register, then write the protected register in succession. If other register is written, the contents of SFR protect register is cleared “00”.

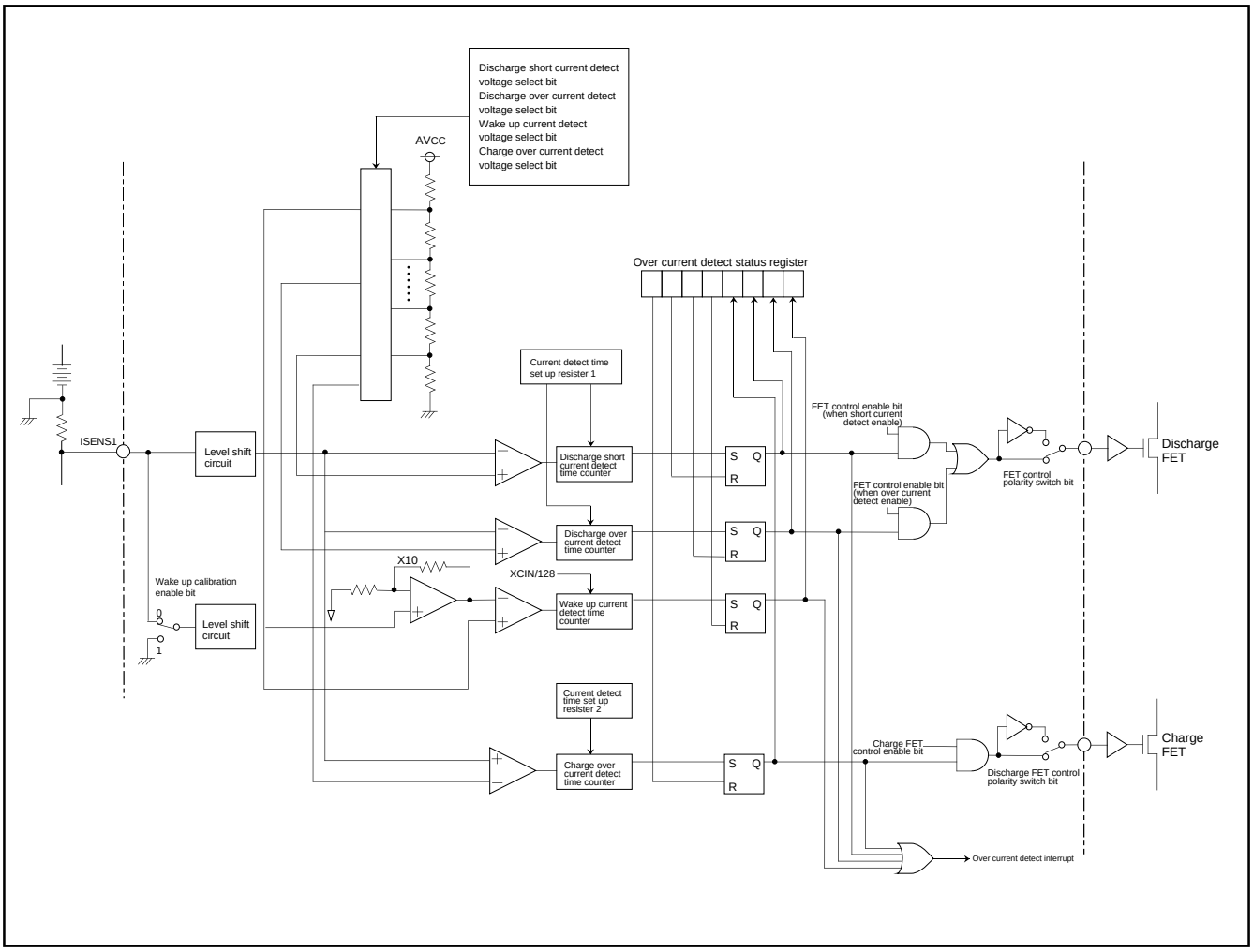


Fig. 51 Block diagram of Over current detector

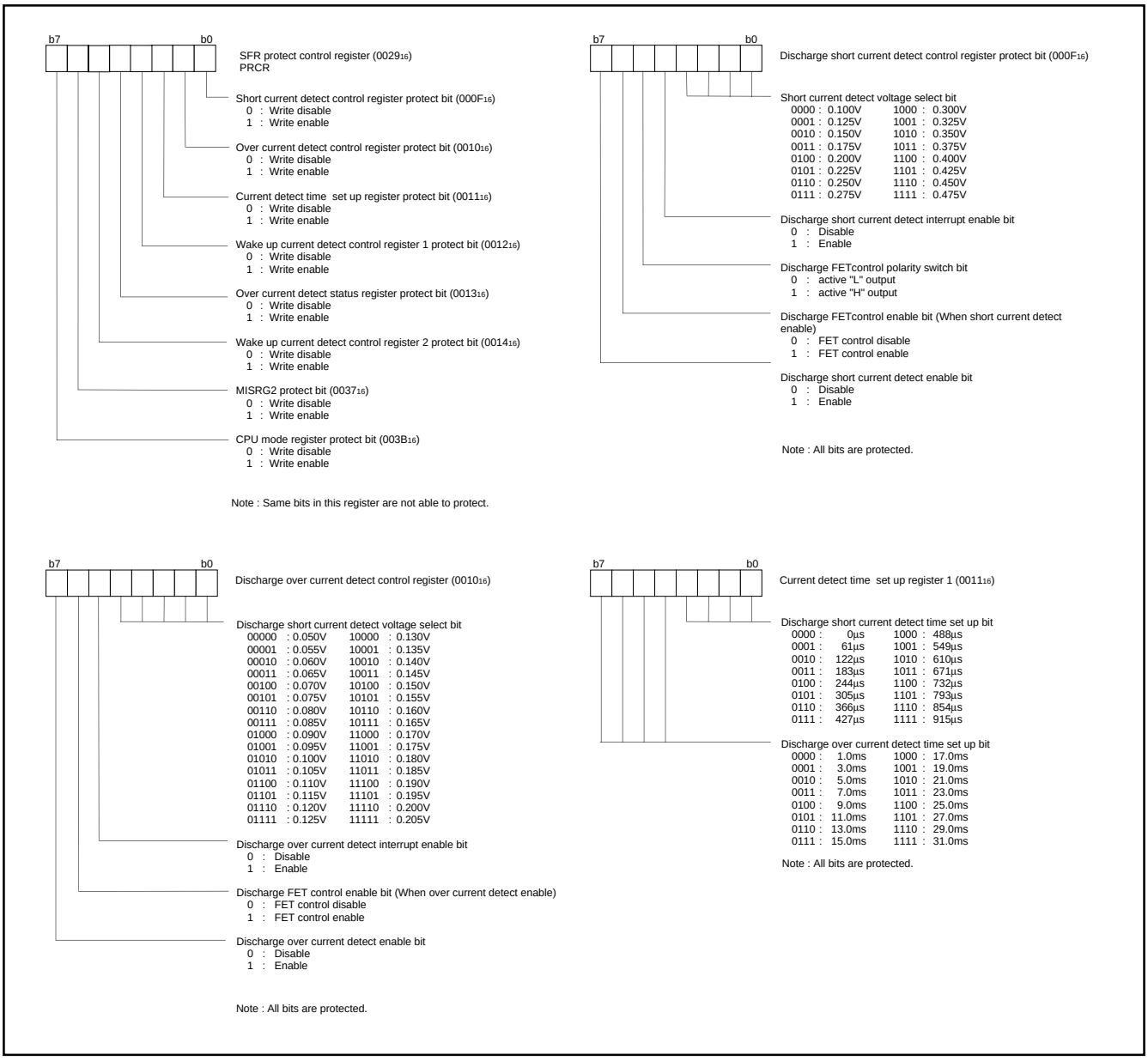


Fig. 52 Over current detector registers (1)

b7 b0

Wake up current detect control register 1 (0012$_{16}$)

Wake up current detect compare voltage select bit

Wake up current detect compare voltage select bit n						compare voltage (V)
b5	b4	b3	b2	b1	b0	
0	0	X	X	X	X	Setting disabled
0	1	0	0	0	0	1.04
0	1	0	0	0	1	1.05
0	1	0	0	1	0	1.06
0	1	0	0	1	1	1.07
⋮	⋮	⋮	⋮	⋮	⋮	0.01n+0.88
1	1	1	1	0	0	1.48
1	1	1	1	0	1	1.49
1	1	1	1	1	0	1.50
1	1	1	1	1	1	1.51

Wake up current detect interrupt enable bit
0 : Disable
1 : Enable

Wake up current detect enable bit
0 : Disable
1 : Enable

Note : All bits are protected.

b7 b0

Over current detect status register(0013$_{16}$)

Wake up current detect flag
0 : Not detected
1 : Detected

Discharge over current detect flag
0 : Not detected
1 : Detected

Discharge over current detect flag
0 : Not detected
1 : Detected

Charge over current detect flag
0 : Not detected
1 : Detected

Wake up current detect restart bit
0 : Invalid
1 : Restart

Discharge over current detect restart bit
0 : Invalid
1 : Restart

Discharge short current detect restart bit
0 : Invalid
1 : Restart

Charge over current detect restart bit
0 : Invalid
1 : Restart

Note : All bits are protected.

b7 b0

Wake up current detect control register 2 (0014$_{16}$)

Reserved (Do not write "1"to this bit)

Not used (returns "0" when read)

Wake up calibration enable bit
0 : Disable
1 : Enable

Reserved (Do not write "1"to this bit)

Not used (returns "0" when read)

Note : All bits are protected.

b7 b0

Charge over current detect control register (0FF0$_{16}$)

Charge over current detect voltage select bit

0000	: 0.025V	1000	: 0.065V
0001	: 0.030V	1001	: 0.070V
0010	: 0.035V	1010	: 0.075V
0011	: 0.040V	1011	: 0.080V
0100	: 0.045V	1100	: 0.085V
0101	: 0.050V	1101	: 0.090V
0110	: 0.055V	1110	: 0.095V
0111	: 0.060V	1111	: 0.100V

Charge over current detect interrupt enable bit
0 : Disable
1 : Enable

Charge FET control polarity switch bit
0 : Active "L" output
1 : Active "H" output

Charge FET control enable bit
0 : FET control disable
1 : FET control enable

Charge over current detect enable bit
0 : Disable
1 : Enable

Note : All bits are protected.
The SFR protect bit control bit is in MISRG register (address 0038$_{16}$).

b7 b0

Current detect time set up register 2 (0FF1$_{16}$)

Charge over current detect time set up bit

0000	: 1.0ms	1000	: 17.0ms
0001	: 3.0ms	1001	: 19.0ms
0010	: 5.0ms	1010	: 21.0ms
0011	: 7.0ms	1011	: 23.0ms
0100	: 9.0ms	1100	: 25.0ms
0101	: 11.0ms	1101	: 27.0ms
0110	: 13.0ms	1110	: 29.0ms
0111	: 15.0ms	1111	: 31.0ms

DFETCNT-INT$_2$ OR output enable bit
0 : Disable
1 : Enable

INT$_2$ polarity switch bit
0 : invert
1 : not invert

CFETCNT-INT$_3$ OR output enable bit
0 : Disable
1 : Enable

INT$_3$ polarity switch bit
0 : invert
1 : not invert

Note : All bits are protected.
The SFR protect bit control bit is in MISRG register (address 0038$_{16}$).

Fig. 53 Over current detector registers (2)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039$_{16}$) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039$_{16}$) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039$_{16}$) may be started before an underflow. When the watchdog timer control register (address 0039$_{16}$) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

●Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039$_{16}$), each watchdog timer H and L is set to "FF$_{16}$".

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039$_{16}$) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 262.144 ms at f(XIN) = 4 MHz frequency and 32.768 s at f(XCIN) = 32 kHz frequency.

When this bit is set to "1", the count source becomes the signal divided by 16 for f(XIN) (or f(XCIN)). The detection time in this case is set to 1024 µs at f(XIN) = 4 MHz frequency and 128 ms at f(XCIN) = 32 kHz frequency. This bit is cleared to "0" after resetting.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039$_{16}$) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.

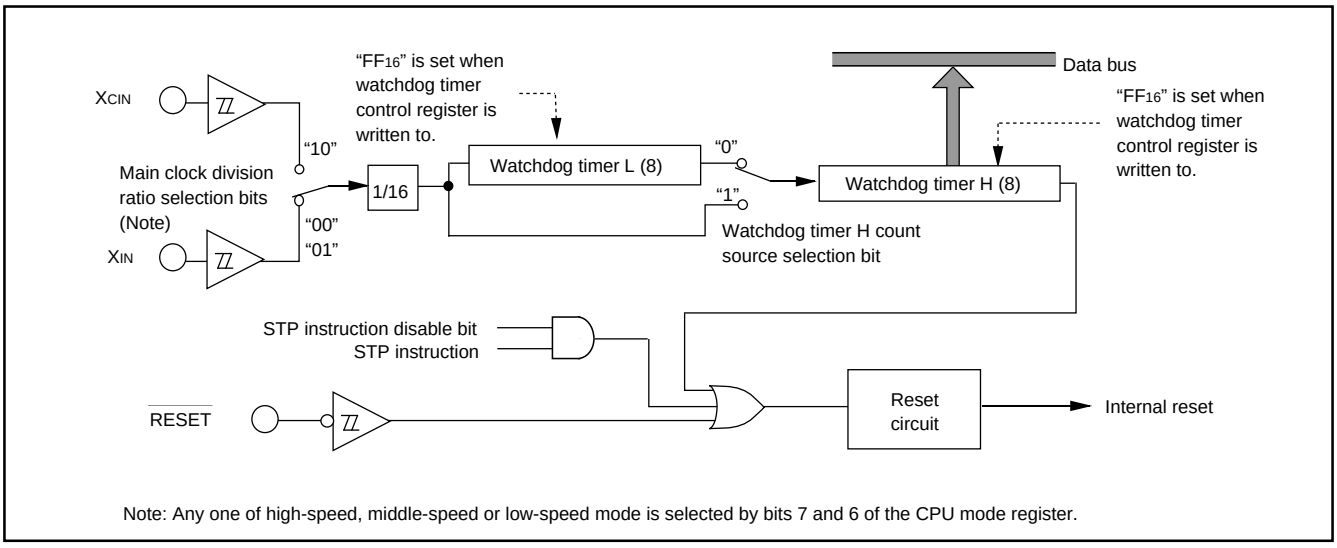


Fig. 54 Block diagram of Watchdog timer

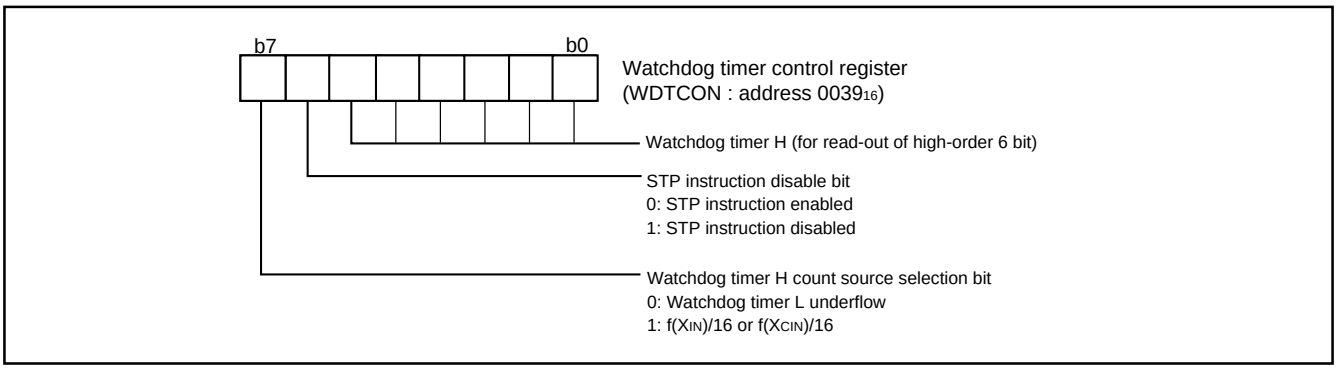


Fig. 55 Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin must be held at an "L" level for 20 X_{IN} cycles or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage must be between 2.45 V and 2.55 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.49 V for V_{CC} of 2.45 V.

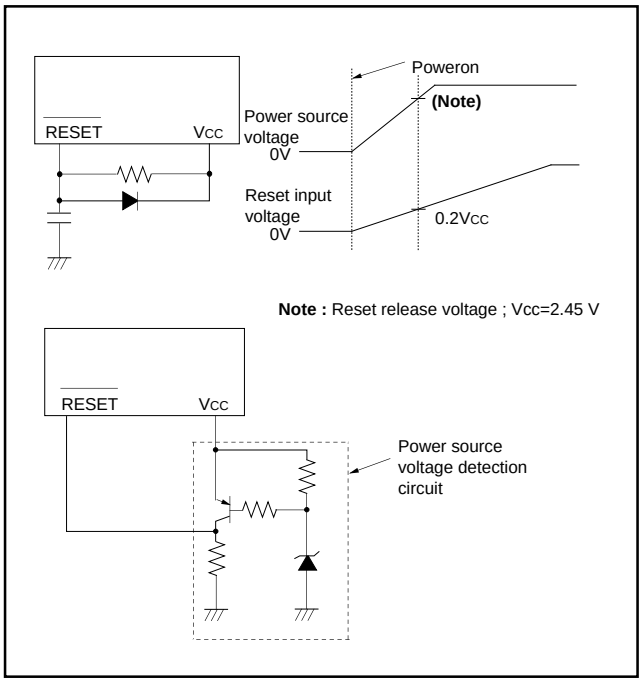


Fig. 56 Reset circuit example

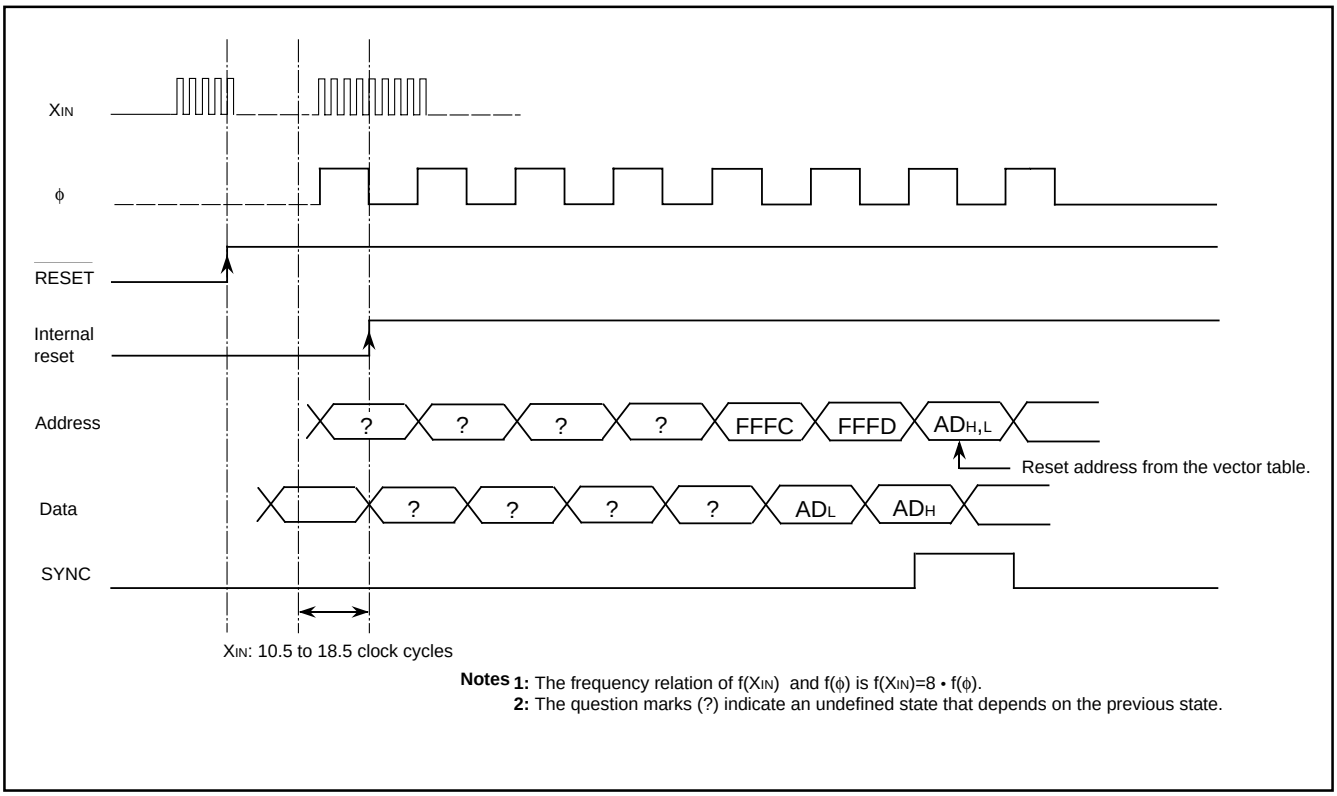


Fig. 57 Reset sequence

		Address	Register contents
(1)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(2)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(3)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(4)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(5)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(6)	Discharge counter latch low-order register (DCHARGEL)	$000A_{16}$	00_{16}
(7)	Discharge counter latch high-order register (DCHARGEH)	$000B_{16}$	00_{16}
(8)	Charge counter latch low-order register (CHARGEL)	$000C_{16}$	00_{16}
(9)	Charge counter latch high-order register (CHARGEH)	$000D_{16}$	00_{16}
(10)	Current integrator control register (CINFCON)	$000E_{16}$	00_{16}
(11)	Discharge short current detector control register (DSCDCON)	$000F_{16}$	00_{16}
(12)	Discharge over current detector control register (DOCDCON)	0010_{16}	00_{16}
(13)	Current detect time set up register 1 (OCDTIME1)	0011_{16}	00_{16}
(14)	Wake up current detector control register 1 (WDDCON1)	0012_{16}	00_{16}
(15)	Over current detect status register (OCDSTS)	0013_{16}	00_{16}
(16)	Wake up current detector control register 2 (WDDCON2)	0014_{16}	00_{16}
(17)	Serial I/O2 control register 1 (SI02CON1)	0015_{16}	00_{16}
(18)	Serial I/O2 control register 2 (SI02CON2)	0016_{16}	0 0 X 0 0 1 1 1
(19)	Serial I/O status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(20)	Serial I/O control register (SIOCON)	$001A_{16}$	00_{16}
(21)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(22)	PWM control register (PWMCON)	$001D_{16}$	00_{16}
(23)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(24)	Timer 1 (T1)	0021_{16}	01_{16}
(25)	Timer 2 (T2)	0022_{16}	00_{16}
(26)	Timer XY mode register (TM)	0023_{16}	00_{16}
(27)	Prescaler X (PREX)	0024_{16}	FF_{16}
(28)	Timer X (TX)	0025_{16}	FF_{16}
(29)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(30)	Timer Y (TY)	0027_{16}	FF_{16}
(31)	Timer count source select register (TCSS)	0028_{16}	00_{16}

		Address	Register contents
(32)	SFR protect control register (PRREG)	0029_{16}	00_{16}
(33)	I^2C address register (S0D)	$002C_{16}$	00_{16}
(34)	I^2C status register (S1)	$002D_{16}$	0 0 0 1 0 0 0 X
(35)	I^2C control register (S1D)	$002E_{16}$	00_{16}
(36)	I^2C clock control register (S2)	$002F_{16}$	00_{16}
(37)	I^2C start/stop condition control register (S2D)	0030_{16}	0 0 0 X X X X X
(38)	I^2C additional register (S3)	0031_{16}	00_{16}
(39)	32kHz oscillation circuit control register 0 (32KOSCC0)	0032_{16}	00_{16}
(40)	32kHz oscillation circuit control register 1 (32KOSCC1)	0033_{16}	00_{16}
(41)	AD control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(42)	MISRG2	0037_{16}	00_{16}
(43)	MISRG	0038_{16}	00_{16}
(44)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(45)	Interrupt edge selection register 1 (INTEDGE1)	$003A_{16}$	00_{16}
(46)	CPU mode register (CPUM)	$003B_{16}$	0 1 1 0 0 0 0 0
(47)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(48)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(49)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(50)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(51)	Flash memory control register 0 (FMCR0)	$0FE0_{16}$	0 0 0 0 0 0 0 1
(52)	Flash memory control register 1 (FMCR1)	$0FE1_{16}$	0 1 0 0 0 0 0 0
(53)	Flash memory control register 2 (FMCR2)	$0FE2_{16}$	00_{16}
(54)	Charge over current detect control register (COCDCON)	$0FF0_{16}$	00_{16}
(55)	Current detect time set up register 2 (OCDTIME2)	$0FF1_{16}$	00_{16}
(56)	High-speed RC oscillator frequency set up register (O4RCFRG)	$0FF2_{16}$	AB_{16}
(57)	High-speed RC oscillator control register (O4RCCOT)	$0FF4_{16}$	0 0 0 0 0 0 0 X
(58)	Interrupt edge selection register 2 (INTEDGE2)	$0FF5_{16}$	00_{16}
(59)	Processor status register	(PS)	X X X X X 1 X X
(60)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X indicates Not fixed .

Fig. 58 Internal status at reset

CLOCK GENERATING CIRCUIT

The 7512Group has four built-in oscillation circuits. Built-in oscillation circuit about 4MHz oscillation, or an oscillation circuit can be formed by connecting a resonator between XIN and XOUT for high speed oscillation, and an oscillation circuit can be formed by connecting capacitor and resistor, or resonator between XCIN and XCOUT for low speed oscillation. The oscillation source (built-in oscillation or XIN-XOUT oscillation) can be controlled by setting clock source switch bit (CPU mode register) and high-speed RC oscillation stop bit (MISRG2) and XIN switching inhibit bit(MISREG2). Immediately after power on, only the built-in oscillation circuit starts oscillation. In case of using XIN-XOUT oscillation circuit, change the clock source bit after start the XIN-XOUT oscillation setting the main clock (XIN -XOUT) stop bit (CPU mode register).

In case of not using XIN -XOUT oscillation circuit, XIN pin and XOUT pin must be open.

Setting the XIN switching inhibit bit "1" (disable switch to XIN), clock source switch bit become invalid, and XIN-XOUT oscillation circuit becomes disabled since. When this bit is set to "1", it cannot be rewritten to "0" by program.

Setting the port Xc switch bit (CPU mode register) "1", 32kHz RC oscillation circuit or XCIN-XCOUT oscillation circuit starts oscillation. The selection of 32kHz RC oscillation circuit or XCIN-XCOUT oscillation circuit is selected by 32kHz RC oscillation enable bit (MISRG2).

In case of using external resonator, connect resonator to XIN pin and XOUT pin (XCIN pin and XCOUT pin). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip.(An external feed-back resistor may be needed depending on conditions.) However, an external feed-back resistor is needed between XCIN and XCOUT.

After reset, XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of high-speed RC oscillation clock or XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of high-speed RC oscillation clock or XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3•f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

32kHz RC oscillation circuit

Setting the port Xc switch bit "1" after setting the 32kHz RC oscillation enable bit "1", the built-in 32kHz RC oscillation circuit starts oscillation. In case of using 32kHz RC oscillation circuit, connect 91kΩ resistor between XCIN-XCOUT, and connect 100pF capacitor between XCIN and GND.

Setting appropriate value to the 32kHz oscillation circuit control register0,1 it is possible to adjust the frequency error cause by evenness of resistor and capacitor value .

The resistor ladder divided by 512 adjusts the frequency, and it makes possible about 50Hz step adjustment.

The theoretical frequency is calculated as follow.

$$f_{32KRC} = \frac{1}{2RCln(1+2R_1/R_2)}$$

Calibration for High-speed RC oscillation circuit

Setting the high-speed RC oscillation circuit calibration enable bit "1", built-in counter starts count the clock which is divided the frequency of the high-speed RC oscillation output by 1/2 for four cycles period of 32kHz RC oscillation clock, and high-speed RC oscillation frequency can be measured.

The built-in counter is 9bit counter and lower 8bit count value is stored in the high-speed RC oscillation circuit frequency counter ($0FF3_{16}$) and higher 1bit is stored in bit 0 of high-speed RC oscillation circuit control register ($0FF4_{16}$).

Renewing the high-speed RC oscillation frequency set up register ($0FF2_{16}$), oscillation frequency is altered. High-speed RC oscillation circuit frequency may change cause of change of VCC or operating, temperature, but adjusting the high-speed oscillation frequency set up register by software, oscillating frequency can be kept fixed.

After power on, built-in high-speed RC oscillation starts the oscillation at about 4MHz.

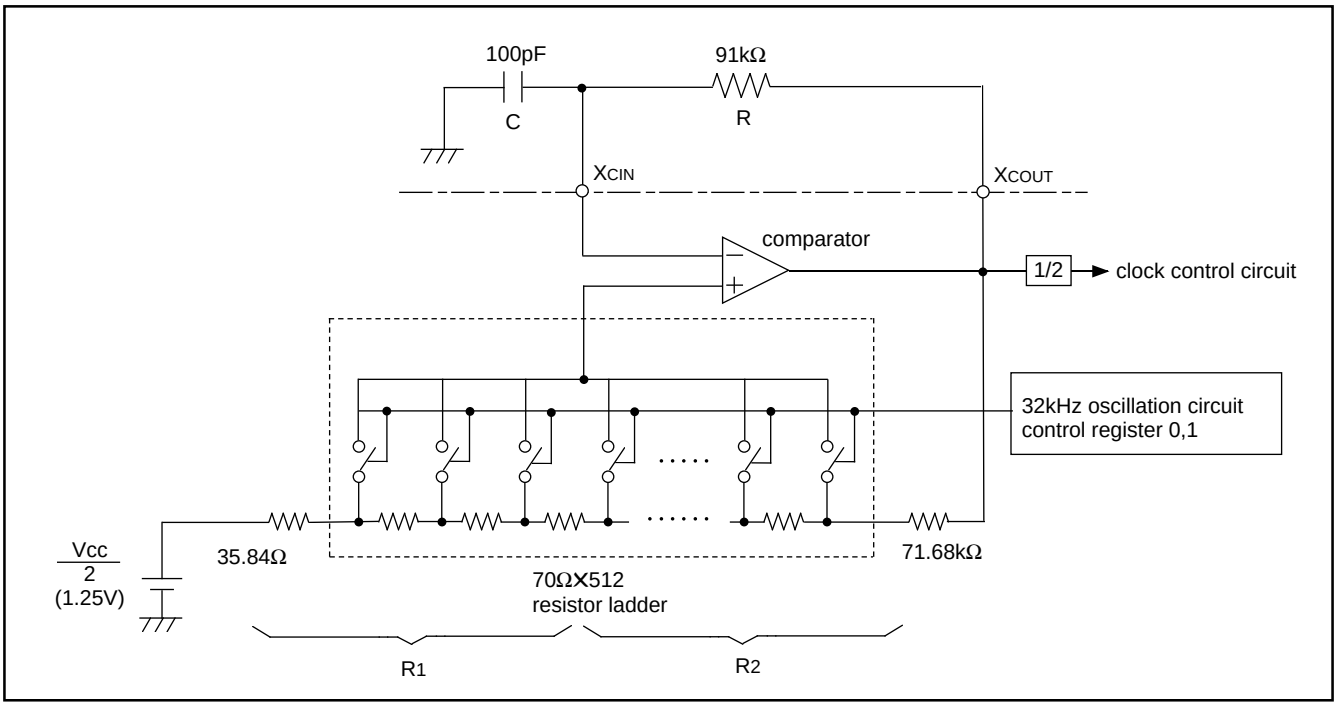


Fig. 59 Block diagram of 32kHz RC oscillation circuit

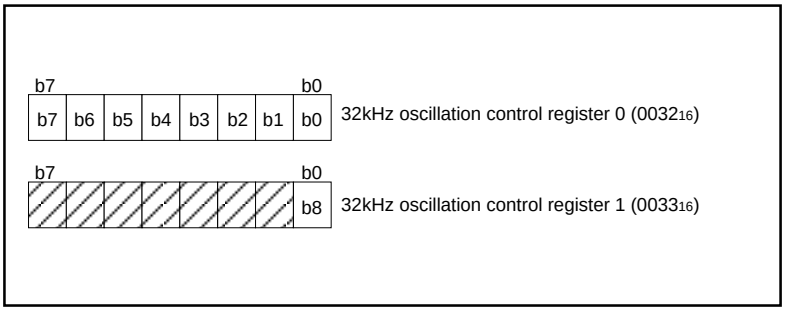
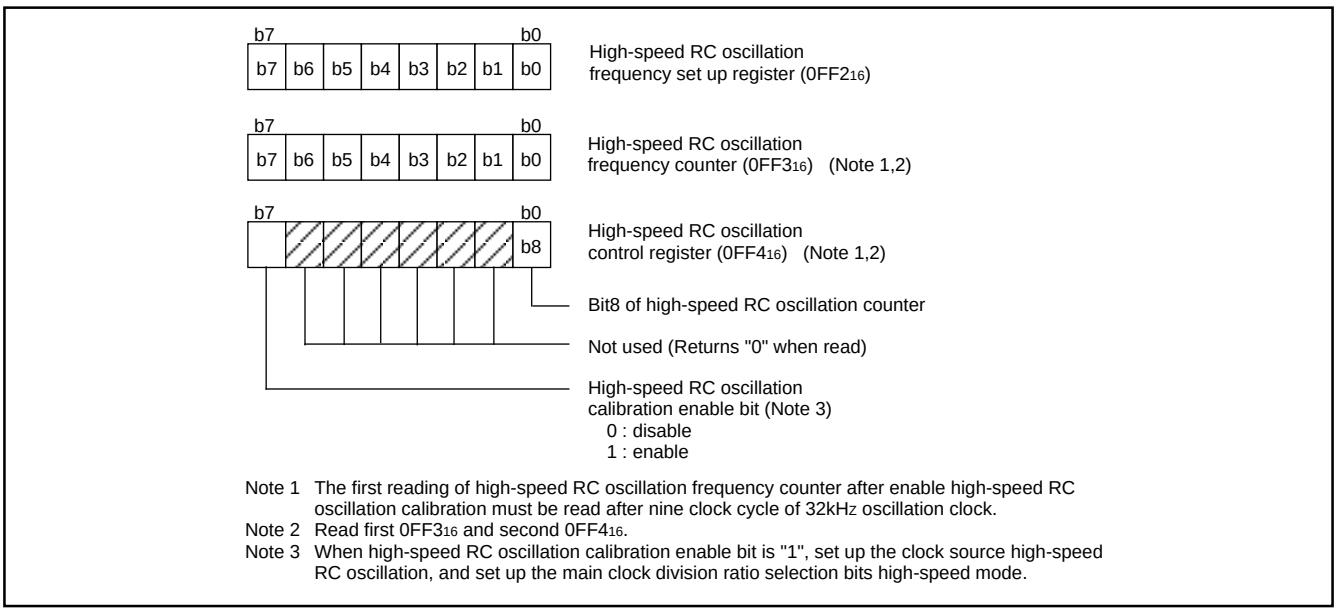


Fig. 60 32kHz oscillation control register



Note 1 The first reading of high-speed RC oscillation frequency counter after enable high-speed RC oscillation calibration must be read after nine clock cycle of 32kHz oscillation clock.
Note 2 Read first 0FF3₁₆ and second 0FF4₁₆.
Note 3 When high-speed RC oscillation calibration enable bit is "1", set up the clock source high-speed RC oscillation, and set up the main clock division ratio selection bits high-speed mode.

Fig. 61 High-speed RC oscillation register

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and high-speed RC oscillation or XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit is "0", the prescaler 12 is set to "FF16" and timer 1 is set to "0116". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

Either high-speed RC oscillation, XIN or XCIN divided by 16 is input to the prescaler 12 as count source. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

In case of using high-speed RC oscillation circuit as main clock, the oscillation stabilizing time does not almost need.

(2) Wait mode

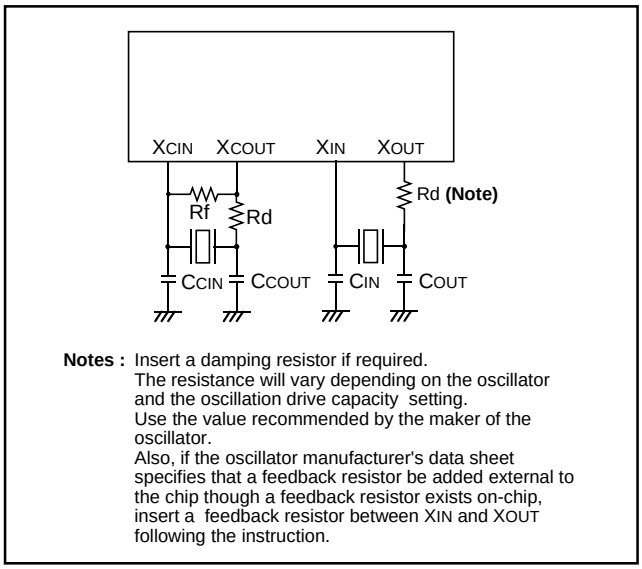
If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.

When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock high-speed RC oscillation, XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.



Notes : Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 62 Ceramic resonator circuit

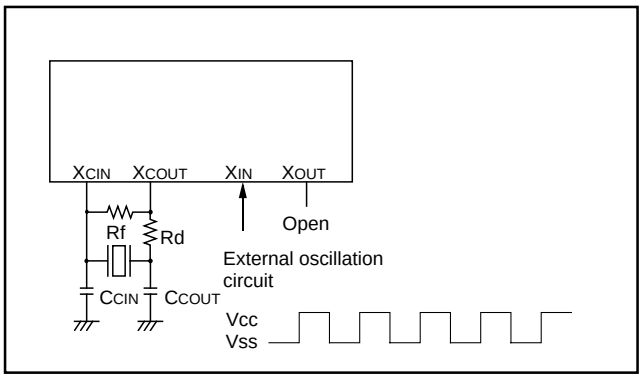


Fig. 63 External clock input circuit

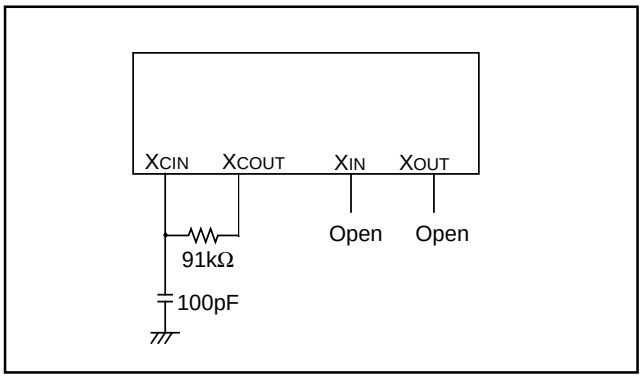
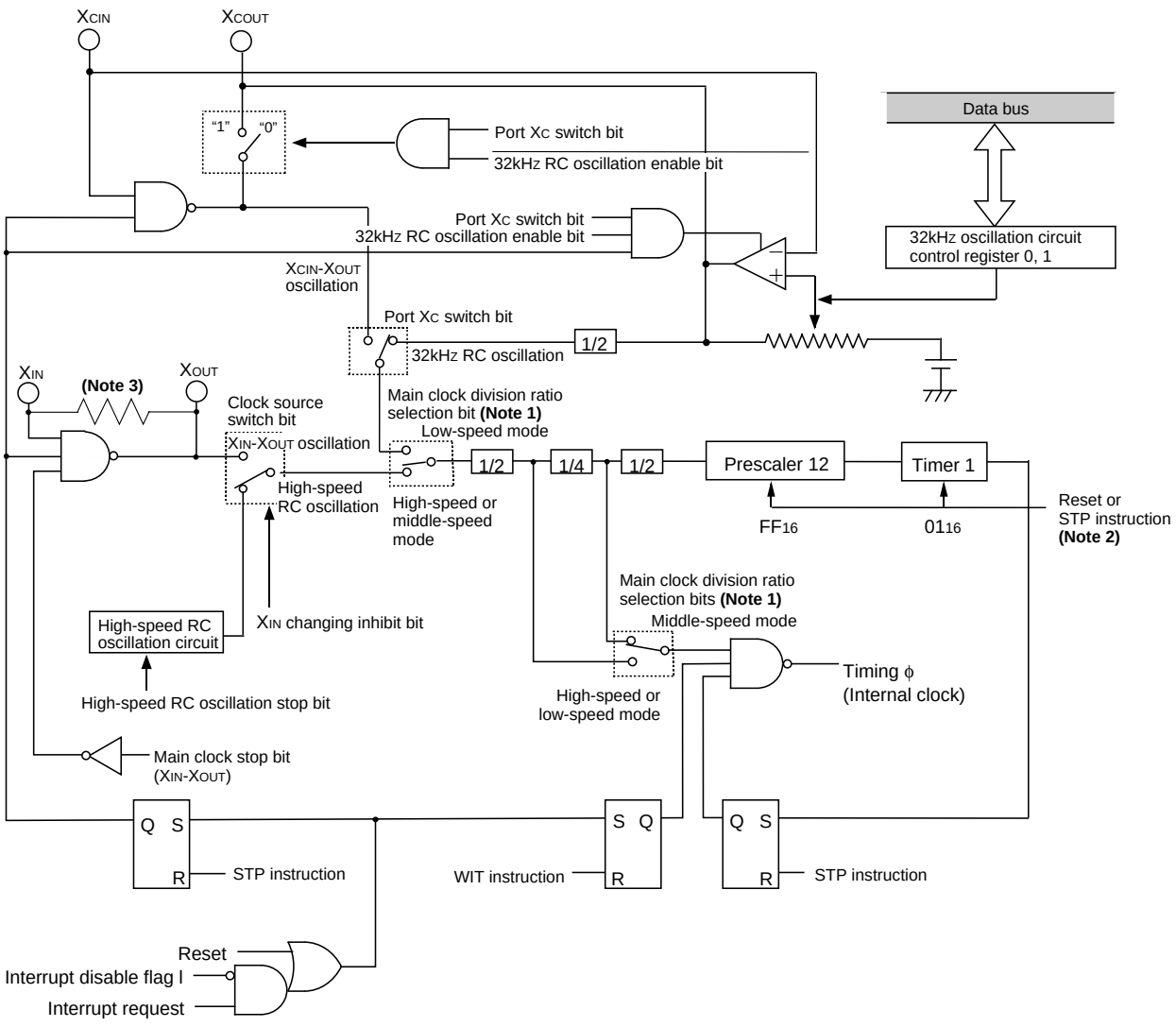


Fig. 64 High-speed RC oscillation circuit and 32kHz RC oscillation circuit

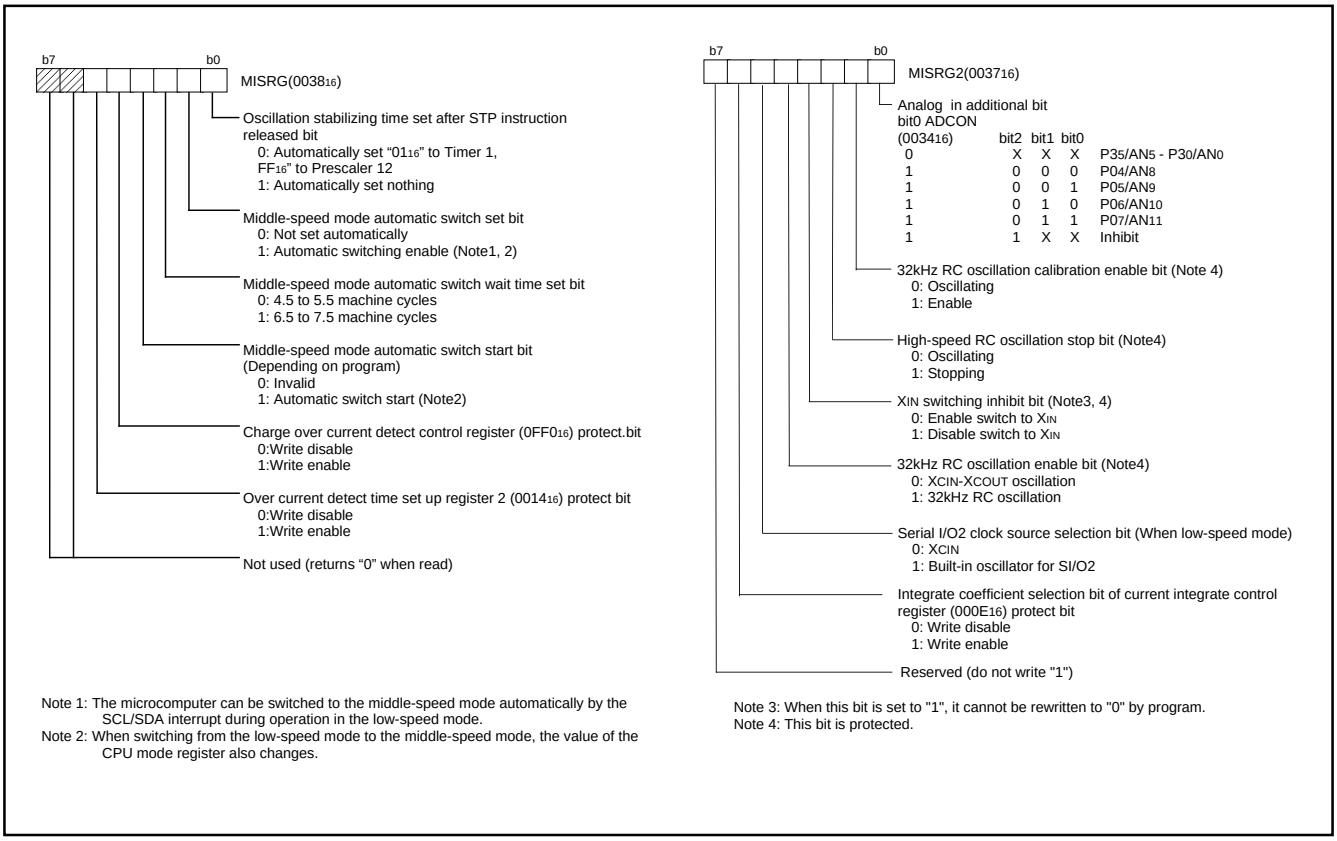


Note 1: Any one of high-speed mode, middle-speed mode or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b1) to "1".
2: When the oscillation stabilizing time set after STP instruction release bit is "0".
3: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 65 System clock generating circuit block diagram (Single-chip mode)

■Notes on middle-speed mode switch set bit

When the middle-speed mode automatic switch set bit is set to “1” during operation in the low-speed mode, XIN oscillation starts automatically by detecting the rising edge or the falling edge of the SCL pin or the SDA pin and the microcomputer switch to the middle-speed mode. Select the timing which switches from the low-speed mode to the middle-speed mode by the middle-speed mode automatic switch wait time set bit. The timing is selectable from 4.5 to 5.5 cycles or 6.5 to 7.5 cycles in the low-speed mode. Select according to the oscillation start characteristic of the oscillator of XIN to be used. By writing “1” in the middle-speed mode automatic switch start bit during operation in the low-speed mode, XIN oscillation starts automatically and the microcomputer changes to the middle-speed mode.



Note 1: The microcomputer can be switched to the middle-speed mode automatically by the SCL/SDA interrupt during operation in the low-speed mode.
Note 2: When switching from the low-speed mode to the middle-speed mode, the value of the CPU mode register also changes.

Note 3: When this bit is set to "1", it cannot be rewritten to "0" by program.
Note 4: This bit is protected.

Fig. 66 Structure of MISRG1, MISRG2

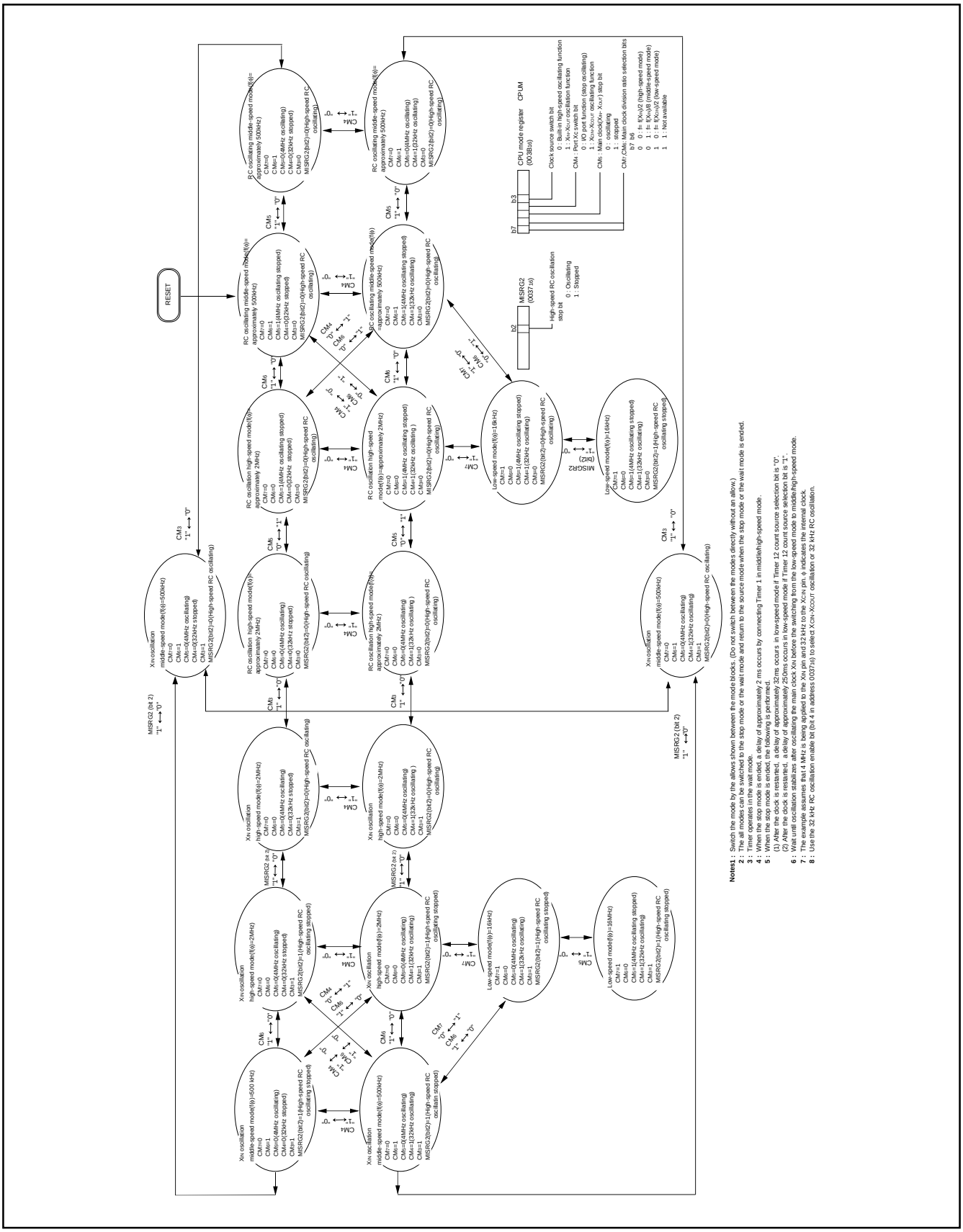


Fig. 67 State transitions of system clock

FLASH MEMORY MODE

The 7512 Group (flash memory version) has flash memory that can be rewritten with a single power source.

For this flash memory, two flash memory modes are available in which to read, program, and erase: the parallel I/O mode in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

Summary

Table 13 lists the summary of the 7512 Group (flash memory version).

The flash memory of the 7512 Group is divided into 4 blocks of User ROM area and Boot ROM area as shown in Figure 68.

In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a control program in a Boot mode. The user can write a rewrite control program in this Boot ROM area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Table 13 Summary of the 7512 Group (flash memory version)

Item		Specifications
Power source voltage		Vcc = 2.5V±2%
Program / Erase voltage		Vcc = 2.5V±2%
Flash memory mode		2 modes (Parallel I/O mode, CPU rewrite mode)
Erase block division	User ROM area	Refer to the Figure 68
	Boot ROM area	1 block (4K bytes) (**Note 1**)
Program method		Byte program
Erase method		Batch erasing
Program/Erase control method		Program/Erase control by software command
Number of commands		5 commands
Number of program/	Block 0 to Block 3	100 times
Erase times	Block A, Block B	1K times
ROM code protection		Available in parallel I/O mode

Note 1: This Boot ROM area can be rewritten in only parallel I/O mode.

(1) CPU Rewrite Mode

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).

In CPU rewrite mode, only the User ROM area shown in Figure 68 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.

The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area to be executed before it can be executed.

Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. See Figure 68 for details about the Boot ROM area.

Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVSS pin low. In this case, the CPU starts operating using the control program in the User ROM area.

When the microcomputer is reset by pulling the P24/SDA2/RXD pin high, the CNVss pin high, the CPU starts operating using the control program in the Boot ROM area (program start address is FFFC16, FFFD16 fixation). This mode is called the “Boot” mode.

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

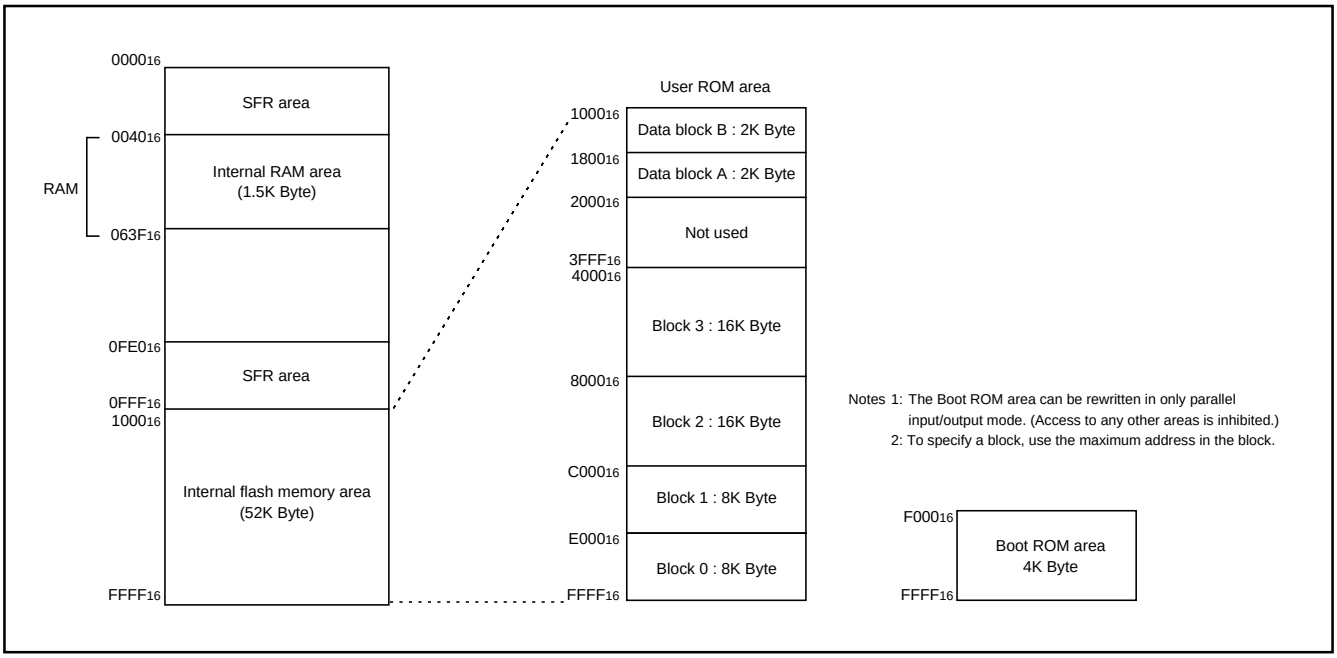


Fig. 68 Block diagram of built-in flash memory (M37512FCHP)

Table 14 The difference between EW0 mode and EW1 mode

Items	EW0 mode	EW1 mode
Processor mode	Single-chip mode	Single-chip mode
Program area for rewrite control program	User ROM area	User ROM area
Operating area for rewrite control program	Rewrite program in the flash memory area must be transfered from another area than flash memory area (ex. RAM area) and executed.	Rewrite program can be executed in the User ROM area. (Note 3)
Rewritable area	User ROM area	User ROM area except rewrite program existing block and interrupt vector area (Note 1)
Restriction of software command	Nothing	•Program, Block erase command Command execution for block existing rewrite program is prohibited. • Read status register command execution is prohibited
The mode after program or erase	Read status register mode	Read array mode
CPU status at program and erase state	Executing	Hold state (I/O port is kept the execution previous state.)
How to detect the flash memory status	•Read the RY/$\overline{BY}$ status flag, program status flag, erase status flag of the flash memory control register 0 on program. •Read the SR7, SR5, SR4 of the status register after execute the read status command	•Read the RY/$\overline{BY}$ status flag, program status flag, erase status flag of the flash memory control register 0 on program.
The condition for shift to erase suspend status (Note 2)	Write "1" to the erase suspend enable bit and erase suspend requirement bit of the flash memory control register on program.	Write "1" to the erase suspend enable bit of the flash memory control register 1 on program and then interrupt request which is enabled occurred.

Note 1 Write "1" to the 8KB userblock E/W prohibit bit of the flash memory control register 1, rewrite operation on block 0, block 1 is enabled.
Note 2 The enable time for reading flash memory after shifting to erase suspend status is max td(SR-ES).
Note 3 Do not execute rewrite program on RAM area. (Do not execute program on RAM area whether rewrite control program or application program.)

●EW0 mode

Setting "1" to CPU rewrite mode selection bit of flash memory control register 0, CPU rewrite mode starts, and software command becomes available. At this time, EW1 mode selection bit of the flash memory control register 1 becomes "0" (EW0 mode). For CPU rewrite mode select bit to be set to "1", it is necessary to write "0" and then "1" in succession.

Program or erase operation is controlled by software command. The state of program or erase end can be checked by reading the flash memory control register or status register.

In case of changing to the erase suspend mode during the erase operation, set the erase suspend enable bit to "1", and set the erase suspend request bit "1". And wait td(SR-ES). The user ROM area can be accessed after checking the erase suspend flag becomes "1". Setting the erase suspend request bit "0"(Erase restart), erase operation restarts.

●EW1 mode

Setting the EW1 mode selection bit "1" (write "0" and then "1" in succession) after setting the CPU rewrite mode selection bit "1" (write "0" and then "1" in succession), the EW1 mode starts.

The state of the program or erase end can be checked by reading the flash memory control register 0. Do not execute the software command of the read status register in the EW1 mode.

Changing the erase suspend function to effective state, execute the block erase command after setting erase suspend enable bit "1". And the interrupt which triggers off shifting to erase suspend state must be enabled. td(SR-ES) later after interrupt request, erase sequence shift to erase suspend state, and interrupt is accepted.

When the interrupt request occurs, erase suspend request bit becomes "1" automatically, and erase operation is suspended. In case of the erase operation is not completed (RY/BY status flag is "0") after interrupt routine ends, setting the erase suspend request bit "0", and execute the block erase command again.

Outline Performance (CPU Rewrite Mode)

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten in CPU rewrite mode.

In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory by executing software commands. This rewrite control program must be transferred to the RAM before it can be executed.

The MCU enters CPU rewrite mode by setting “1” to the CPU Rewrite Mode Select Bit (bit 1 of address $0FE0_{16}$). Software commands are accepted once the mode is entered.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 69 shows the flash memory control register 0.

Bit 0 is the RY/$\overline{BY}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is “0” (busy). Otherwise, it is “1” (ready).

Bit 1 is the CPU Rewrite Mode Select Bit. When this bit is set to “1”, the MCU enters CPU rewrite mode. Software commands are accepted once the mode is entered. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the RAM for write to bit 1. To set this bit to “1”, it is necessary to write “0” and then write “1” in succession. The bit can be set to “0” by only writing “0”.

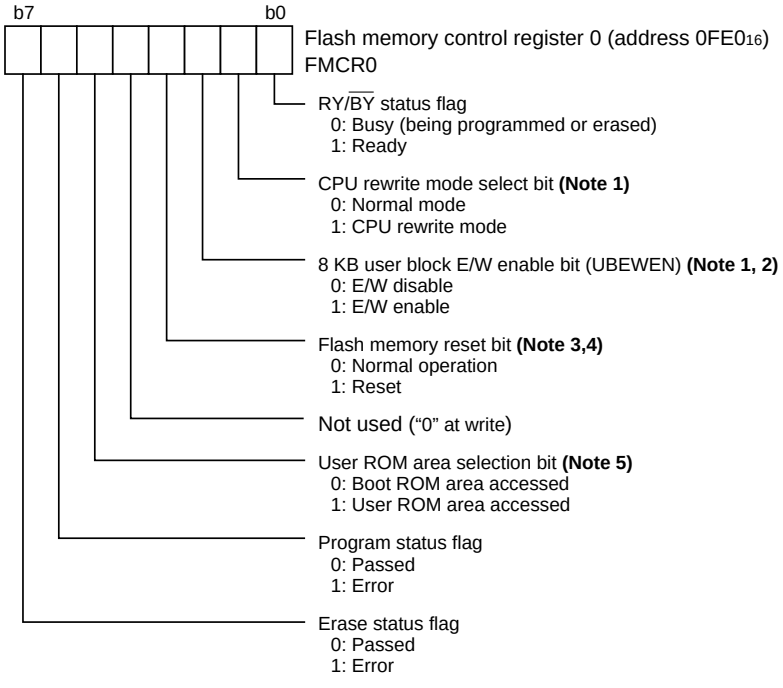
Bit 2 is 8KB user block E/W enable bit. Setting this bit and bit 4 (All user block E/W enable bit) of the flash memory control register 2 ($0FE2_{16}$) according to the table T-3, E/W protect is done at CPU Rewrite mode for User block

Bit 3 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU Rewrite Mode Select Bit is “1”, setting “1” for this bit resets the control circuit. To release the reset, it is necessary to set this bit to “0”.

Bit 5 is User ROM area selection bit, and this bit is only available in Boot mode. Setting this bit “1”, User ROM area can be accessed, and CPU rewrite is available.

Bit 6 is the program status flag, and this flag changes “1” when flash memory write operation ends at abnormal state. If program error occurs, corresponding block is not available.

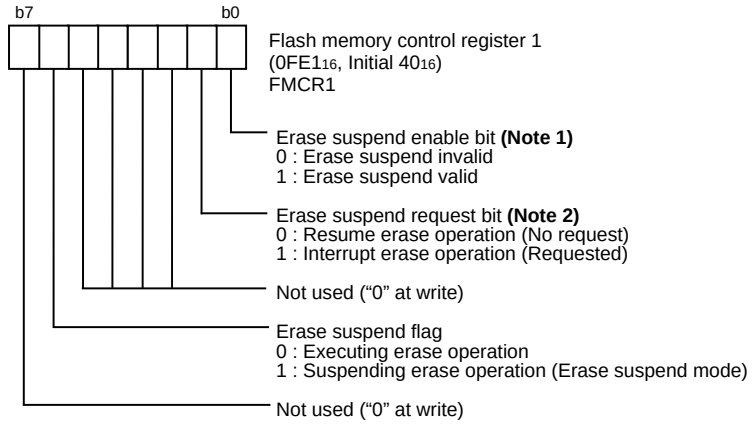
Bit 7 is the erase status flag, and this flag changes “1” when flash memory erase operation ends at abnormal state. If erase error occurs, corresponding block is not available.



Notes **1**: For this bit to be set to “1”, the user needs to write “0” and then “1” to it in succession. To reset this bit “0”, only write “0”.
2: This bit is valid when the CPU rewrite mode select bit is “1”.
3: This bit is valid when the CPU rewrite mode select bit is “1”. Fix this bit “0” when the CPU rewrite mode select bit is “0”.
4: Setting this bit “1” (Resetting the flash memory control circuit), access to the flash memory is disabled for 10 µsec.
5: Writing this bit must be executed in the RAM.

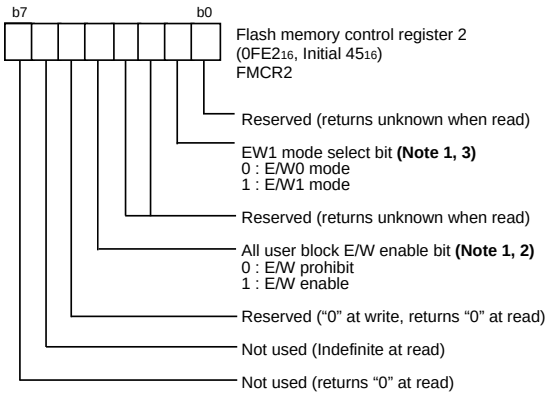
Fig. 69 Structure of flash memory control register

Figure 70 shows the flash memory control register 1.
Bit 0 is erase suspend enable bit, and setting this bit “1” erase suspend mode which makes erase operation interrupt briefly during erase operation. To set this bit to “1”, it is necessary to write “0” and then write “1” in succession. This bit can be set to “0” by only writing “0”.
Bit 1 is erase suspend request bit. Writing this bit “1” when the erase suspend enable bit is “1”, erase operation is interrupted.
Bit 6 is erase suspend flag, and becomes “0” during erase operation.
Figure 71 shows flash memory control register 2.
Bit 1 is EW1 mode select bit. Setting this bit “1”, EW1 mode becomes available.
Bit 4 is All user block E/W enable bit.



Note 1 To set this bit “1”, write “0” and then write “1” in succession. To reset this bit “0”, only write “0”.
2 This bit is valid only when erase suspend enable bit is “1”.

Fig. 70 Structure of flash memory control register 1



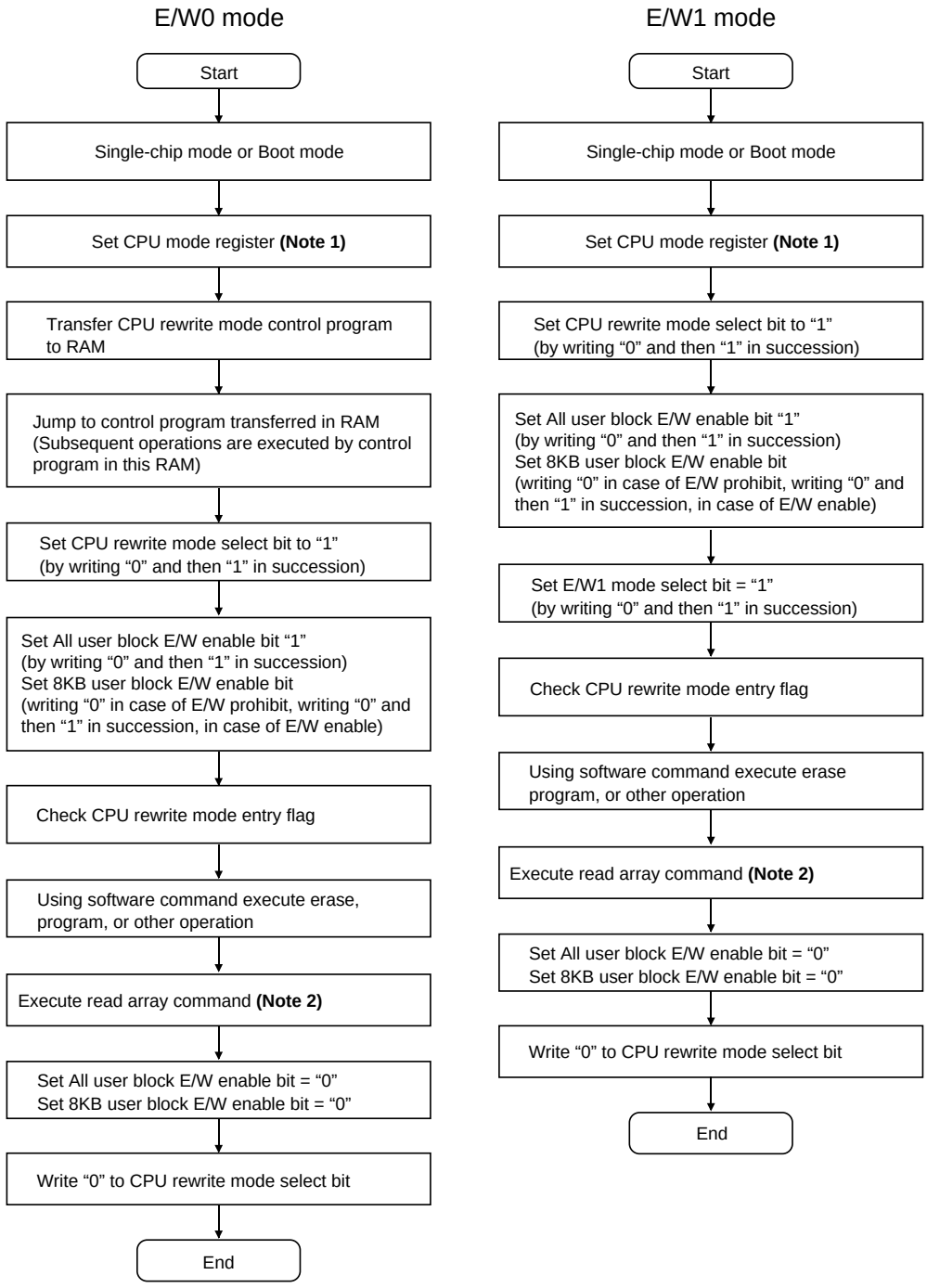
Note 1 To set this bit “1”, it is necessary to write “0” and then write “1” in succession. This bit can be set to “0” by only writing “0”.
Note 2 This bit can be written only CPU rewrite mode selection bit “1”.
Note 3 Setting this bit “1” must be done at CPU rewrite mode select bit is “1”.

Fig. 71 Structure of flash memory control register 2

Table. 15 Specification of E/W protect

All user block E/W enable bit	8KB user block E/W enable bit	8 KBX2 block Addresses C00016 to FFFF16	16 KBX2 block Addresses 40016 to BFFF16	Data block Addresses 10016 to 1FFF16
0	0	Protect	Protect	Enable
0	1	Protect	Protect	Enable
1	0	Protect	Enable	Enable
1	1	Enable	Enable	Enable

Figure 72 shows a flowchart for setting/releasing CPU rewrite mode.



Notes 1: Set bits 6, 7 (main clock division ratio selection bits) at CPU mode register ($003B_{16}$).
2: Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command.

Fig. 72 CPU rewrite mode set/release flowchart

Precautions on CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

(1) Operation speed

During CPU rewrite mode, set the internal clock frequency 4.0 MHz or less using the main clock division ratio selection bits (bit 6, 7 at $003B_{16}$).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during EW0 mode .

(3) Interrupts inhibited against use

The interrupts cannot be used during EW0 mode because they refer to the internal data of the flash memory.

In the EW1 mode, the interrupts cannot be used during program operation or erase operation which is disabled erase suspend function.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset

Reset is always valid. In case of CNV_{SS} = H when reset is released, boot mode is active. So the program starts from the address contained in address $FFFC_{16}$ and $FFFD_{16}$ in boot ROM area.

Software Commands (CPU Rewrite Mode)

Table 16 lists the software commands.

After setting the CPU Rewrite Mode Select Bit of the flash memory control register to "1", execute a software command to specify an erase or program operation.

Each software command is explained below.

●Read Array Command (FF_{16})

The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D_0 to D_7).

The read array mode is retained intact until another command is written.

●Read Status Register Command (70_{16})

The read status register mode is entered by writing the command code "70_{16}" in the first bus cycle. The contents of the status register are read out at the data bus (D_0 to D_7) by a read in the second bus cycle.

The status register is explained in the next section.

In the EW1 mode, do not execute this command.

●Clear Status Register Command (50_{16})

This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

●Program Command (40_{16})

Program operation starts when the command code "40_{16}" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification will start.

Whether the write operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ Status Flag.

The RY/$\overline{BY}$ Status Flag is "0" (busy) during write operation and "1" (ready) when the write operation is completed as is the status register bit 7.

Do not execute this command for rewrite control program address in the EW1 mode.

In the E/W0 mode, when the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D_0 to D_7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.

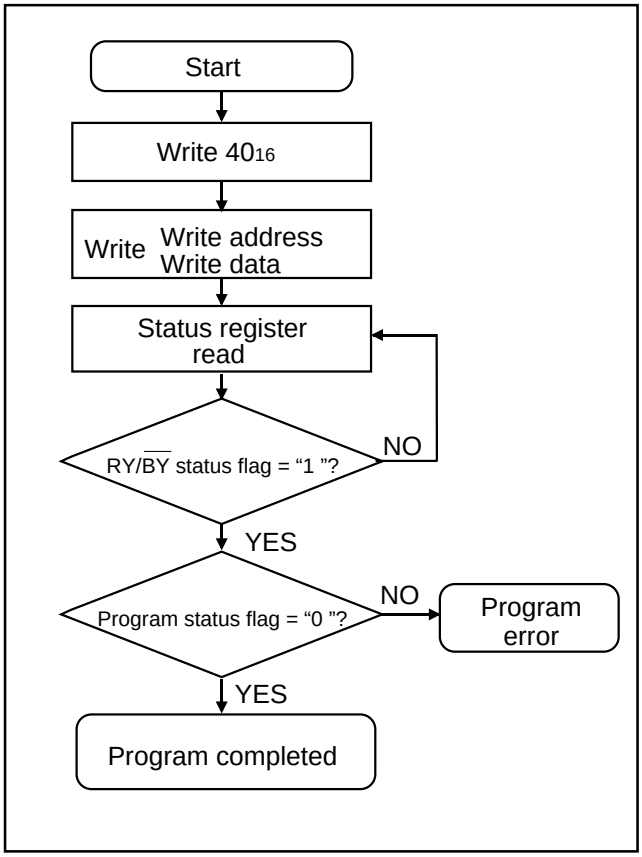


Fig. 73 Program flowchart

Table 16 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X **(Note 1)**	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD **(Note 2)**
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA **(Note 3)**	WD **(Note 3)**
Block erase	2	Write	X	20_{16}	Write	BA **(Note 4)**	$D0_{16}$

Notes 1: X denotes a given address in the User ROM area .
2: SRD = Status Register Data
3: WA = Write Address, WD = Write Data
4: BA = Block Address to be erased (Input the maximum address of each block.)

●Block Erase Command (20_{16}/$D0_{16}$)

By writing the command code "20_{16}" in the first bus cycle and the confirmation command code "$D0_{16}$" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ Status Flag of flash memory control register.

The RY/$\overline{BY}$ Status Flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.

In case of using erase suspend function in the EW0 mode, check that the erase sequence is shifted to erase suspend mode with erase suspend flag. Reading the erase status flag after block erase, the result of the block erase is gotten.

Do not execute this command for rewrite control program address in the EW1 mode.

In the EW0 mode, at the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.

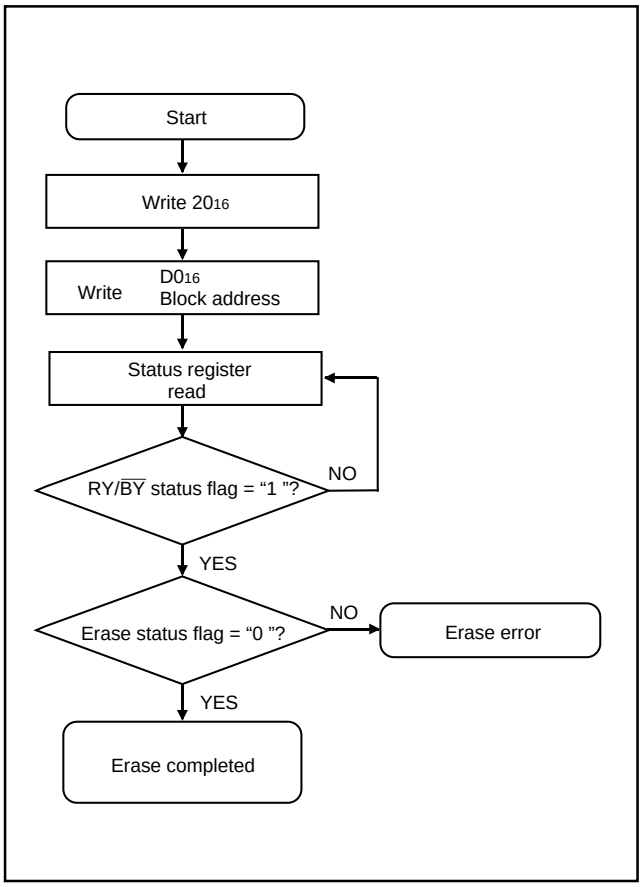


Fig. 74 Erase flowchart in no erase suspend

Status Register (SRD)

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways: in the EW0 mode.

(1) By reading an arbitrary address from the User ROM area after writing the read status register command (70_{16})
(2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input.

Also, the status register can be cleared by writing the clear status register command (50_{16}).
After reset, the status register is set to "80_{16}".
Table 17 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.
After power-on, the sequencer status is set to "1" (ready).

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

•Program status (SR4)

The program status indicates the operating status of write operation. When a write error occurs, it is set to "1".
The program status is set to "0" when it is cleared.

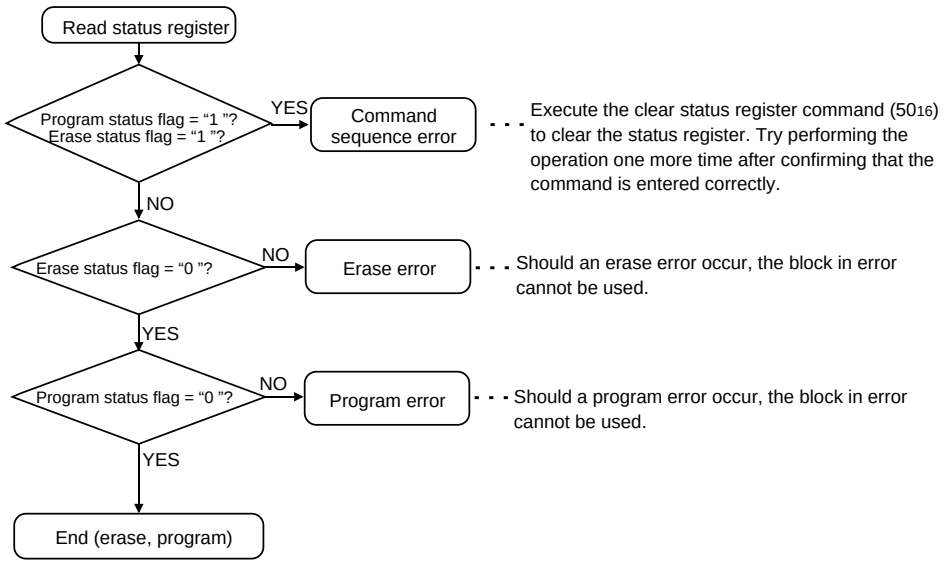
If "1" is written for any of the SR5 and SR4 bits, the program, erase all blocks, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, if any commands are not correct, both SR5 and SR4 are set to "1".

Table 17 Definition of each bit in status register (SRD)

Symbol	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 75 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of erase status flag and program status flag is set to "1", none of the read array, the program, erase all blocks, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 75 Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory Version

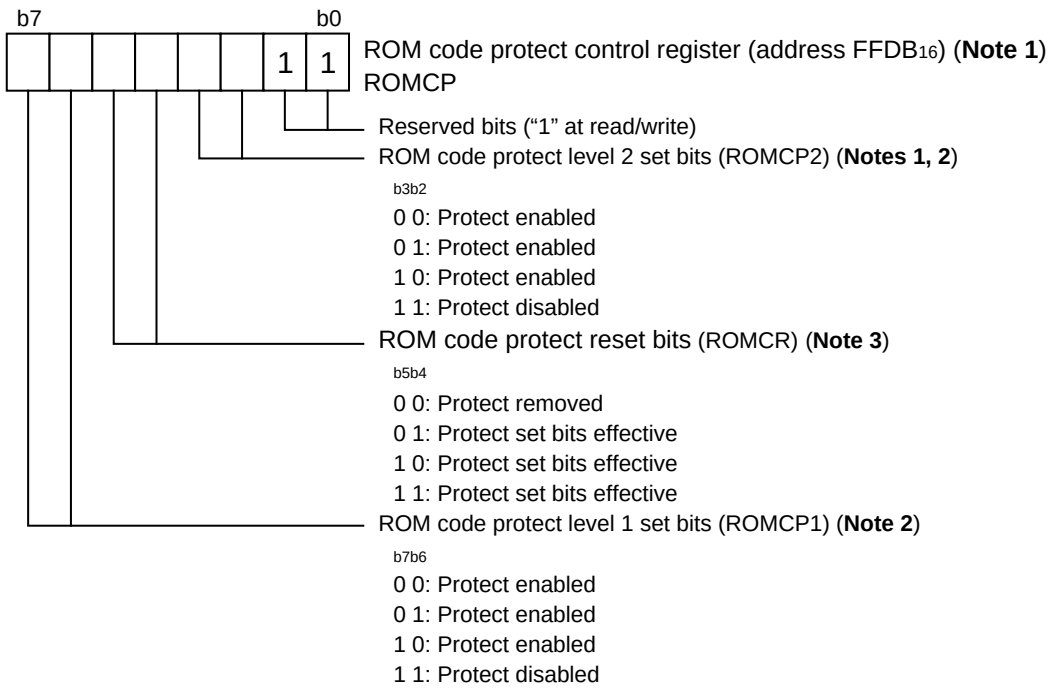
To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode.

●ROM Code Protect Function (in Parallel I/O Mode)

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control (address FFDB16) in parallel I/O mode. Figure 76 shows the ROM code protect control (address FFDB16). (This address exists in the User ROM area.)

If one or both of the pair of ROM Code Protect Bits is set to “0”, the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM Code Protect Reset Bits are set to “00”, the ROM code protect is turned off, so that the contents of internal flash memory can be read out or modified. Once the ROM code protect is turned on, the contents of the ROM Code Protect Reset Bits cannot be modified in parallel I/O mode. Use the CPU rewrite mode to rewrite the contents of the ROM Code Protect Reset Bits. Rewriting of only the ROM code protect control address (address FFDB16) cannot be performed. When rewriting the ROM code protect reset bit, rewrite the whole user ROM area (block 0) containing the ROM code protect control address.



Notes 1: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.

2: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.

3: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in CPU rewrite mode.

Fig. 76 Structure of ROM code protect control

(2) Parallel I/O Mode

Parallel I/O mode is the mode which parallel output and input software command, address, and data required for the operations (read, program, erase, etc.) to a built-in flash memory. Use the exclusive external equipment flash programmer which supports the 7512 Group (flash memory version). Refer to each programmer maker's handling manual for the details of the usage.

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 13 can be rewritten. Both areas of flash memory can be operated on in the same way.

The boot ROM area is 4K bytes in size. It is located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the Boot ROM area, an erase block operation is applied to only one 4K byte block.

Electrical characteristics for Flash ROM E/W Cycles

Table 18 Characteristics (Note 1) for 100 E/W cycle products

(Vcc = 2.5V±2%, Ta = 0 to 60 °C, unless otherwise noted)

Symbol	Parameter		Condition	Limits			Unit
				Min.	Typ. (Note 2)	Max.	
—	Erase/Write cycle (Note 3)			100 (Note 4)			cycle
—	Byte write time		Vcc=2.5V, Ta=25°C		75	600	µs
—	Block erase time	2Kbyte block	Vcc=2.5V, Ta=25°C		0.2	9	s
		8Kbyte block			0.4	9	s
		16Kbyte block			0.7	9	s
td(SR–ES)	Time delay from Suspend Request until Erase Suspend					8	ms
—	Data retention time (Note 5)			20			year

Table 19 Characteristics (Note 6) for 1000 E/W cycle products [Block A and Block B (Note 7)]

(Vcc = 2.5V±2%, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ. (Note 2)	Max.	
—	Erase/Write cycle (Note 3, 8, 9)		1000 (Note 4)			cycle
—	Byte write time	Vcc=2.5V, Ta=25°C		100		µs
—	Block erase time (2Kbyte block)	Vcc=2.5V, Ta=25°C		0.3		s
td(SR–ES)	Time delay from Suspend Request until Erase Suspend				8	ms

Notes 1: Specified for all blocks.
2: Vcc=2.5V; Ta=25°C.
3: Definition of E/W cycle: Each block may be written to a variable number of times - up to a maximum of the total number of distinct byte addresses - for every block erase. Performing multiple writes to the same address before an erase operation is prohibited.
4: Maximum number of E/W cycles for which operation is guaranteed.
5: At Ta=55°C condition
6: Specified for Block A and Block B E/W cycles > 100
7: To reduce the number of E/W cycles, a block erase should ideally be performed after writing as many different byte addresses (only one time each) as possible. It is important to track the total number of block erases.
8: Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
9: Customers desiring E/W failure rate information should contact their Renesas technical support representative.

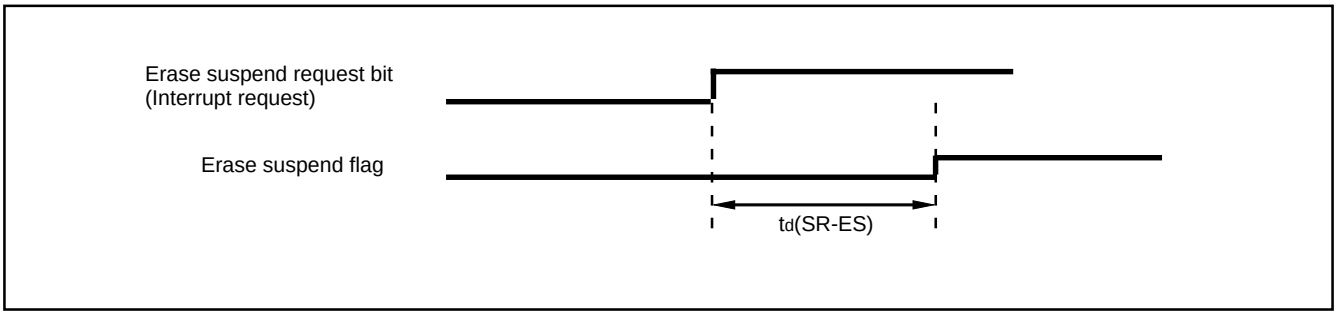


Fig. 77 The transition of the timing of the erase / erase suspend

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1."

Serial I/O continues to output the final bit from the TxD pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.

When in serial I/Os 1 and 3 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is "H."

A/D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) is at least on 500 kHz during an A/D conversion.

Do not execute the STP instruction during an A/D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is double of the XIN period in high-speed mode.

NOTES ON USAGE

Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin), and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF–0.1 µF is recommended.

Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation. In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

ELECTRICAL CHARACTERISTICS

Table 20 Absolute maximum ratings (Executing flash memory mode, flash memory electrical characteristics is applied.)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 3.2	V
V_I	Input voltage $P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$, ADV_{REF}, AV_{CC}, ISENS1		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P1_0$–$P1_7$, $P2_2$–$P2_5$, $P4_3$, $P4_4$		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV$_{SS}$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P1_0$–$P1_7$, $P2_2$–$P2_5$, $P4_3$, $P4_4$		–0.3 to 5.8	V
P_d	Power dissipation	Ta = 25 °C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Table 21 Recommended operating conditions (1)
(Vcc = 2.5V±2%, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage (At 4 MHz)	2.45	2.5	2.55	V
V_{SS}	Power source voltage		0		V
ADV_{REF}	A/D convert reference voltage	2.0		V_{CC}	V
ADV_{SS}	A/D convert power source voltage		0		V
V_{IA}	Analog input voltage AN_0–AN_5, AN_8–AN_{11}	ADV_{SS}		V_{CC}	V
AV_{CC}	Analog power source voltage	2.45	2.5	2.55	V
AV_{SS}	Analog power source voltage		0		V
ISENS0	Analog input voltage		0		V
ISENS1	Analog input voltage	-0.2		0.2	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P1_0$–$P1_7$, $P2_2$–$P2_5$, $P4_3$, $P4_4$	0.8V_{CC}		5.8	V
V_{IH}	“H” input voltage (when I^2C-BUS input level is selected) SDA_1, SDA_2, SCL_1, SCL_2	0.7V_{CC}		5.8	V
V_{IH}	“H” input voltage (when SMBUS input level is selected) SDA_1, SDA_2, SCL_1, SCL_2	1.4		5.8	V
V_{IH}	“H” input voltage $\overline{RESET}$, X_{IN}, CNV$_{SS}$	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_5$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage (when I^2C-BUS input level is selected) SDA_1, SDA_2, SCL_1, SCL_2	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (when SMBUS input level is selected) SDA_1, SDA_2, SCL_1, SCL_2	0		0.6	V
V_{IL}	“L” input voltage $\overline{RESET}$, CNV$_{SS}$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage X_{IN}	0		0.16V_{CC}	V

Table 22 Recommended operating conditions (2)
(Vcc = 2.5V±2%, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P3_0$–$P3_5$ (Note 1)			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P2_0$, $P2_1$, $P2_6$–$P2_7$, $P4_0$–$P4_2$, $P4_5$ (Note1)			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P3_0$–$P3_5$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P1_0$–$P1_7$ (Note1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P2_0$–$P2_7$,$P4_0$–$P4_5$ (Note1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P3_0$–$P3_5$ (Note1)			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P2_0$, $P2_1$, $P2_6$, $P2_7$,$P4_0$–$P4_2$, $P4_5$ (Note1)			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P3_0$–$P3_5$ (Note1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P1_0$–$P1_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P2_0$–$P2_7$,$P4_0$–$P4_5$ (Note1)			40	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$ (Note 2)			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current	$P1_0$–$P1_7$ (Note 2)			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$ (Note 3)			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_5$ (Note 3)			5	mA
$I_{OL(avg)}$	"L" peak output current	$P1_0$–$P1_7$ (Note 3)			15	mA
$f(X_{IN})$	Main clock input oscillation frequency (V_{CC} = 2.5V ± 2%) (Note 4)			4	5	MHz
$f(X_{IN})$	Sub-clock input oscillation frequency (V_{CC} = 2.5V ± 2%) (Note 4,5)			32.768	50	KHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50%.
5: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 23 Electrical characteristics (1)
(V_{CC} = 2.5V±2%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$ **(Note)**	I_{OH} =–1.0 mA V_{CC} =2.5V±2%	V_{CC} –0.8			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_5$	I_{OL} =1.0 mA V_{CC} =2.5V±2%			0.8	V
V_{OL}	"L" output voltage $P1_0$–$P1_7$	I_{OL} =10 mA V_{CC} =2.5V±2%			0.8	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0–INT_3			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.4		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.4		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P2_0$, $P2_1$, $P2_6$, $P2_7$, $P3_0$–$P3_5$, $P4_0$–$P4_2$, $P4_5$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current ISENS0, ISENS1	V_I = V_{CC}			1.0	µA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_5$, $P4_0$–$P4_5$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current ISENS0, ISENS1	V_I = V_{SS}			–1.0	µA
I_{IL}	"L" input current $\overline{RESET}$,CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		2.55	V

Table 24 Electrical characteristics (2)
(V_{CC} = 2.5V±2%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 4 MHz or high-speed RC oscillating (4MHz) $f(X_{CIN})$ = 32.768 kHz or RC oscillating Output transistors “off” Current integrator and current detector stopped		1.5	2.5	mA
		High-speed mode $f(X_{IN})$ = 4 MHz or high-speed RC oscillating (4MHz) (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” Current integrator and current detector stopped		0.8		mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz or 32kHz RC oscillating Output transistors “off” Current integrator and current detector stopped		420		µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (cristal)	cristal	6.4		µA
		or 32kHz RC oscillating (in WIT state) Output transistors “off” Current integrator and current detector stopped	RC	30		µA
		Middle-speed mode $f(X_{IN})$ = 4 MHz or high-speed RC oscillating (4MHz) $f(X_{CIN})$ = stopped Output transistors “off” Current integrator and current detector stopped		1.0		mA
		Middle-speed mode $f(X_{IN})$ = 4 MHz or high-speed RC oscillating (4MHz) (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off” Current integrator and current detector stopped		0.8		mA
		Increment when A/D conversion is executed $f(X_{IN})$ = 4 MHz or high-speed RC oscillating (4MHz)		200		µA
		Flash memory write	$f(X_{IN})$ = 4MHz V_{CC} = 2.5V	12		mA
		Flash memory erase	$f(X_{IN})$ = 4MHz V_{CC} = 2.5V	22		mA

Table 25 Electrical characteristics (3)
(Vcc = 2.5V±2%, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
Icc	Power source current	Increment when current integrator is executed			800		µA
		Increment when over current detector is executed.	Short current detector		20		µA
			Over current detector		20		µA
			Charge over current detector		20		µA
			Wake up current detector		25		µA
			Two detectors used other than Wake up current detector		30		µA
			Three detectors used other than Wake up current detector		40		µA
			Wake up current detector and another use		35		µA
			Wake up current detector and other two used		45		µA
			Wake up current detector and other three used		55		µA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C (Note)		0.1	1.0	µA
			Ta = 85 °C			10	µA

Note : When using the 32kHz RC oscillation circuit or the XCIN-XCOUT oscillation, before STP instruction execution select the modes other than the low-speed mode with the main clock division ratio selection bit (CM7, CM6) and then set ports $P2_1$ and $P2_0$ to output port ("L" output).

Table 26 High-speed RC oscillation circuit electrical characteristics
(Vcc = AVcc = 2.5V±2%, Vss =AVss = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f_{4MRC}	Oscillating frequency ajustment width (Note)	f(XIN)=4 to 5 MHz			±3.0	%
f_{4MRCS}	Oscillating frequency shift by temperature			0.2	0.5	%/°C

Notes : The bigger setting value of the high-speed RC oscillator frequency set up register (address $0FF2_{16}$) makes the oscillating frequency of the high-speed RC oscillation circuit lower. However, since the oscillating frequency is set higher when setting the values from $7F_{16}$ to 80_{16} or from BF_{16} to $C0_{16}$, be careful of frequency adjustment by software.

Table 27 32kHz RC oscillation circuit electrical characteristics
(Vcc = AVcc = 2.5V±2%, Vss =AVss = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	External registor, and capacitor tolerance	Total tolerance of the resistor and capacitor when External registor=91kΩ when External capacitor=100pF			10	%
–	Oscillating frequency adjustment resolution				0.07	kHz
–	Oscillating frequency shift by Vcc voltage	Ta=25 °C		0.5		%
–	Oscillating frequency shift by temperature	Vcc=AVcc=2.5V, –20 to 85 °C		0.5		%
–	Oscillating frequency shift by Vcc voltage and temperature				2	%

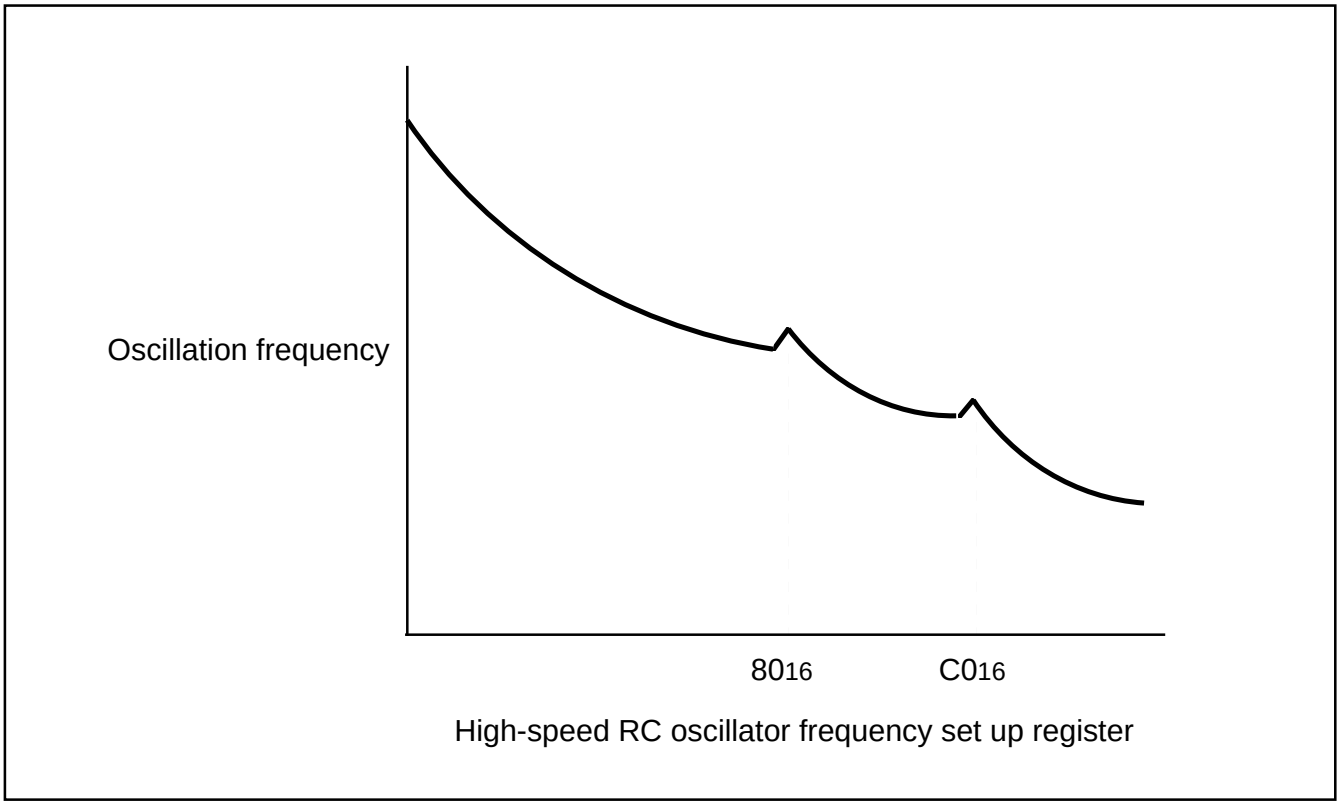


Fig. 78 High-speed RC oscillation circuit register value - Oscillating frequency characteristics

Table 28 A/D converter characteristics
(V_{CC} = 2.5 ± 2%, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 4MHz, f(X_{CIN}) = 32.768KHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	bit
–	Absolute accuracy (excluding quantization error)					±4	LSB
t_{CONV}	Conversion time		High-speed mode, middle-speed mode			61	tc(ϕ)
			Low-speed mode		40		µs
R_{LADDER}	Ladder resistor				35		kΩ
I_{VREF}	Reference power source input current	V_{REF} "on"	V_{REF} = 2.5 V	40	100	140	µA
		V_{REF} "off"				5.0	µA
$I_{I(AD)}$	A/D port input current				0.5	5.0	µA

Table 29 Easy thermal sensor electrical characteristics
(V_{CC} = 2.5V±2%, V_{SS} =AV_{SS} = 0V, Ta = –20 to 85 °C, f(X_{IN}) = 4MHz, f(X_{CIN}) = 32.768KHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Easy thermal sensor output voltage at room temperature	Ta=27°C		1.38		V
–	The rate of the easy thermal sensor output voltage by temperature	V_{CC} = V_{REF} = 2.5 V		3.4		mV/ °C

Table 30 Current integrator electrical characteristics
(V_{CC} = AV_{CC} = 2.5V±2%, V_{SS} =AV_{SS} = 0V, Ta = –20 to 85 °C, f(X_{IN}) = 4MHz, f(X_{CIN}) = 32.768KHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{INF}	Integrate period			125		ms
V_{ISENS1}	ISENS1 input range		–0.15		0.2	V
A_D	Integrate coefficient of integrator for discharge		0.68	1.00	1.35	µV•sec
A_C	Integrate coefficient of integrator for charge		0.68	1.00	1.35	µV•sec
t_{RD}	Reset time of integrator for discharge			300		ns
t_{RC}	Reset time of integrator for charge			300		ns
b'	Count value at 0V input		–2400		2400	–
V_{REFD}	Internal reference voltage for discharge integrator		0.09	0.1	0.11	V
V_{REFC}	Internal reference voltage for charge integrator		–0.11	–0.1	–0.09	V
–	linearity error after reset time caribration	V_{CC}=2.5V±2%, Ta=0 to 60 °C			1	%
		V_{CC}=2.5V±2%, Ta=–20 to 85 °C			3	%

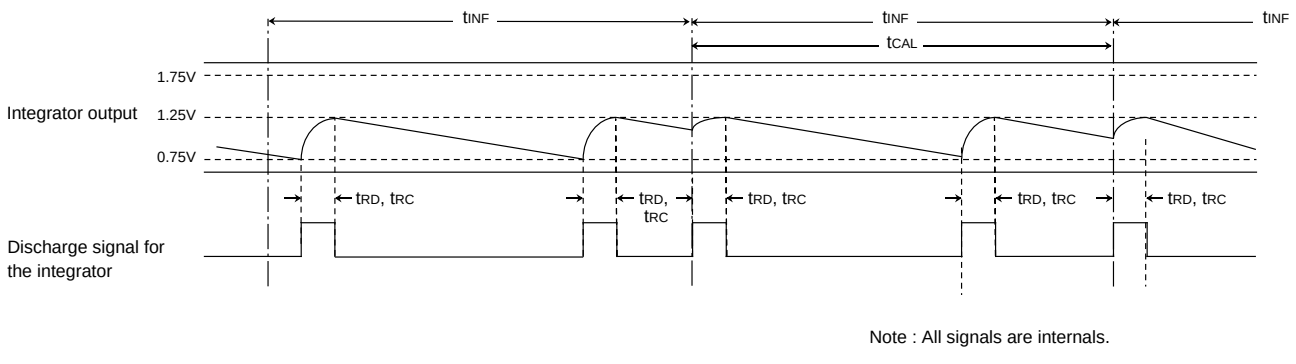


Fig. 79 Current integrator timing diagram

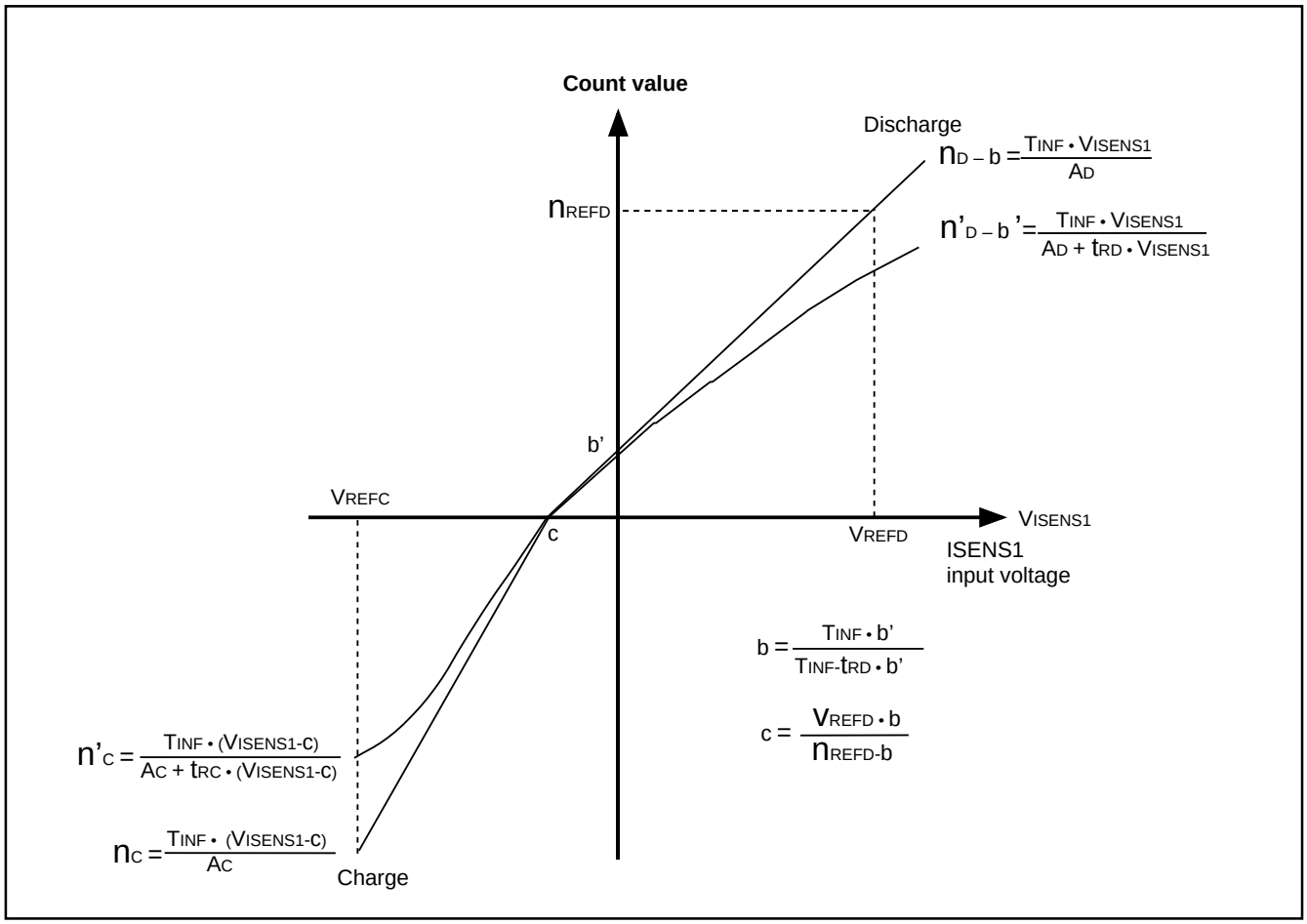


Fig. 80 V_{ISENS1}-Count value characteristics of current integrator

Table 31 Over current detector electrical characteristics
(V_{CC} = AV_{CC} = 2.5V±2%, V_{SS} = AV_{SS} = 0V, Ta = –20 to 85 °C, f(X_{IN}) = 4MHz, f(X_{CIN}) = 32.768MHz)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Discharge short current detect voltage error				±15	mV
–	Discharge over current detect voltage error				±15	mV
–	Charge over current detect voltage error				±15	mV
–	Wake up detect voltage		8	10	12	mV
–	Discharge short current detect time error				30.5	µs
–	Discharge over current detect time error			T.B.D.		
–	Discharge over current detect time error			T.B.D.		µs
–	Wake up detect time		58.6		62.5	ms

TIMING REQUIREMENTS

Table 32 Timing requirements
(Vcc = 2.5V±2%, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw($\overline{\text{RESET}}$)	Reset input “L” pulse width	20			XIN cycles
tc(XIN)	External clock input cycle time	250			ns
twH(XIN)	External clock input “H” pulse width	100			ns
twL(XIN)	External clock input “L” pulse width	100			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	500			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width	230			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width	230			ns
twH(INT)	INT0 to INT3 input “H” pulse width	230			ns
twL(INT)	INT0 to INT3 input “L” pulse width	230			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (Note)	2000			ns
twH(SCLK1)	Serial I/O1 clock input “H” pulse width (Note)	950			ns
twL(SCLK1)	Serial I/O1 clock input “L” pulse width (Note)	950			ns
tsu(RxD-SCLK1)	Serial I/O1 clock input set up time	400			ns
th(SCLK1-RxD)	Serial I/O1 clock input hold time	200			ns
tc(SCLK2)	Serial I/O2 clock input cycle time	2000			ns
twH(SCLK2)	Serial I/O2 clock input “H” pulse width	950			ns
twL(SCLK2)	Serial I/O2 clock input “L” pulse width	950			ns
tsu(SIN2-SCLK2)	Serial I/O2 clock input set up time	400			ns
th(SCLK2-SIN2)	Serial I/O2 clock input hold time	300			ns

Note : When f(XIN) = 4 MHz and bit 6 of address 001A16 is “1” (clock synchronous).
Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is “0” (UART).

Table 33 Switching characteristics
(Vcc = 2.5V±2%, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
twH (SCLK1)	Serial I/O1 clock output “H” pulse width	Fig. 82	tc(SCLK1)/2–50			ns
twL (SCLK1)	Serial I/O1 clock output “L” pulse width		tc(SCLK1)/2–50			ns
td (SCLK1-TxD)	Serial I/O1 output delay time (Note 1)				350	ns
tv (SCLK1-TxD)	Serial I/O1 output valid time (Note 1)		–30			ns
tr (SCLK1)	Serial I/O1 clock output rising time				50	ns
tf (SCLK1)	Serial I/O1 clock output falling time				50	ns
twH (SCLK2)	Serial I/O2 clock output “H” pulse width		tc(SCLK2)/2–240			ns
twL (SCLK2)	Serial I/O2 clock output “L” pulse width		tc(SCLK2)/2–240			ns
td (SCLK2-SOUT2)	Serial I/O2 output delay time (Note 2)				400	ns
tv (SCLK2-SOUT2)	Serial I/O2 output valid time (Note 2)		0			ns
tf (SCLK2)	Serial I/O2 clock output falling time				50	ns
tr (CMOS)	CMOS output rising time (Note 3)			20	50	ns
tf (CMOS)	CMOS output falling time (Note 3)			20	50	ns

Notes 1: For twH(SCLK1), twL(SCLK1), when the P25/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register (bit 7 of address 001516) is “0”.
3: The XOUT pin is excluded.

MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Table 34 Multi-master I²C-BUS bus line characteristics

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	Hold time for SCL clock = “0”	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1C_b **(Note)**	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time for SCL clock = “1”	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1C_b **(Note)**	300	ns
$t_{SU;DAT}$	Data setup time	250		100		ns
$t_{SU;STA}$	Setup time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Setup time for STOP condition	4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

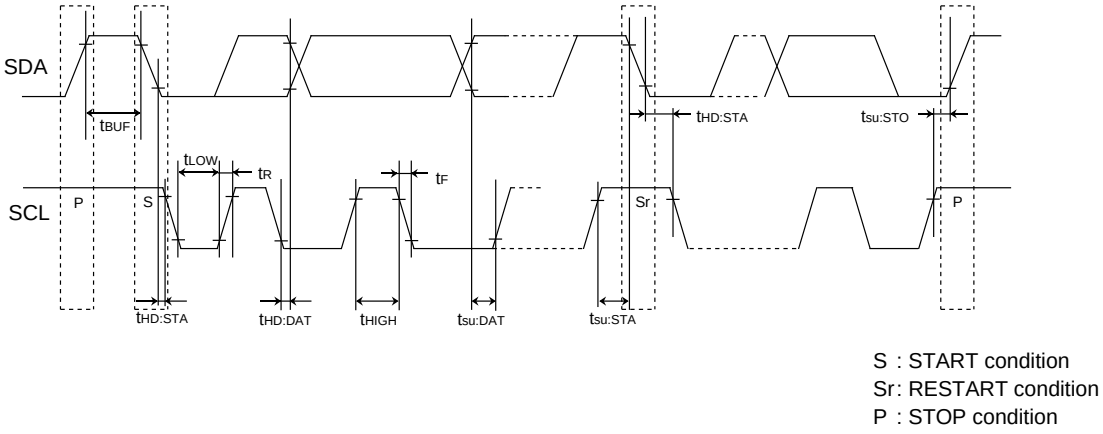


Fig. 81 Timing diagram of multi-master I²C-BUS

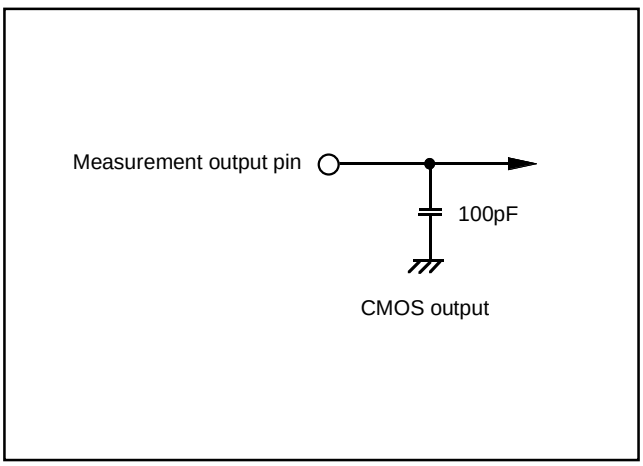


Fig. 82 Circuit for measuring output switching characteristics (1)

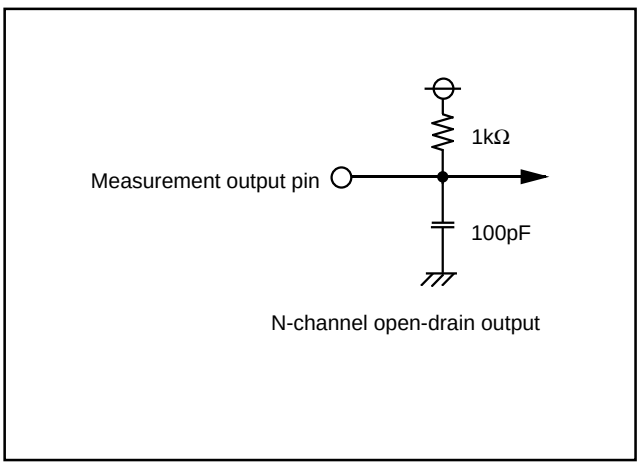


Fig. 83 Circuit for measuring output switching characteristics (2)

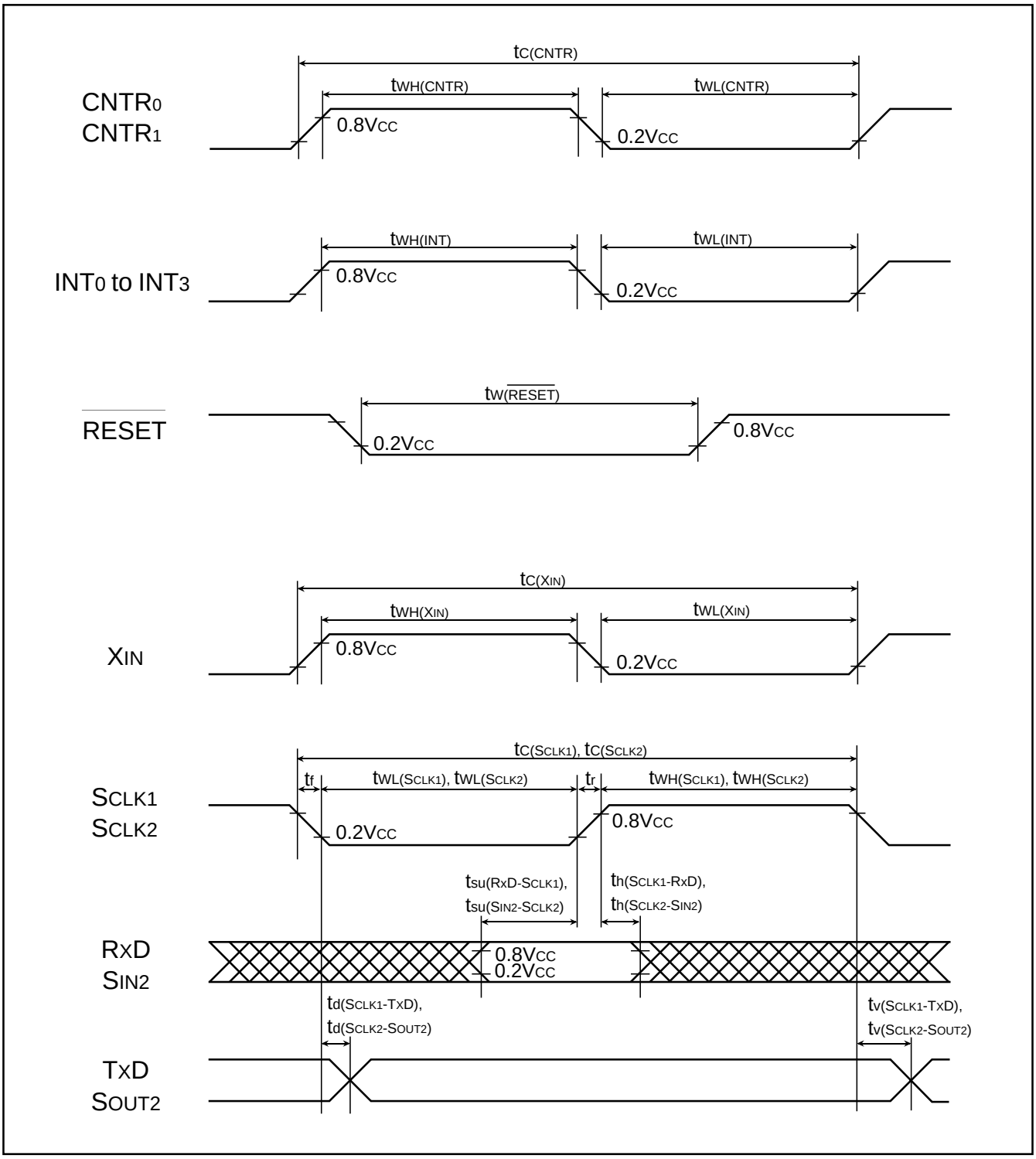


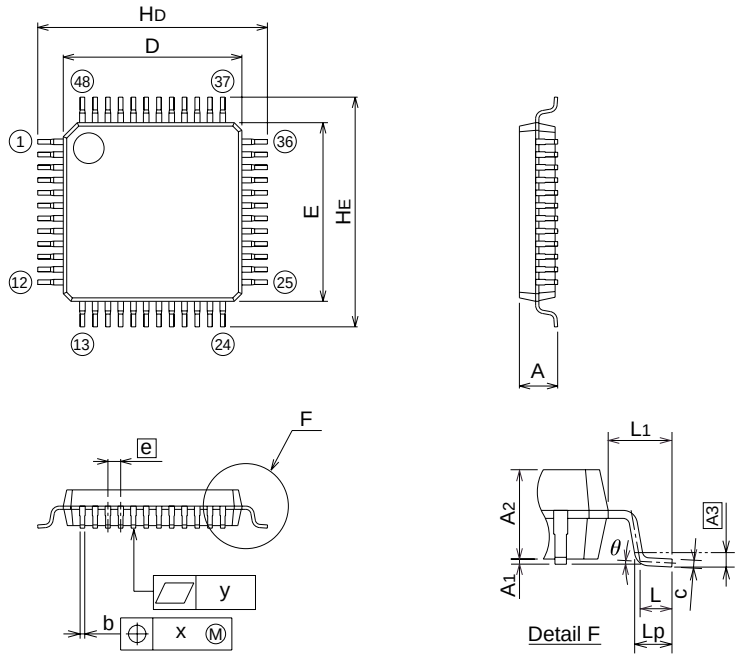
Fig. 84 Timing diagram

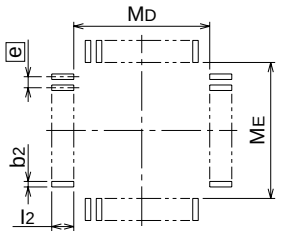
PACKAGE OUTLINE

48P6Q-A Recommended

Plastic 48pin 7×7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	–	–	Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.5	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

REVISION HISTORY	7512 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov.10, 2004	–	First edition issued
1.01	Feb.18, 2005	14	Fig.11 Ports $P4_4$ and $P4_5$ are partly revised.

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