

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

SKYY

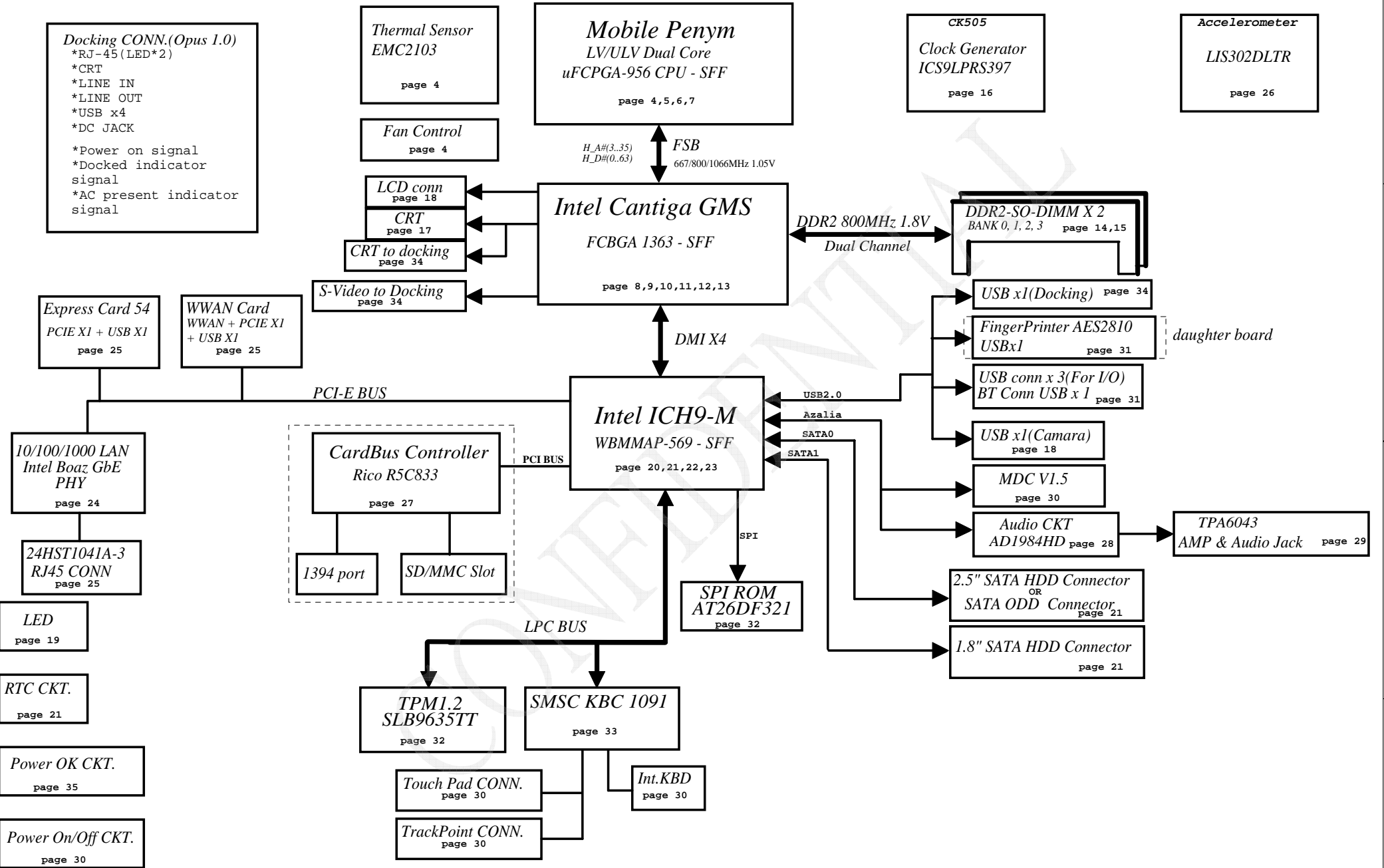
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DC/DC Interface CKT.
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Power OK CKT.
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RTC CKT.
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24HST1041A-3
RJ45 CONN
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10/100/1000 LAN
Intel Boaz GbE
PHY
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Express Card 54
PCIE X1 + USB X1
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Docking CONN.(Opus 1.0)
*RJ-45 (LED*2)
*CRT
*LINE IN
*LINE OUT
*USB x4
*DC JACK

*Power on signal
*Docked indicator
signal
*AC present indicator
signal

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
	S0	O	O	O
	S1	O	O	O
	S3	O	O	O
	S5 S4/AC	O	O	X
	S5 S4/ Battery only	O	X	X
S5 S4/AC & Battery don't exist	X	X	X	

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

CONN@ : means ME part.

45@ : means install after SMT.

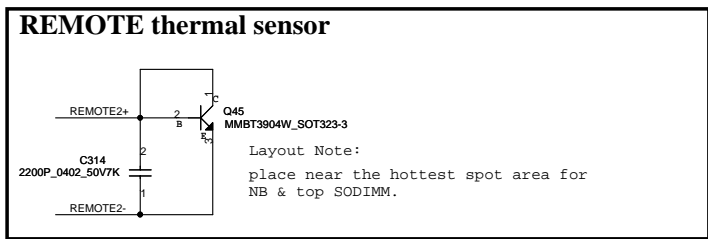
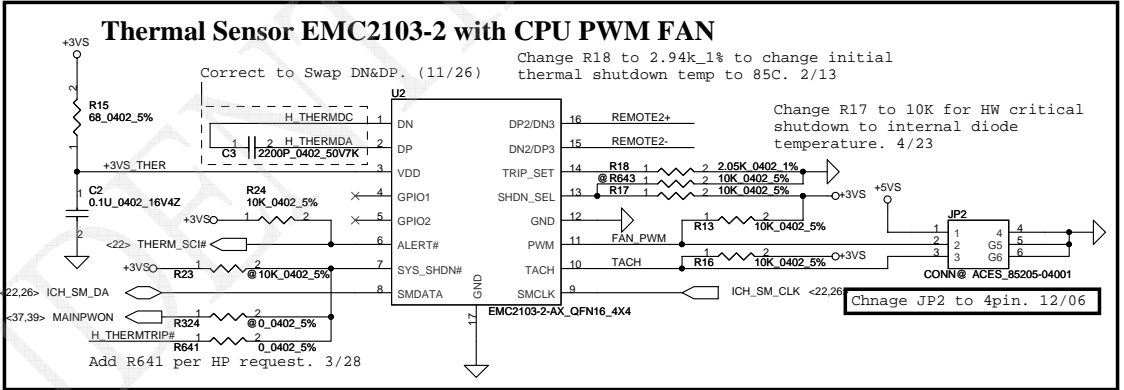
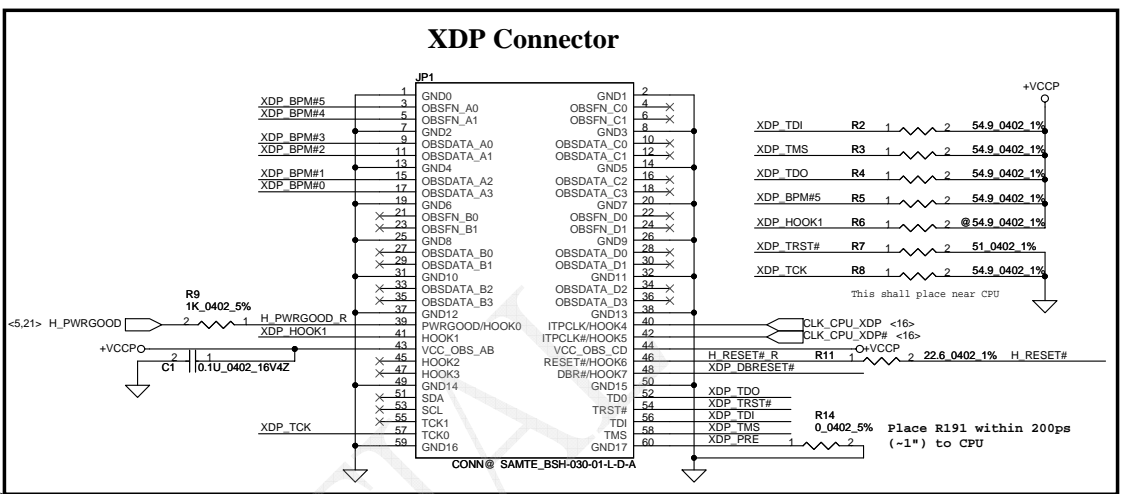
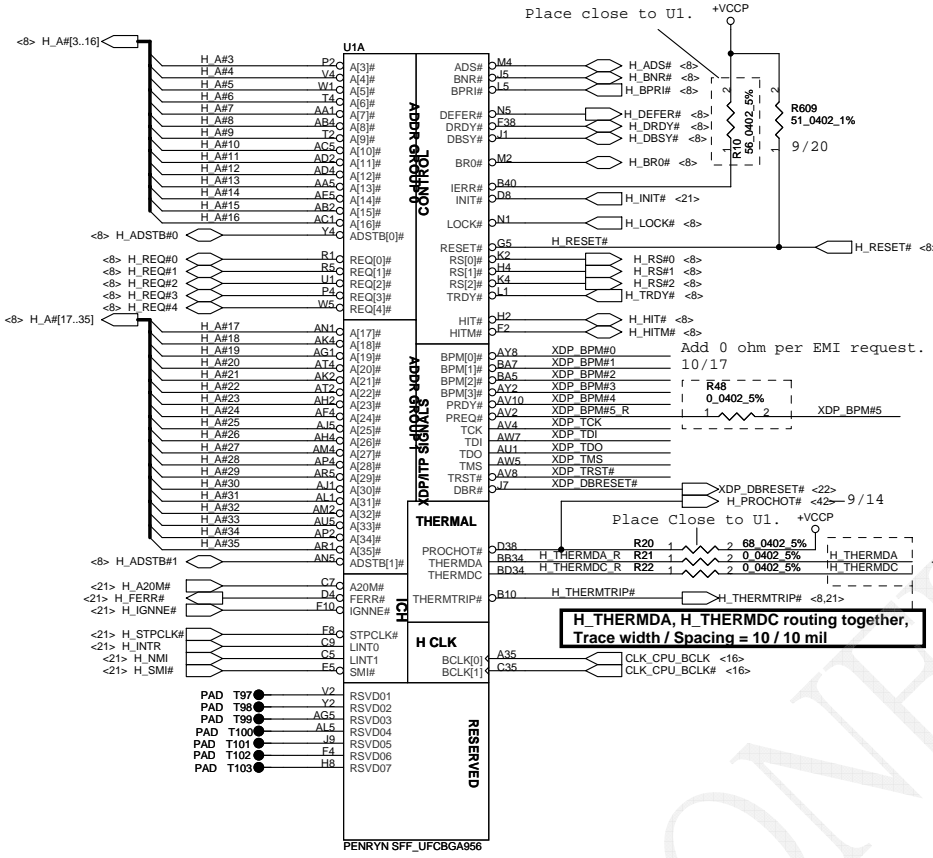
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

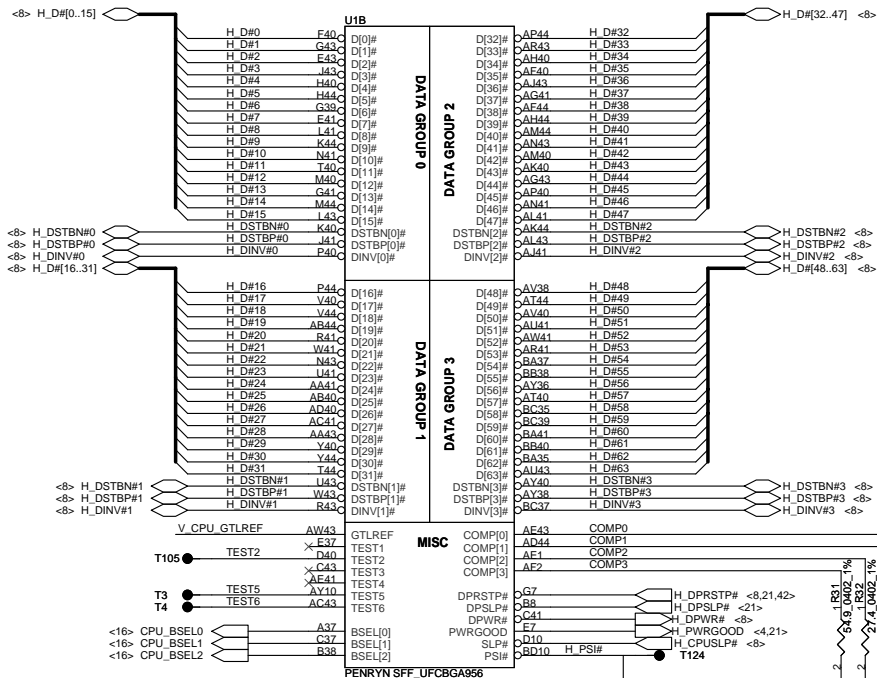
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
CLOCK GENERATOR (EXT.)	D2	11010010

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Change R23, R24 connect to +3VS and add PU/PD for U2. (9/3)
 NI R23, reserve R324 and connect to MAINPWON. (10/5)

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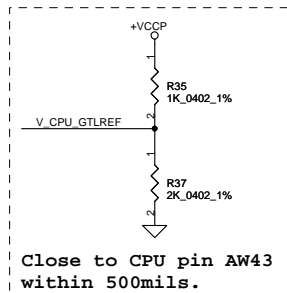


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

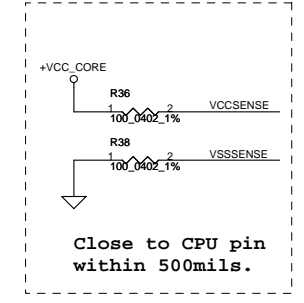
Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



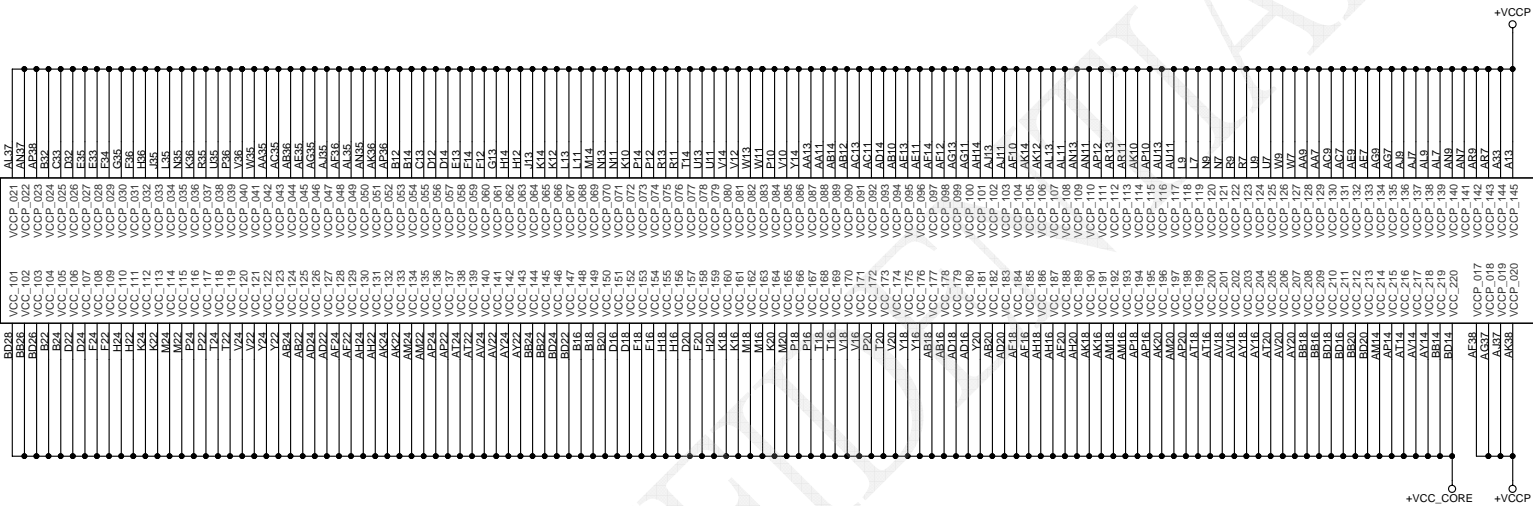
Close to CPU pin AW43 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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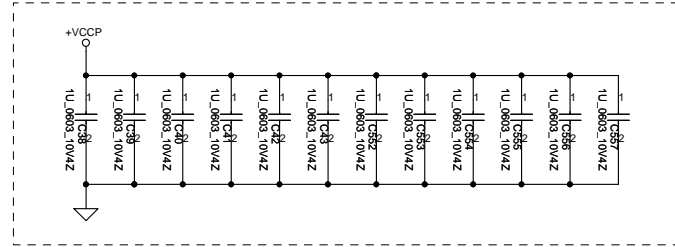
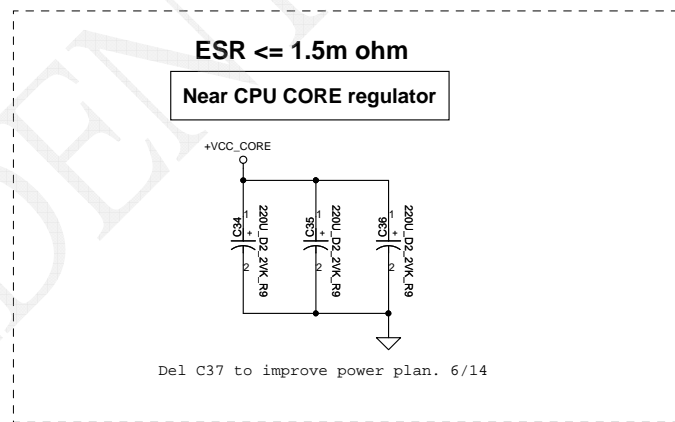
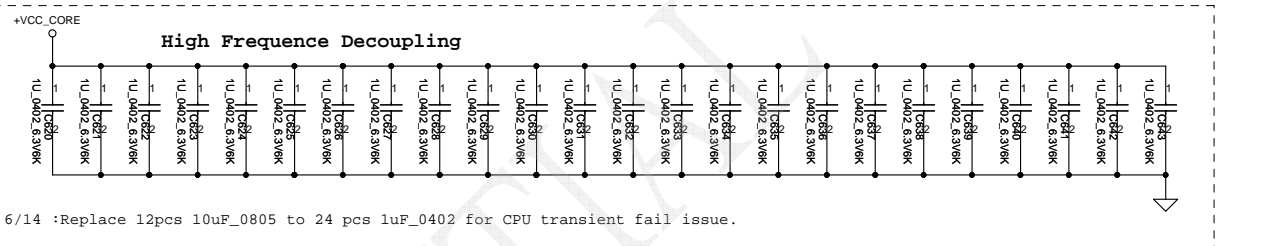
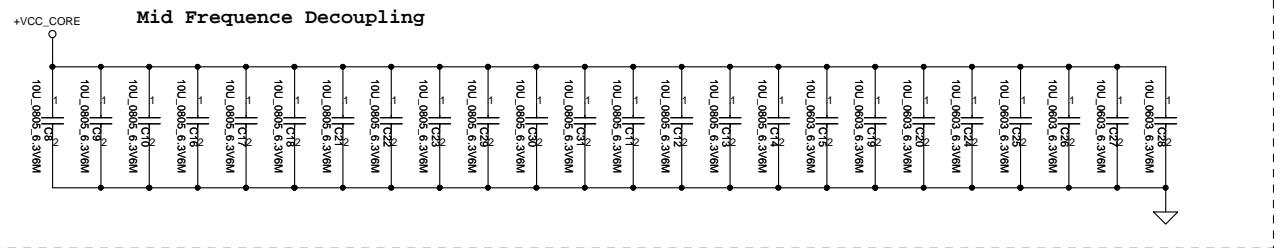


U1F
PENRYN SFF_UFCBGA956

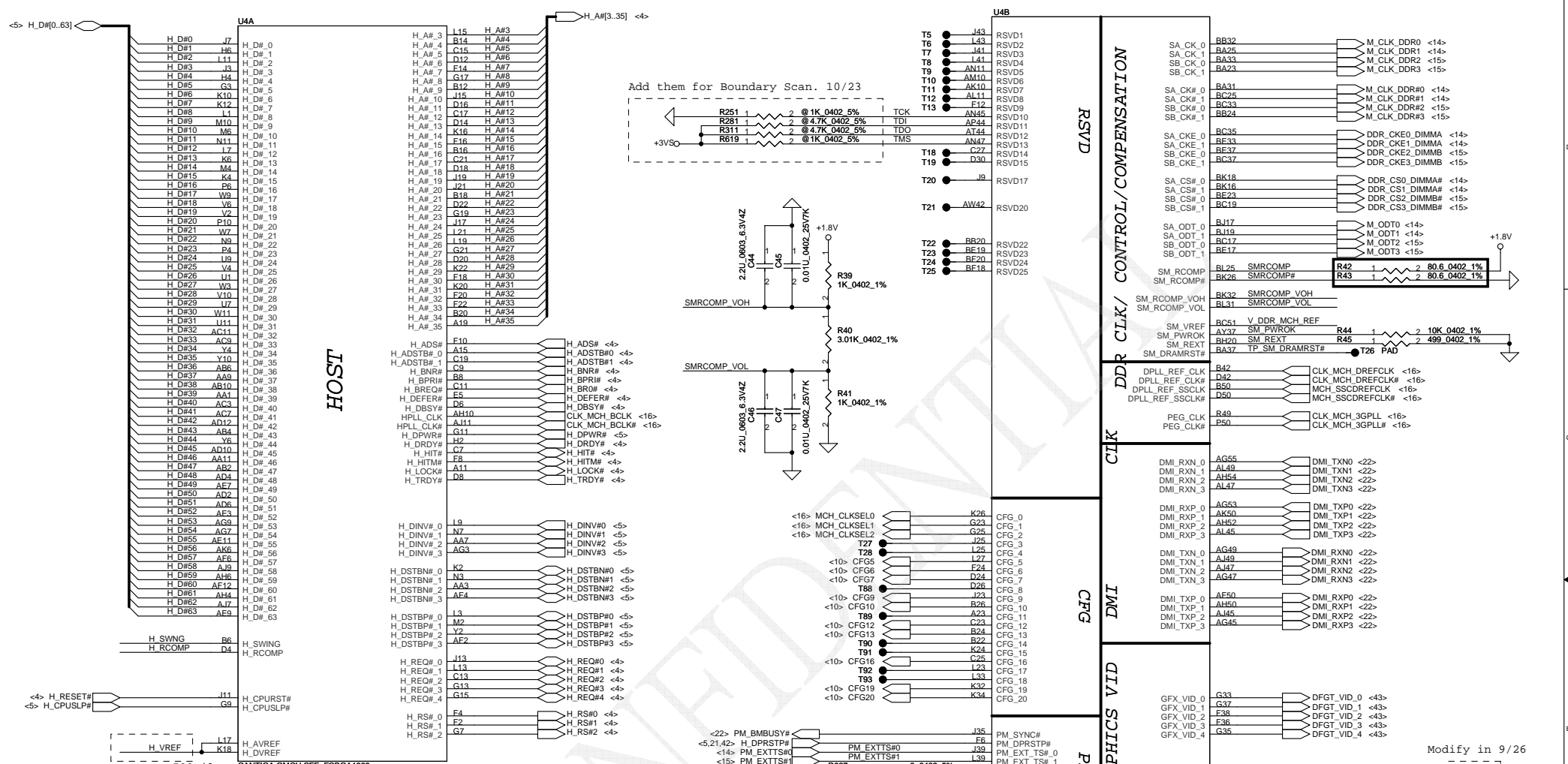
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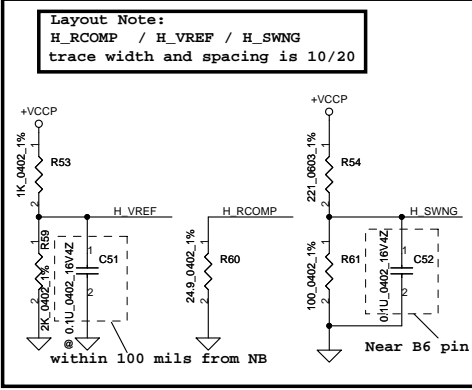
UID		U1E	
B42	VSS001	G25	VSS_164
F44	VSS002	G24	VSS_165
D42	VSS003	G23	VSS_166
F42	VSS005	AV34	VSS_167
H42	VSS006	AW35	VSS_168
K42	VSS007	AW33	VSS_169
M42	VSS008	AW34	VSS_170
P42	VSS009	AT36	VSS_171
T42	VSS010	AV36	VSS_172
Y42	VSS011	BA33	VSS_173
AB42	VSS012	BC33	VSS_174
AD42	VSS014	BD36	VSS_175
AE42	VSS015	C27	VSS_177
AH42	VSS016	C29	VSS_178
AK42	VSS017	C31	VSS_179
AM42	VSS018	E29	VSS_180
AY44	VSS020	E27	VSS_181
AV44	VSS021	G27	VSS_182
AT42	VSS022	E31	VSS_183
AV42	VSS023	G31	VSS_184
AA42	VSS024	J29	VSS_185
BA43	VSS026	L29	VSS_187
BB42	VSS027	L27	VSS_188
CA9	VSS028	N29	VSS_190
G37	VSS029	AE25	VSS_191
H38	VSS030	E33	VSS_192
J39	VSS031	J31	VSS_193
L39	VSS032	L31	VSS_194
M38	VSS033	N31	VSS_195
N39	VSS034	AE23	VSS_196
R39	VSS035	E31	VSS_197
T38	VSS036	N31	VSS_198
U39	VSS037	AE23	VSS_199
W39	VSS038	AE21	VSS_200
Y38	VSS039	AE21	VSS_201
AA39	VSS040	AE25	VSS_202
AD38	VSS041	AE23	VSS_203
AE39	VSS043	AE23	VSS_205
AG39	VSS044	AE23	VSS_207
AH38	VSS045	AE23	VSS_208
AL39	VSS047	AE23	VSS_210
AM38	VSS048	AE23	VSS_211
AN39	VSS049	AE23	VSS_212
AR37	VSS051	AE23	VSS_214
AT38	VSS052	AE23	VSS_215
AU39	VSS053	AE23	VSS_216
AW39	VSS054	AE23	VSS_217
AX39	VSS056	AE23	VSS_219
AY37	VSS057	AE23	VSS_220
BA39	VSS058	AE23	VSS_221
BD40	VSS059	AE23	VSS_222
RD38	VSS060	AE23	VSS_223
R38	VSS061	AE23	VSS_224
D36	VSS062	AE23	VSS_225
K34	VSS064	AE23	VSS_227
M34	VSS065	AE23	VSS_228
M36	VSS066	AE23	VSS_229
P34	VSS067	AE23	VSS_230
T34	VSS068	AE23	VSS_231
V34	VSS069	AE23	VSS_232
T36	VSS070	AE23	VSS_233
Y34	VSS071	AE23	VSS_234
AB34	VSS072	AE23	VSS_235
AD34	VSS073	AE23	VSS_236
AD36	VSS074	AE23	VSS_237
AE34	VSS075	AE23	VSS_238
AH34	VSS077	AE23	VSS_240
AH36	VSS078	AE23	VSS_241
AK34	VSS079	AE23	VSS_242
AM34	VSS080	AE23	VSS_243
AP34	VSS081	AE23	VSS_244
		E21	VSS_245
		E21	VSS_246
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		E21	VSS_279
		E21	VSS_280



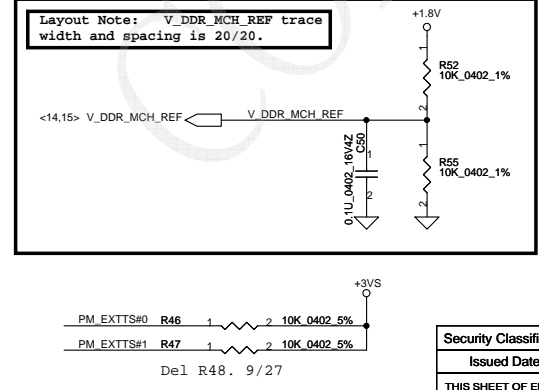
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layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



layout note:
Place them close to U4 pin BC51.

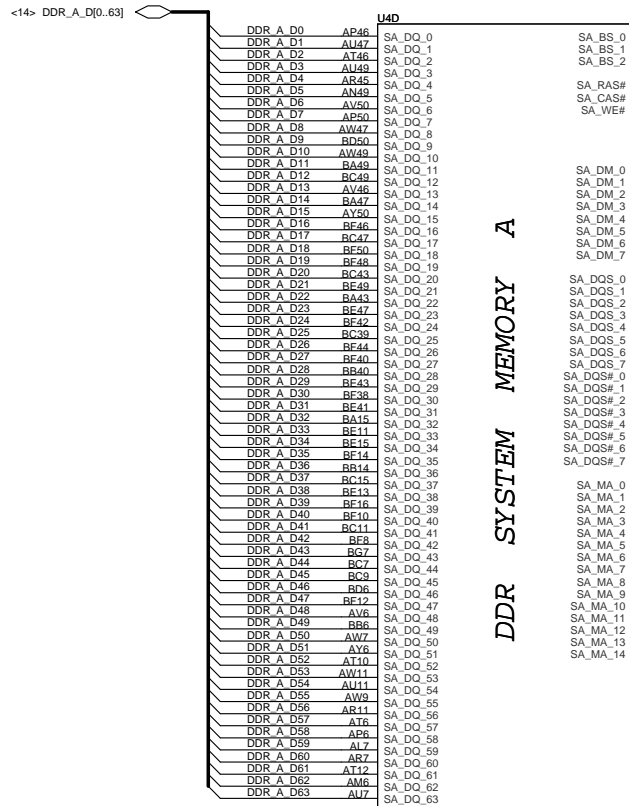


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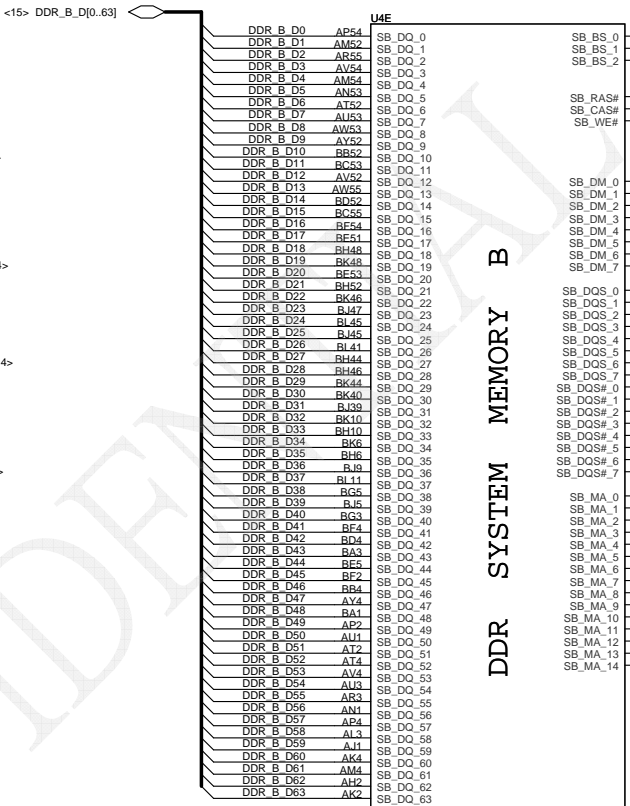
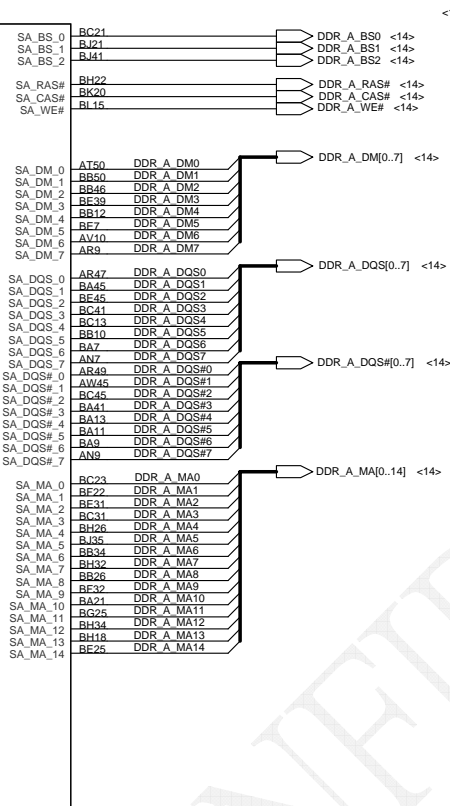
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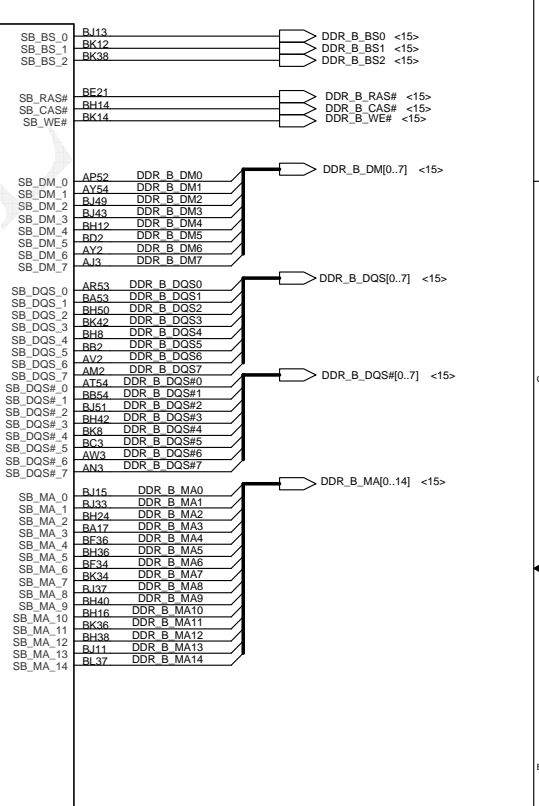
CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY A



CANTIGA GMCH SFF_FCBGA1363

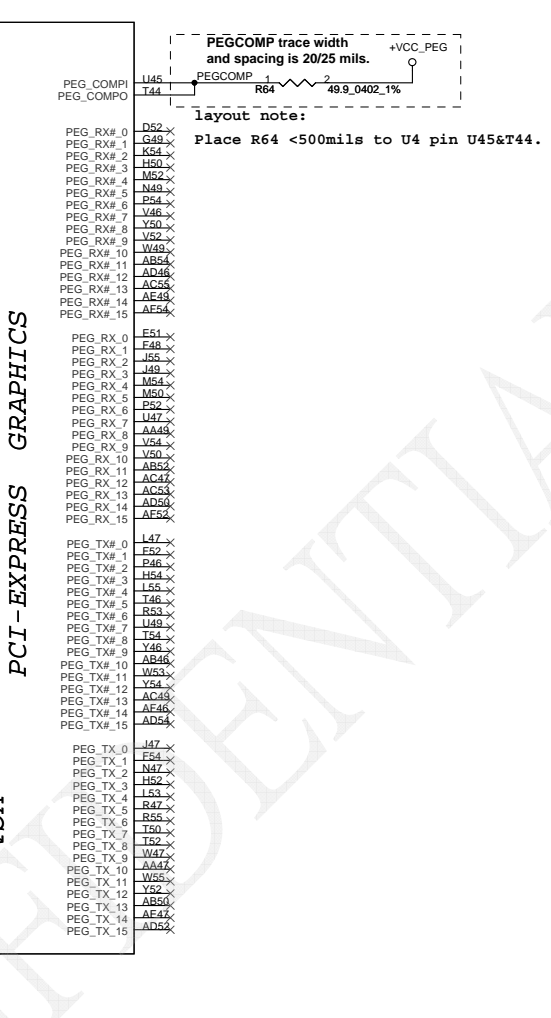
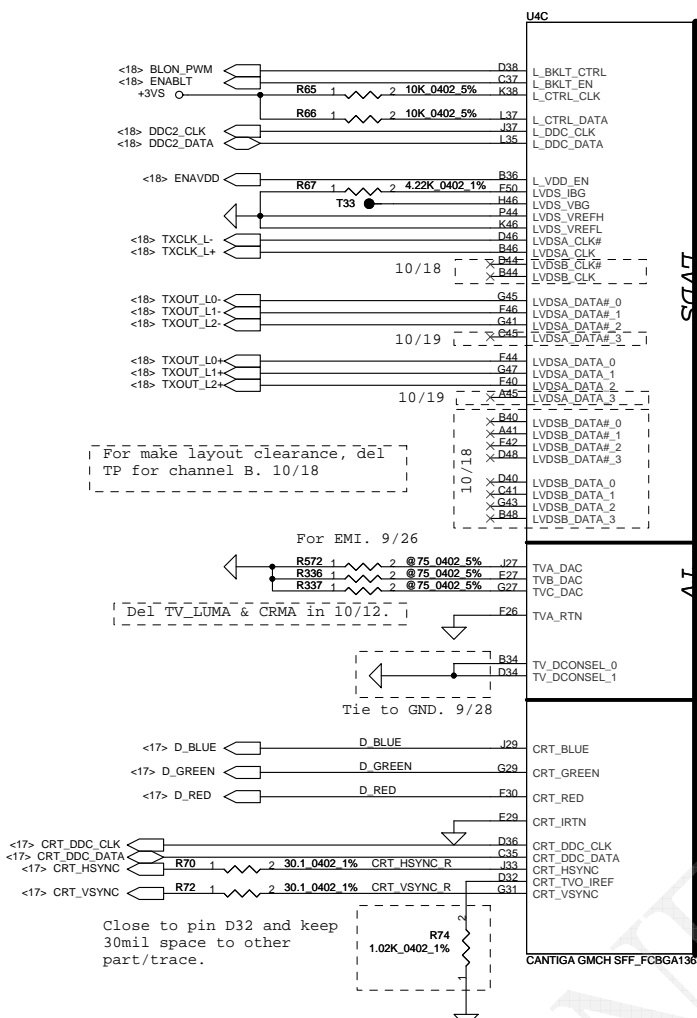
DDR SYSTEM MEMORY B



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Strap Pin is

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



PEGCOMP trace width and spacing is 20/25 mils.

layout note:
Place R64 <500mils to U4 pin U45&T44.

For make layout clearance, del TP for channel B. 10/18

For EMI. 9/26

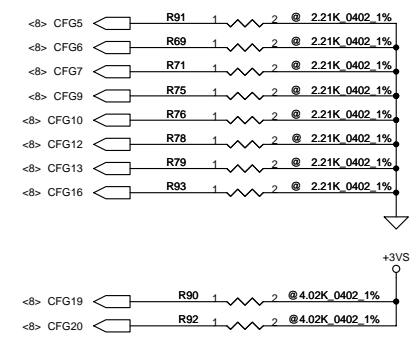
Del TV_LUMA & CRMA in 10/12.

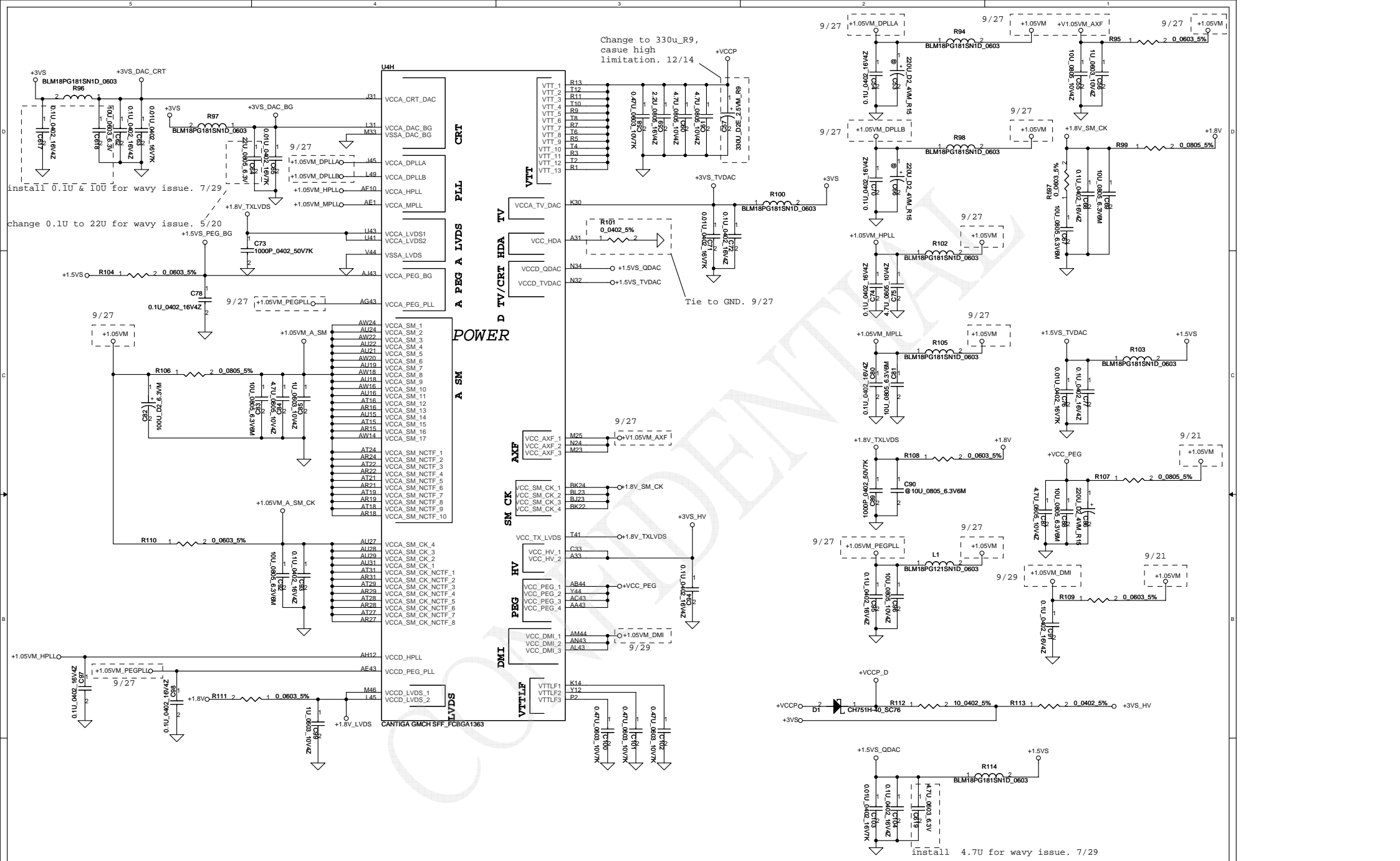
Tie to GND. 9/28

Close to pin D32 and keep 30mil space to other part/trace.

Remove R84 ~ R86 since already have 75ohm of page17. 10/27

Del R82, R83. 10/18

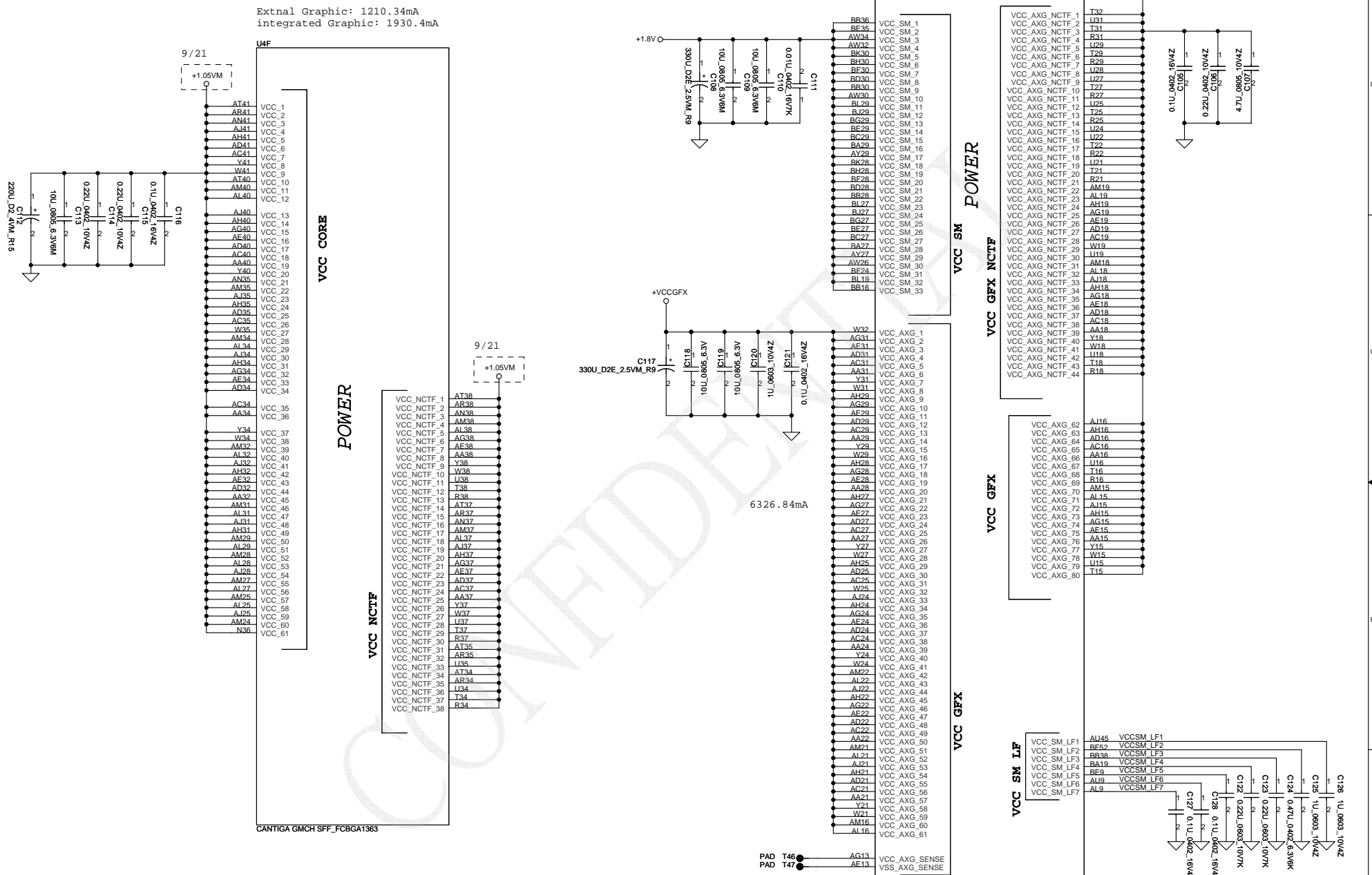




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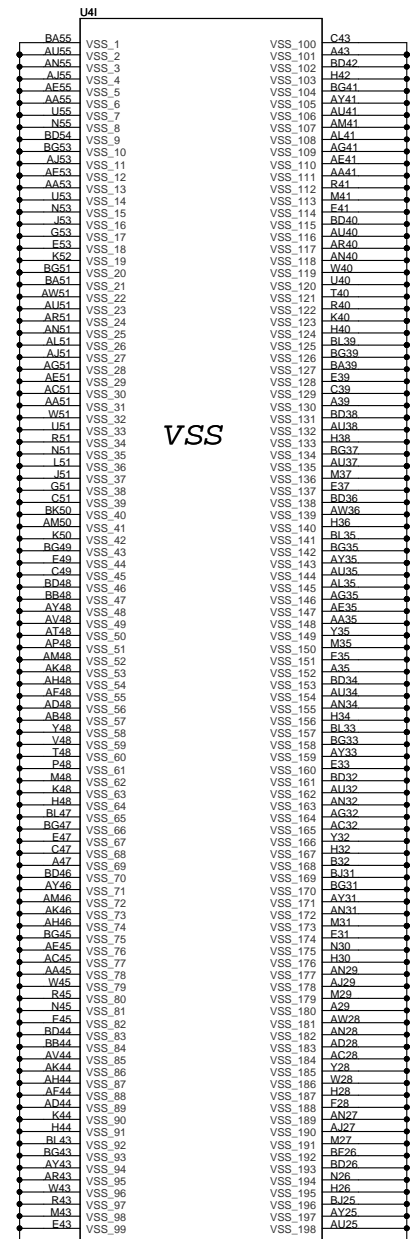
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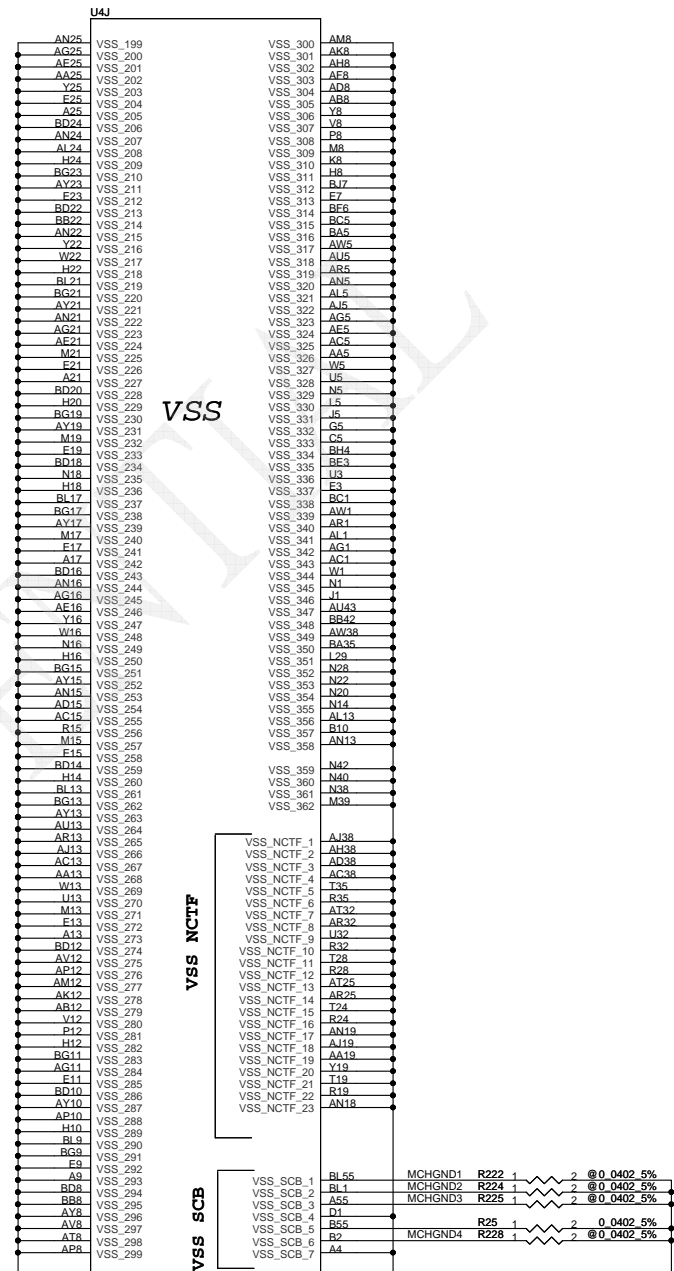
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VSS

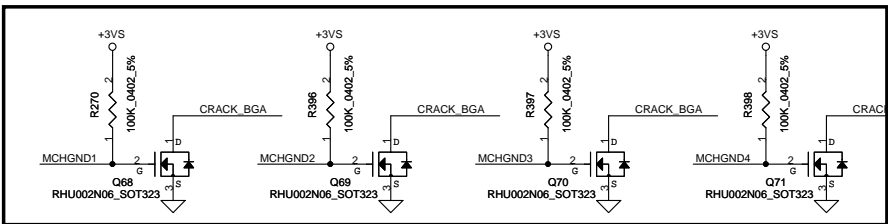
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VSS

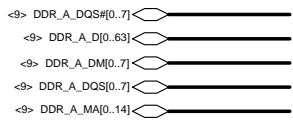
VSS NCTF

VSS SCB

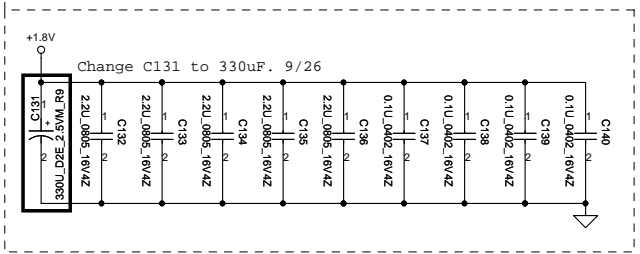


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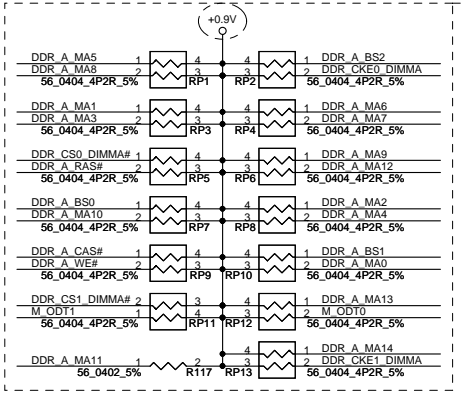
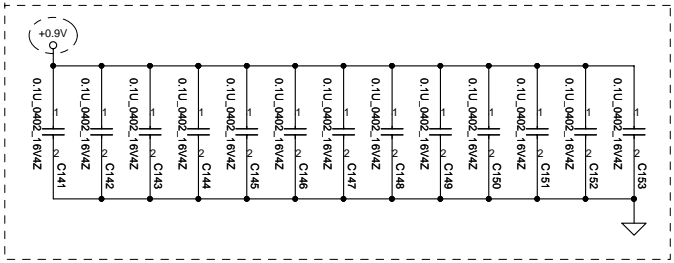
SCHEMATIC, M/B LA-4021P



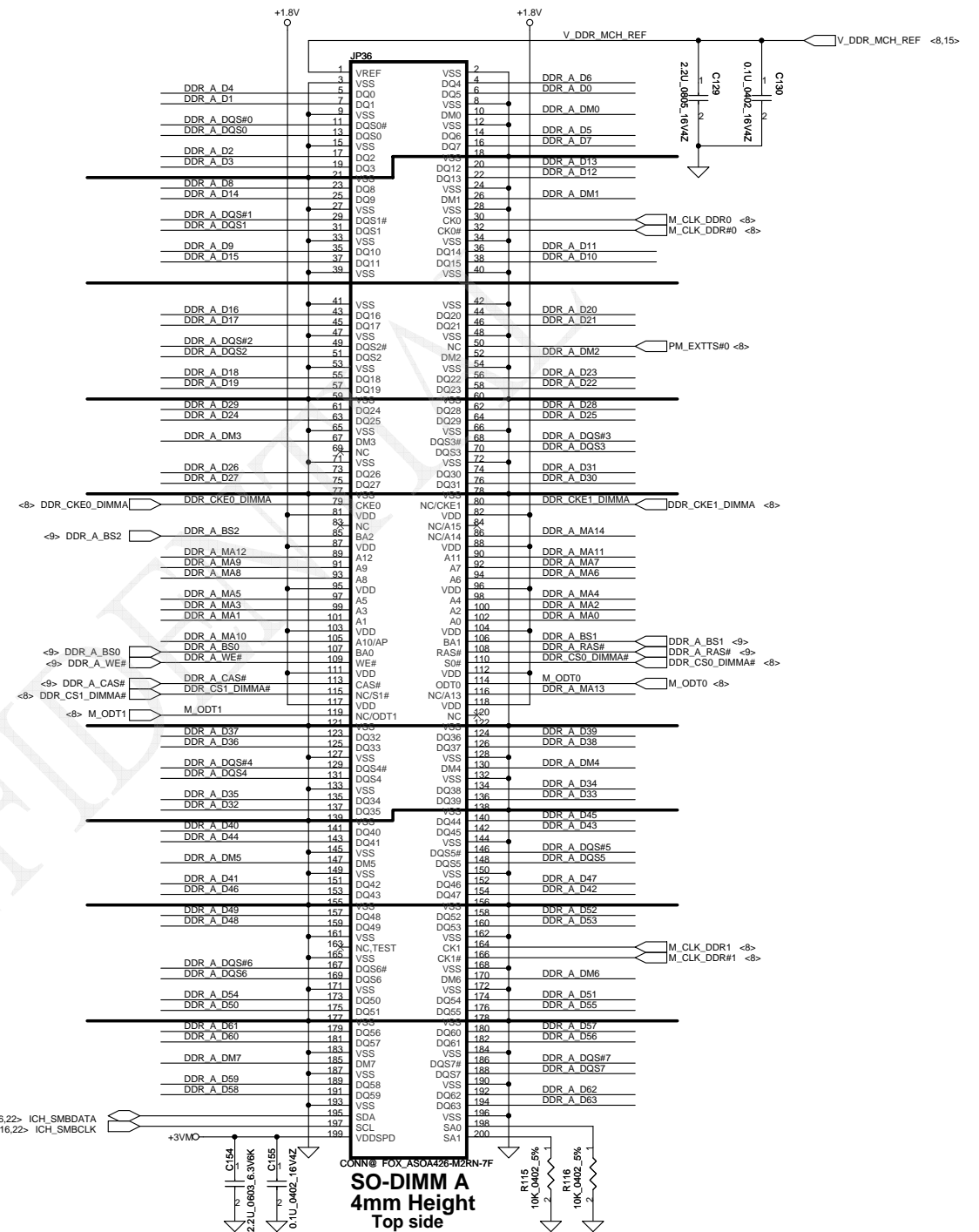
Layout Note:
Place near JP36



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



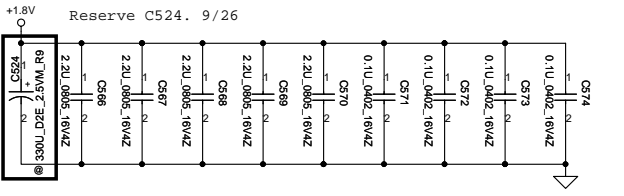
Layout Note:
Place these resistor closely JP9, all trace length Max=1.5"



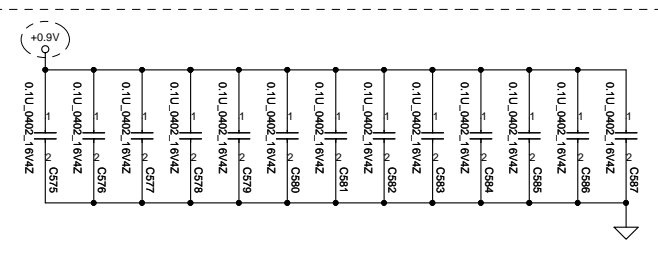
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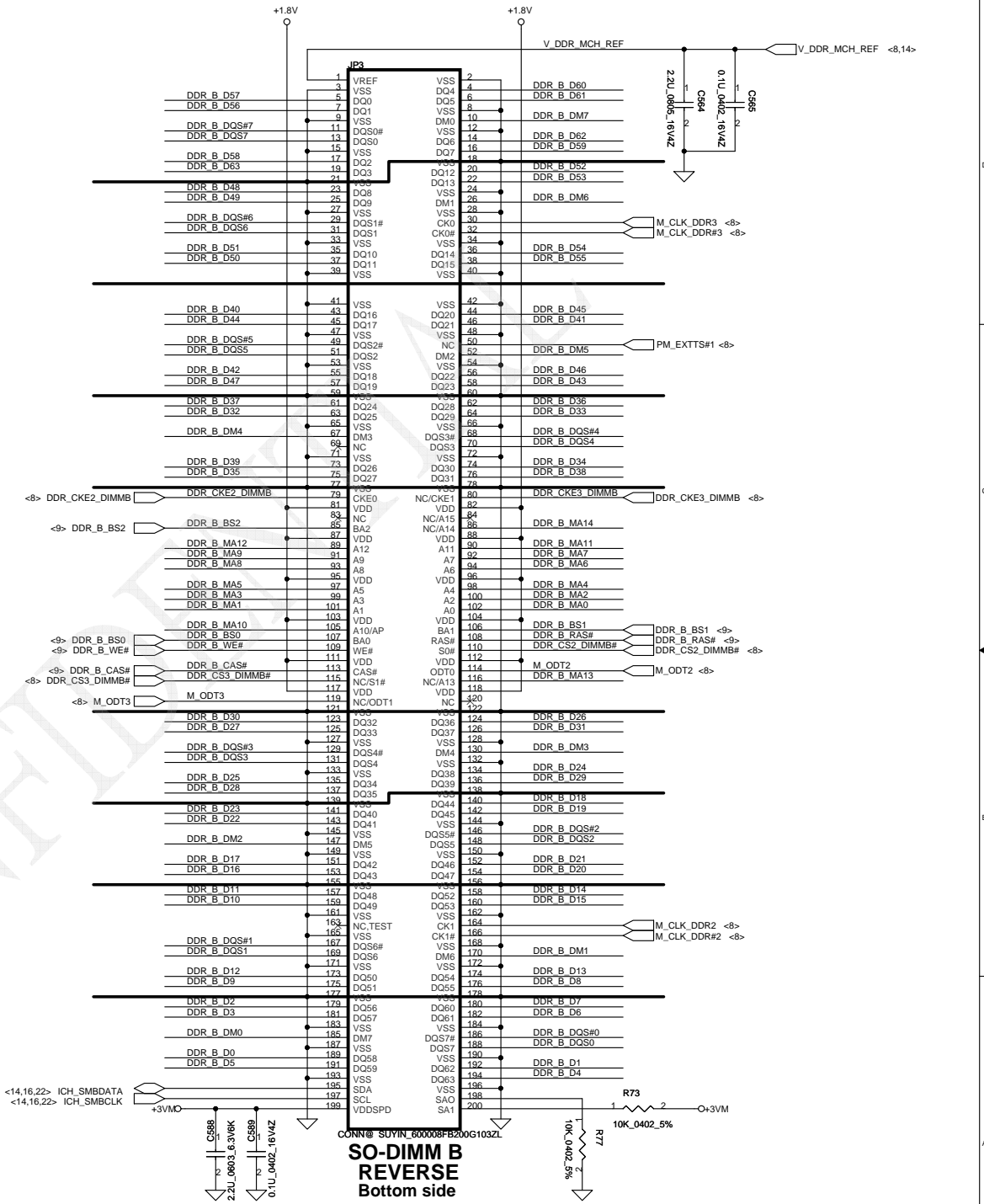
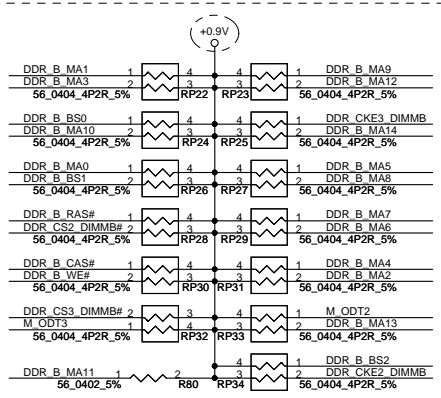
Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

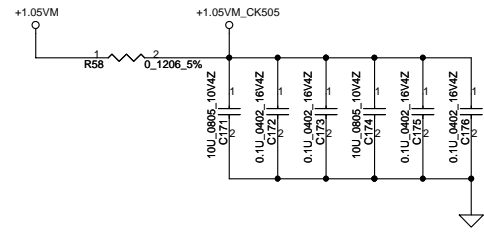
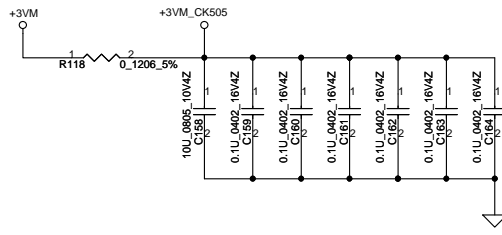


Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



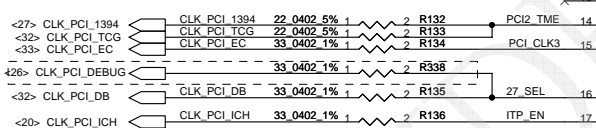
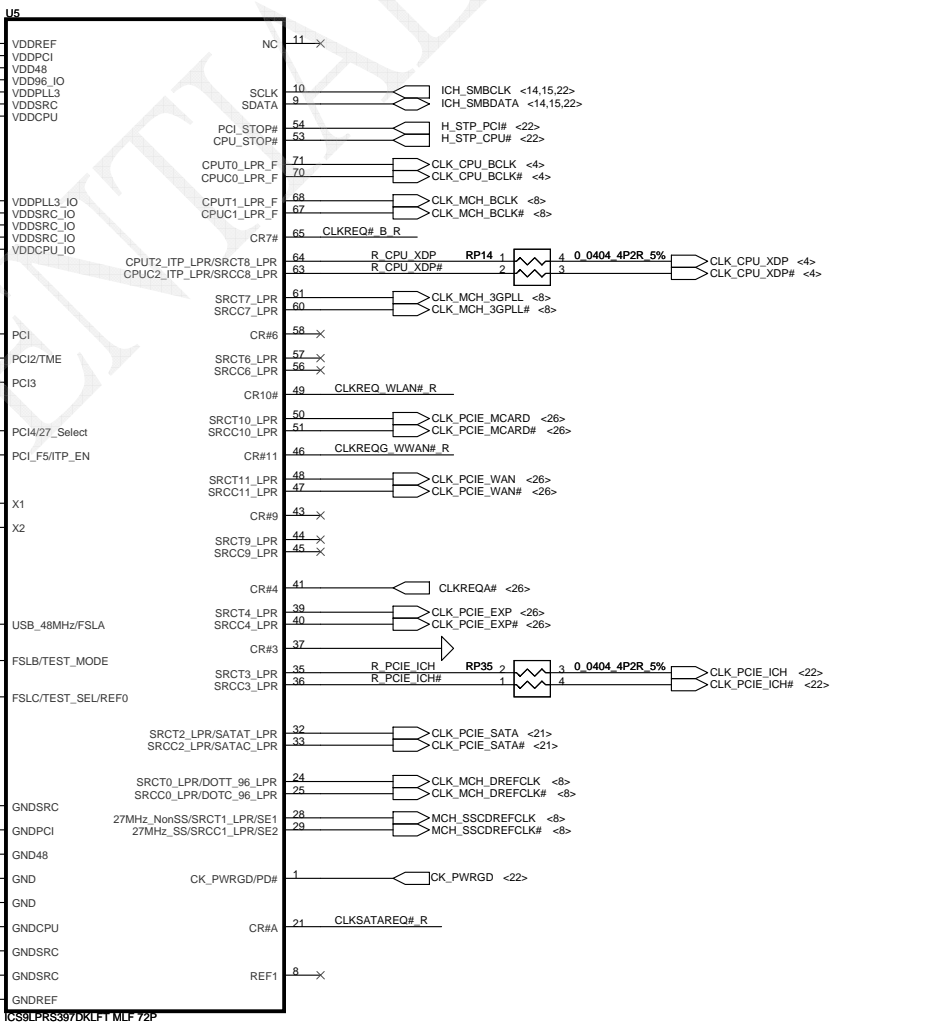
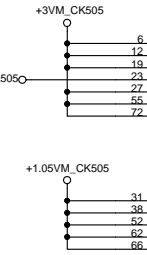
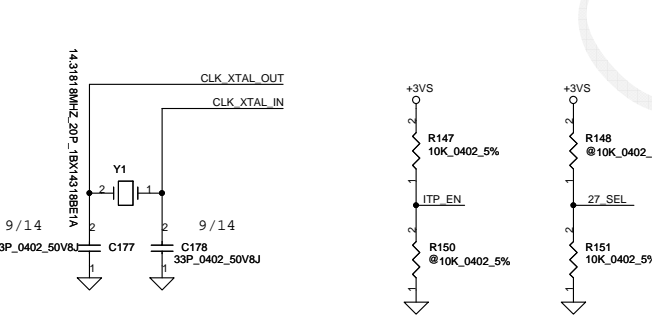
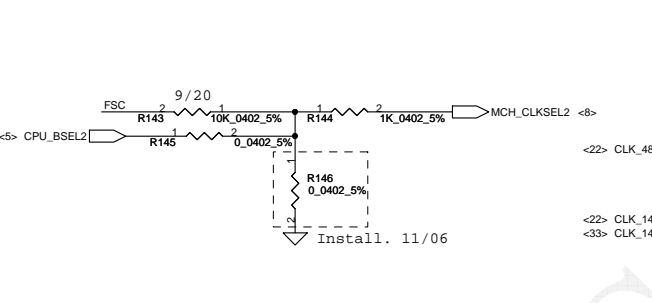
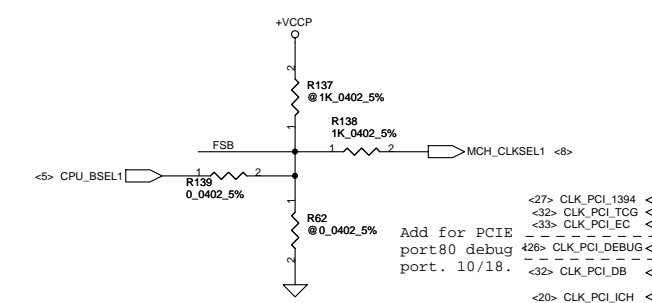
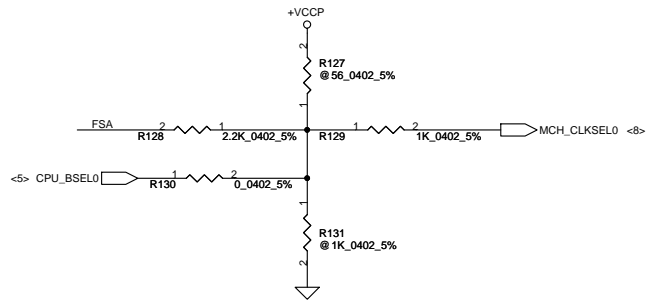
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



Component	Value	Location
C156	2	1 CLK_48M_ICH @ 5P_0402_50V8C
C157	1	2 CLK_14M_ICH 12P_0402_50V8J
C165	2	1 CLK_PCI_ICH @ 4.7P_0402_50V8C
C166	1	1 12P_0402_50V8J
C167	2	1 CLK_PCI_EC @ 4.7P_0402_50V8C
C168	2	1 CLK_PCI_TCG @ 4.7P_0402_50V8C
C169	2	1 CLK_PCI_1394 @ 5P_0402_50V8C
C170	2	1 CLK_PCI_DB @ 5P_0402_50V8C

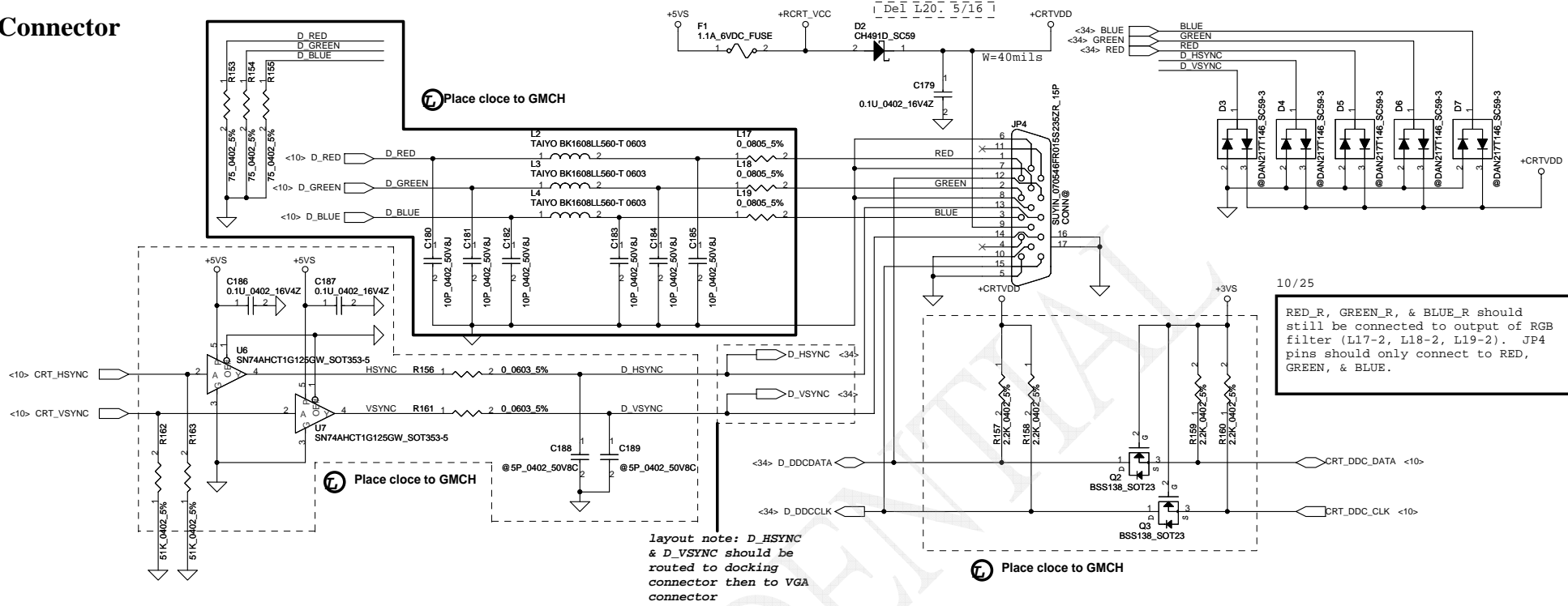
Mount C157 & C166 top solve WWAN noise issue. 1/23
Place close to U5



Add for PCIe port80 debug port. 10/18.

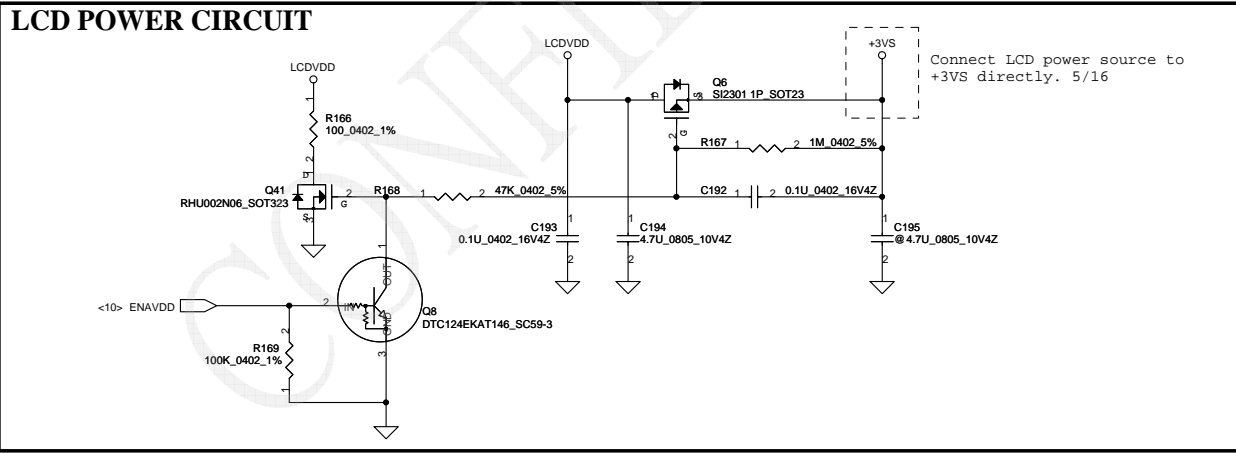
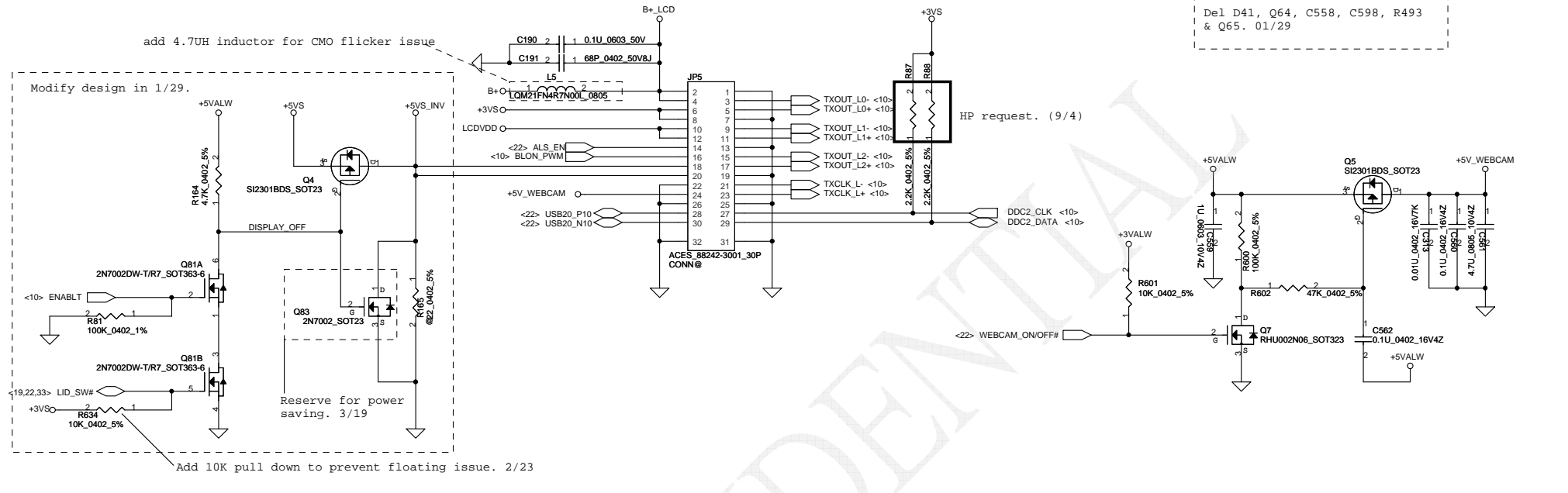
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CRT Connector

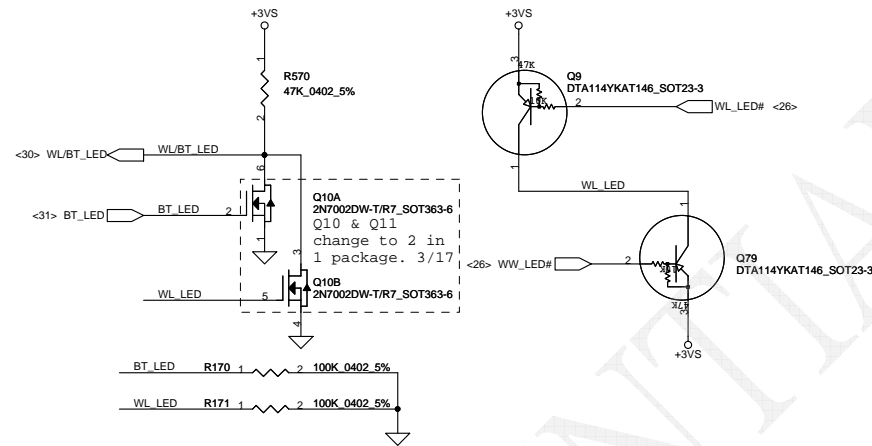


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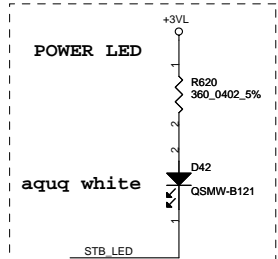
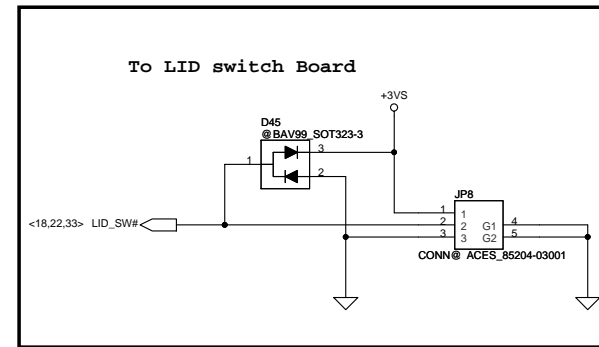
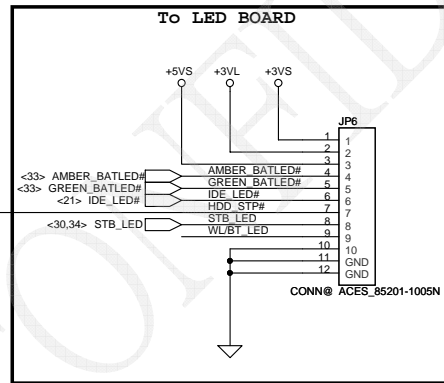
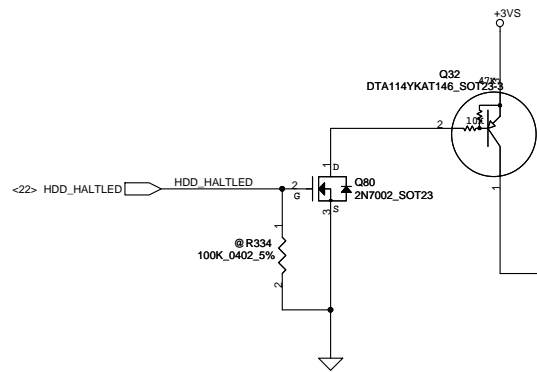
LCD/PANEL BD. CONN.



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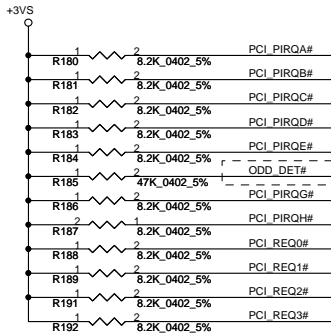
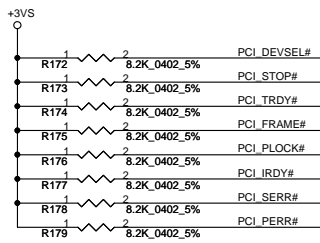


Cause space issue, move them from LED board to M/B. 10/09



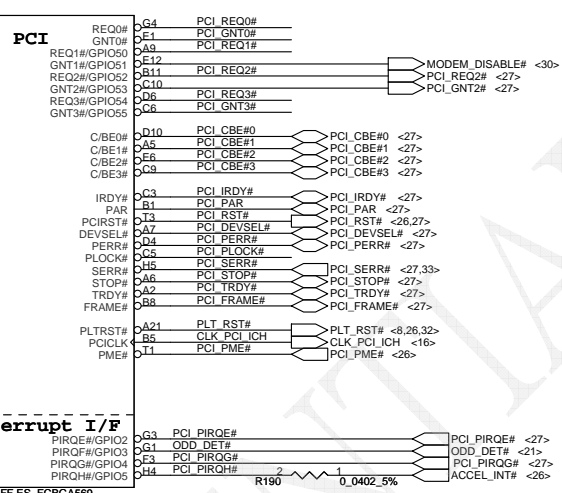
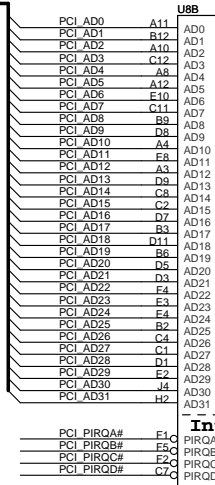
Add in 11/28.
Place them close to SW1.

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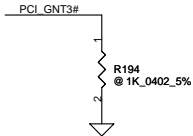


Change to ODD_DET#. 10/18

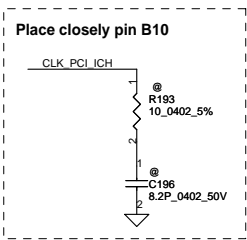
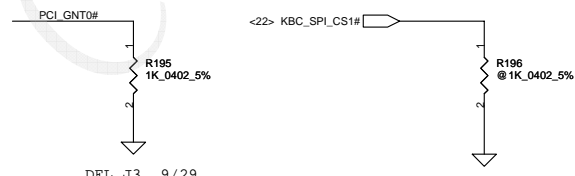
<27> PCI_AD[0..31]



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default*

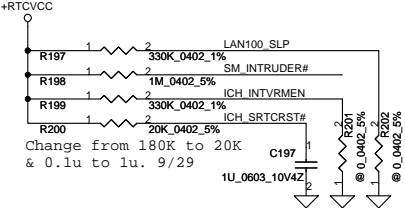


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

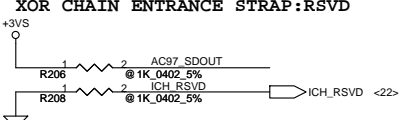


DEL J3. 9/29

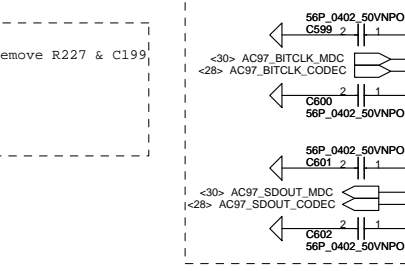
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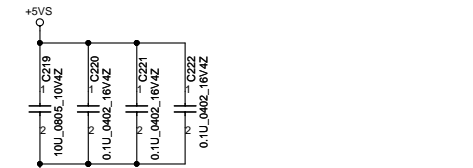
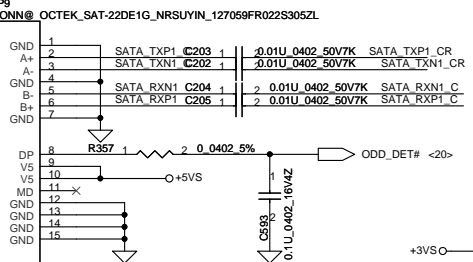
ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal (D)
1	1	PCIE Bit



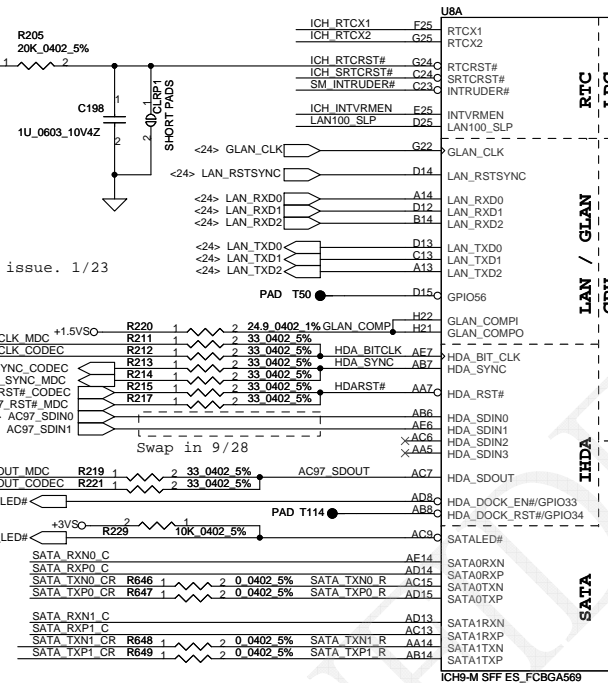
Add C599 ~ C602 to solve WWAN noise issue. 1/23



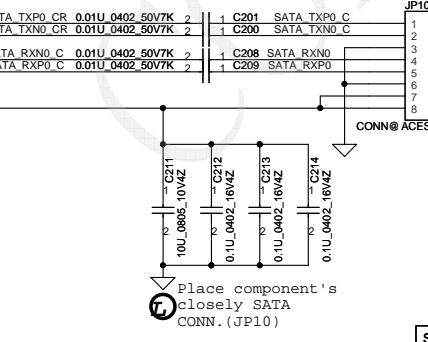
SATA CD-ROM Connector



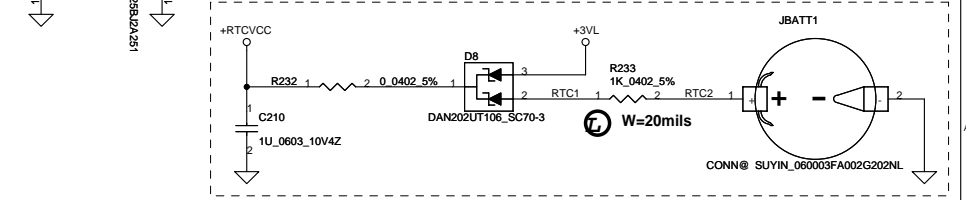
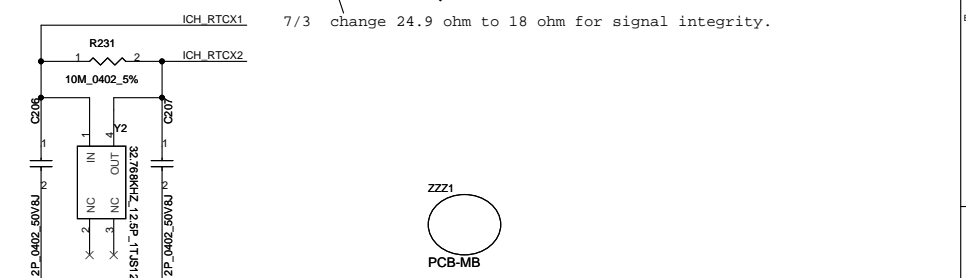
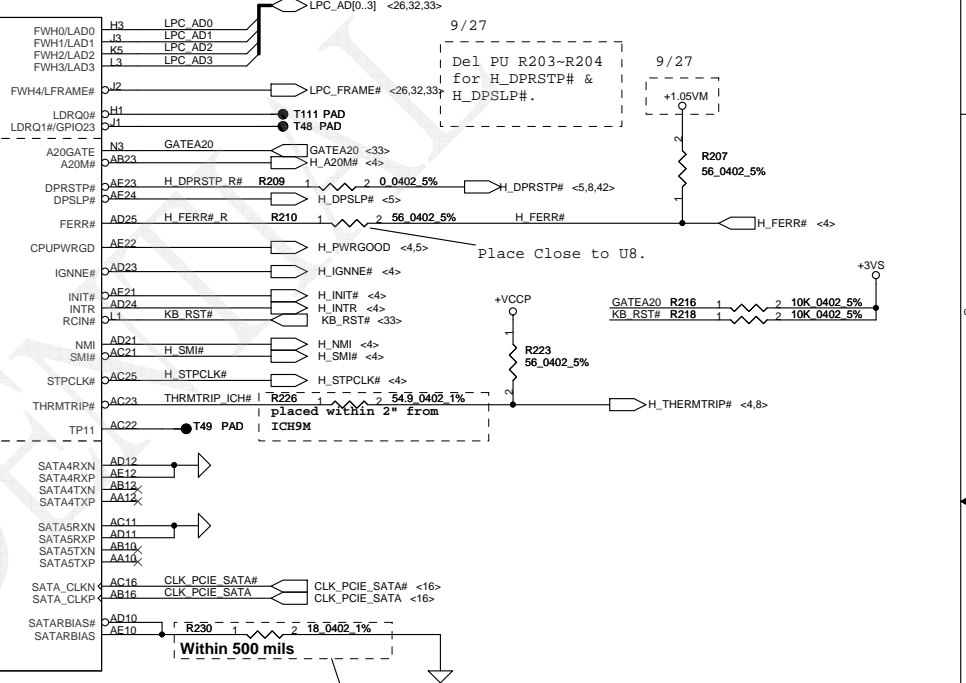
Place component's closely SATA CONN. (JP9)



1.8" SATA HDD CONN

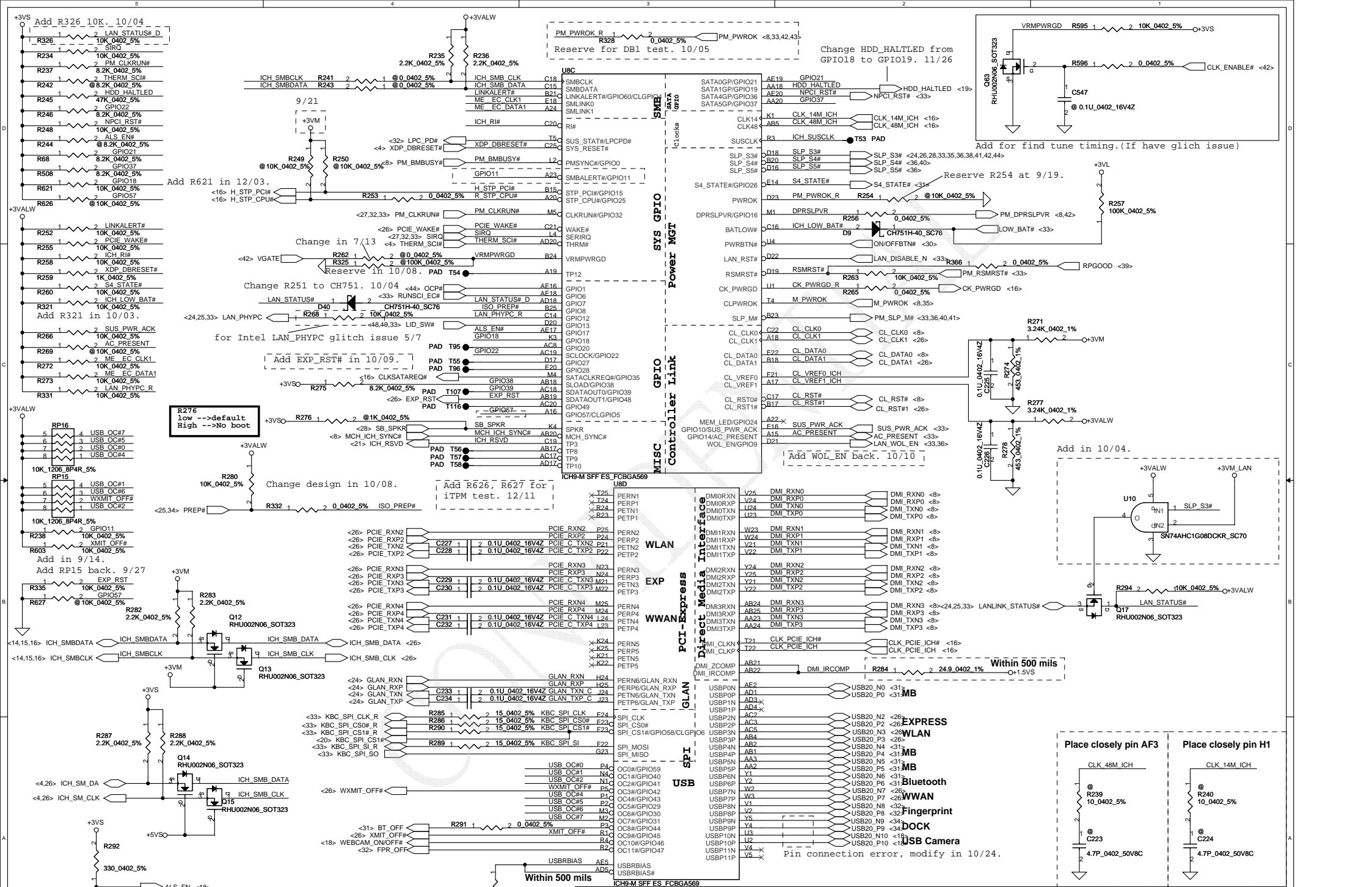


Place component's closely SATA CONN. (JP10)



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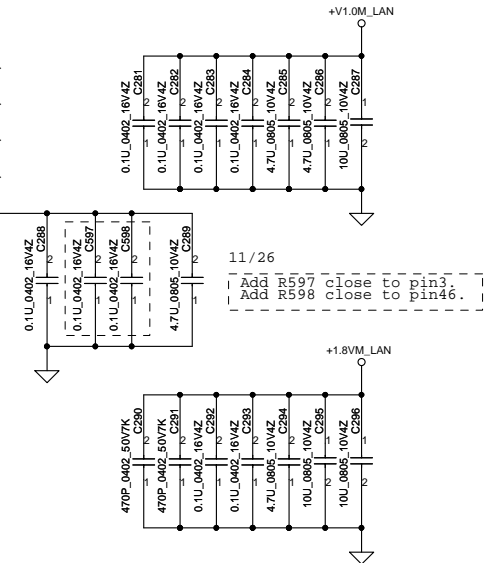
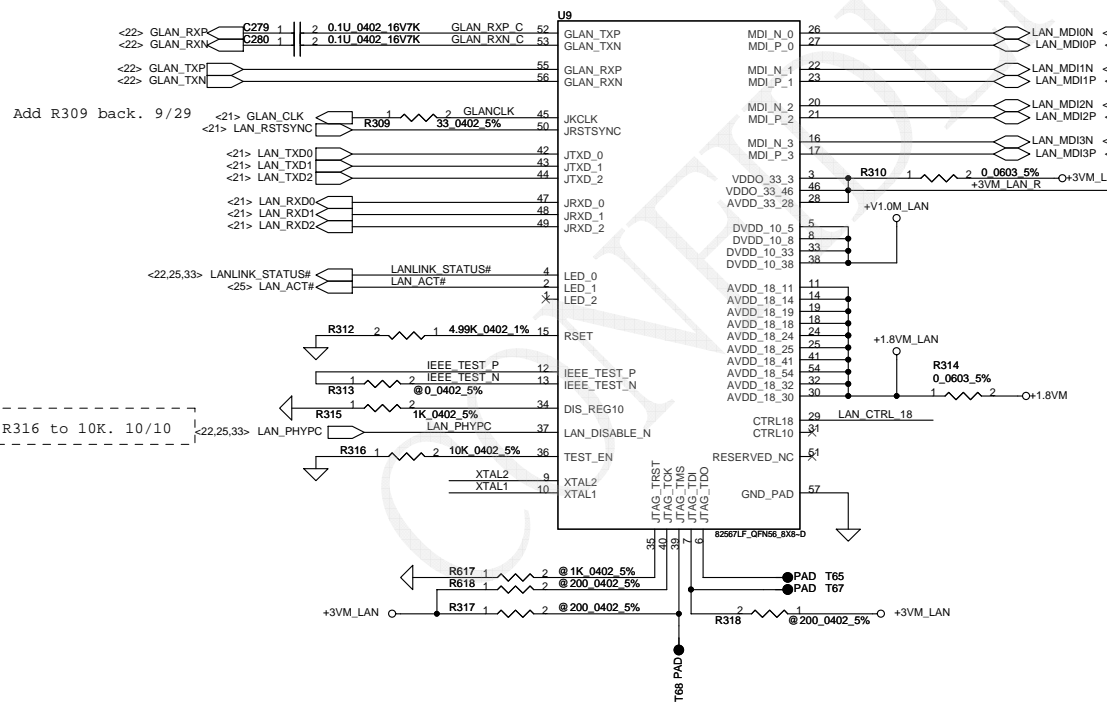
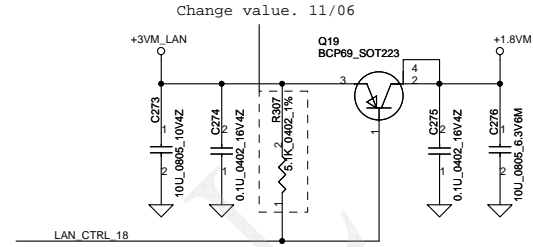
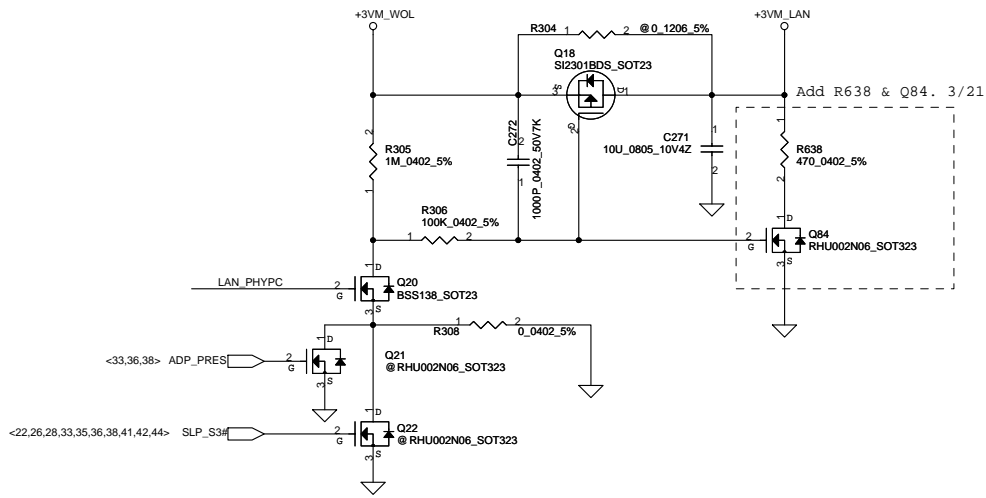


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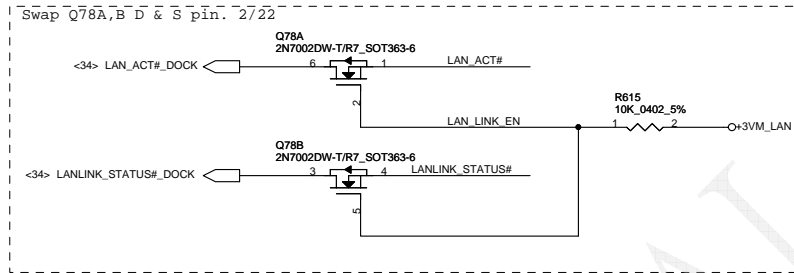
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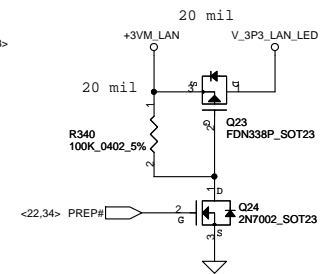
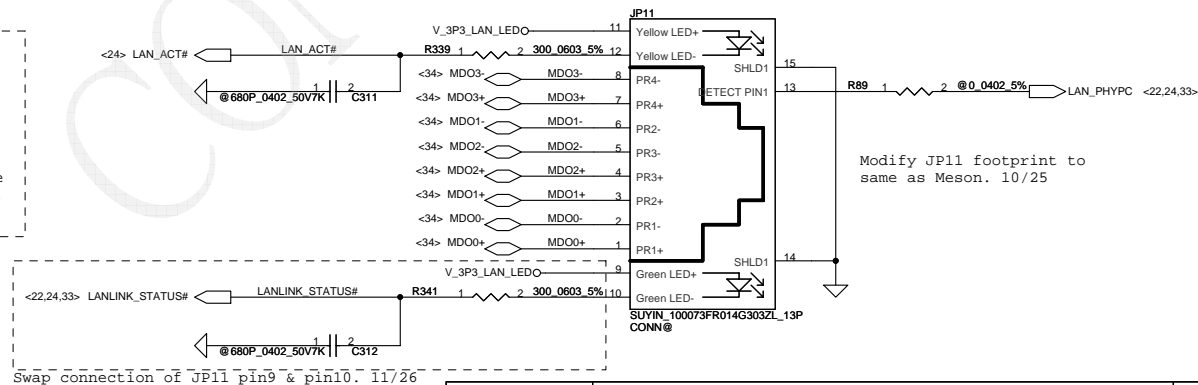
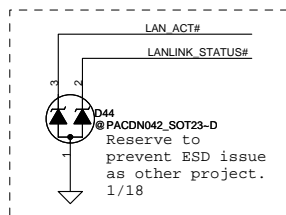
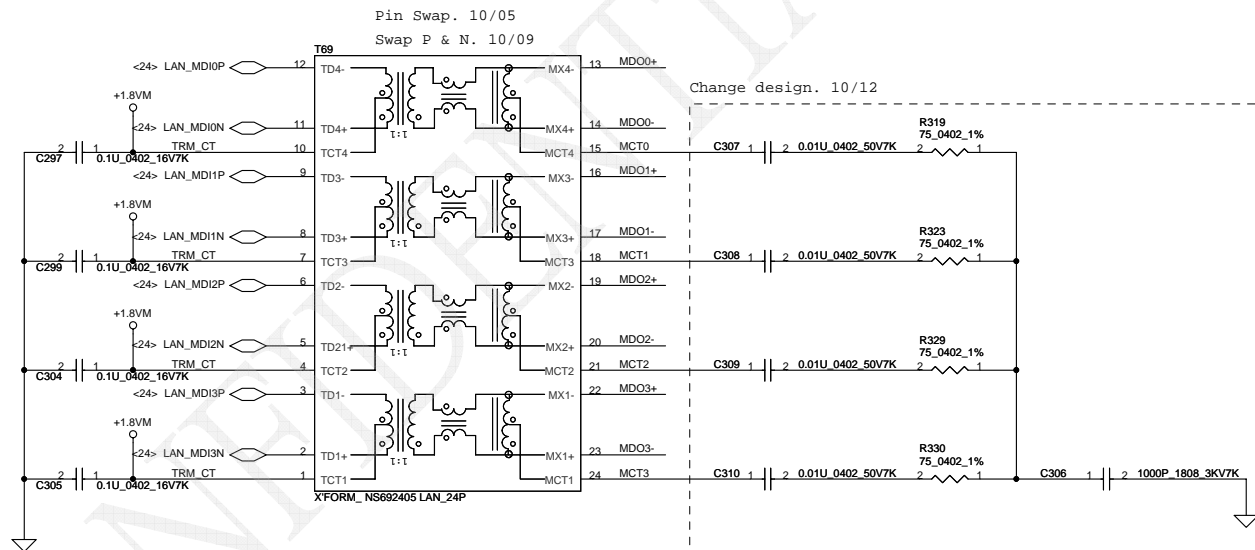
Rev B



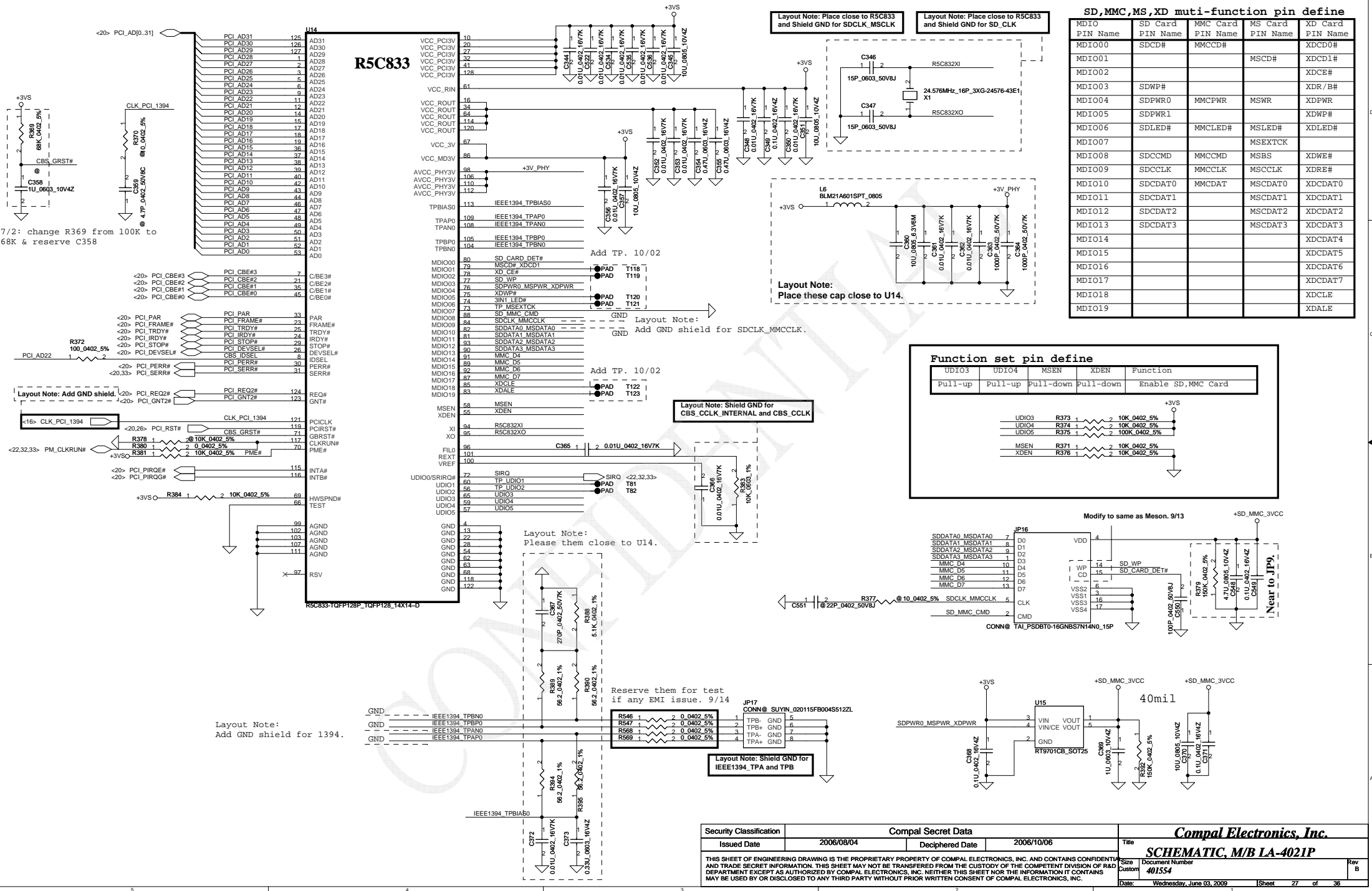
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Delete all termination cause they are already inside BOAZMAN. 9/28



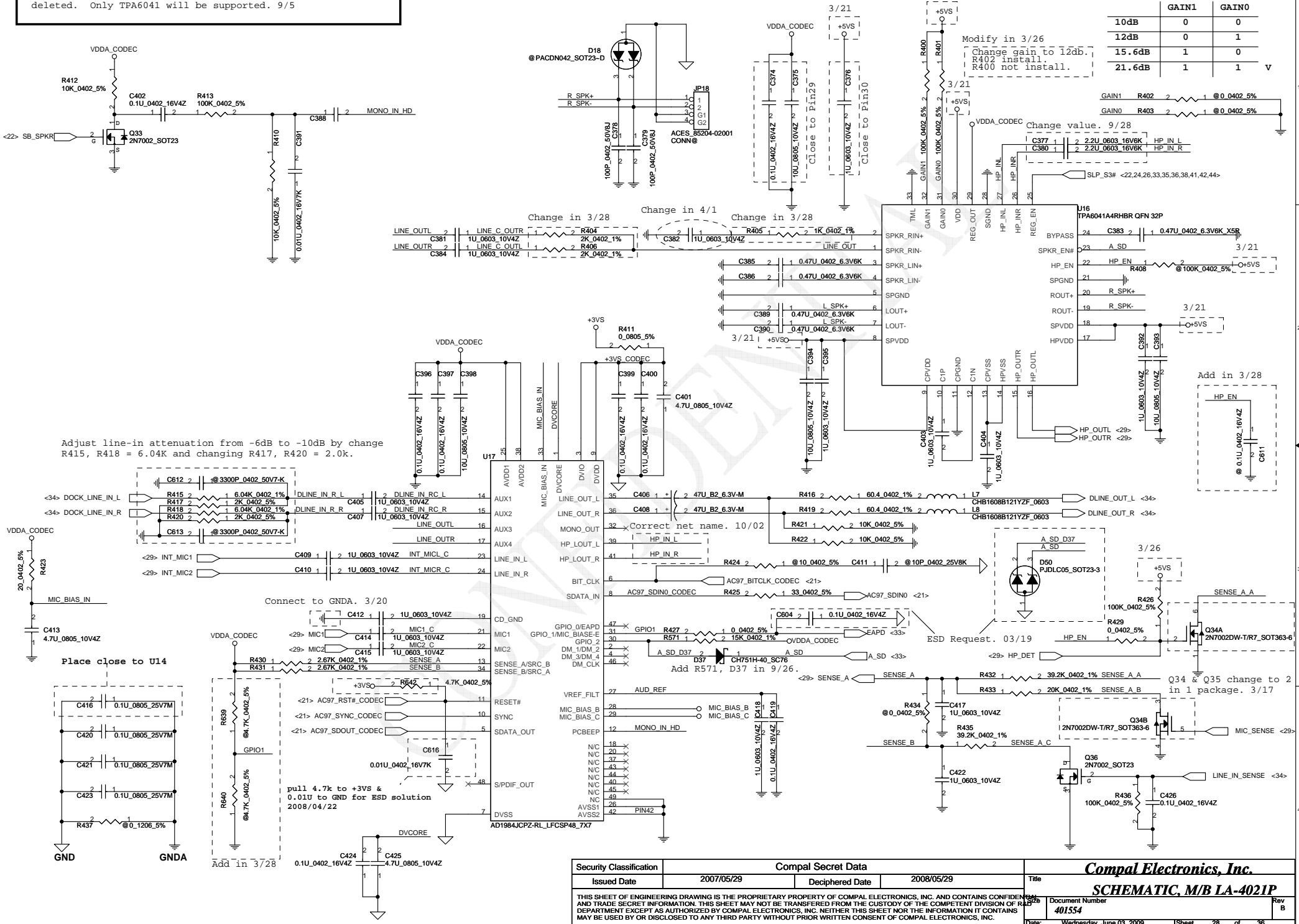
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			<p>Sheet 25 of 36</p> <p>Rev B</p>



TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

AMP. FOR INTERNAL SPEAKER

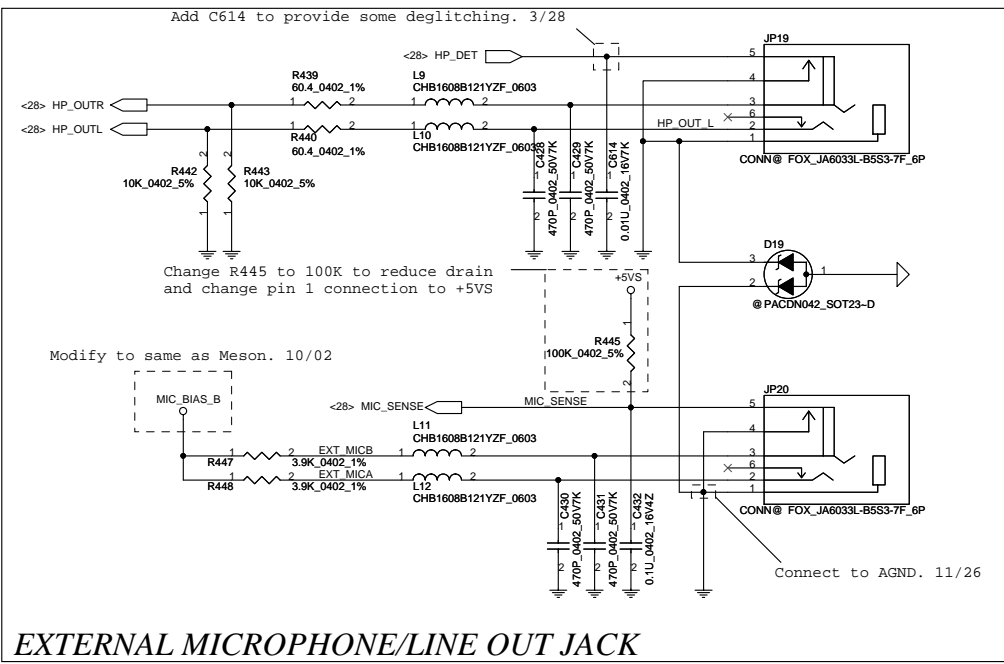
	GAIN1	GAIN0
10dB	0	0
12dB	0	1
15.6dB	1	0
21.6dB	1	1



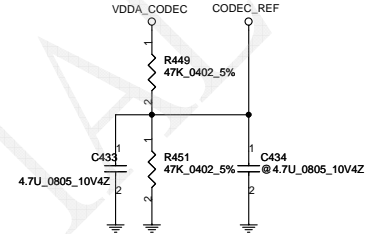
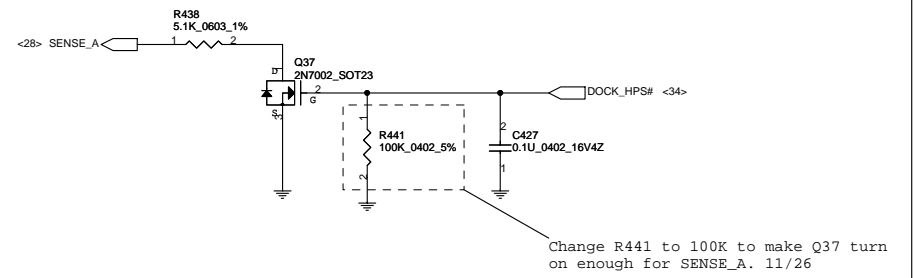
Security Classification	Compal Secret Data	
Issued Date	2007/05/29	Deciphered Date
		2008/05/29

Compal Electronics, Inc.	
Title	SCHMATIC, M/B LA-4021P
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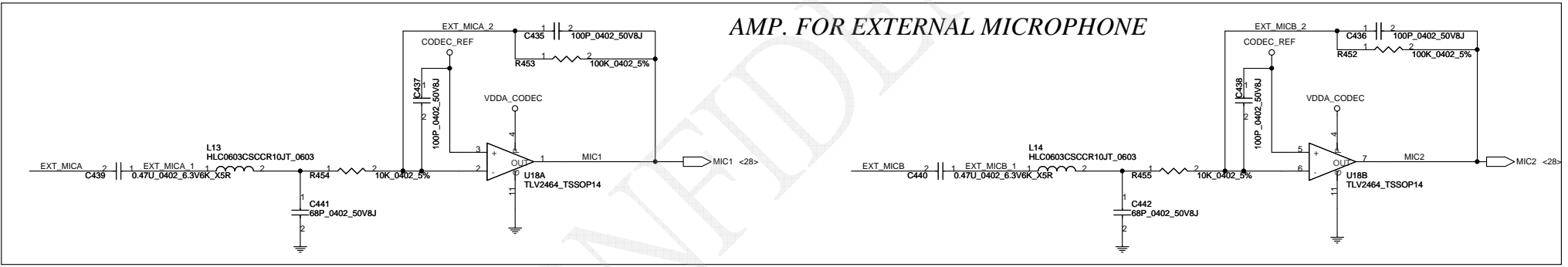
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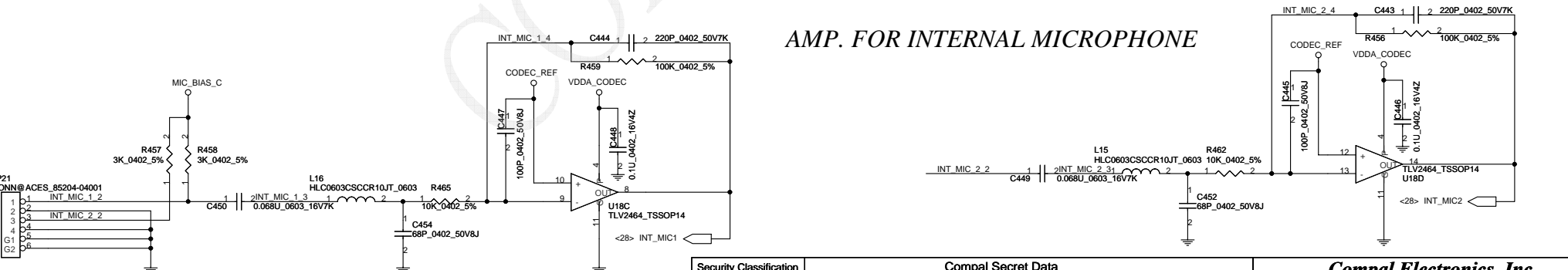
EXTERNAL MICROPHONE/LINE OUT JACK



AMP. FOR EXTERNAL MICROPHONE

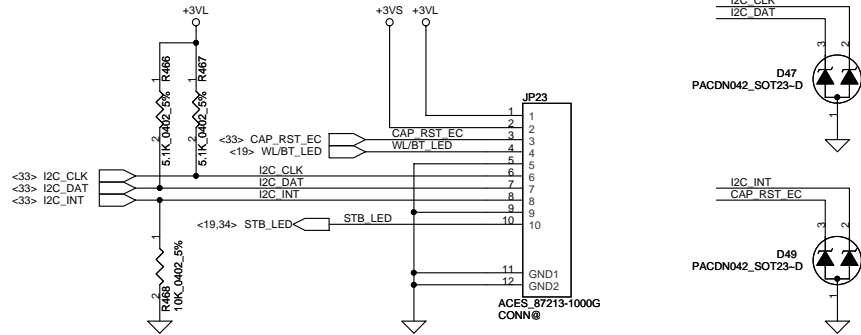


AMP. FOR INTERNAL MICROPHONE

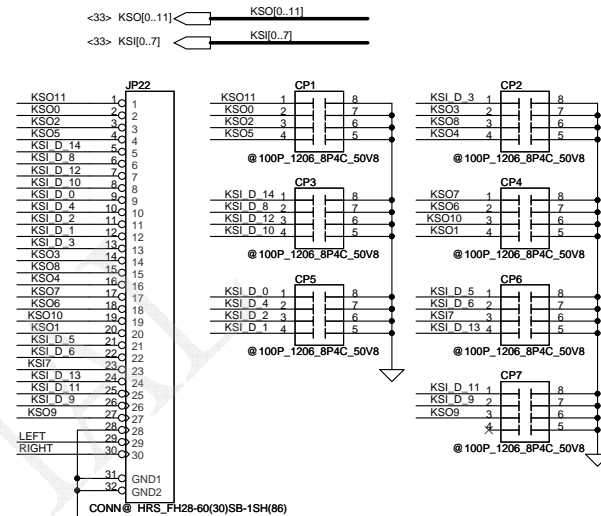


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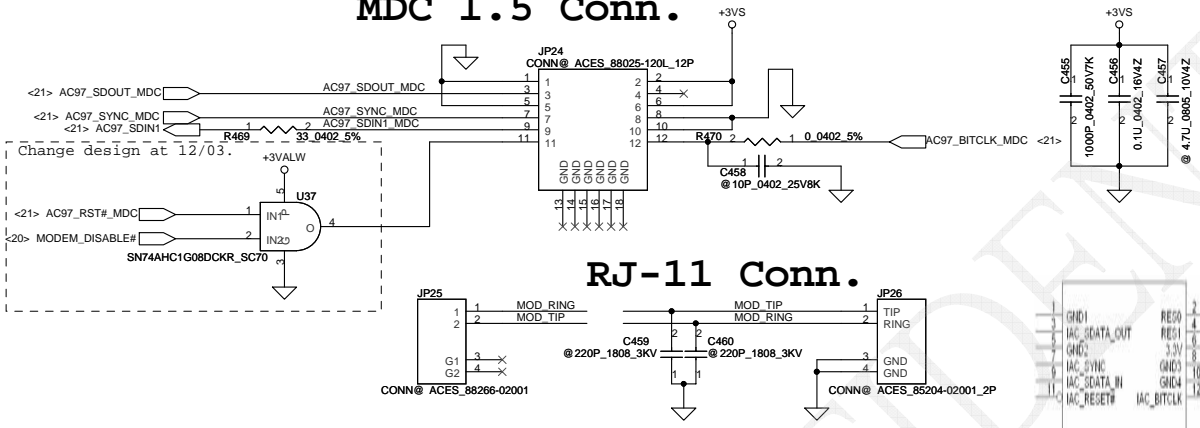
SWITCH BOARD.



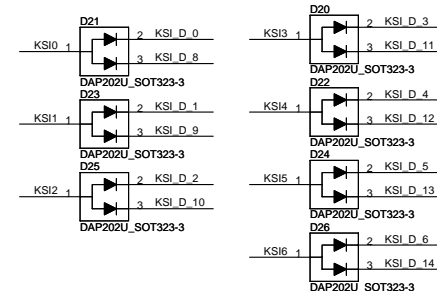
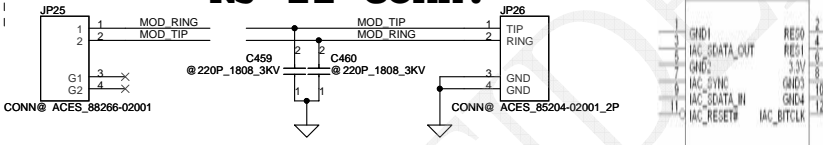
INT_KBD CONN.



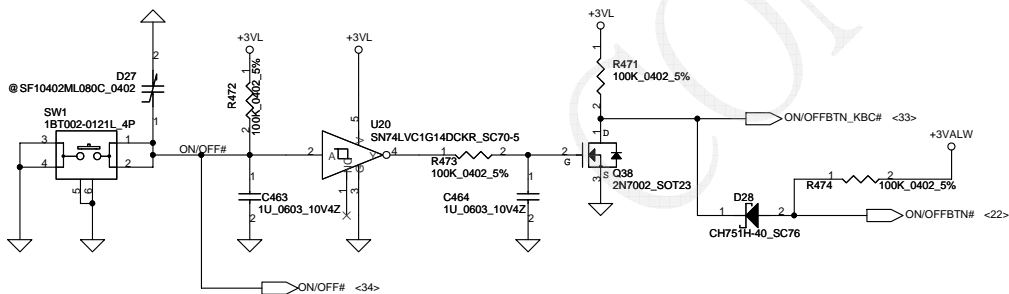
MDC 1.5 Conn.



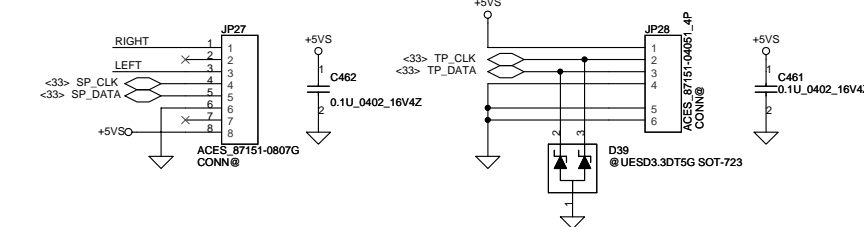
RJ-11 Conn.



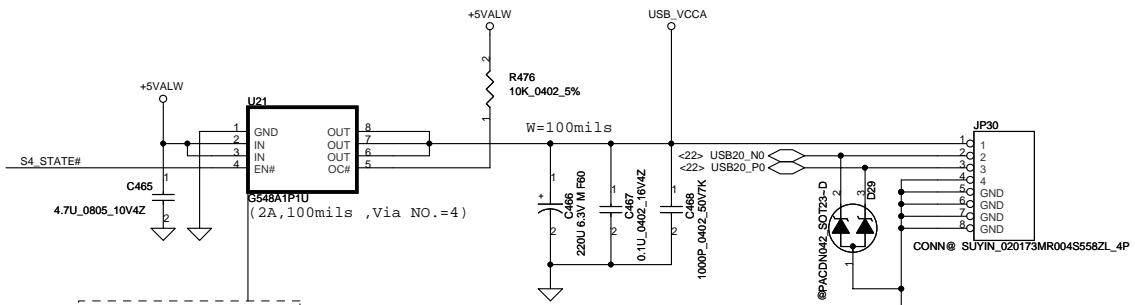
Power button



TrackPoint CONN. T/P BOARD.

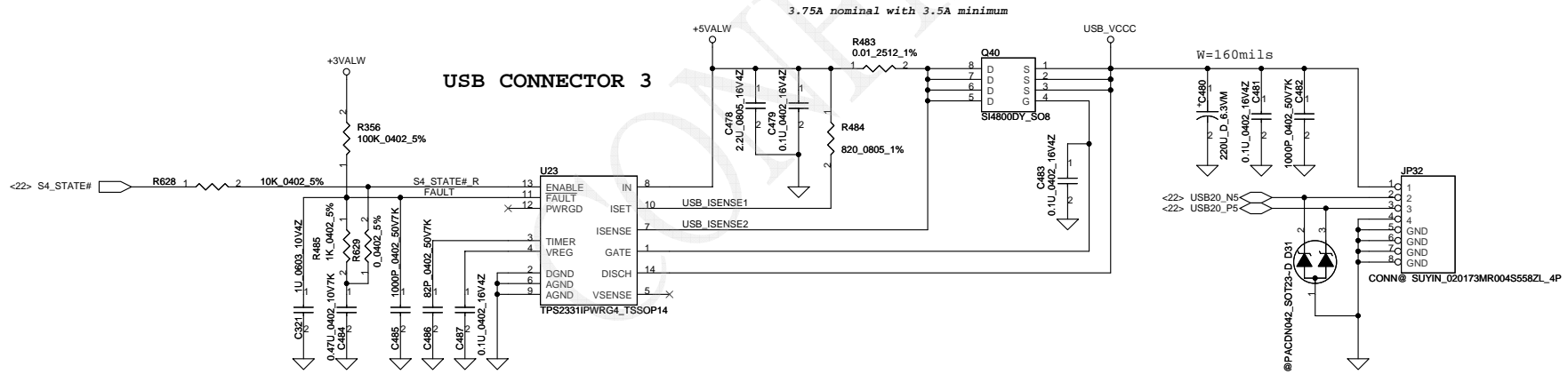
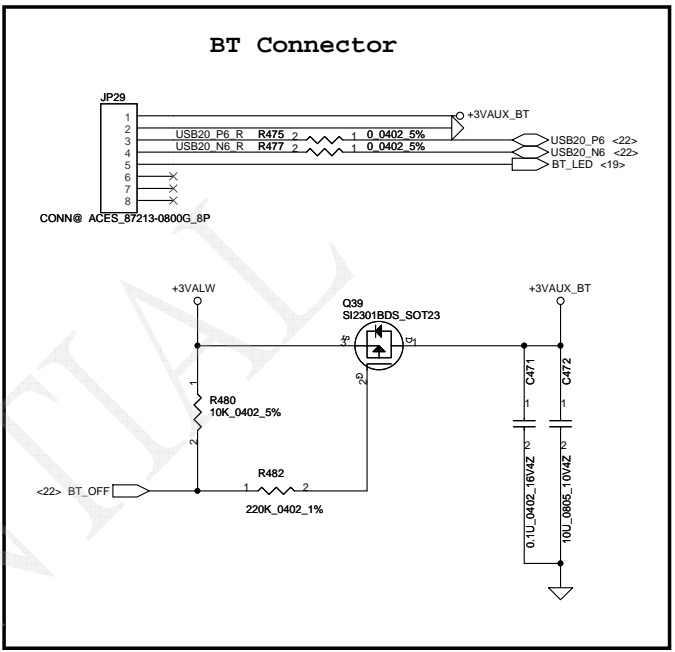
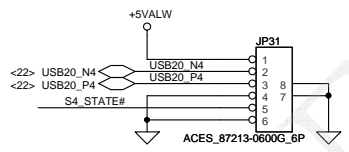


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Change U21 to active high part. 12/11

U22, D30, R481, C474 ~ C477 will move to USB board side to save M/B space.



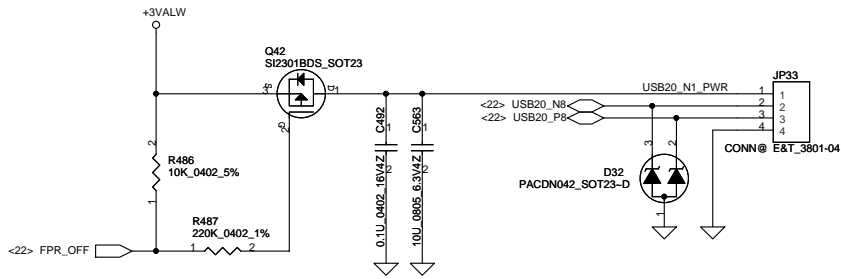
Change for S11 to prevent USB power short to GND cause system shutdown. 0130

Change C486 from 2200pF to 680pF.
 Change C321 from 1000pF to 1uF.
 Change R356 from 10K to 100K.
 Change R484 from 1000pF to 0.47uF.
 Change R484 from 1K to 820.

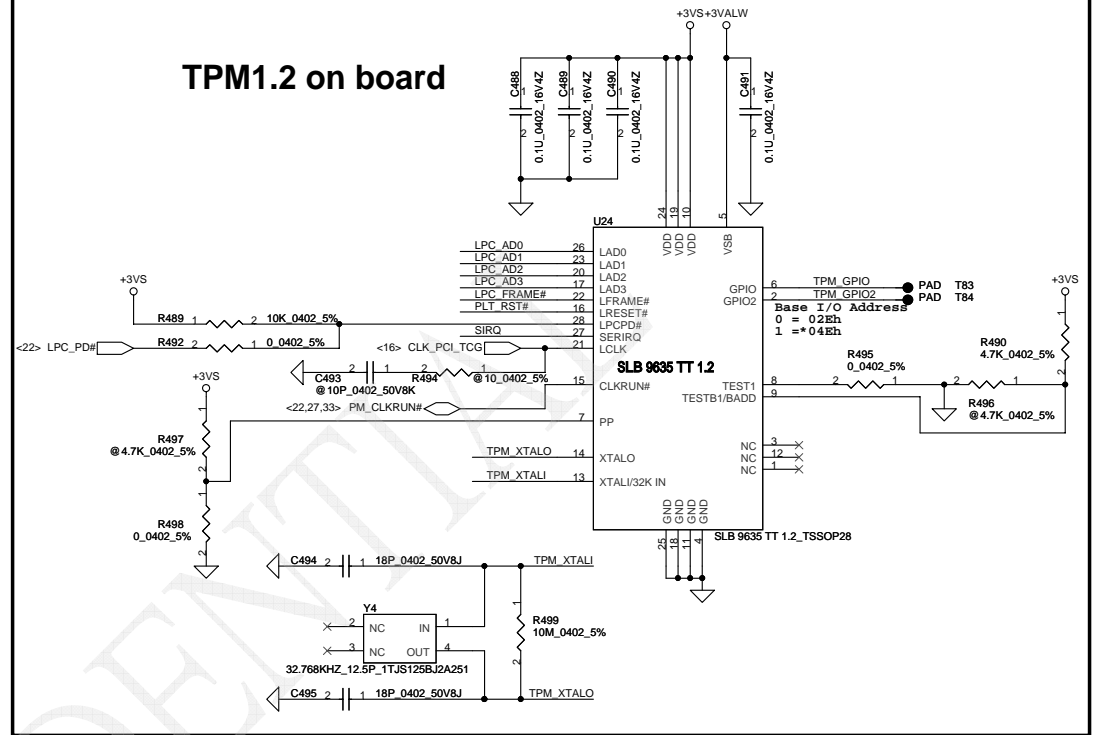
Currently power USB will not enable after OCP, so add R629 make it enable after OCP free.

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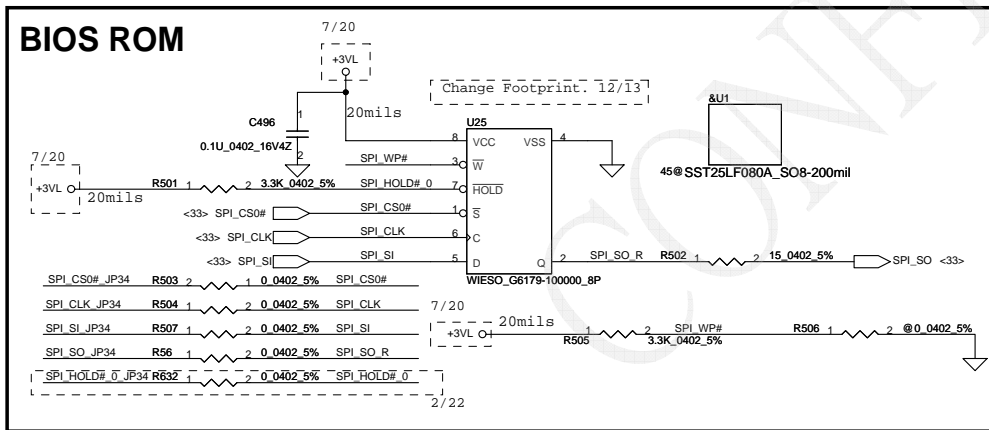
Finger printer



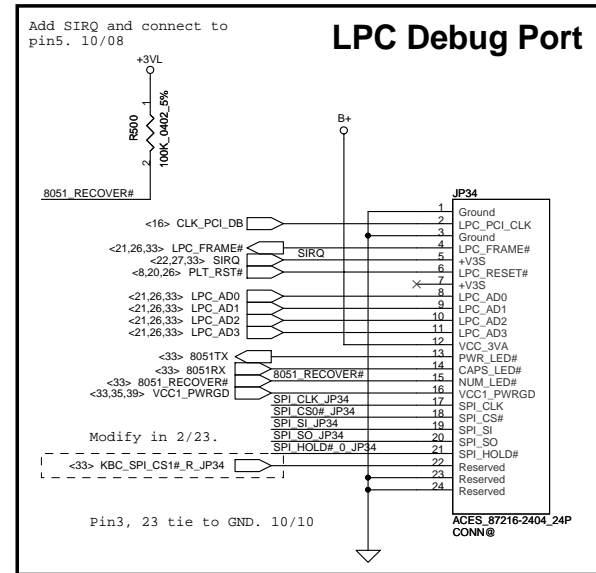
TPM1.2 on board



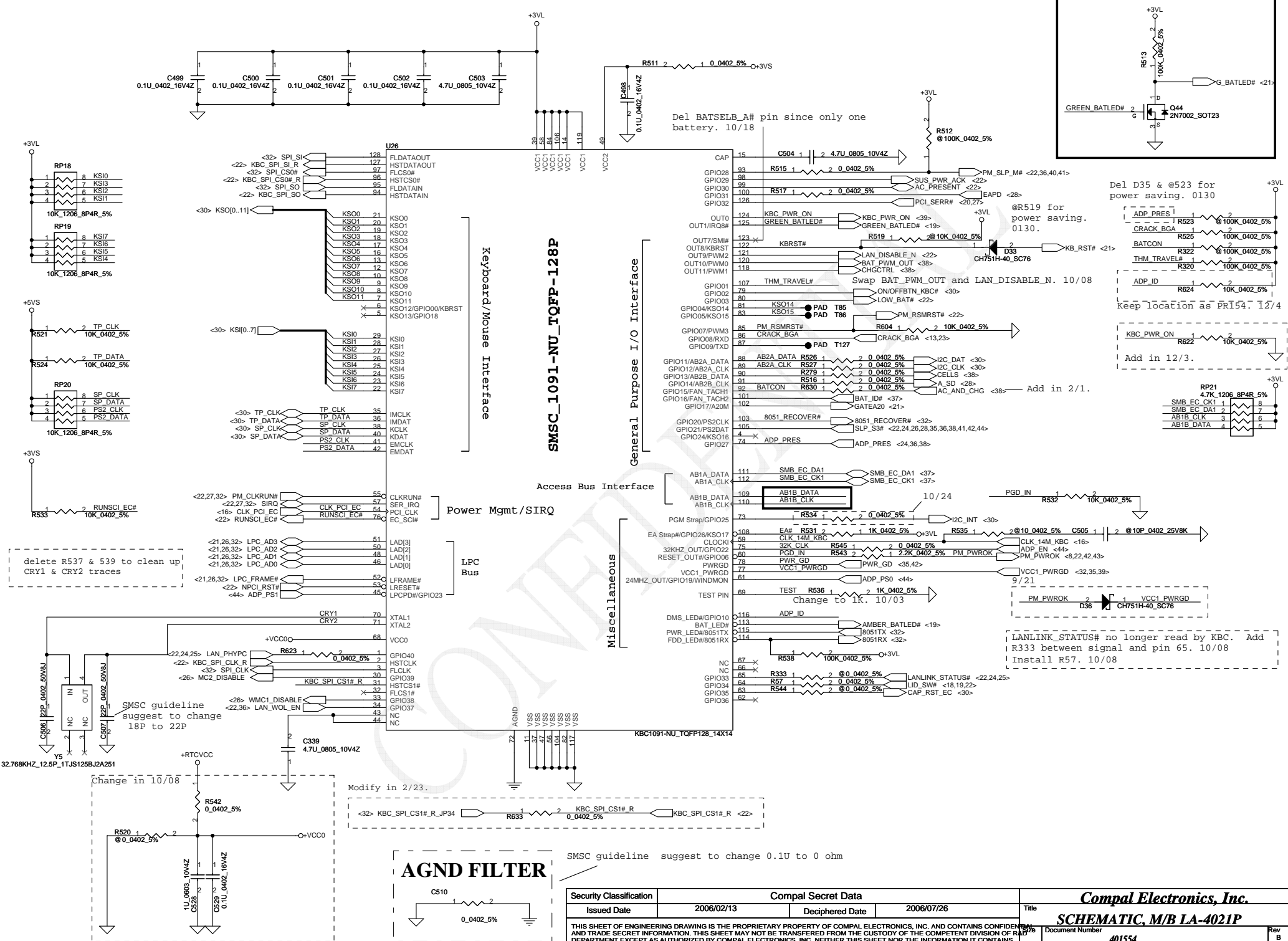
BIOS ROM



LPC Debug Port

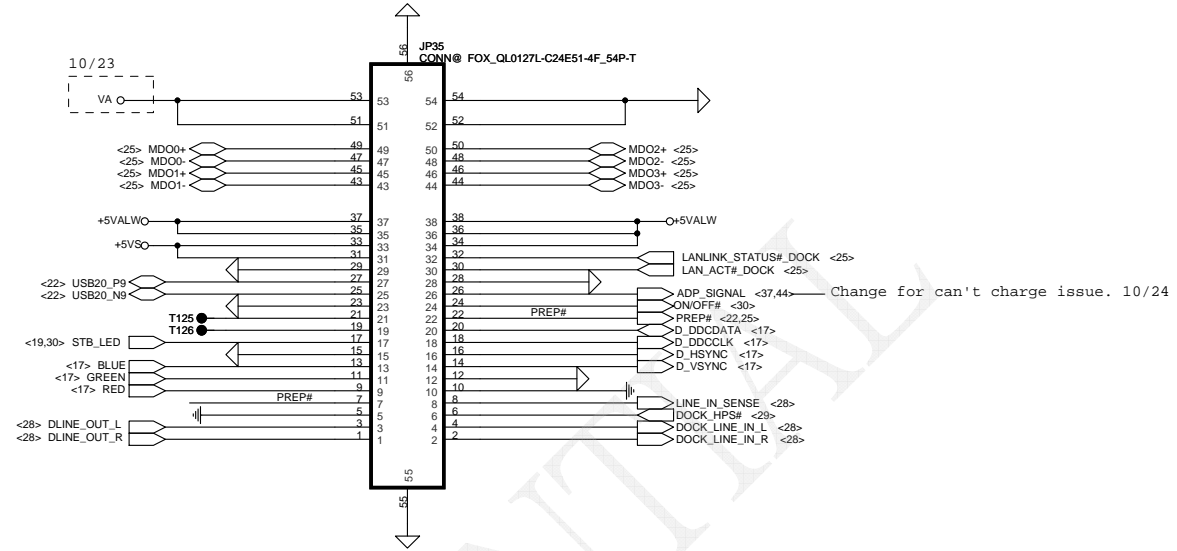
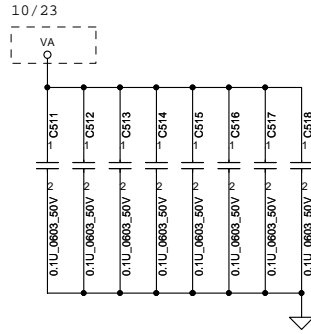


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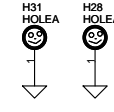
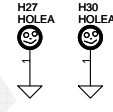
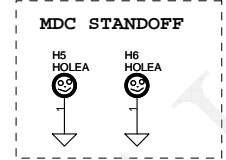
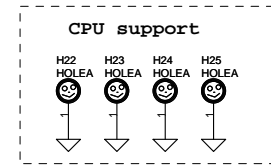
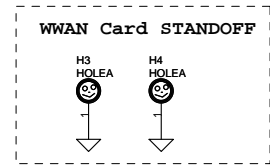
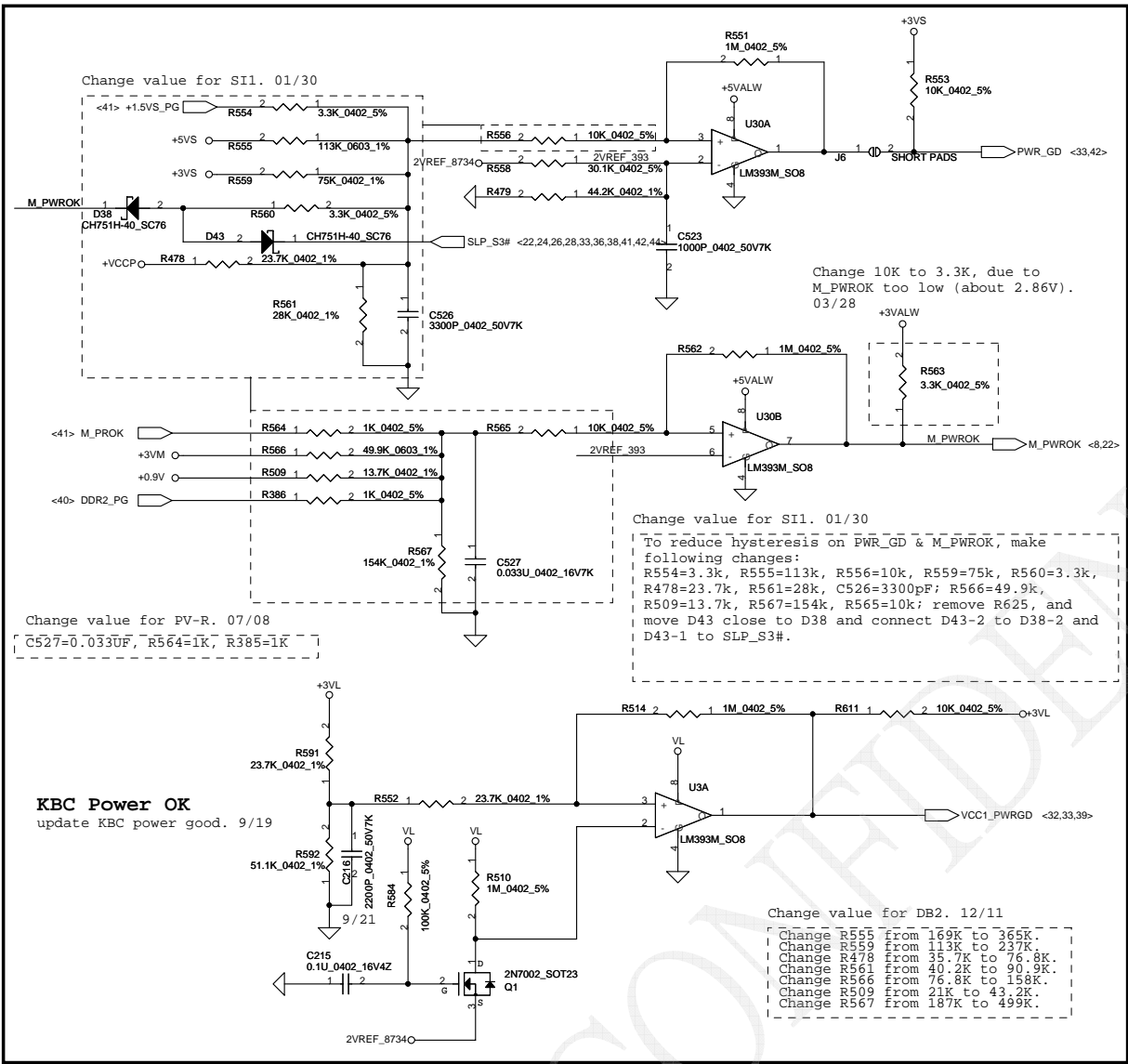
DOCKING CONNECT



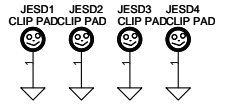
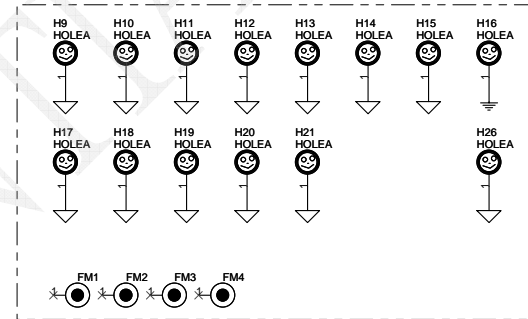
Delete:

1. L21 ~ L23.
2. C605 ~ C610.
3. R635 ~ R637.
4. U27 ~ U29.
5. C519 ~ C521.
6. R548 ~ R550.

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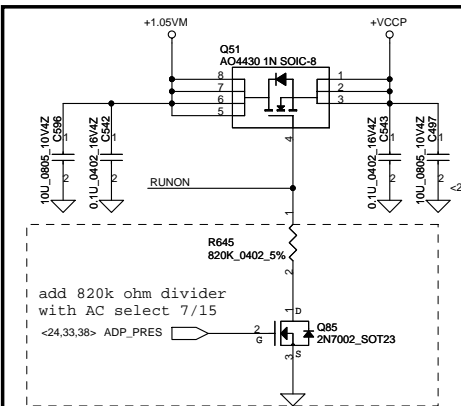


Del H1, H7 & H8. 1/18

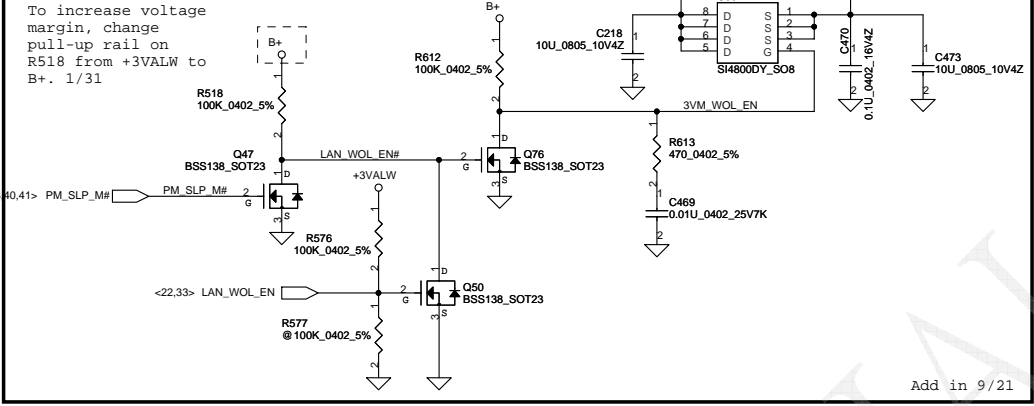


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				401534	B
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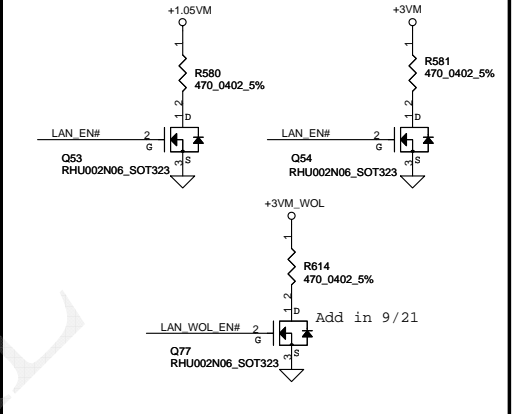
+1.05VM to +VCCP Transfer



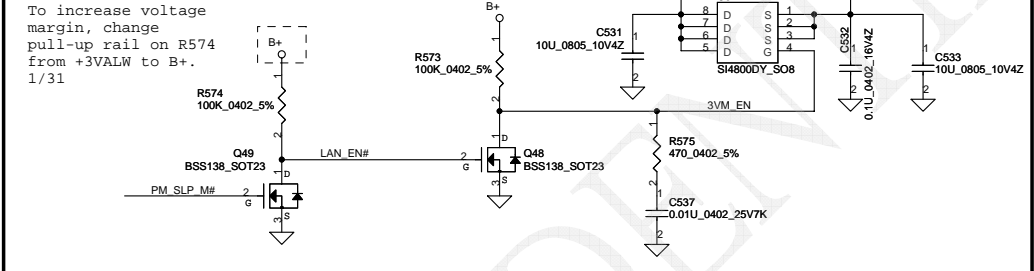
+3VALW to +3VM_WOL Transfer



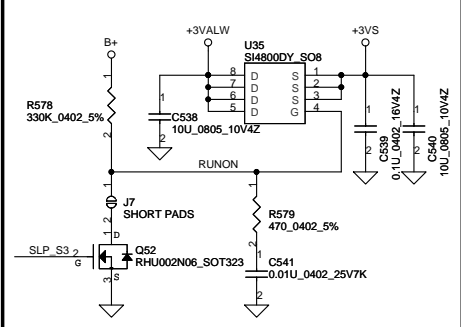
Discharge circuit-2 for V-M



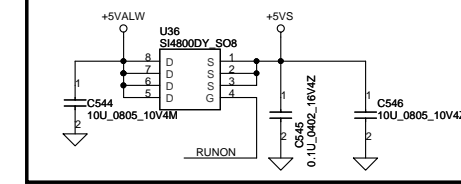
+3VALW to +3VM Transfer



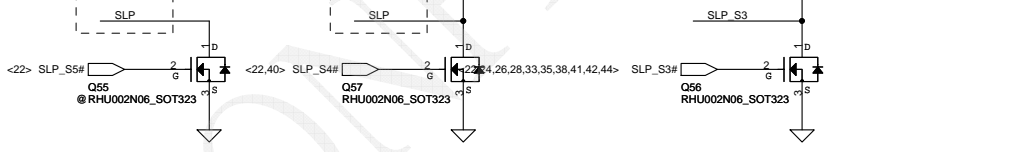
+3VALW to +3VS Transfer



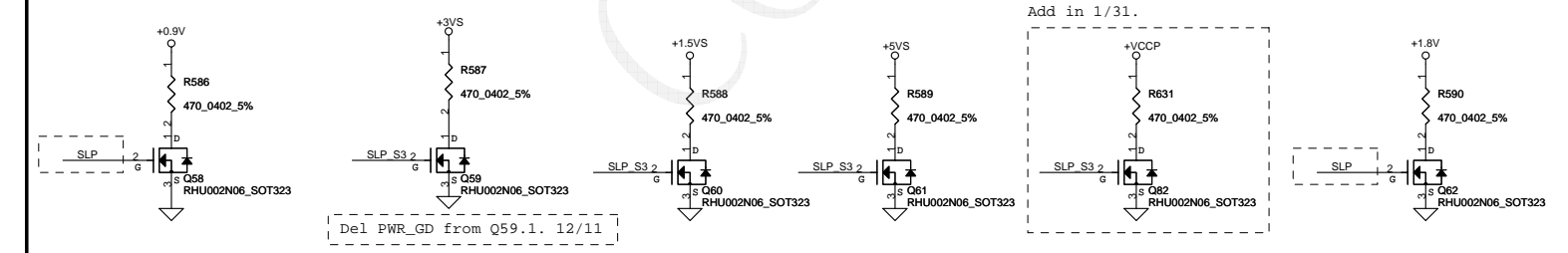
+5VALW to +5VS Transfer



Design Change at 9/14.



Discharge circuit-1



SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V