# First International Computer,Inc

## Protable Computer Group  HW Department

Board name : Mother Board Schematic

Project : LM7W

Version : 0.2

Initial Date : August 31 , 2005

1. Schematic Page Description :
2. PCI & IRQ & DMA Description :
3. Block Diagram :
4. Nat name Description :
5. Board Stack up Description :
6. Schematic modify Item and History :
7. power on & off & S3 Sequence :
8. Layout Guideline :
9. switch setting

Manager Sign by:

Drawing by : Tom_Lin

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LAN Circuit check by:

Audio Circuit check by:

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Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <> | Rev: 0.2

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# 1. Schematic Page Description :

## LM7 Schematic Ver : 0.1



# 2. PCI & IRQ & DMA Description :

| IDSEL | CHIP |
|---|---|
| AD17 | Mini PCI(Wireless LAN) |
| AD23 | CardBus |

| PCIINT | CHIP |
|---|---|
| IRQA | MiniPCI/NB |
| IRQB | MiniPCI/CardBus |
| IRQC | MiniPCI |
| IRQD | |

BUSMASTER

| REQ | CHIP |
|---|---|
| REQ0 / GNT0 | MiniPCI |
| REQ1 / GNT1 | CardBus |
| REQ2 / GNT2 | Mini PCI(Wireless LAN) |
| REQ3 / GNT3 | |
| REQ4 / GNT4 | |

| IRQ Channel | Desciption | |
|---|---|---|
| IRQ0 | System timer | |
| IRQ1 | Keyboard | |
| IRQ2 | (Casacde) | |
| IRQ3 | LAN / MODEM | |
| IRQ4 | ~~Serial Port~~ | |
| IRQ5 | AUDIO / VGA / USB | |
| IRQ6 | ~~FLOPPY DISK~~ | |
| IRQ7 | ~~LPT~~ | |
| IRQ8 | RTC | |
| IRQ9 | ACPI | |
| IRQ10 | FIR (Disable by default) | (MODEM/LAN) |
| IRQ11 | Cardbus | |
| IRQ12 | PS/2 mouse | |
| IRQ13 | FPU | |
| IRQ14 | HDD | |
| IRQ15 | CDROM | |

| DMA Channel | Device | |
|---|---|---|
| DMA0 | FIR (disable by default) | (MODEM / LAN) |
| DMA1 | ~~ECP~~ | |
| DMA2 | ~~FLOPPY DISK~~ | |
| DMA3 | AUDIO | |
| DMA4 | (Cascade) | |
| DMA5 | Unused | |
| DMA6 | Unused | |
| DMA7 | Unused | |


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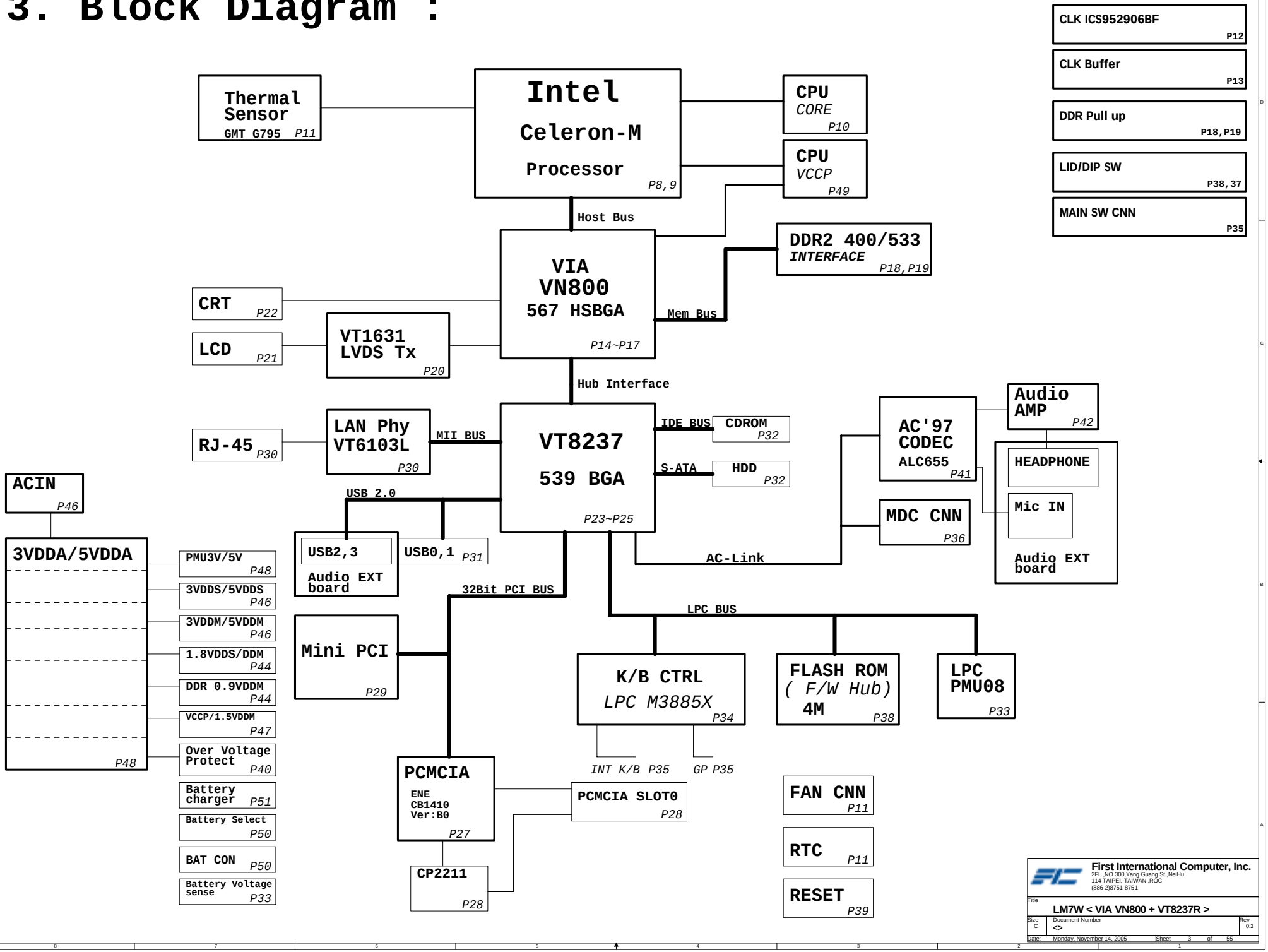
# 3. Block Diagram :

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# 4. Nat name Description :

## Voltage Rails

| | |
|---|---|
| DCIN | Primary DC system power supply |
| PMU5V | 5.0V always on power rail by LATCH or ACIN |
| PMU3V | 3.3V always on power rail by LATCH or ACIN |
| 5VDDA | 5.0V always on power rail by DCON or PSUSC0 |
| 3VDDA | 3.3V always on power rail by DCON or PSUSC0 |
| 3VDDS | 3.3V power rail |
| 5VDDS | 5.0V power rail |
| 3VDDM | 3.3V switched power rail |
| 5VDDM | 5.0V switched power rail |
| Vcore_CPU | Core Voltage for CPU |
| | |
| VCCP | 1.05V for AGTL+ Termination Voltage |
| 1.8VDDM | 1.8V for CPU PLL Voltage |
| DDR_0.9VDDM | 0.9V DDR Termination Voltage |
| 1.5VDDM | 1.5V switched power rail |
| 1.5VDDS | 1.5V power rail |
| 1.5VDDA | 1.5V always on power rail |
| 2.5VDDS | 2.5V power rail for DDR |

## Part Naming Conventions

| | | |
|---|---|---|
| C | = | Capacitor |
| CN | = | Connector |
| D | = | Diode |
| F | = | Fuse |
| L | = | Inductor |
| Q | = | Transistor |
| R | = | Resistor |
| RP | = | Resistor Pack |
| U | = | Arbitrary Logic Device |
| Y | = | Crystal and Osc |

## Net Name Suffix

| | | |
|---|---|---|
| 0 | = | Active Low signal |

## Signal Conditioning

| | | |
|---|---|---|
| _D_ | = | Damped (by a resistor) |
| _Q_ | = | Isolated (by a Q-switch) |
| _L_ | = | Filtered (by an inductor or bead) |

# 5.Board Stack up Description

## PCB Layers

| | | |
|---|---|---|
| Layer 1 | | Component Side, Microstrip signal Layer |
| Layer 2 | | Ground Plane |
| Layer 3 | | Stripline Layer(AGTL,CLOCK,DDR) |
| Layer 4 | | Power Plane |
| Layer 5 | | Ground Plane |
| Layer 6 | | Stripline Layer(Analog,LVDS,other) |
| Layer 7 | | Ground Plane |
| Layer 8 | | Solder Side,Microstrip signal Layer |

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# 6.Schematic modify Item and History :

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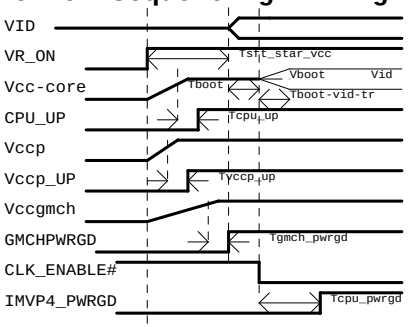
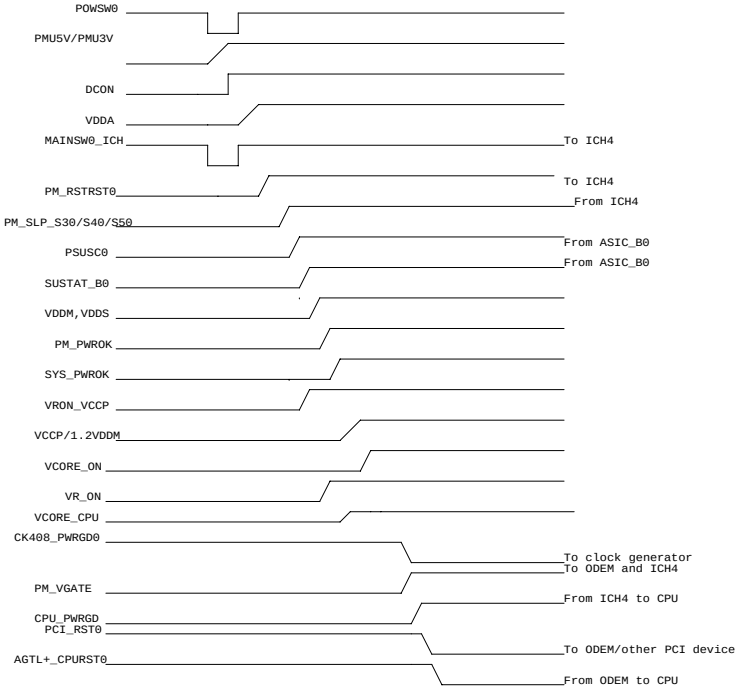
# 7. power on & off & S3 Sequence :

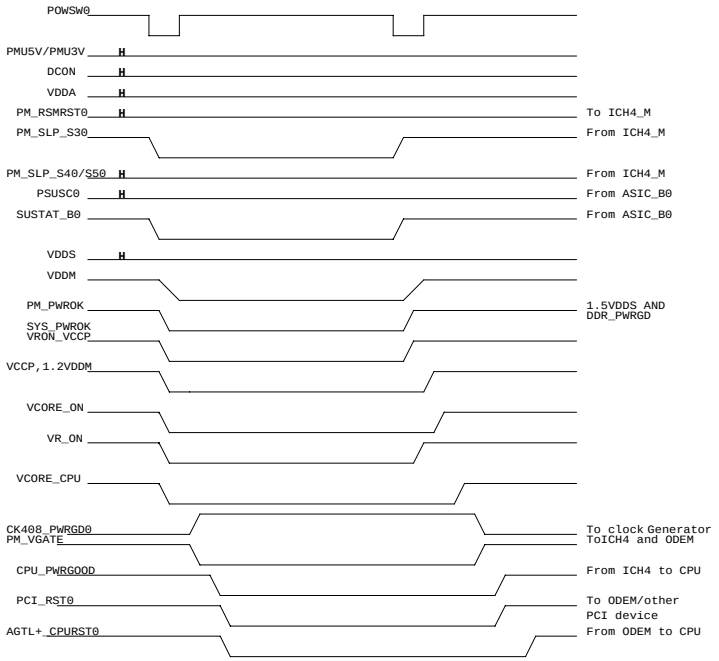
## Power On Sequencing Timing Diagram




## BATTERY ONLY POWER ON TIMING




## S3 SUSPEND AND RESUME TIMING





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# 8. Layout Guideline :

*Montara-GM DDR Layout Guidelines*

*Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length*

*DDR Signal Groups*

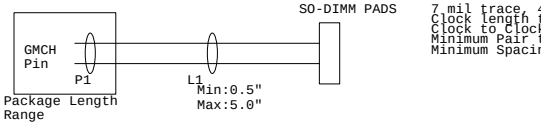
| Group | Signal Name |
|---|---|
| Clocks | SCK[5:0]<br>SCK#[5:0] |
| Data | SDQ[71:0]<br>SDQS[8:0]<br>SDM[8:0] |
| Control | SCKE[3:0]<br>SCS#[3:0] |
| Command | SMA[12:6,3:0]<br>SBA[1:0]<br>SRAS#<br>SCAS#<br>SWE# |
| CPC | SMA[5,4,2,1]<br>SMAB[5,4,2,1] |
| Feedback | RCVENOUT#<br>RCVENIN# |

*Length Matching Formulas*

| Signal Group | Minimum Length | Maximum Length |
|---|---|---|
| Control to Clock | Clock - 1.0" | Clock + 0.5" |
| Command to Clock | Clock - 1.0" | Clock + 2.0" |
| CPC to Clock | Clock - 1.0" | Clock + 0.5" |
| Strobe to Clock | Clock - 1.0" | Clock + 0.5" |
| Data to Strobe | Strobe - 25 mils | Strobe + 25 mils |

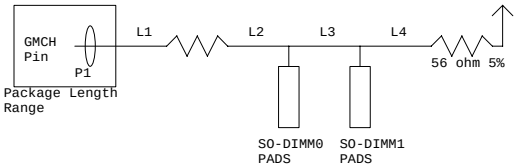
| CLOCKS | LENGTH | TRACE / SPACE | NOTES |
|---|---|---|---|
| HCLKCPU[1..0]<br>HCLKNB[1..0]<br>HCLKITP[1..0] | 2" ~ 8 " | 5 / 20 mils<br>(5 mil space between + & - ) | 1.Differentials pairs with the same length (within 10 mil)<br>2.CPU & NB trace mismatch within 450 mil |
| 66MCLK_ICH<br>66MCLK_GMCH<br>AGPCLK_ATI | 4.5" ~ 9.0 "<br>MAX : 8.5" | 5 / 20 mils | * 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils |
| PCLKICH<br>PCLKCB<br>PCLK1394<br>PCLKUSB20<br>PCLKOP<br>PCLKFWH<br>PCLKSIO<br>PCLKLAN | 4.5"~9.0" | 5 / 20 mils | 1.Making PCI length with minimum various<br>2.Max skew = 1ns |
| 14MCLK_SIO<br>14MCLK_ICH<br>14MCLK_AC97 | 4.5"~9.0" | 5 / 10 mils | |
| 48MCLK_ICH<br>48MCLK_CB | 3.5" ~ 12.5" | 5 / 20 mils | |

*Clock Signals Topologies and Routing Guidelines*




7 mil trace, 4 mil pair space
Clock length tolerenve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

*Data Signals Topologies and Routing Guidelines*

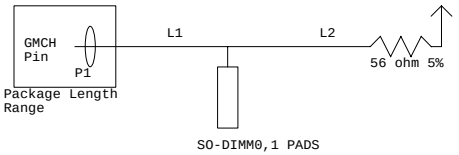



Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0 "
Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 0.5"
SDQ/SDM to SDQS : +/-'25 mils

SDQ/SDM to SDQS Mapping

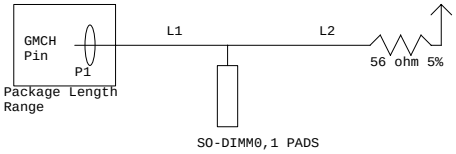
| Signal | Mask | Relative To | Mismatching |
|---|---|---|---|
| SDQ[7..0] | SDM[0] | SDQS[0] | +/- 25 mil |
| SDQ[15..8] | SDM[1] | SDQS[1] | +/- 25 mil |
| SDQ[23..16] | SDM[2] | SDQS[2] | +/- 25 mil |
| SDQ[31..24] | SDM[3] | SDQS[3] | +/- 25 mil |
| SDQ[39..32] | SDM[4] | SDQS[4] | +/- 25 mil |
| SDQ[56..40] | SDM[5] | SDQS[5] | +/- 25 mil |
| SDQ[55..48] | SDM[6] | SDQS[6] | +/- 25 mil |
| SDQ[63..56] | SDM[7] | SDQS[7] | +/- 25 mil |
| SDQ[71..64] | SDM[8] | SDQS[8] | +/- 25 mil |

*Control Signals Topologies and Routing Guidelines*



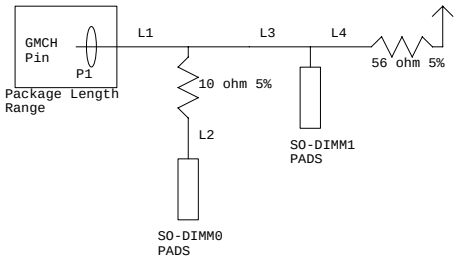

Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

*CPC Signals Topologies and Routing Guidelines*




Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

*Command Signals Topologies and Routing Guidelines*




Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.0"
L3 : Max 2.0"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"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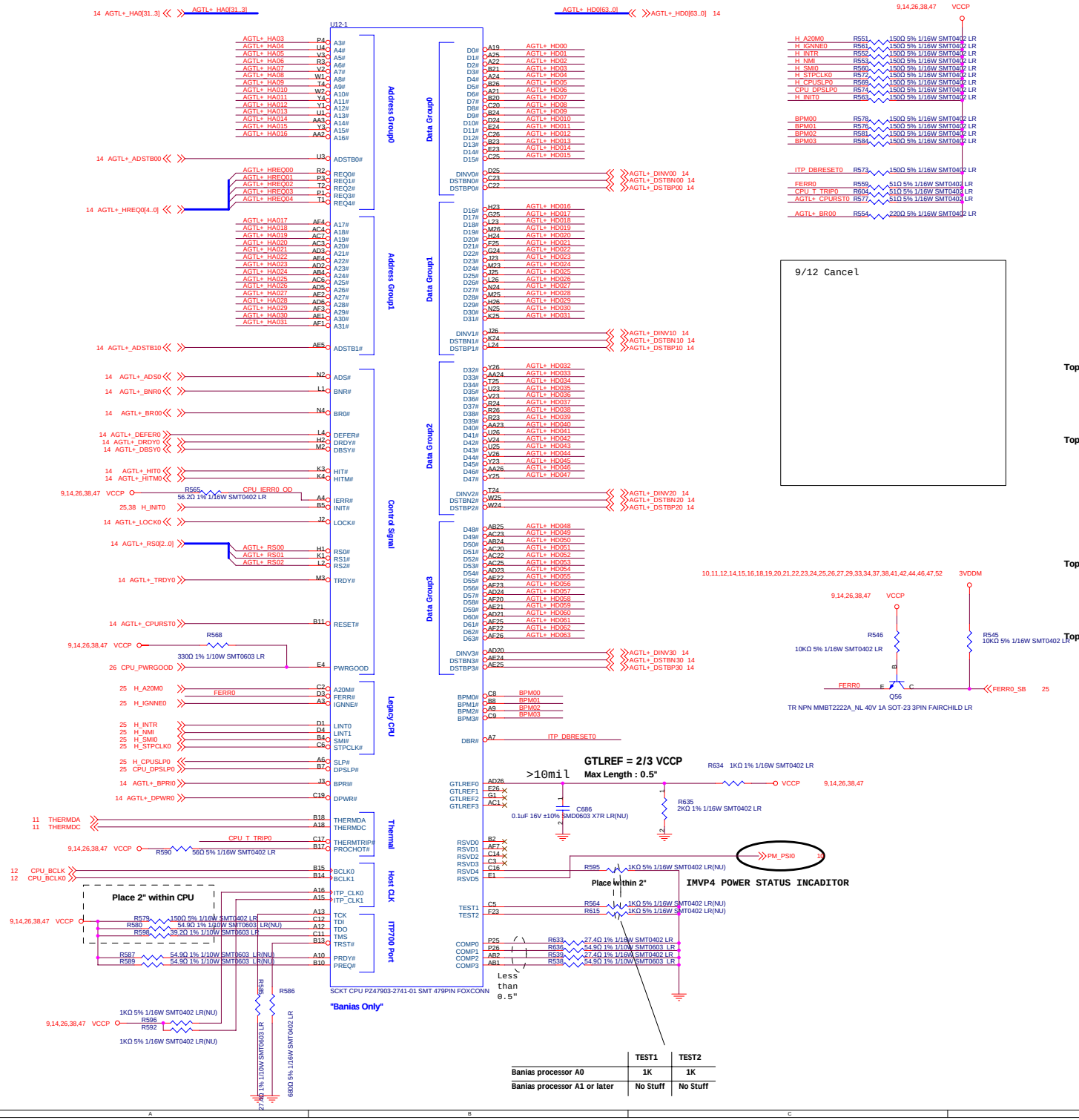



## System Bus Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

| Transmission Line Type | Total Trace Length | Normal Impedance | Spacing (mils) |
|---|---|---|---|
| Strip-line(Int. Layer)<br>Micro-strip(Ext. Layer) | 1.0 ~ 6.5 inch | 55+/-10% | 4 & 8(Int. Layer)<br>5 & 10(Ext. Layer) |

## Source Synchronous DATA :

DATA#[63..0] , DINV#[3..0] , DSTBN#[3..0] , DSTBP#[3..0]

| Transmission Line Type | Total Trace Length | Normal Impedance | Spacing (mils) |
|---|---|---|---|
| Strip-line | 1.0 ~ 5.5 inch | 55+/-10% | 4 & 12 |

| Signals Name | Signals Matching | Strobes associated with the group | Strobe Matching |
|---|---|---|---|
| DATA#[15..0] , DINV0# | +/- 100 mils | DSTBP0#,DSTBN0# | +/- 25 mils |
| DATA#[31..16] , DINV1# | +/- 100 mils | DSTBP1#,DSTBN1# | +/- 25 mils |
| DATA#[47..32] , DINV2# | +/- 100 mils | DSTBP2#,DSTBN2# | +/- 25 mils |
| DATA#[63..48] , DINV3# | +/- 100 mils | DSTBP3#,DSTBN3# | +/- 25 mils |

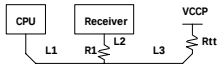
## Source Synchronous ADDRESS :

Address#[31..3] , REQ#[4..0] , ADSTB#[1..0]

| Transmission Line Type | Total Trace Length | Normal Impedance | Spacing (mils) |
|---|---|---|---|
| Strip-line | 1.0 ~ 6.5 inch | 55+/-10% | 4 & 12 |

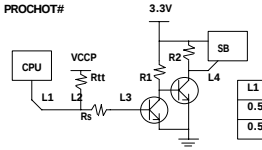
| Signals Name | Signals Matching | Strobes associated with the group | Strobe Matching |
|---|---|---|---|
| A#[16..3] , REQ#[4..0] | +/- 200 mils | ADSTB0# | +/- 25 mils |
| A#[31..17 | +/- 200 mils | ADSTB1# | +/- 25 mils |

**Topology : IERR# , FERR# , THERMTRIP#**




| L1 | L2 | L3 | R1 | Rtt | Transmission Line |
|---|---|---|---|---|---|
| 0.5" - 12" | 0" - 3.0" | 0" - 3.0" | 56 +/-5% | 56 +/-5% | Micro-strip |
| 0.5" - 12" | 0" - 3.0" | 0" - 3.0" | 56 +/-5% | 56 +/-5% | Strip-line |

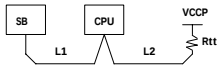
**Topology : PROCHOT#**




Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

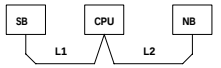
| L1 | L2 | L3 | L4 | Rtt | Transmission Line |
|---|---|---|---|---|---|
| 0.5" - 12" | 0" - 3.0" | 0" - 3.0" | 0.5" - 12" | 56 +/-5% | Micro-strip |
| 0.5" - 12" | 0" - 3.0" | 0" - 3.0" | 0.5" - 12" | 56 +/-5% | Strip-line |

**Topology : PWRGOOD**



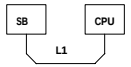

| L1 | L2 | Rtt | Transmission Line |
|---|---|---|---|
| 0.5" - 12" | 0" - 3.0" | 330 +/-5% | Micro-strip |
| 0.5" - 12" | 0" - 3.0" | 330 +/-5% | Strip-line |

**Topology : DPSLP#**



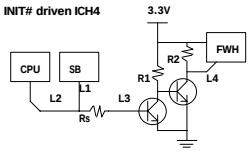

| L1 | L2 | Transmission Line |
|---|---|---|
| 0.5" - 12" | 0.5" - 6.5" | Micro-strip |
| 0.5" - 12" | 0.5" - 6.5" | Strip-line |

**Topology : LINT1 , LINT0 , A20M# , IGNNE# , SLP# , SMI# , STPCLK#**




| L1 | Transmission Line |
|---|---|
| 0.5" - 12" | Micro-strip |
| 0.5" - 12" | Strip-line |

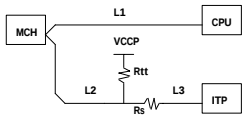
**Topology : INIT# driven ICH4**




Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

| L1 + L2 | L3 | L4 | Transmission Line |
|---|---|---|---|
| 0.5" - 12" | 0" - 3.0" | 0.5" - 6.0" | Micro-strip |
| 0.5" - 12" | 0" - 3.0" | 0.5" - 6.0" | Strip-line |

**Topology : CPU RESET#**




| L1 | L2 + L3 | L3 | Rs | Rtt |
|---|---|---|---|---|
| 1.0" - 6.0" | 12.0" max | 0.5" max | 22.6 +/-1% | 54.9 +/-1% |

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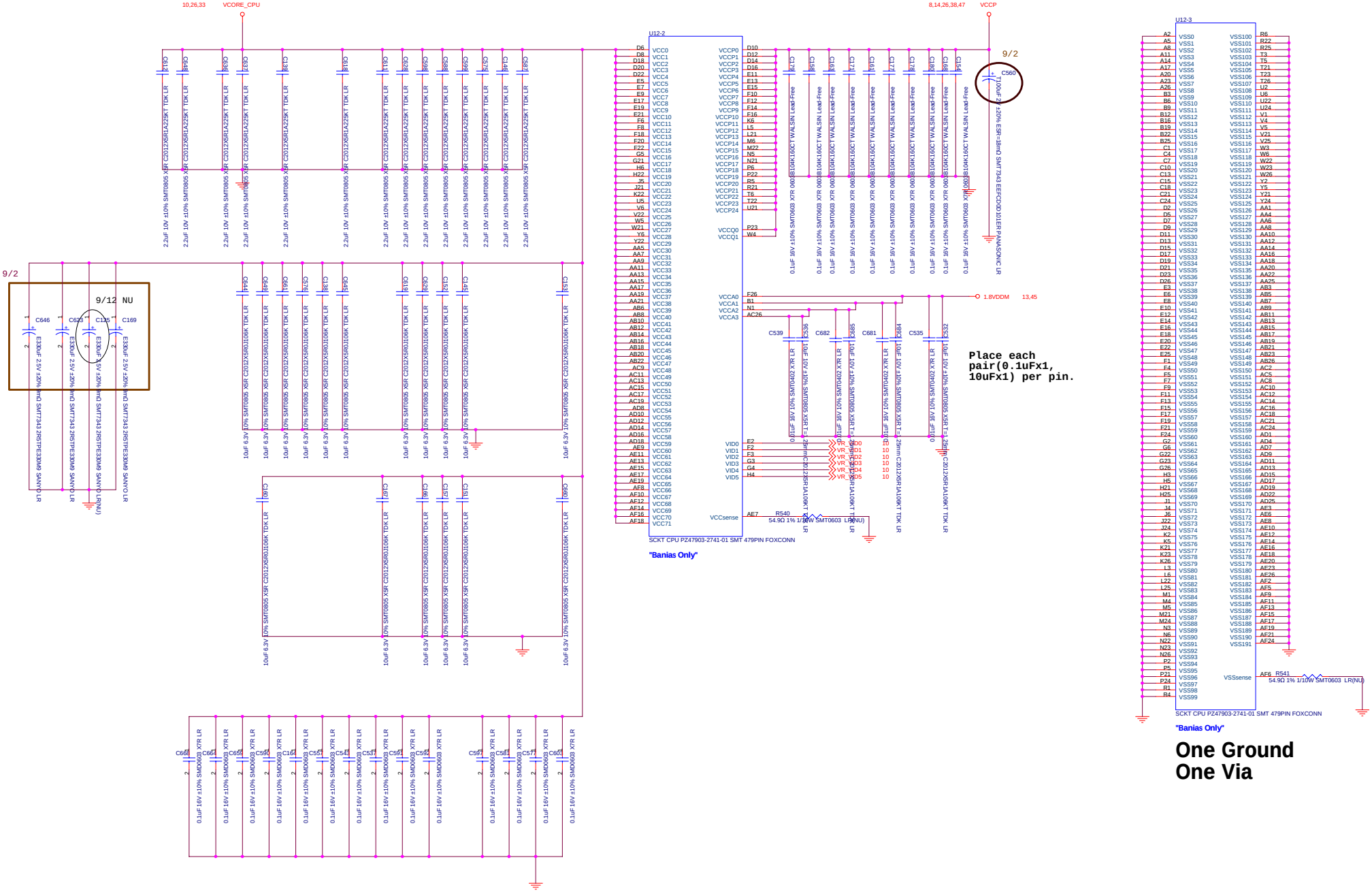


# One Ground One Via


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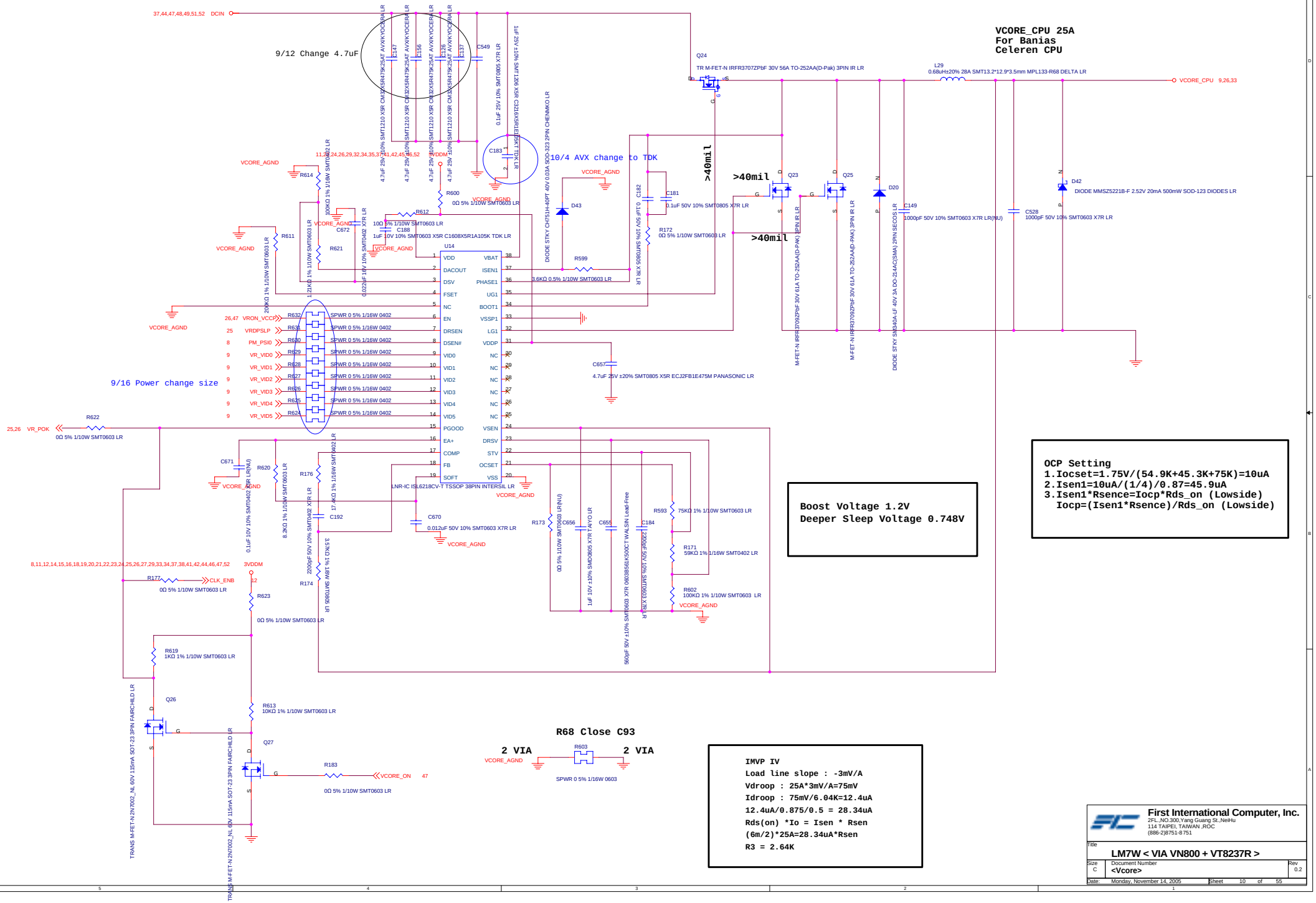
# VCORE_CPU




| | |
|---|---|
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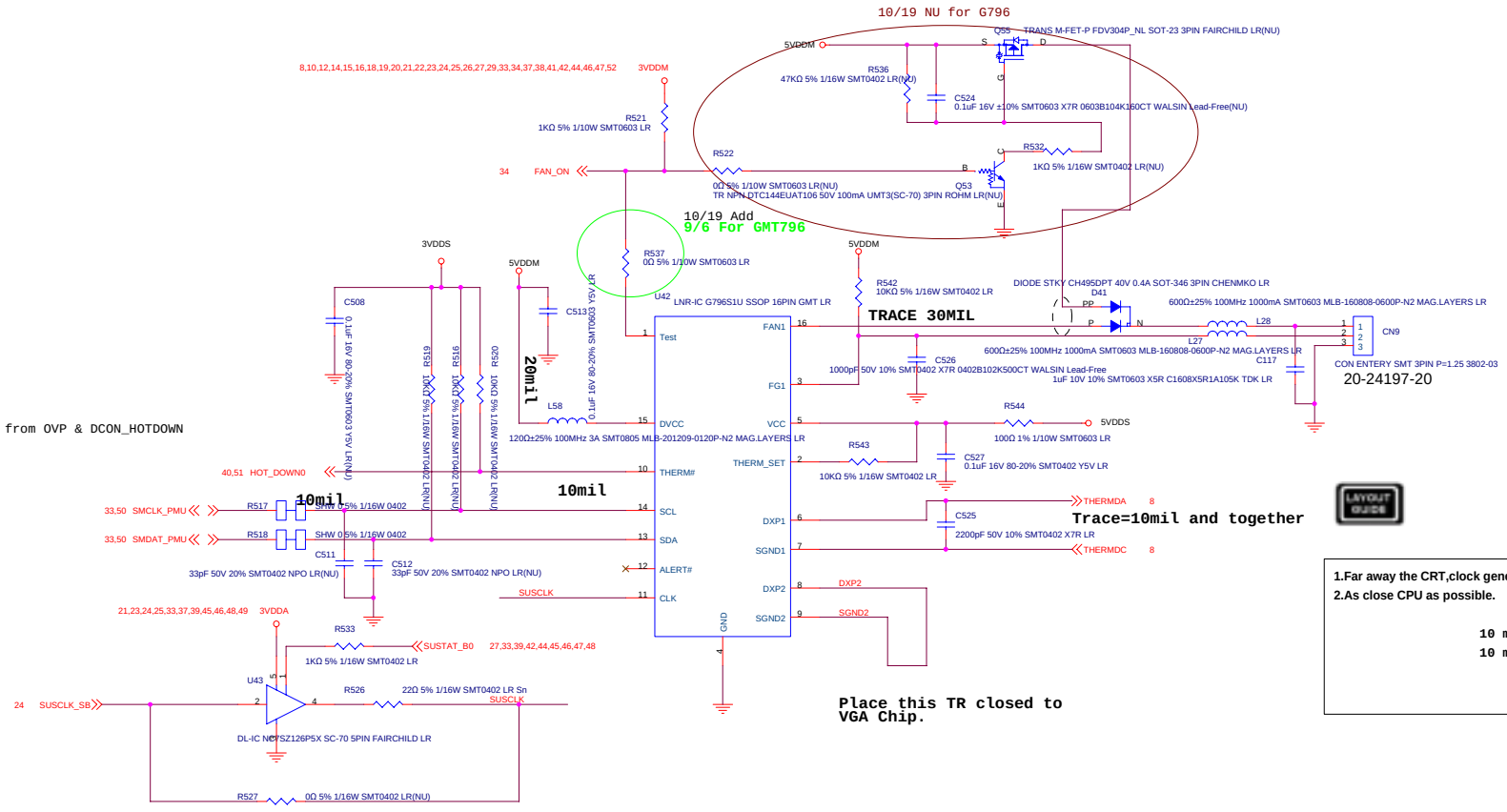
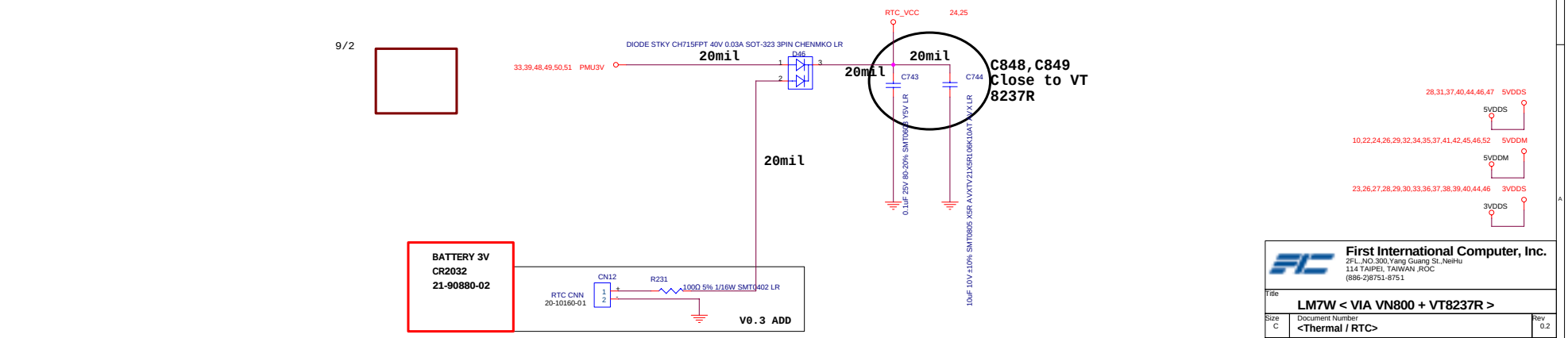
# THERMAL SENSOR




# RTC Discharge Circuit





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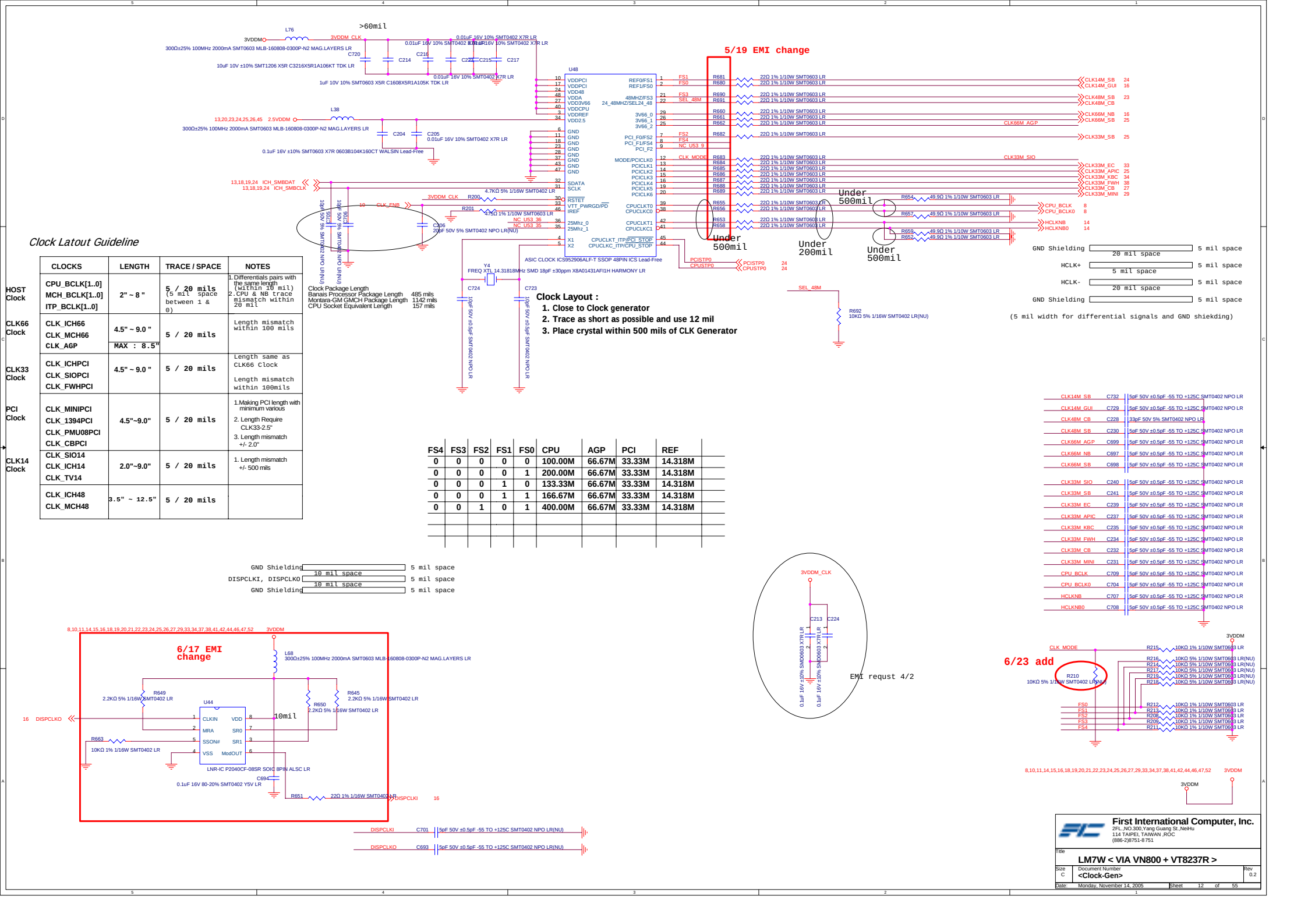
Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <Thermal / RTC> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 11 of 55

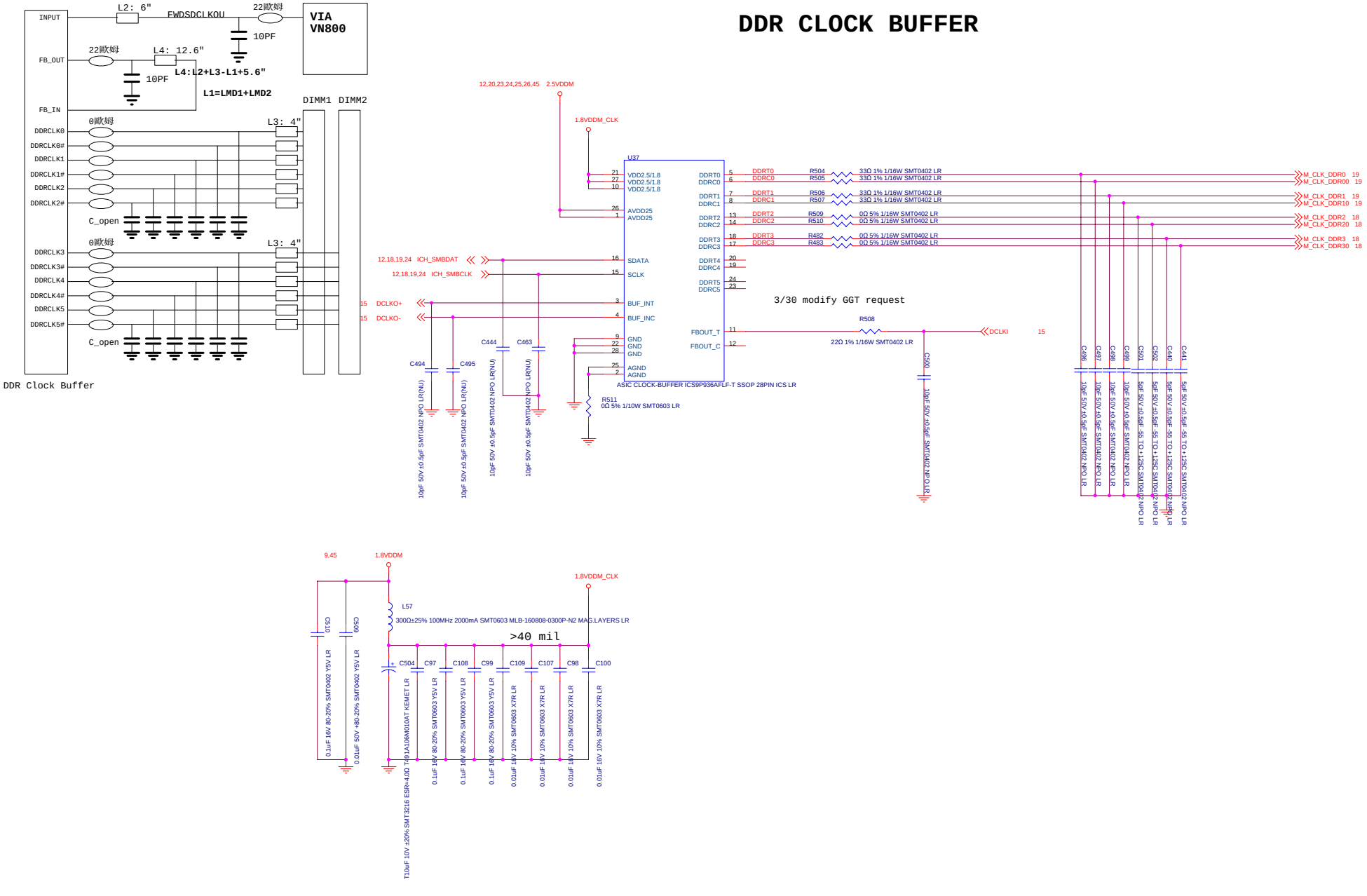



*Clock Latout Guideline*

| | CLOCKS | LENGTH | TRACE / SPACE | NOTES |
|---|---|---|---|---|
| HOST Clock | CPU_BCLK[1..0]<br>MCH_BCLK[1..0]<br>ITP_BCLK[1..0] | 2" ~ 8 " | 5 / 20 mils (5 mil space between 1 & 0) | 1. Differentials pairs with the same length (within 10 mil)<br>2. CPU & NB trace mismatch within 20 mil |
| CLK66 Clock | CLK_ICH66<br>CLK_MCH66<br>CLK_AGP | 4.5" ~ 9.0 "<br>MAX : 8.5" | 5 / 20 mils | Length mismatch within 100 mils |
| CLK33 Clock | CLK_ICHPCI<br>CLK_SIOPCI<br>CLK_FWHPCI | 4.5" ~ 9.0 " | 5 / 20 mils | Length same as CLK66 Clock<br>Length mismatch within 100mils |
| PCI Clock | CLK_MINIPCI<br>CLK_1394PCI<br>CLK_PMU08PCI<br>CLK_CBPCI | 4.5"~9.0" | 5 / 20 mils | 1.Making PCI length with minimum various<br>2. Length Require CLK33-2.5"<br>3. Length mismatch +/- 2.0" |
| CLK14 Clock | CLK_SIO14<br>CLK_ICH14<br>CLK_TV14 | 2.0"~9.0" | 5 / 20 mils | 1. Length mismatch +/- 500 mils |
| | CLK_ICH48<br>CLK_MCH48 | 3.5" ~ 12.5" | 5 / 20 mils | |

| FS4 | FS3 | FS2 | FS1 | FS0 | CPU | AGP | PCI | REF |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 100.00M | 66.67M | 33.33M | 14.318M |
| 0 | 0 | 0 | 0 | 1 | 200.00M | 66.67M | 33.33M | 14.318M |
| 0 | 0 | 0 | 1 | 0 | 133.33M | 66.67M | 33.33M | 14.318M |
| 0 | 0 | 0 | 1 | 1 | 166.67M | 66.67M | 33.33M | 14.318M |
| 0 | 0 | 1 | 0 | 1 | 400.00M | 66.67M | 33.33M | 14.318M |

# DDR CLOCK BUFFER





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| Size | Document Number | Rev |
|---|---|---|
| C | <clock buffer> | 0.2 |

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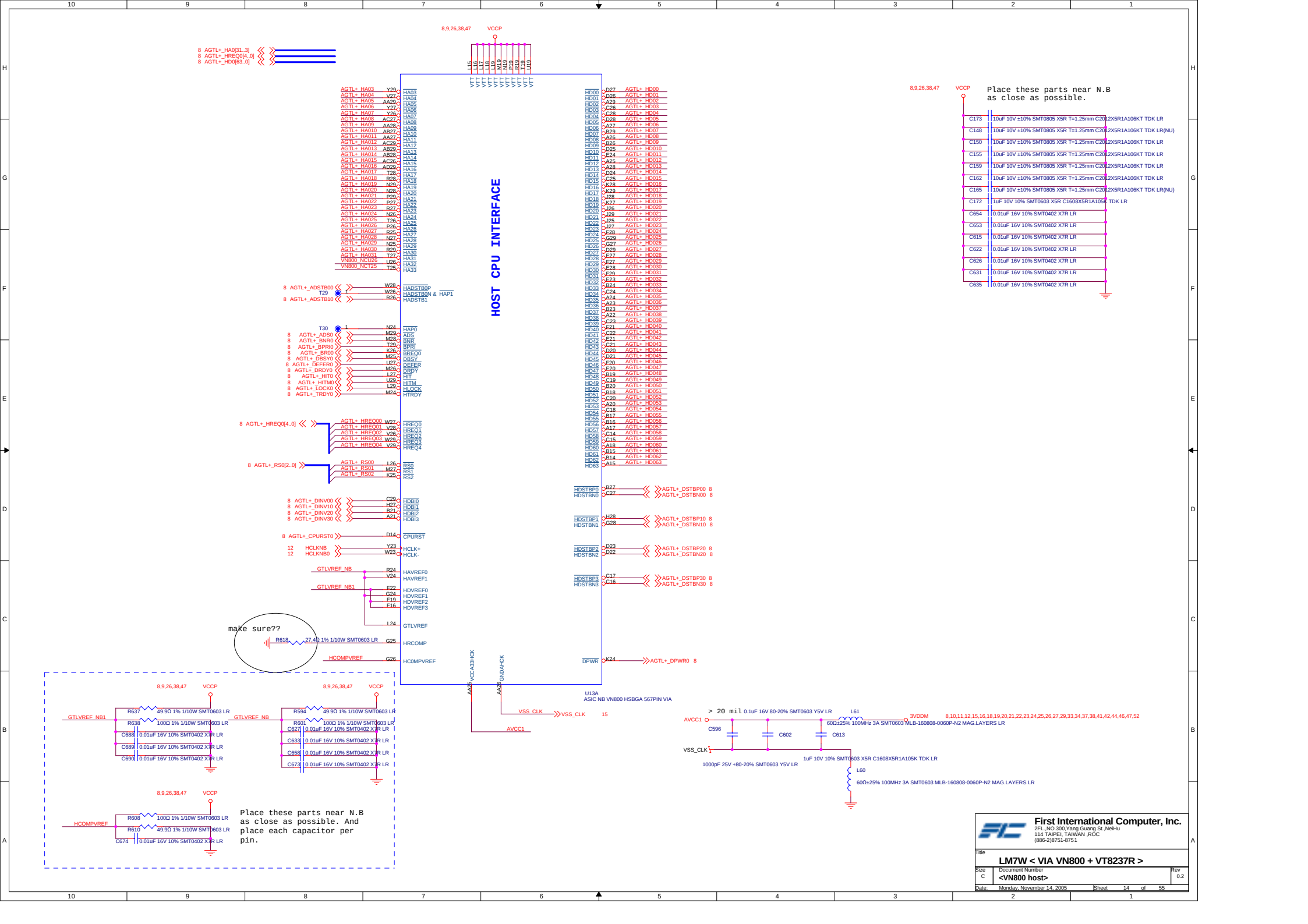
HOST CPU INTERFACE
U13A
ASIC NB VN800 HSBGA 567PIN VIA
make sure??
Place these parts near N.B as close as possible.
Place these parts near N.B as close as possible. And place each capacitor per pin.
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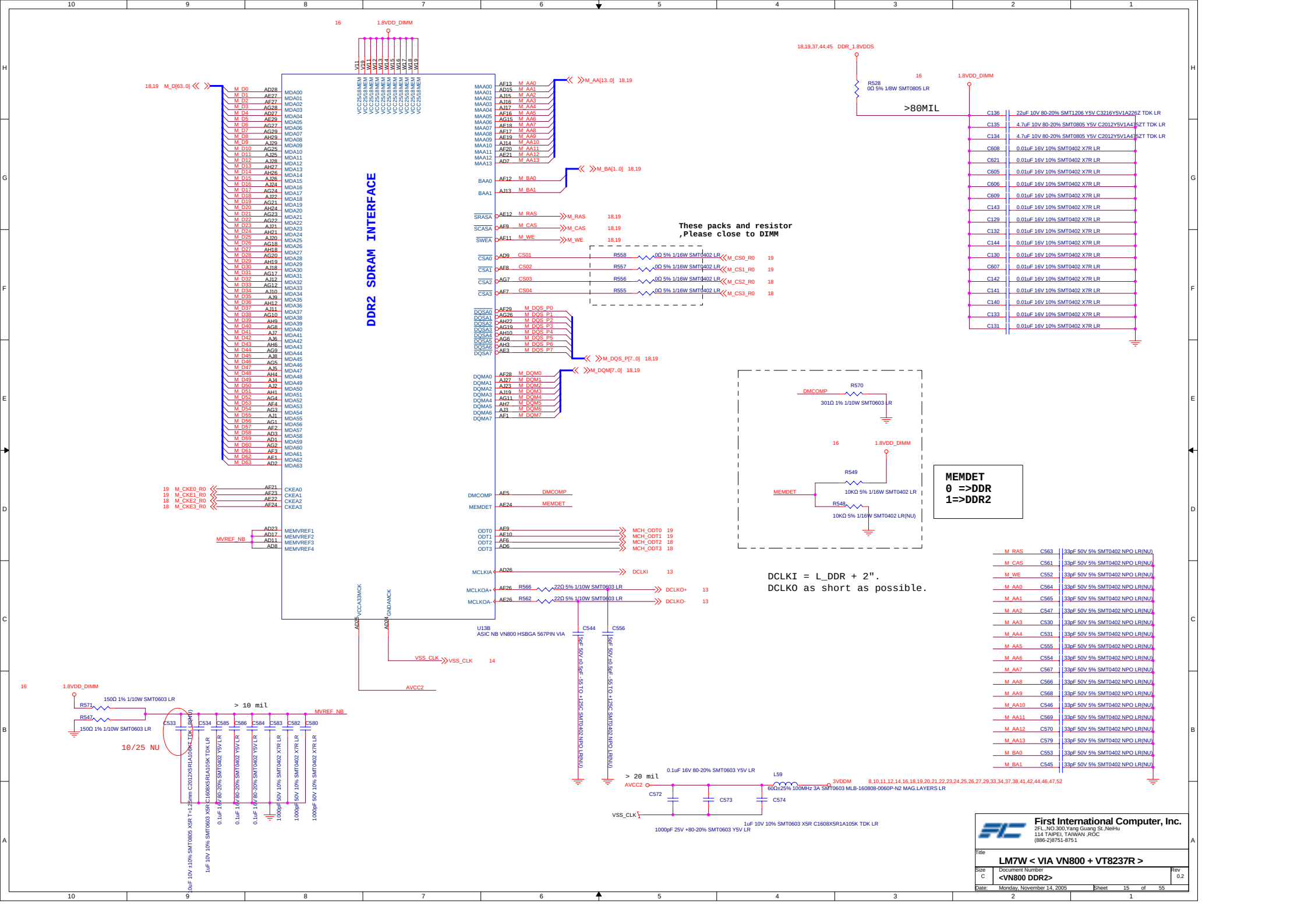
LM7W < VIA VN800 + VT8237R >
<VN800 host>
Monday, November 14, 2005
Sheet 14 of 55




MEMDET
0 =>DDR
1=>DDR2

| | |
|---|---|
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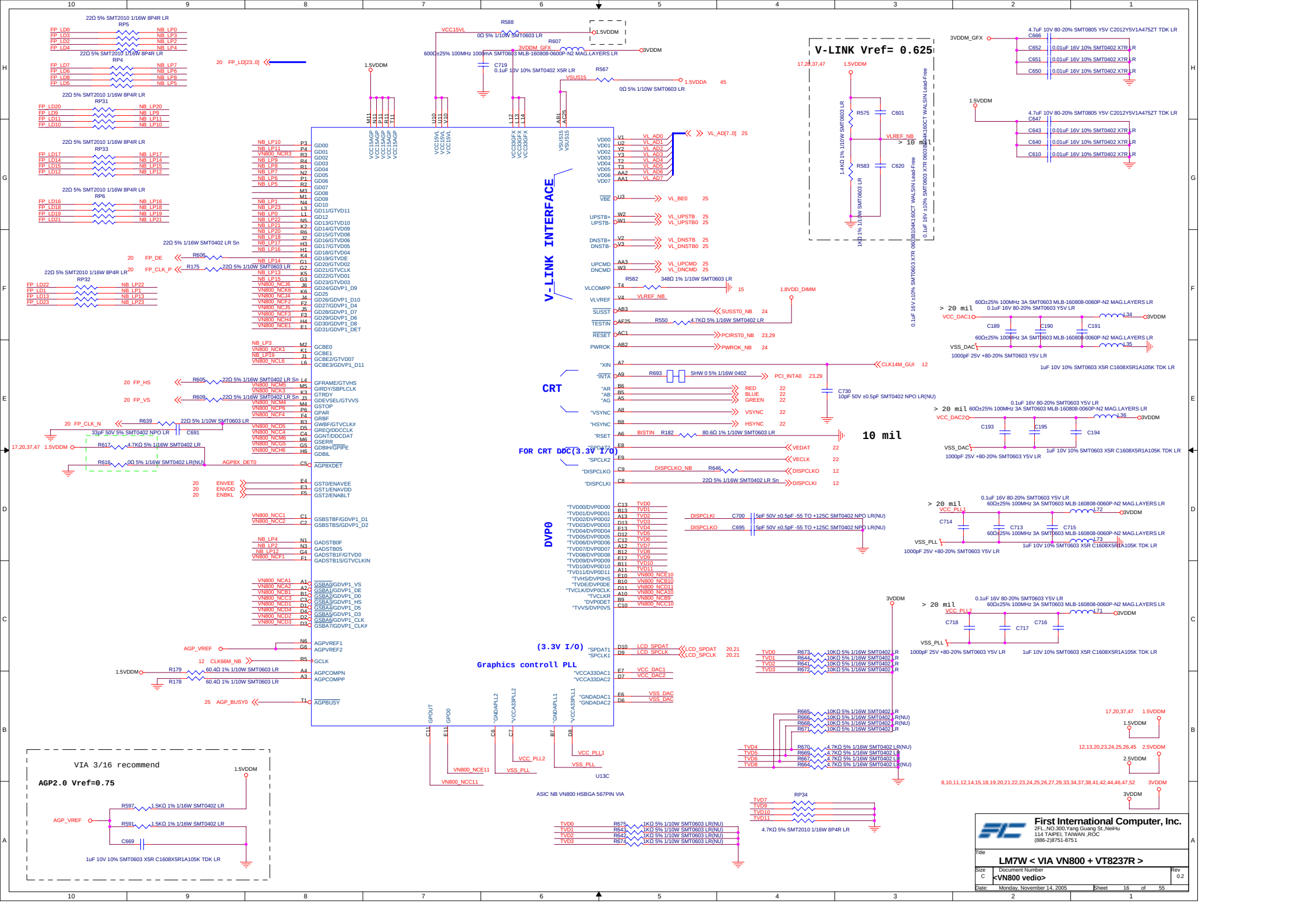
| Title | LM7W < VIA VN800 + VT8237R > |
| Size C | Document Number <VN800 DDR2> Rev 0.2 |
| Date: Monday, November 14, 2005 | Sheet 15 of 55 |


V-LINK Vref= 0.625
V-LINK INTERFACE
CRT
FOR CRT DDC(3.3V I/O)
DVP0
(3.3V I/O)
Graphics controll PLL
10 mil
VIA 3/16 recommend
AGP2.0 Vref=0.75
ASIC NB VN800 HSBGA 567PIN VIA
U13C
First International Computer, Inc.
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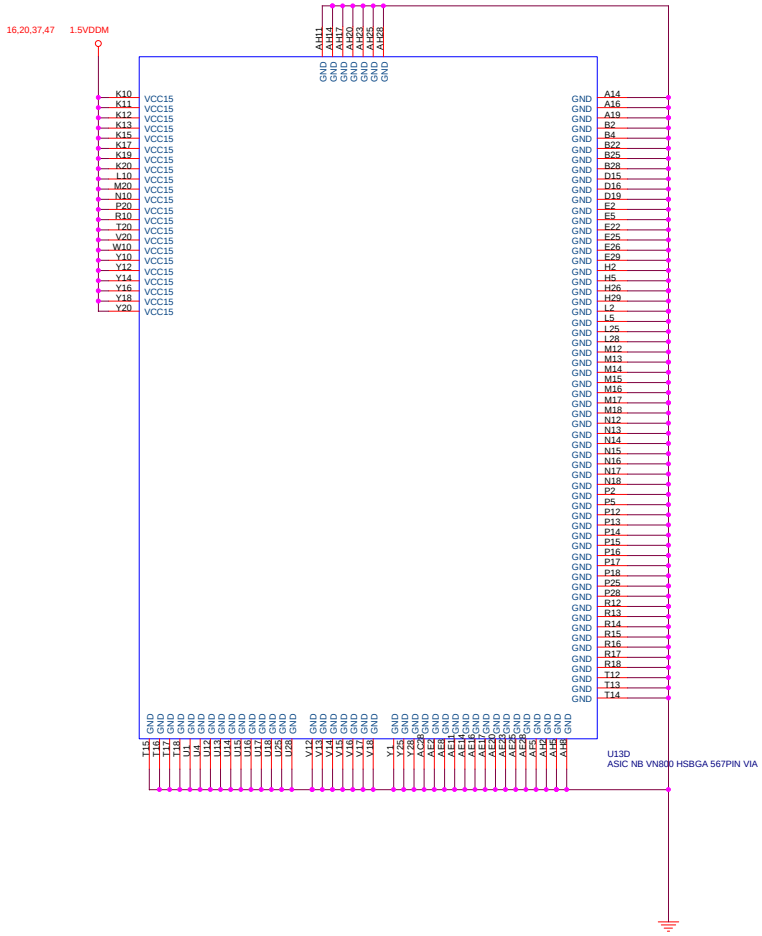
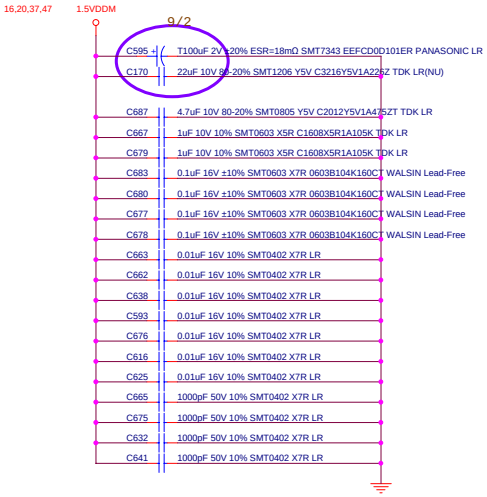
(886-2)8751-8751
LM7W < VIA VN800 + VT8237R >
<VN800 vedio>
Monday, November 14, 2005
16 of 55





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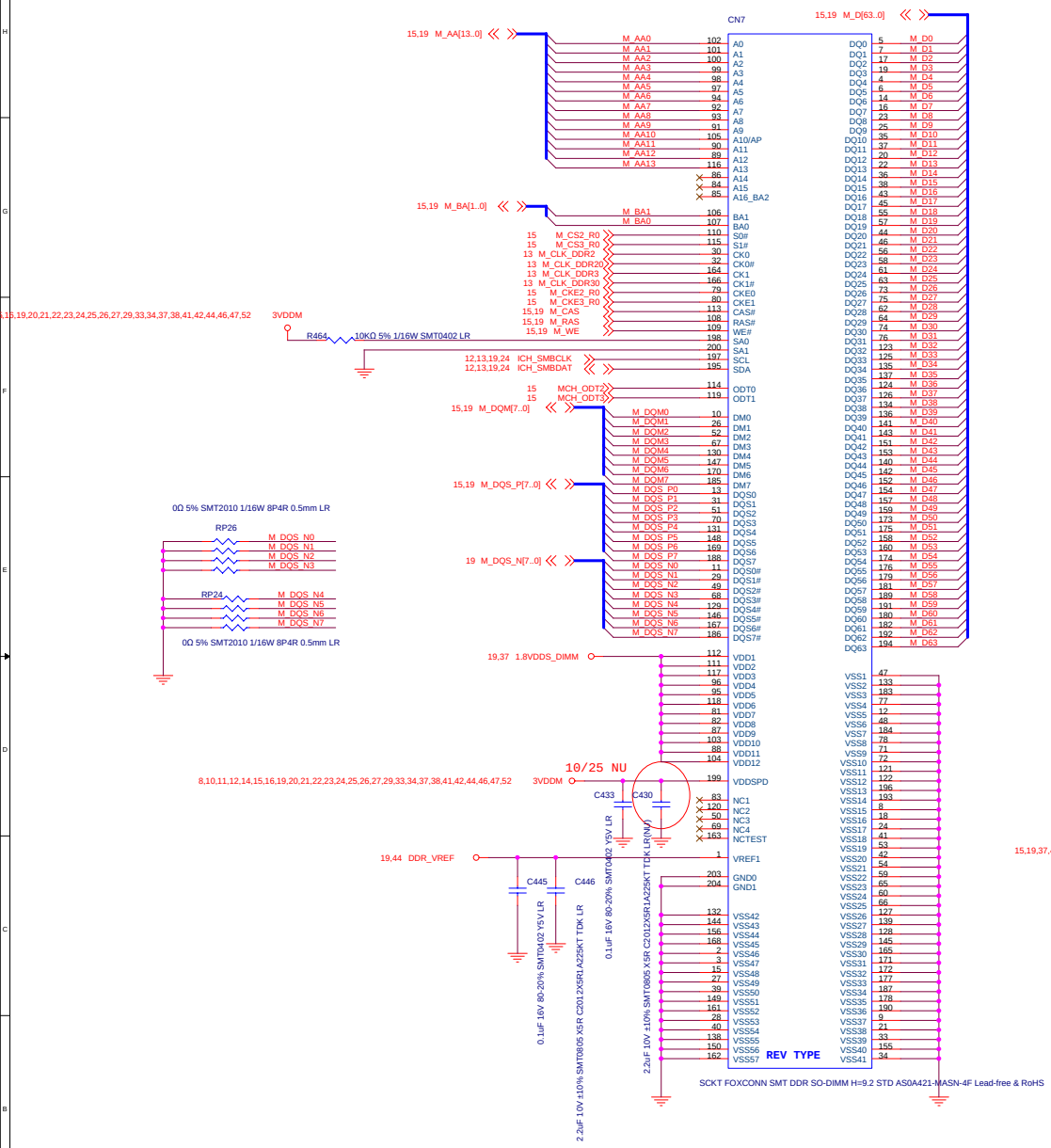
Title
**LM7W < VIA VN800 + VT8237R >**

| Size | Document Number | Rev |
|---|---|---|
| C | <VN800 power> | 0.2 |

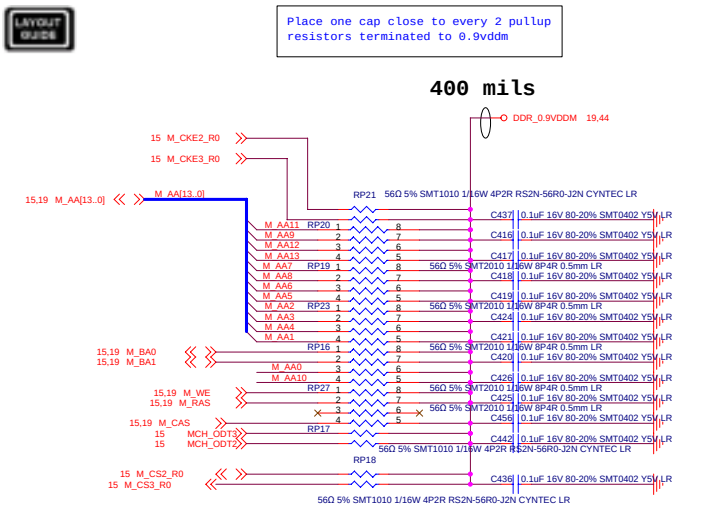
Date: Monday, November 14, 2005 Sheet 17 of 55




**SO DIMM 1**

Place one cap close to every 2 pullup resistors terminated to 0.9vddm

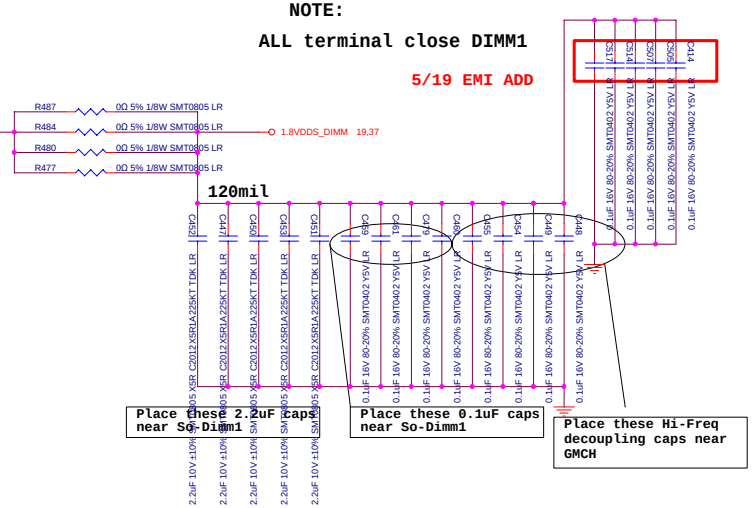
**400 mils**




**NOTE:**

**ALL terminal close DIMM1**

**5/19 EMI ADD**

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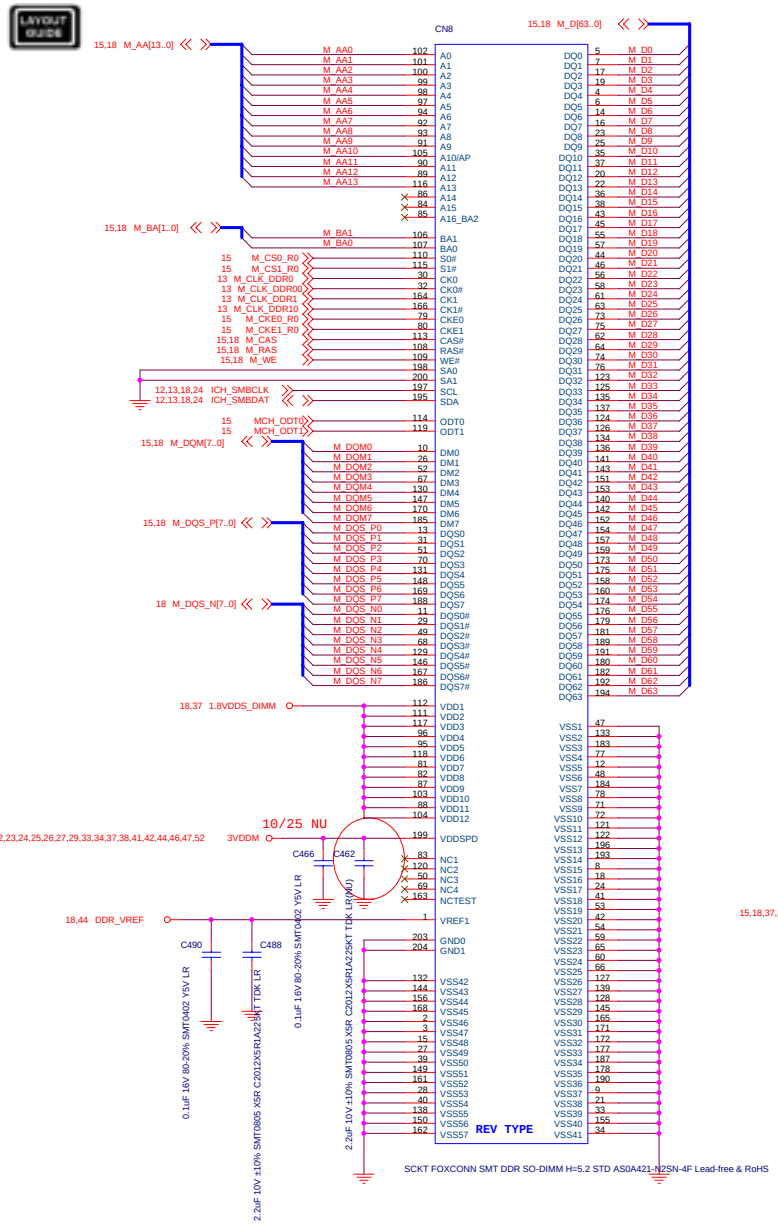
Title: **LM7W < VIA VN800 + VT8237R >**

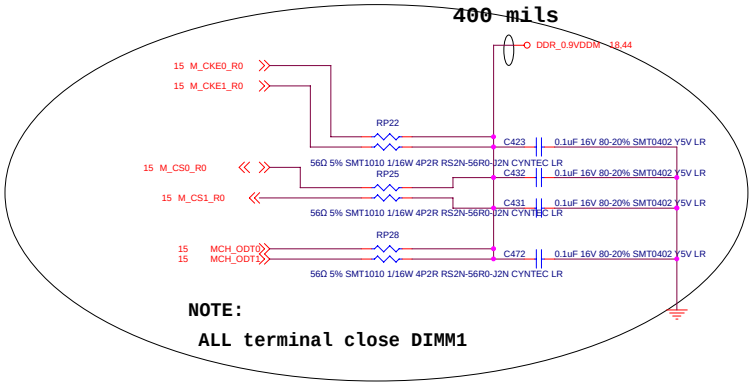
Size: C | Document Number: **<DDR-dimm-1>** | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 18 of 55



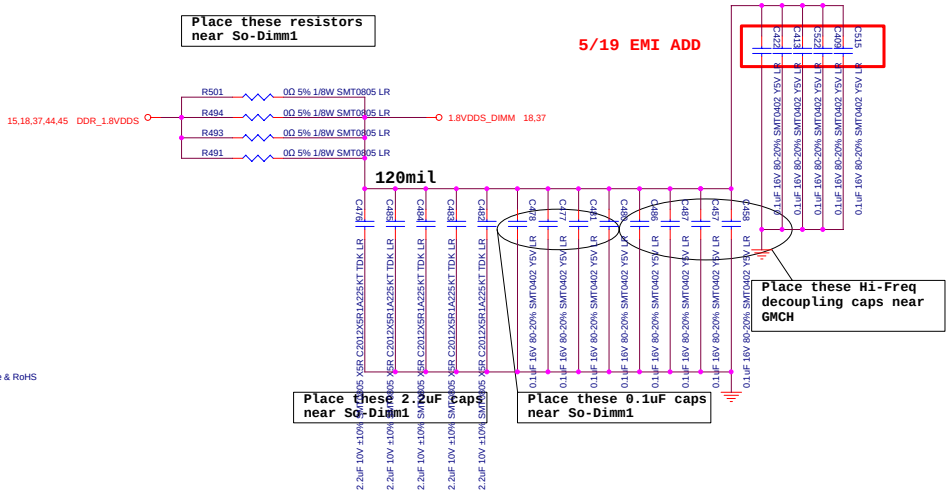

**SO DIMM 0**

Place one cap close to every 2 pullup resistors terminated to 0.9vddm




**NOTE:**
**ALL terminal close DIMM1**

Place these resistors near So-Dimm1





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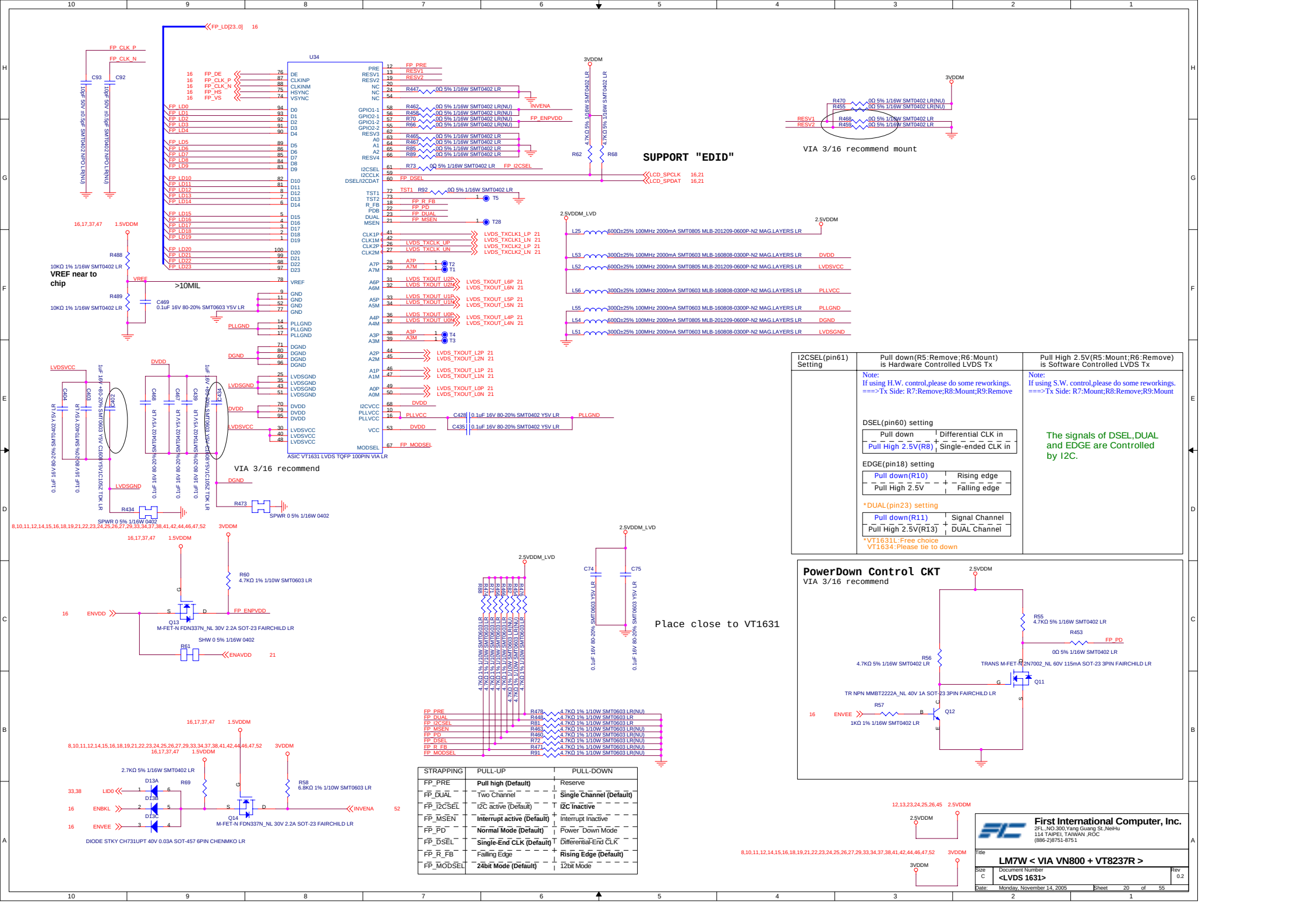
Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <DDR-dimm-2> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 19 of 55




| I2CSEL(pin61) Setting | Pull down(R5:Remove;R6:Mount) is Hardware Controlled LVDS Tx | Pull High 2.5V(R5:Mount;R6:Remove) is Software Controlled LVDS Tx |
|---|---|---|
| | Note:<br>If using H.W. control,please do some reworkings.<br>===>Tx Side: R7:Remove;R8:Mount;R9:Remove<br><br>DSEL(pin60) setting<br>Pull down / Differential CLK in<br>Pull High 2.5V(R8) / Single-ended CLK in<br><br>EDGE(pin18) setting<br>Pull down(R10) / Rising edge<br>Pull High 2.5V / Falling edge<br><br>*DUAL(pin23) setting<br>Pull down(R11) / Signal Channel<br>Pull High 2.5V(R13) / DUAL Channel<br><br>*VT1631L:Free choice<br>VT1634:Please tie to down | Note:<br>If using S.W. control,please do some reworkings.<br>===>Tx Side: R7:Mount;R8:Remove;R9:Mount<br><br>The signals of DSEL,DUAL and EDGE are Controlled by I2C. |

| STRAPPING | PULL-UP | PULL-DOWN |
|---|---|---|
| FP_PRE | **Pull high (Default)** | Reserve |
| FP_DUAL | Two Channel | **Single Channel (Default)** |
| FP_I2CSEL | I2C active (Default) | **I2C Inactive** |
| FP_MSEN | **Interrupt active (Default)** | Interrupt Inactive |
| FP_PD | **Normal Mode (Default)** | Power_Down Mode |
| FP_DSEL | **Single-End CLK (Default)** | Differential-End CLK |
| FP_R_FB | Failling Edge | **Rising Edge (Default)** |
| FP_MODSEL | **24bit Mode (Default)** | 12bit Mode |

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Title: **LM7W < VIA VN800 + VT8237R >**

| Size | Document Number | Rev |
|---|---|---|
| C | <LVDS 1631> | 0.2 |

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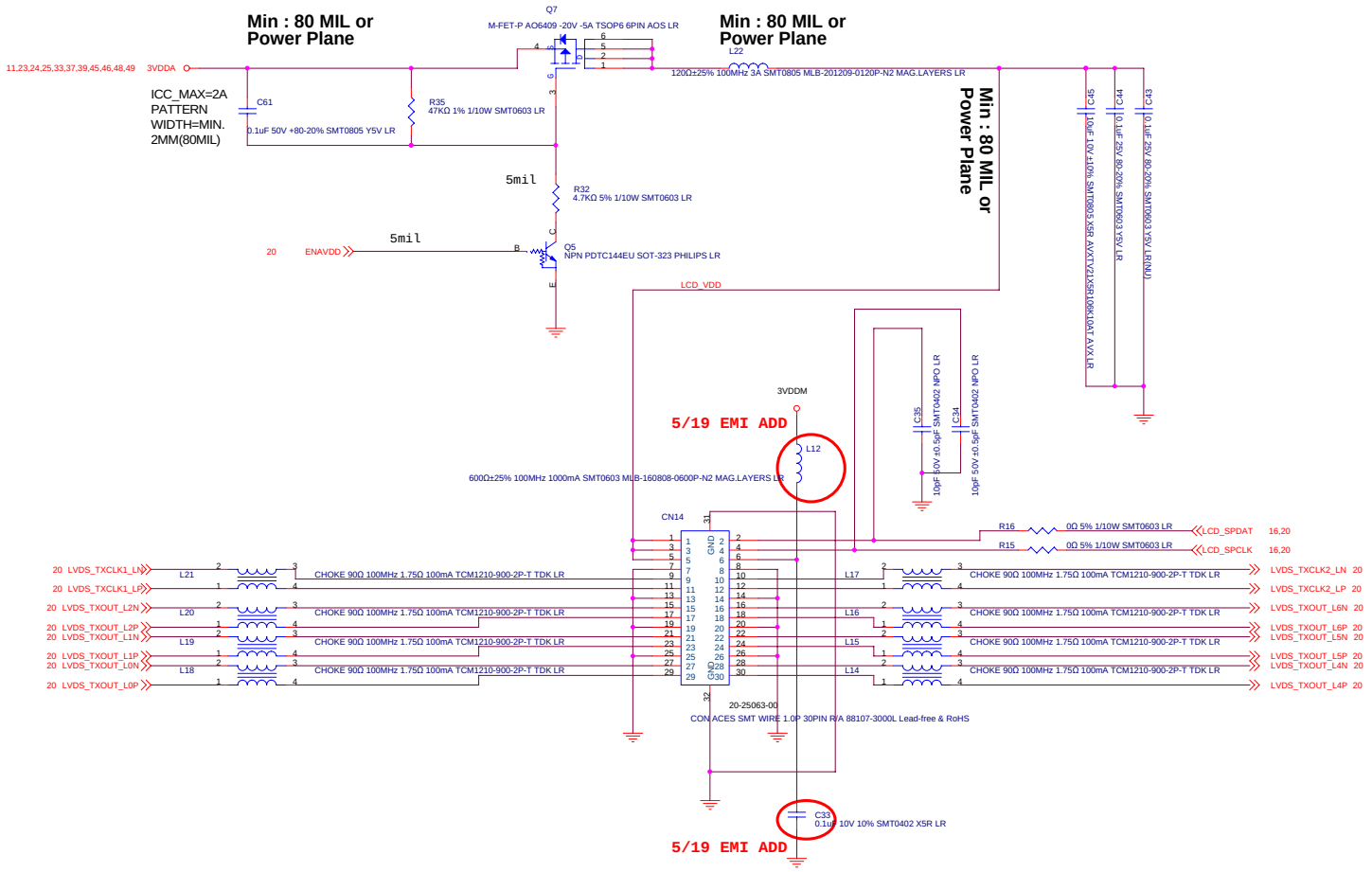


## LVDS Interface

| Signal | LENGTH | TRACE | SPACE | TRACE MUTCHING | Impedance | Note |
|---|---|---|---|---|---|---|
| LVDS | 10"<br>Cable MAX 16" | 4 mils (stripline)<br>6 mils (microstrip) | 20 mils<br>7 mils (edge to edge)<br>20 mils (pair to pair)<br>20 mils (to non LVDS signal) | +/-20 mils (data to data)<br>+/-20 mils (with a clock pair)<br>X +/-20 mils (clock to clock) | 100 ohms +/-15% | Breakout region from NB should be less than 500 mils |

8,10,11,12,14,15,16,18,19,20,22,23,24,25,26,27,29,33,34,37,38,41,42,44,46,47,52 3VDDM

3VDDM

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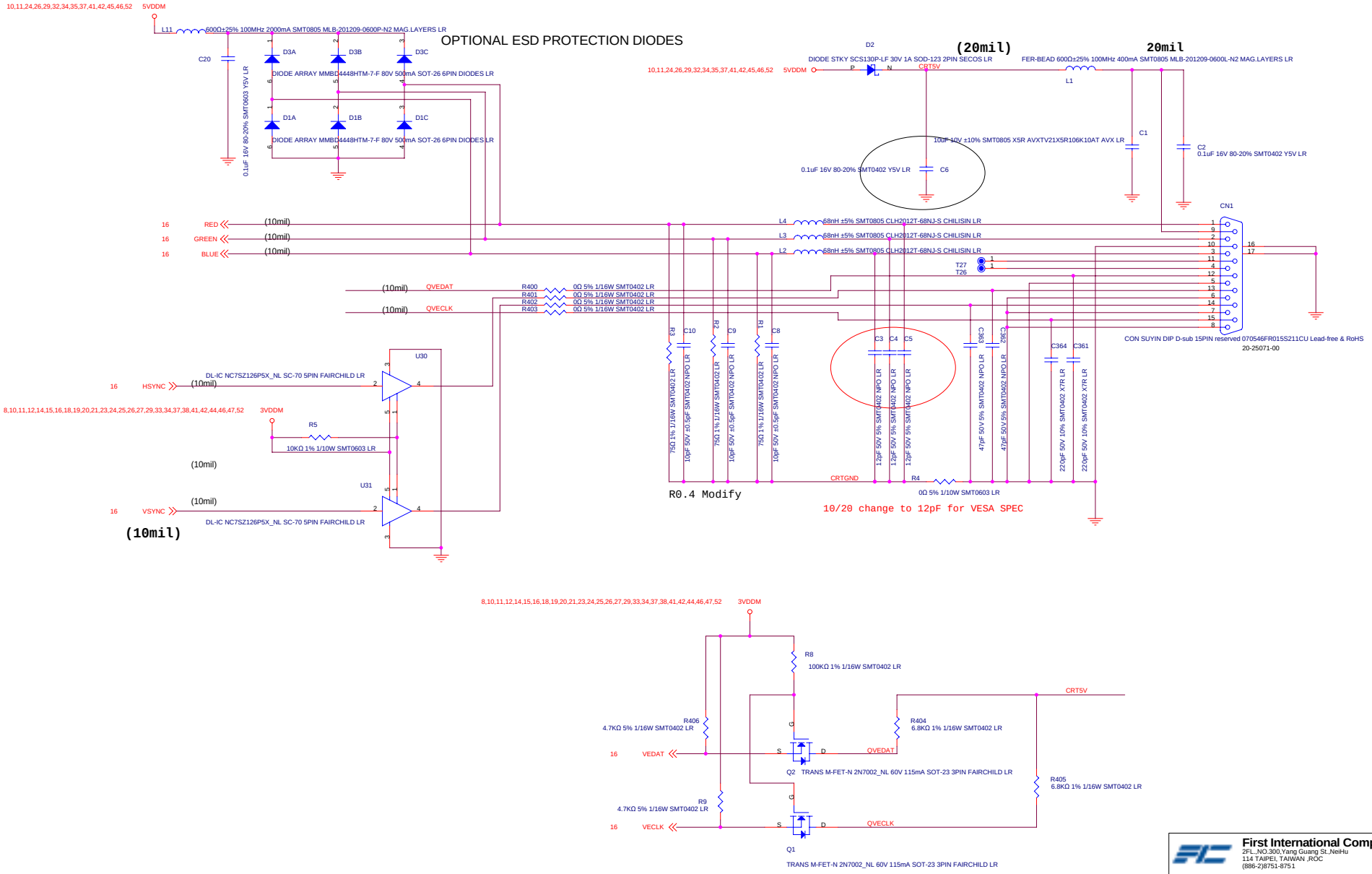
Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <LCD connecter> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 21 of 55





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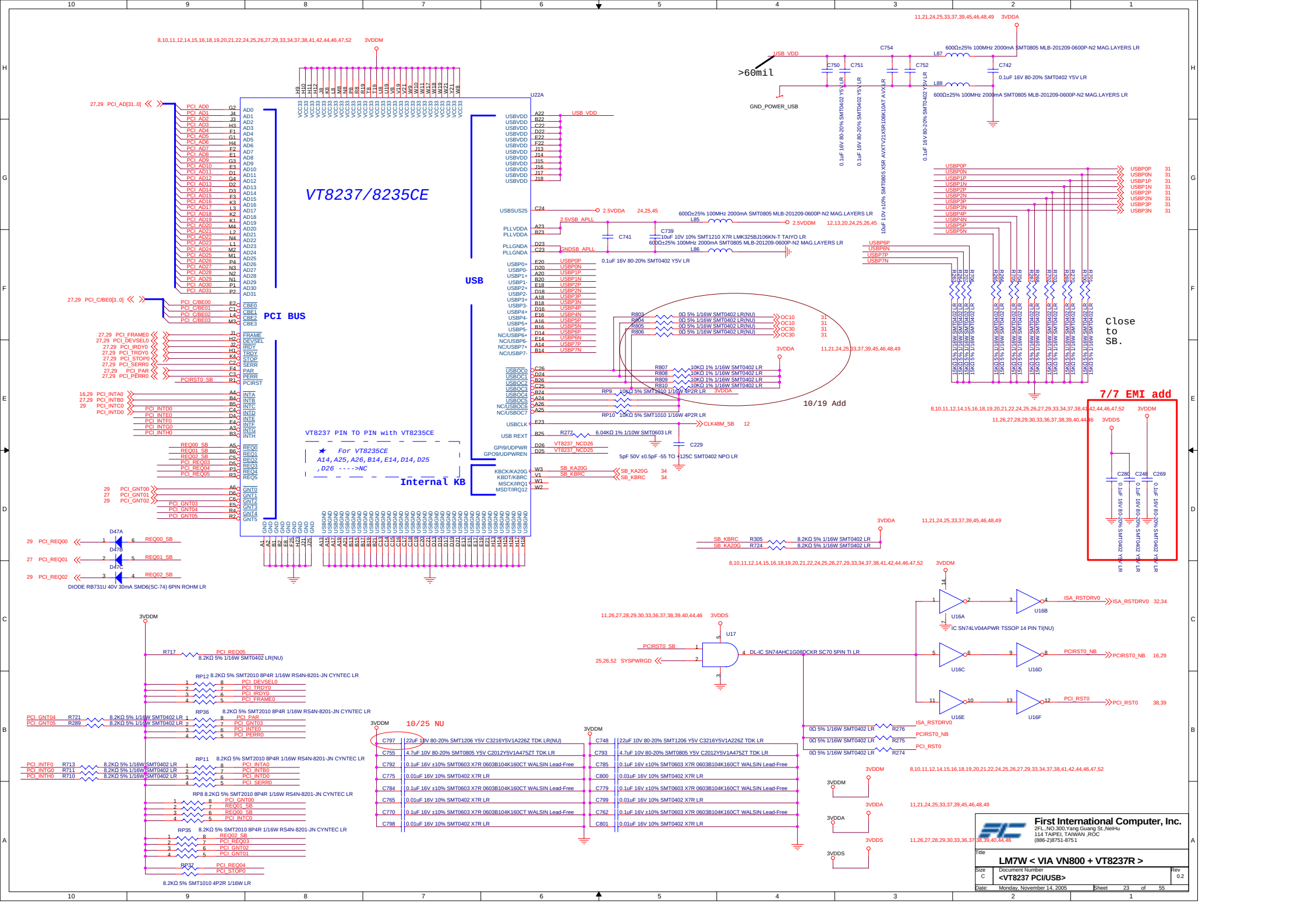
Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <CRT connector> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 22 of 55


VT8237/8235CE
PCI BUS
USB
Internal KB
VT8237 PIN TO PIN with VT8235CE
★ For VT8235CE
A14,A25,A26,B14,E14,D14,D25
,D26 ---->NC
10/19 Add
7/7 EMI add
Close to SB.
10/25 NU
>60mil
DIODE RB731U 40V 30mA SMD6(SC-74) 6PIN ROHM LR
IC SN74LV04APWR TSSOP 14 PIN TI(NU)
DL-IC SN74AHC1G08DCKR SC70 5PIN TI LR
8.2KΩ 5% SMT1010 4P2R 1/16W LR
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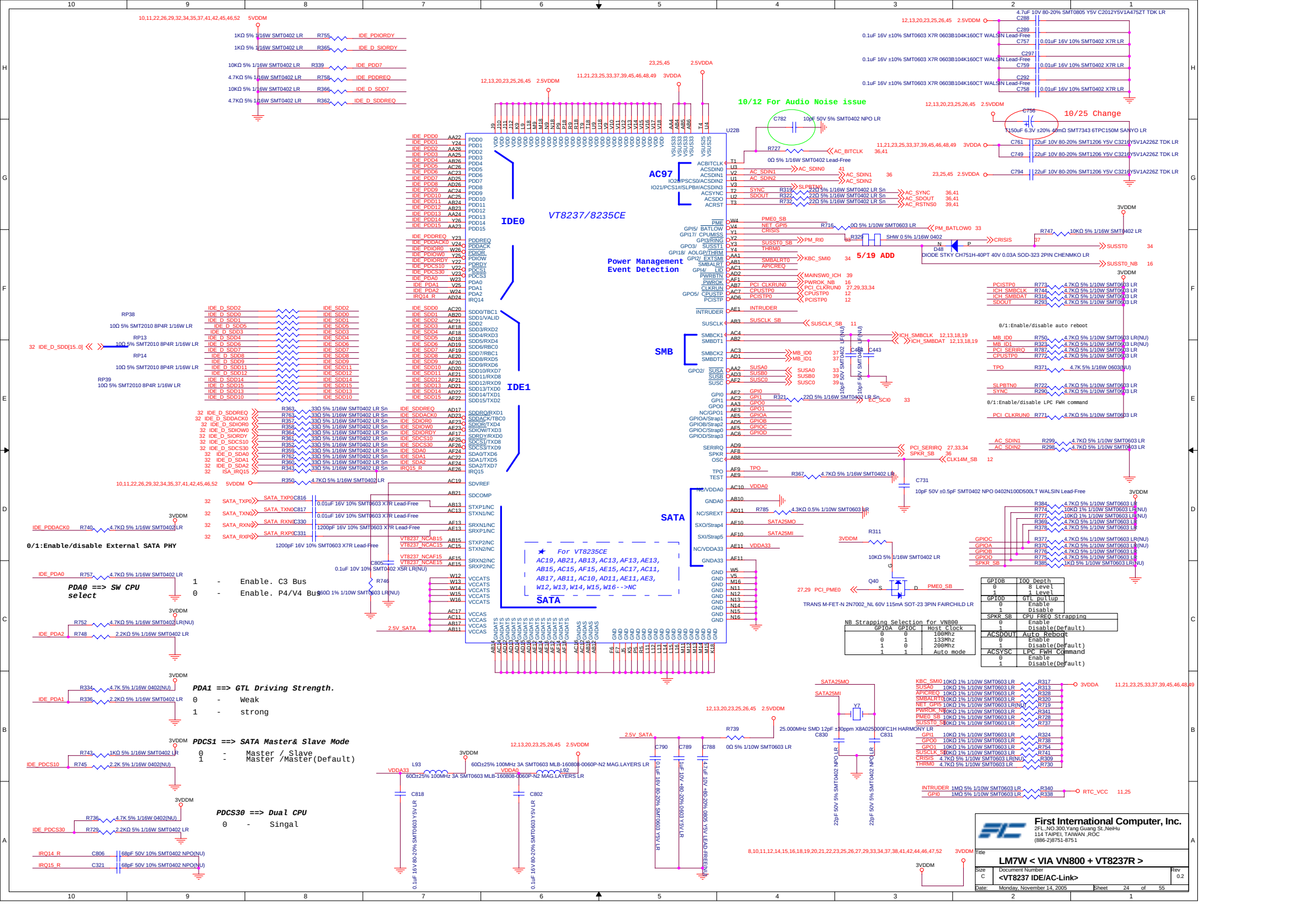
LM7W < VIA VN800 + VT8237R >
<VT8237 PCI/USB>
Monday, November 14, 2005
Sheet 23 of 55


VT8237/8235CE
IDE0
IDE1
AC97
SMB
SATA
Power Management
Event Detection
10/12 For Audio Noise issue
10/25 Change
5/19 ADD
PDA0 ==> SW CPU select
PDA1 ==> GTL Driving Strength.
PDCS1 ==> SATA Master& Slave Mode
PDCS30 ==> Dual CPU
0/1:Enable/disable External SATA PHY
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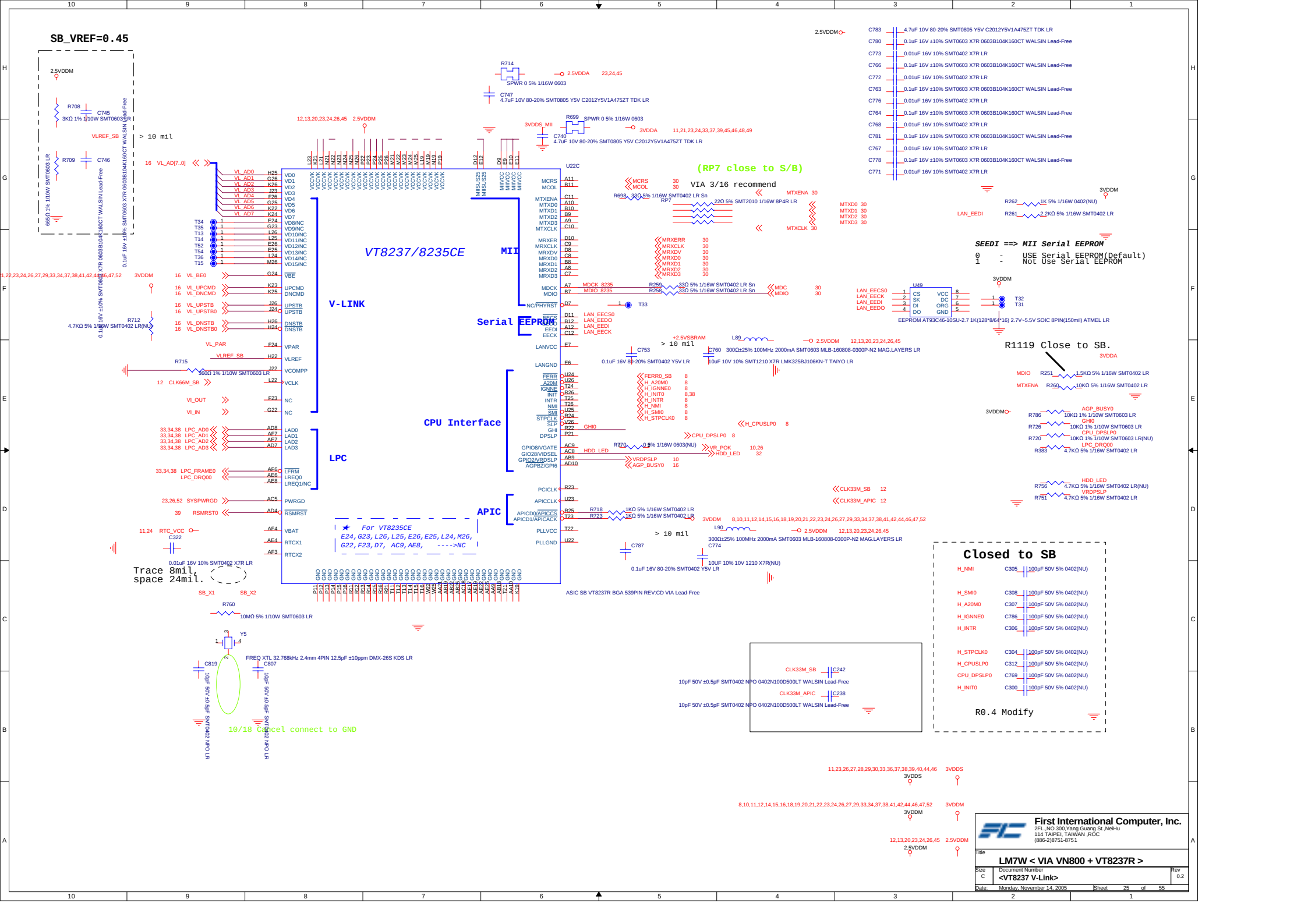
(886-2)8751-8751
LM7W < VIA VN800 + VT8237R >
<VT8237 IDE/AC-Link>
Monday, November 14, 2005


SB_VREF=0.45
VT8237/8235CE
V-LINK
MII
Serial EEPROM
CPU Interface
LPC
APIC
(RP7 close to S/B)
VIA 3/16 recommend
SEEDI ==> MII Serial EEPROM
0 - USE Serial EEPROM(Default)
1 - Not Use Serial EEPROM
R1119 Close to SB.
Closed to SB
R0.4 Modify
Trace 8mil, space 24mil.
10/18 Cancel connect to GND
ASIC SB VT8237R BGA 539PIN REV:CD VIA Lead-Free
First International Computer, Inc.
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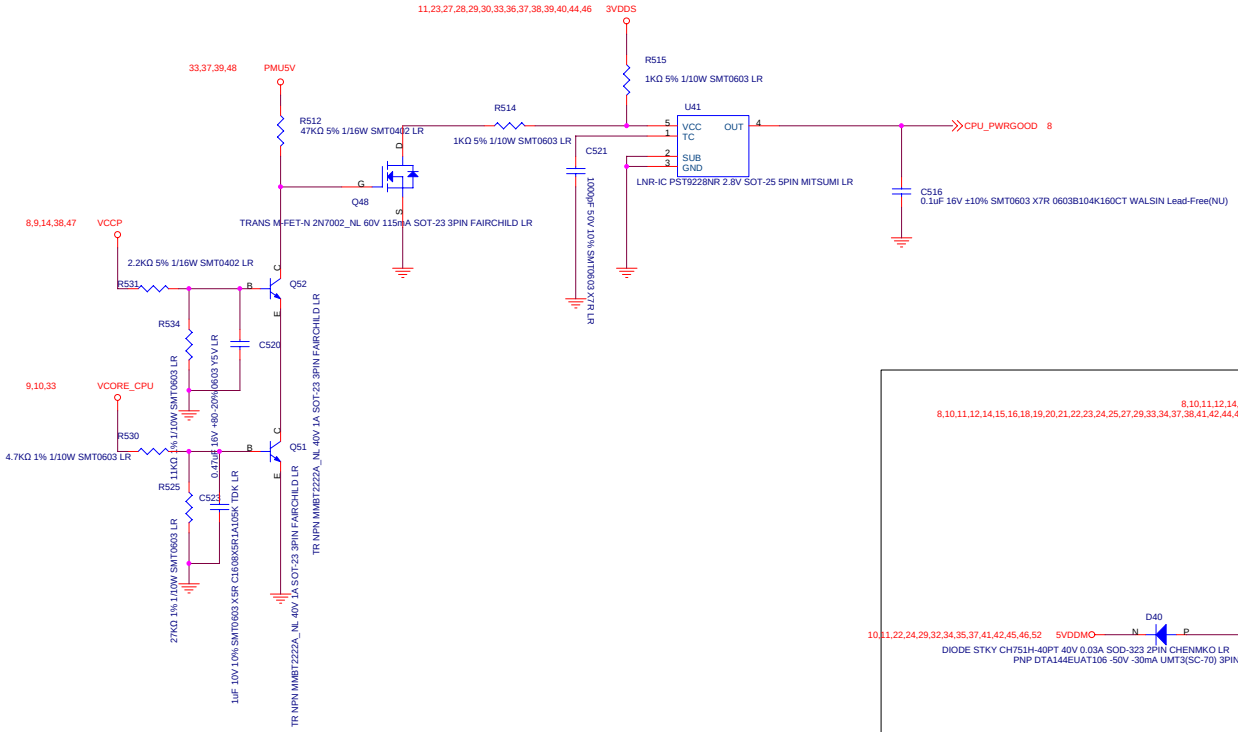
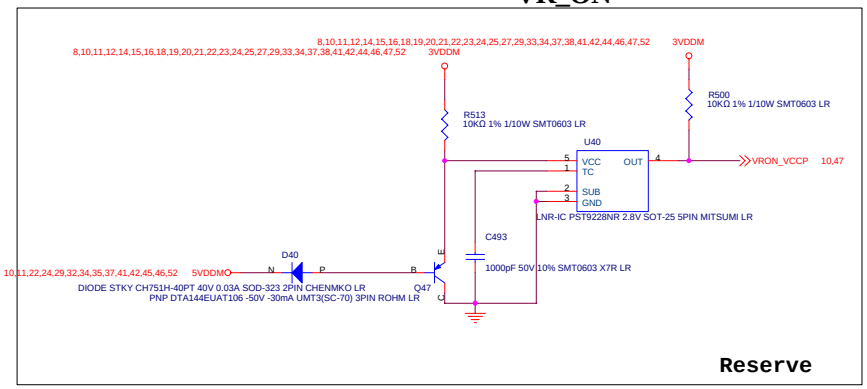
LM7W < VIA VN800 + VT8237R >
<VT8237 V-Link>
Monday, November 14, 2005

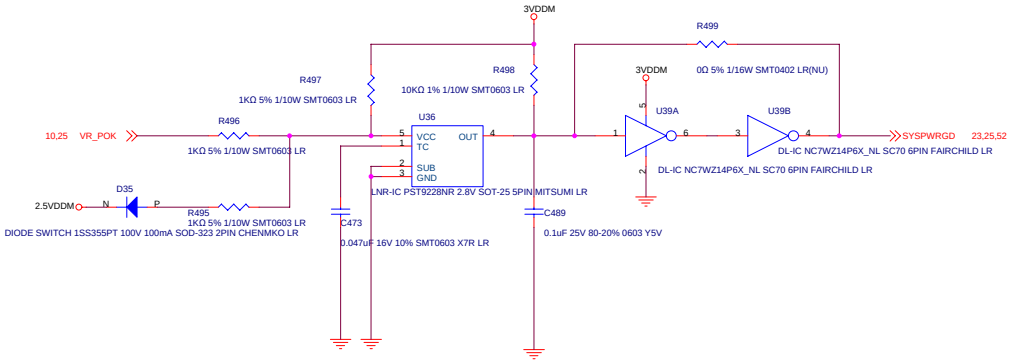
## CPU POWER OK CIRCUIT

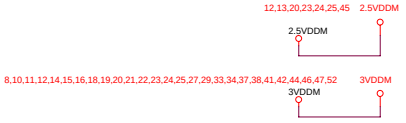



## VR_ON




## SYSTEM POWER OK CIRCUIT





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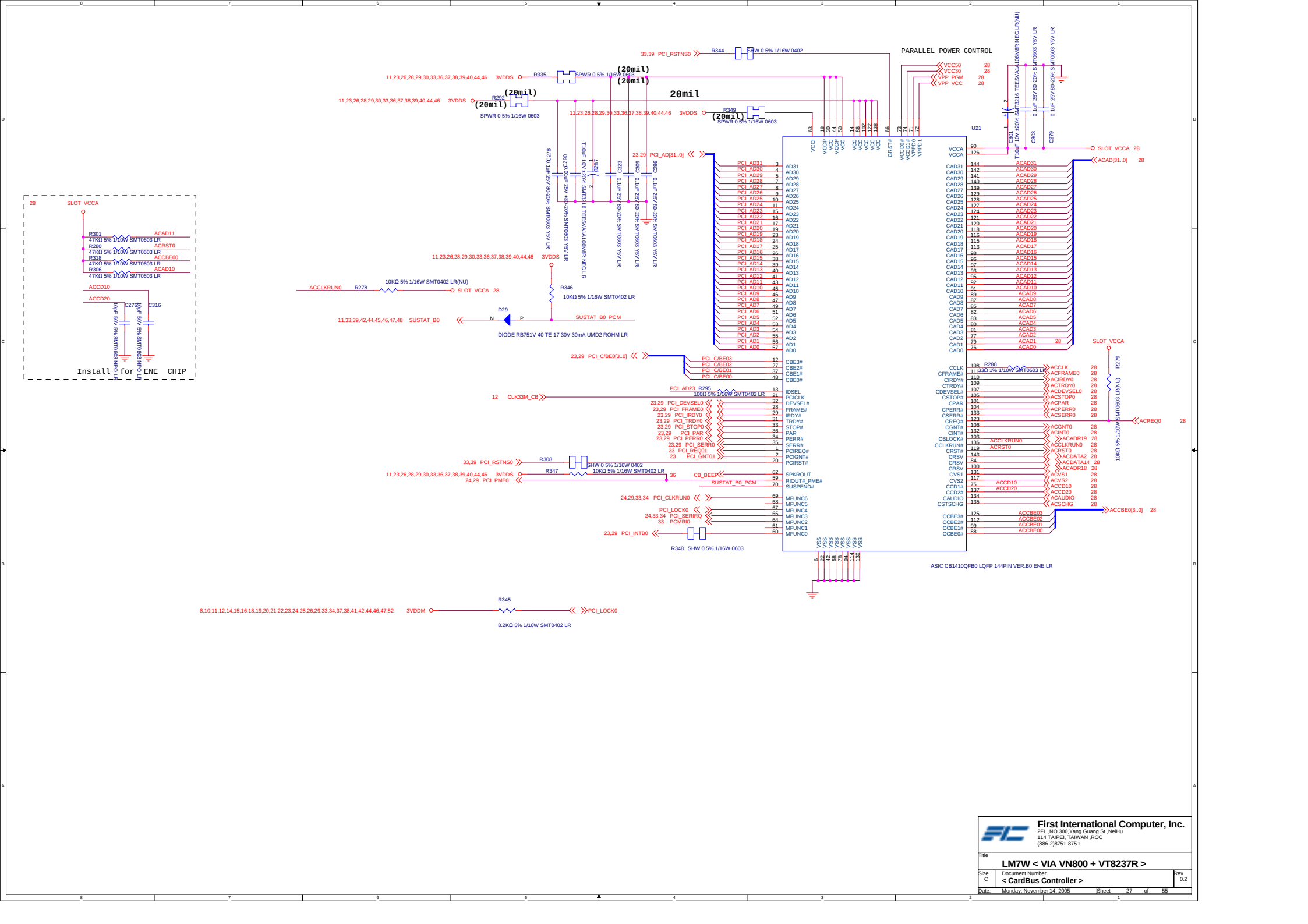
Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <POWER Good> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 26 of 55


PARALLEL POWER CONTROL
20mil
(20mil)
SPWR 0 5% 1/16W 0603
SHW 0 5% 1/16W 0402
10KΩ 5% 1/16W SMT0402 LR(NU)
10KΩ 5% 1/16W SMT0402 LR
8.2KΩ 5% 1/16W SMT0402 LR
33Ω 1% 1/10W SMT0603 LR
100Ω 5% 1/16W SMT0402 LR
DIODE RB751V-40 TE-17 30V 30mA UMD2 ROHM LR
ASIC CB1410QFB0 LQFP 144PIN VER:B0 ENE LR
Install for ENE CHIP
SLOT_VCCA
ACAD[31..0]
ACCBE0[3..0]
SUSTAT_B0_PCM
PCI_AD[31..0]
PCI_C/BE0[3..0]
PCI_RSTNS0
PCI_CLOCK0
PCI_SERIRQ
PCI_INTB0
PCI_CLKRUN0
PCI_PME0
CB_BEEP
CLK33M_CB
ACCLKRUN0
ACRST0
ACCD10
ACCD20
ACREQ0
First International Computer, Inc.
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(886-2)8751-8751
LM7W < VIA VN800 + VT8237R >
< CardBus Controller >
Monday, November 14, 2005
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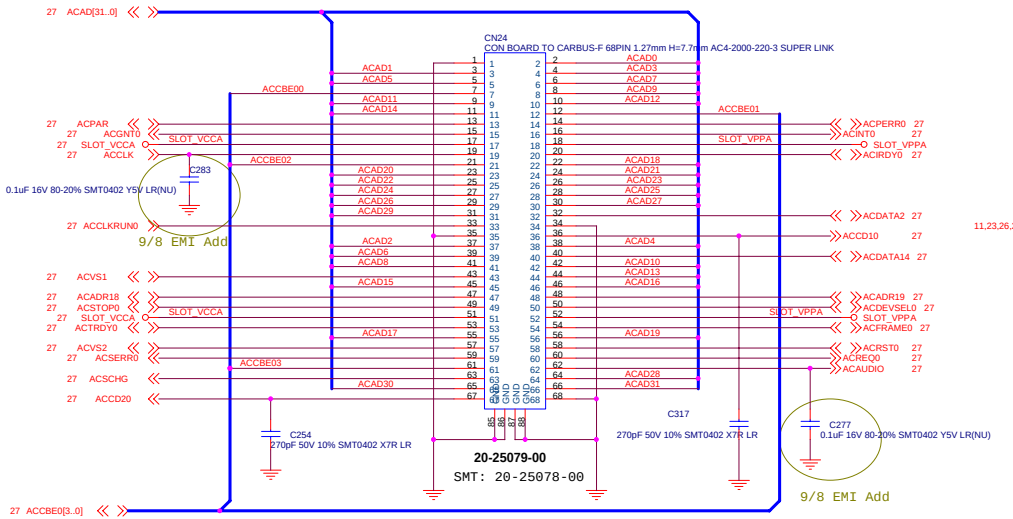


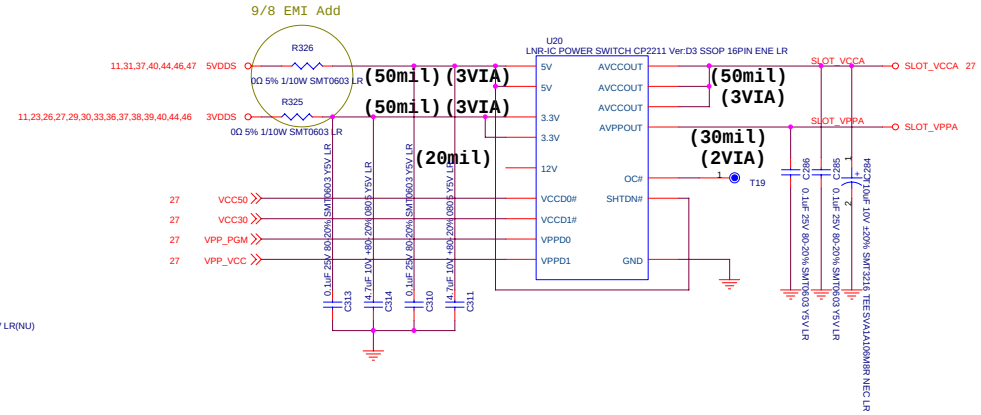



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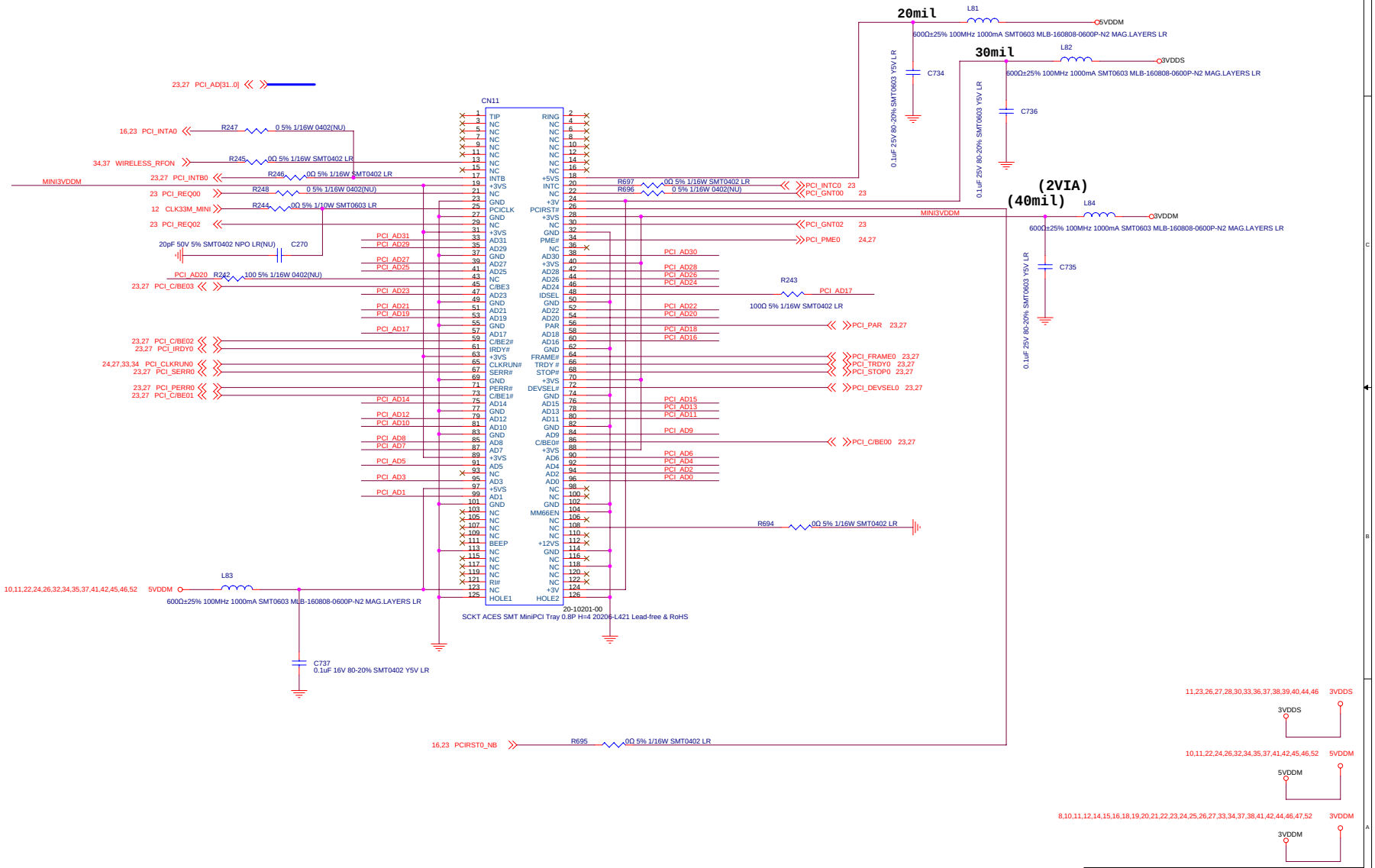
Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: < CardBus Power/CNN > | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 28 of 55

# TYPE III MODEM / LAN CONNECTOR





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Title: **LM7W < VIA VN800 + VT8237R >**

| Size | Document Number | Rev |
|---|---|---|
| C | <Mini-PCI> | 0.2 |

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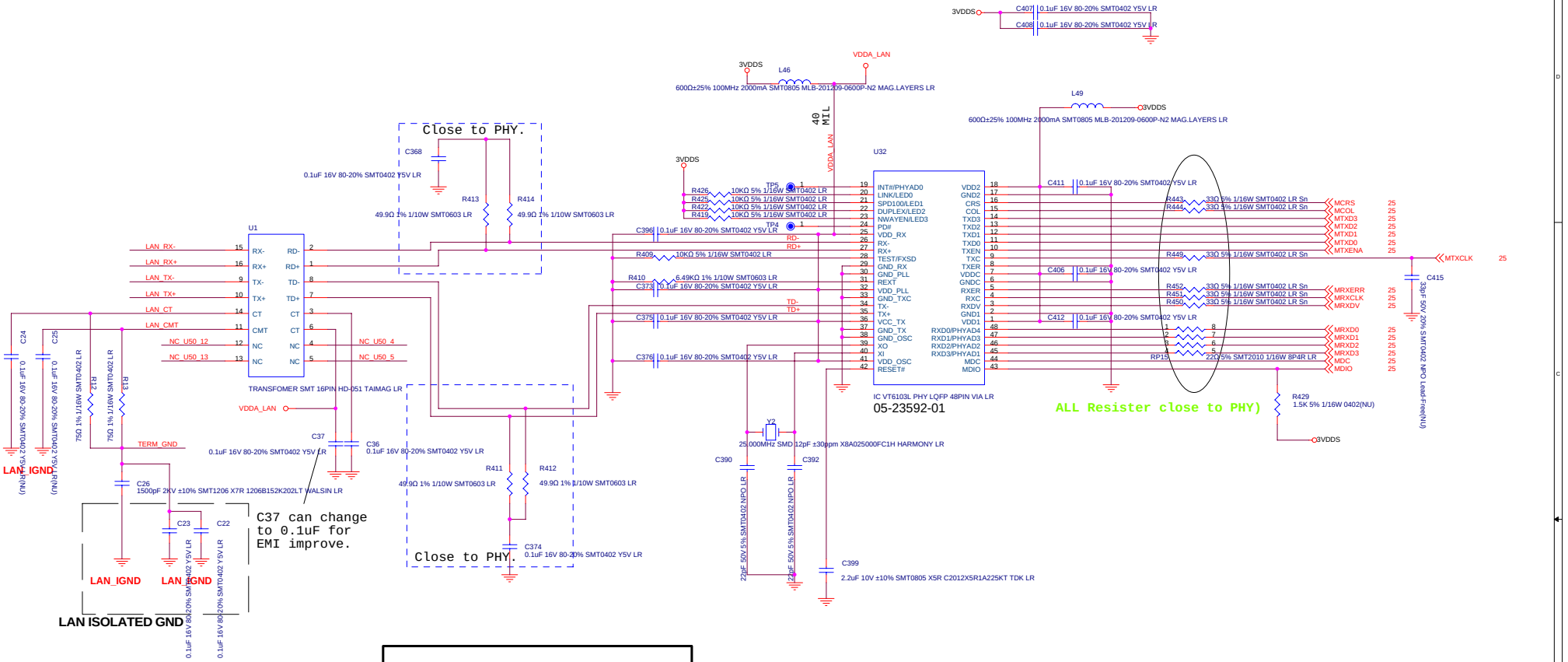
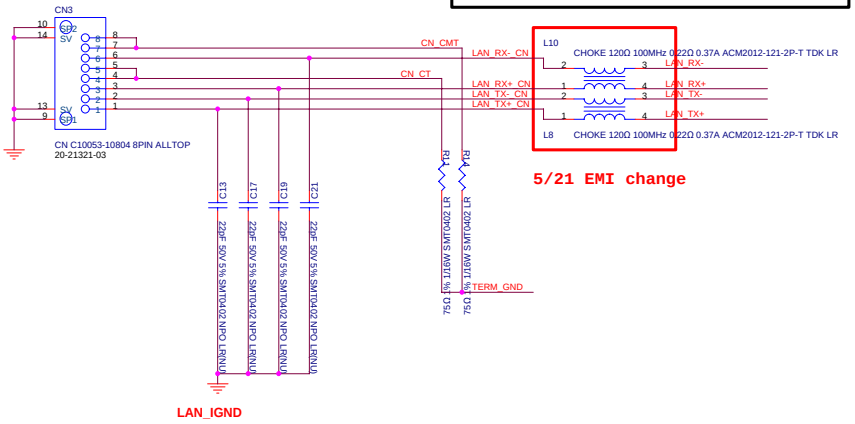



**TX & RX layout guide**

| | | |
|---|---|---|
| other | 24 MIL | |
| TX+ | 10 MIL | 6 MIL |
| TX- | 24 MIL | 6 MIL |
| other | | |

## LAN RJ45 JACK





11,23,26,27,28,29,33,36,37,38,39,40,44,46 3VDDS

3VDDS

| | | |
|---|---|---|
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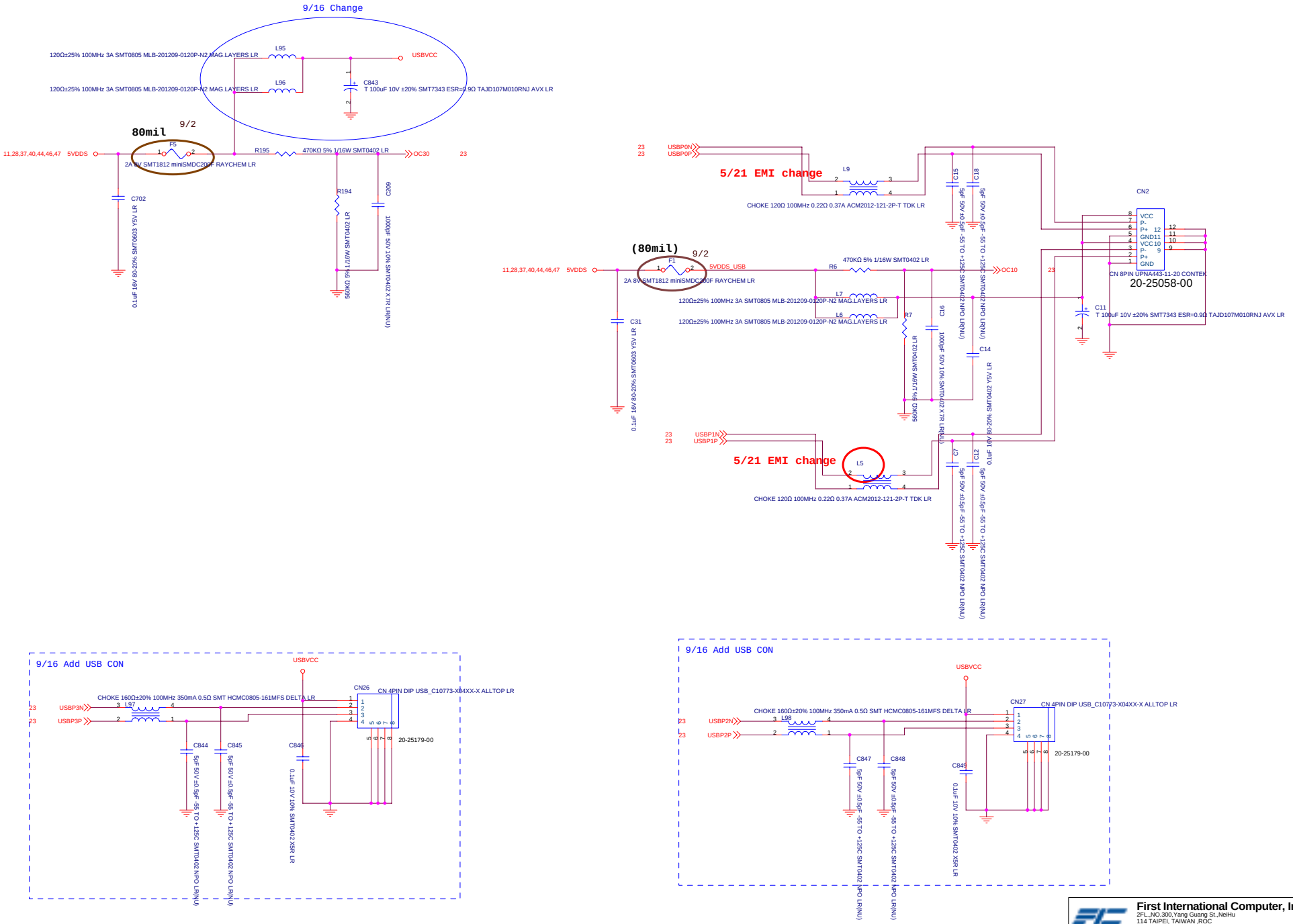
| Title | LM7W < VIA VN800 + VT8237R > | |
| Size C | Document Number <VT6103L LAN PHY> | Rev 0.2 |
| Date: Monday, November 14, 2005 | Sheet 30 of 55 | |





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Title
**LM7W < VIA VN800 + VT8237R >**

| Size | Document Number | Rev |
|---|---|---|
| C | <USB CNN> | 0.2 |

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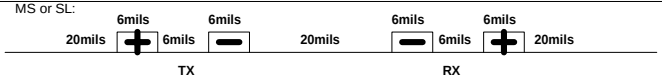
## SATA Layout Note:

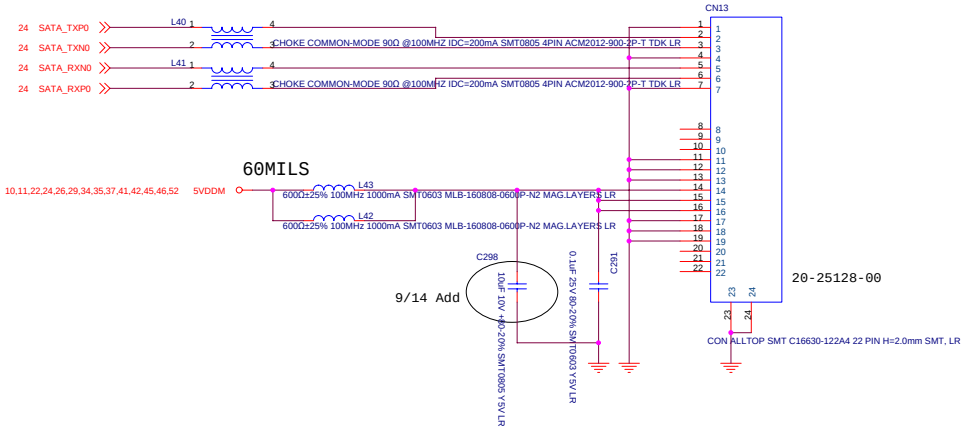
MS or SL:




* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

NOTE

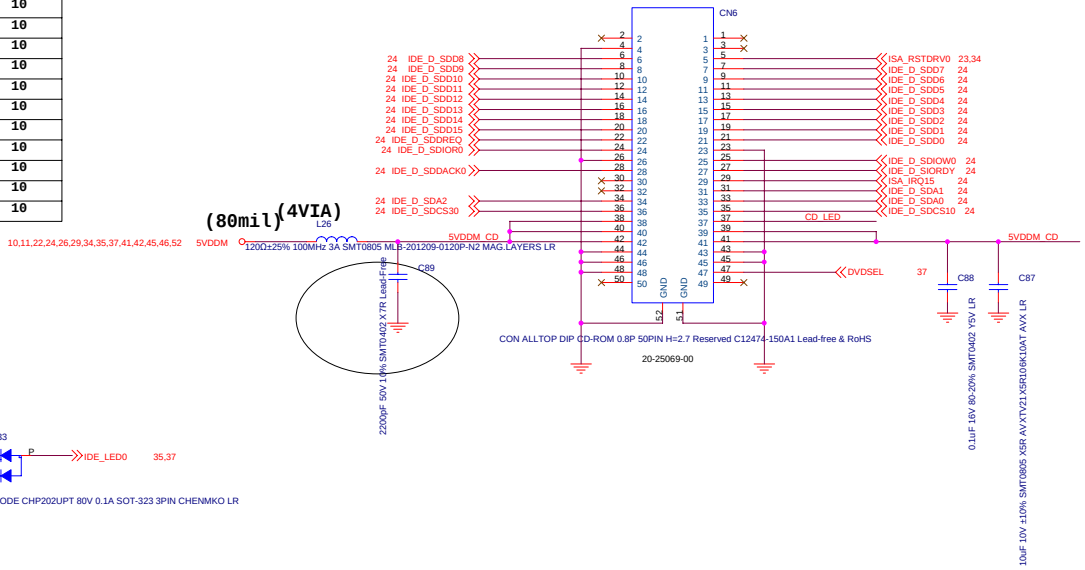
SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND




## IDE Signals

| Signals | MAX Length (inch) | Width (mils) | Space (mils) |
|---|---|---|---|
| IDE_PDD[15:0] | 8 | 5 | 10 |
| IDE_SDD[15:0] | 8 | 5 | 10 |
| IDE_PDA0-2 | 8 | 5 | 10 |
| IDE_SDA0-2 | 8 | 5 | 10 |
| IDE_PDCS 10-30# | 8 | 5 | 10 |
| IDE_PDDREQ | 8 | 5 | 10 |
| IDE_SDDREQ | 8 | 5 | 10 |
| IDE_PDIOW# | 8 | 5 | 10 |
| IDE_PATADET | 8 | 5 | 10 |
| IDE_SATADET | 8 | 5 | 10 |
| IDE_PDDACK# | 8 | 5 | 10 |
| IDE_SDDACK# | 8 | 5 | 10 |

# CDROM CNN





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Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <IDE connector> | Rev: 0.2

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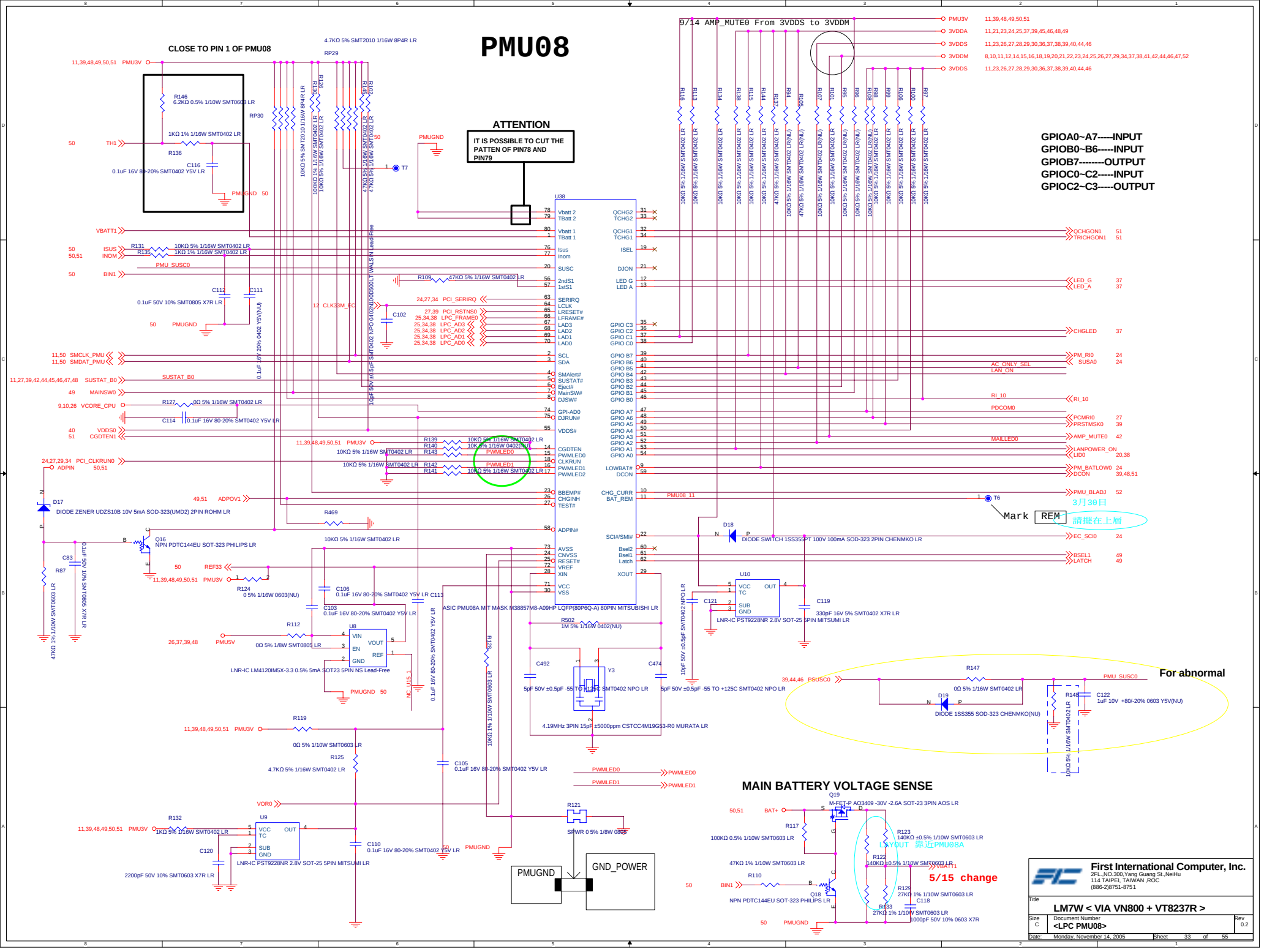
# PMU08


CLOSE TO PIN 1 OF PMU08
ATTENTION
IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79
9/14 AMP_MUTE0 From 3VDDS to 3VDDM
PMU3V 11,39,48,49,50,51
3VDDA 11,21,23,24,25,37,39,45,46,48,49
3VDDS 11,23,26,27,28,29,30,36,37,38,39,40,44,46
3VDDM 8,10,11,12,14,15,16,18,19,20,21,22,23,24,25,26,27,29,34,37,38,41,42,44,46,47,52
3VDDS 11,23,26,27,28,29,30,36,37,38,39,40,44,46
GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT
U38
ASIC PMU08A MIT MASK M38857M8-A09HP LQFP(80P6Q-A) 80PIN MITSUBISHI LR
Mark REM 請擺在上層
3月30日
For abnormal
MAIN BATTERY VOLTAGE SENSE
5/15 change
LAYOUT 靠近PMU08A
LNR-IC PST9228NR 2.8V SOT-25 5PIN MITSUMI LR
LNR-IC LM4120IM5X-3.3 0.5% 5mA SOT23 5PIN NS Lead-Free
4.19MHz 3PIN 15pF ±5000ppm CSTCC4M19G53-R0 MURATA LR
DIODE ZENER UDZS10B 10V 5mA SOD-323(UMD2) 2PIN ROHM LR
DIODE SWITCH 1SS355PT 100V 100mA SOD-323 2PIN CHENMKO LR
DIODE 1SS355 SOD-323 CHENMKO(NU)
NPN PDTC144EU SOT-323 PHILIPS LR
M-FET-P AO3409 -30V -2.6A SOT-23 3PIN AOS LR
SPWR 0 5% 1/8W 0805
GND_POWER
PMUGND
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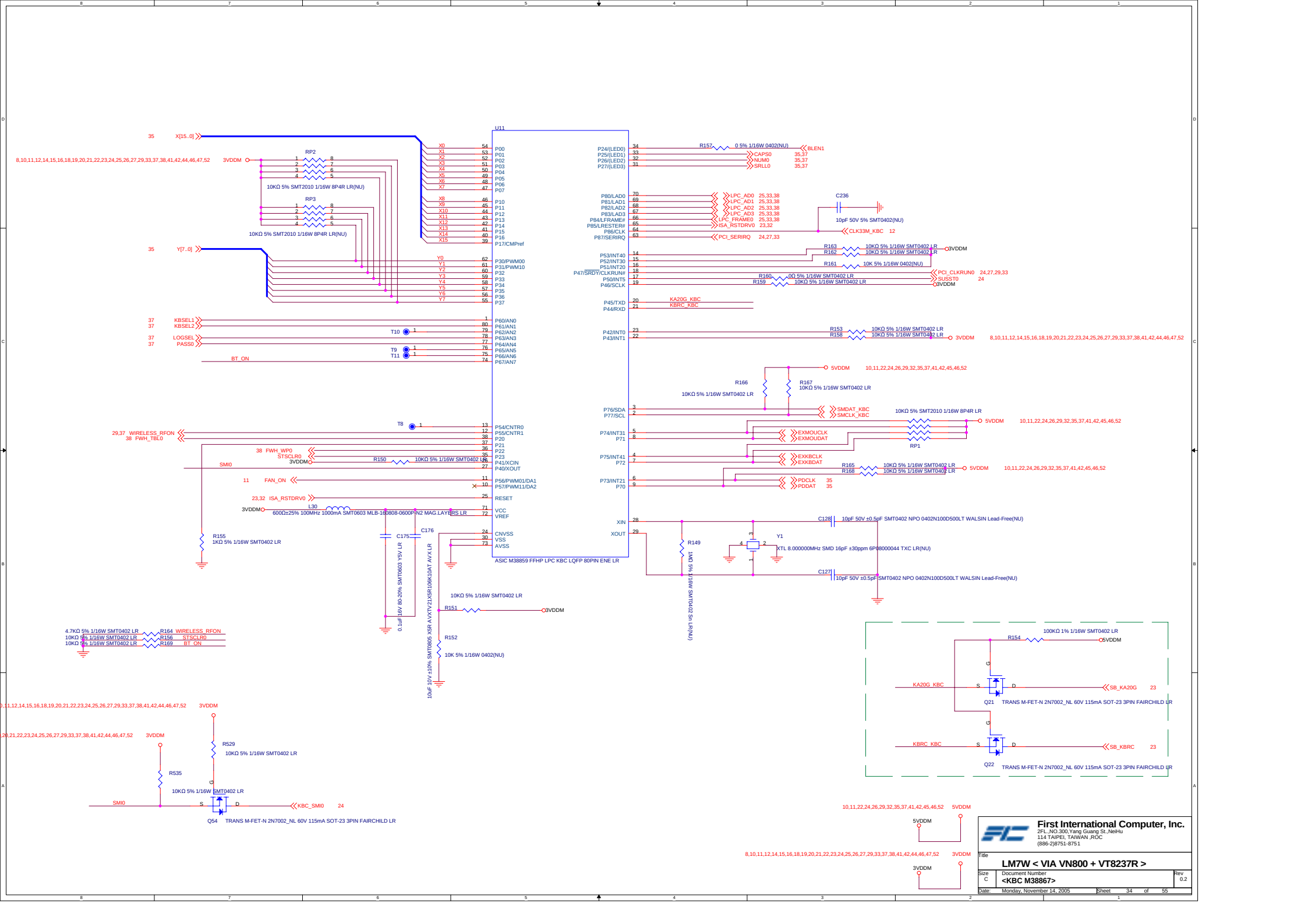
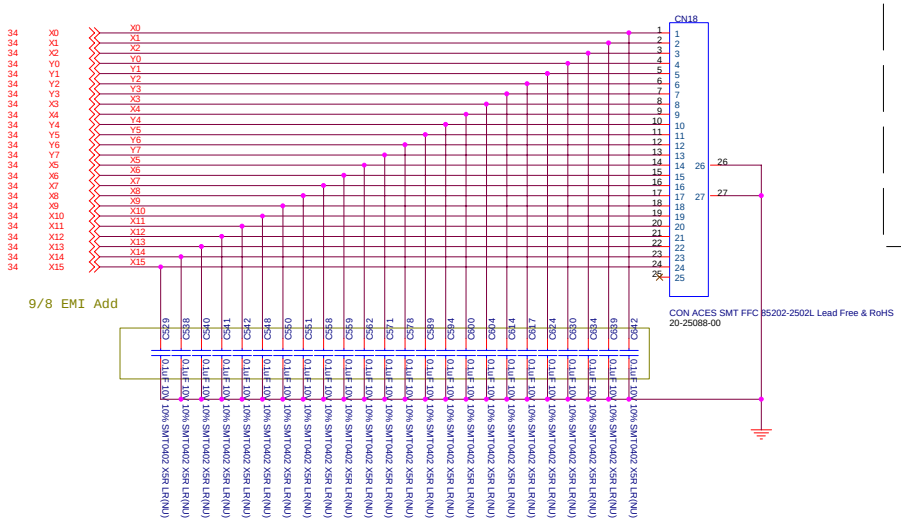
Title
LM7W < VIA VN800 + VT8237R >
Size C
Document Number
<LPC PMU08>
Rev 0.2
Date: Monday, November 14, 2005
Sheet 33 of 55

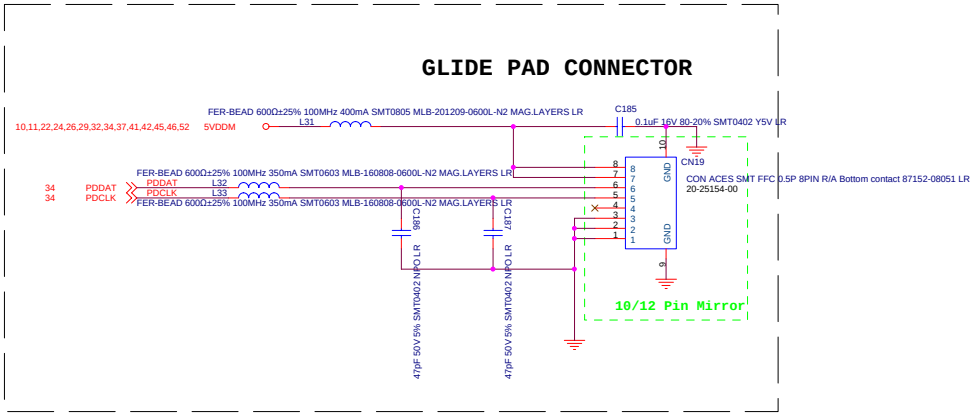


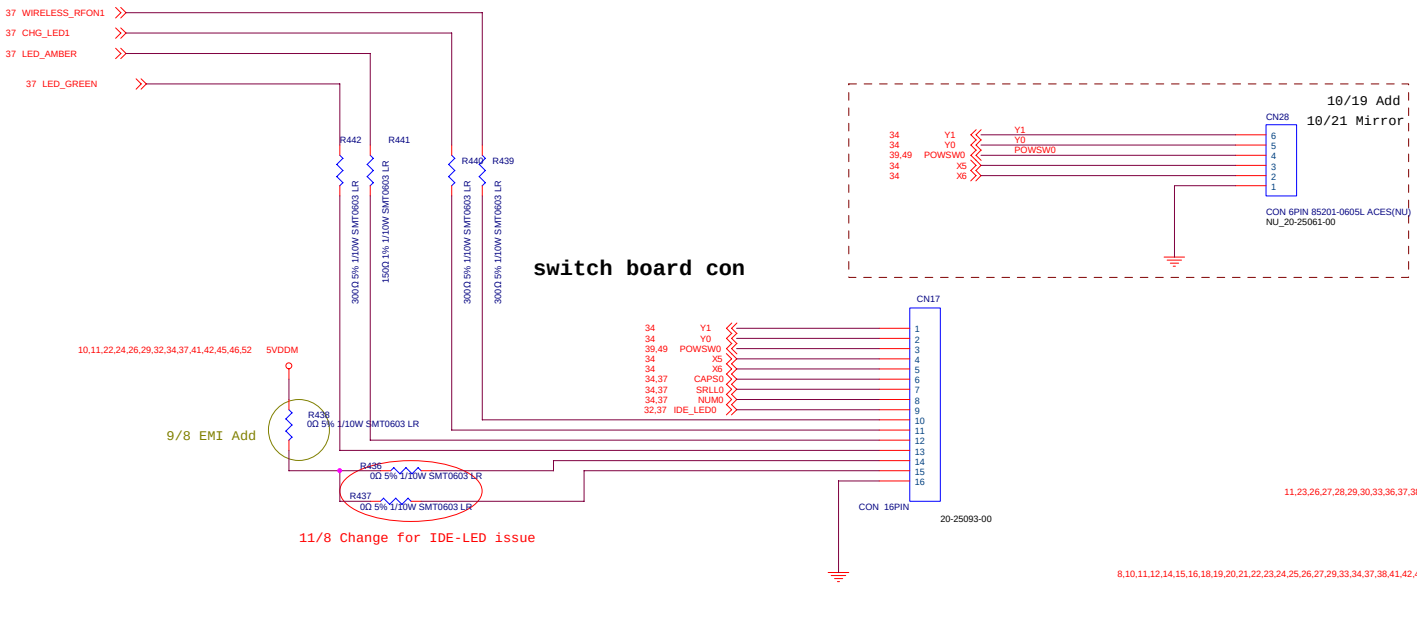

| | |
|---|---|
| Company | First International Computer, Inc. |
| Address | 2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC |
| Phone | (886-2)8751-8751 |
| Title | LM7W < VIA VN800 + VT8237R > |
| Size | C |
| Document Number | <KBC M38867> |
| Rev | 0.2 |
| Date | Monday, November 14, 2005 |
| Sheet | 34 of 55 |

# INT KB CNN




## GLIDE PAD CONNECTOR




| | | |
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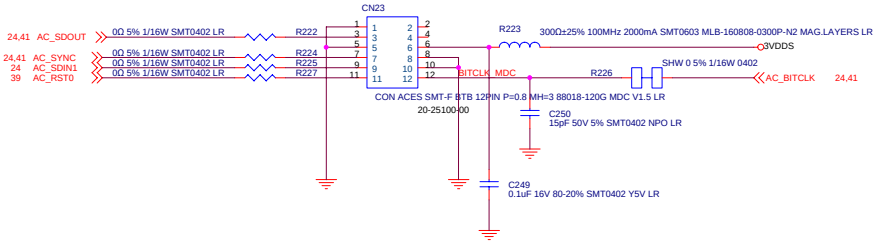
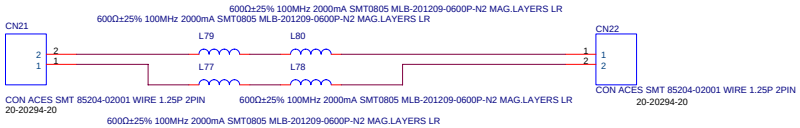
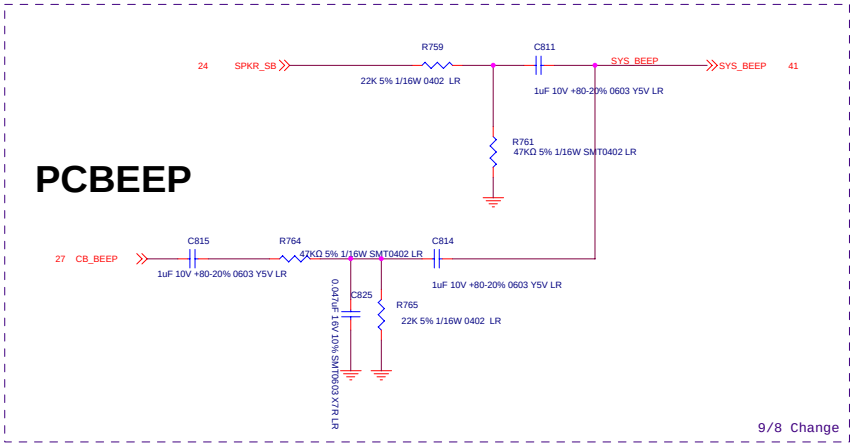
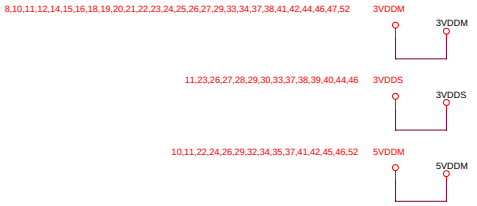
| (886-2)8751-8751 | | |
| Title | LM7W < VIA VN800 + VT8237R > | |
| Size C | Document Number <INT K/B /GP/SW CNN> | Rev 0.2 |
| Date: Monday, November 14, 2005 | Sheet 35 of 55 | |

# MDC 1.5 CNN





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Title
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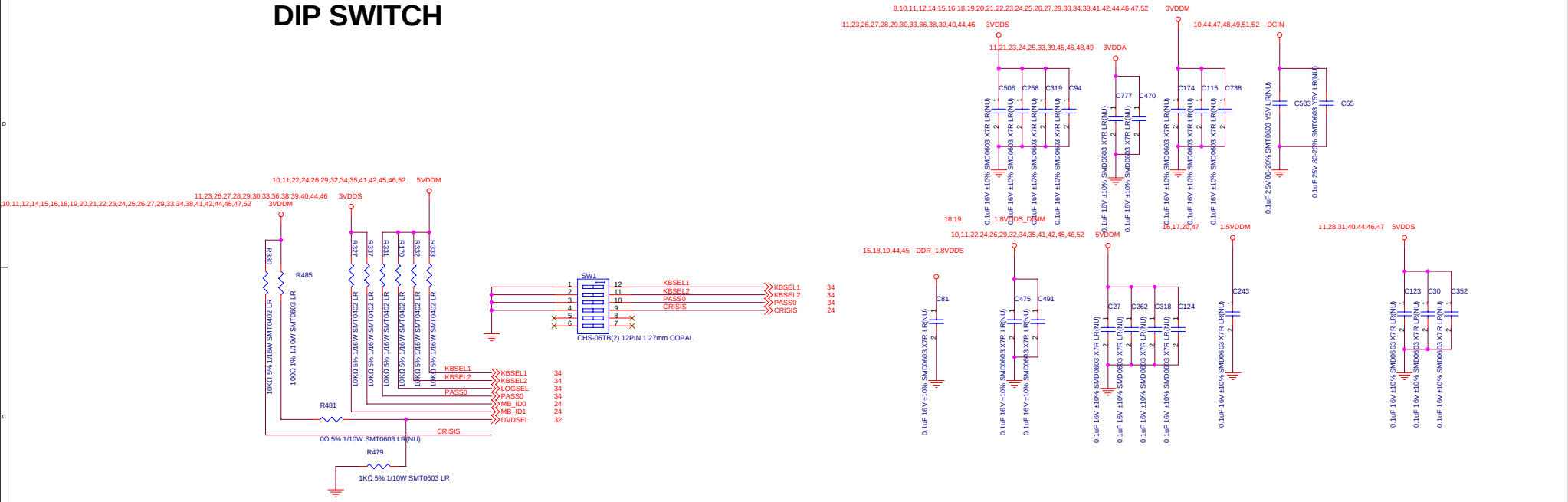
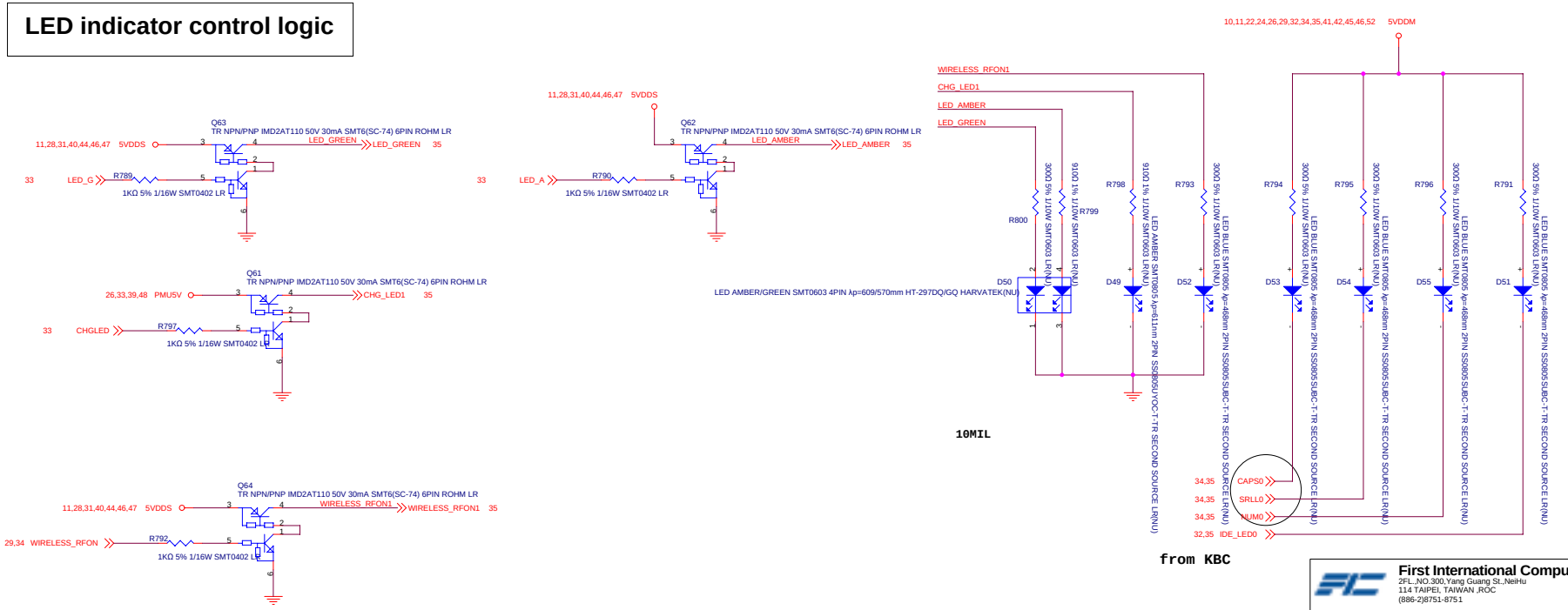
| Size | Document Number | Rev |
|---|---|---|
| C | <MDC CNN / PCBEEP> | 0.2 |

Date: Monday, November 14, 2005 Sheet 36 of 55

# DIP SWITCH




## LED indicator control logic





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| | | |
|---|---|---|
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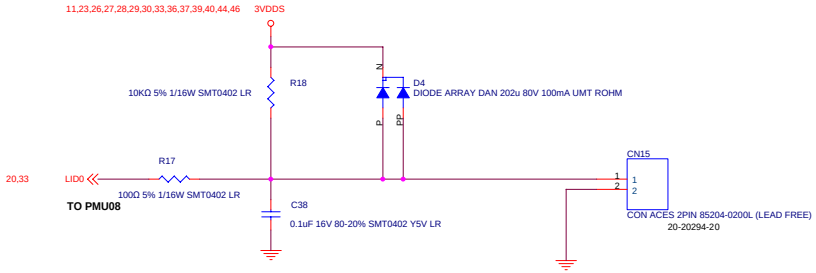
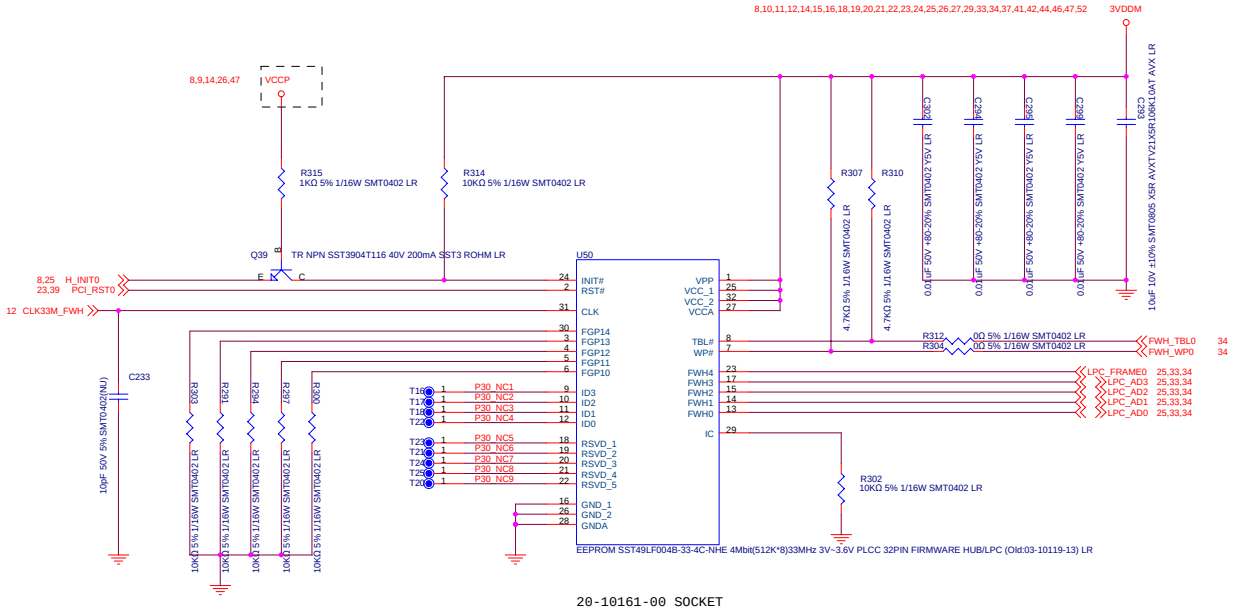
| Size: C | Document Number: <DIP SW/ LED> | Rev: 0.2 |
| Date: Monday, November 14, 2005 | Sheet 37 of 55 | |

# LID Switch




# 4M FLASH ROM




20-10161-00 SOCKET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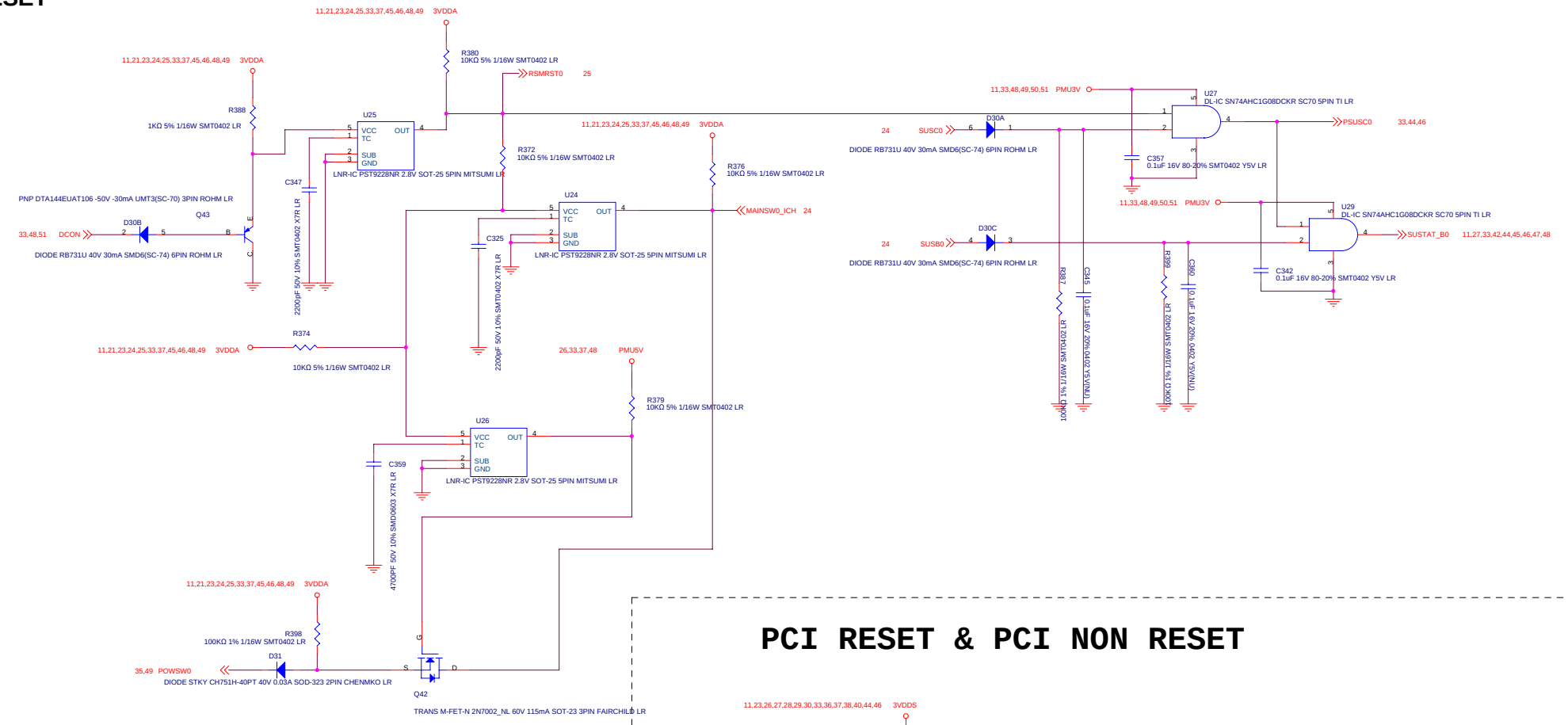
Title: LM7W < VIA VN800 + VT8237R >

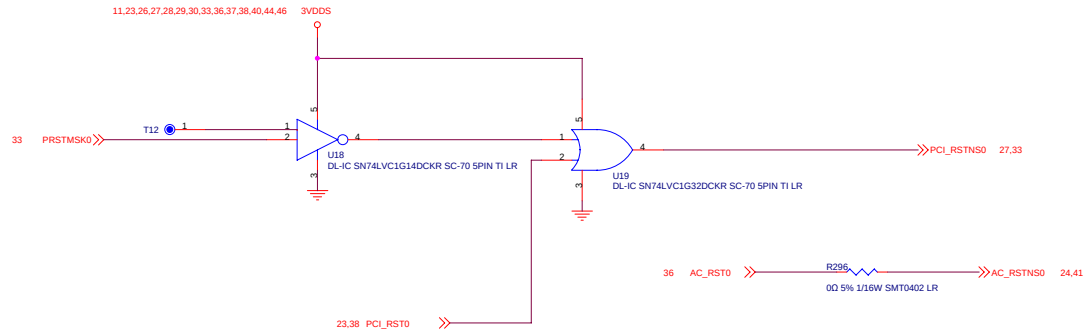
Size: C | Document Number: <LID SW/ BIOS> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 38 of 55

# RESUME RESET




# PCI RESET & PCI NON RESET





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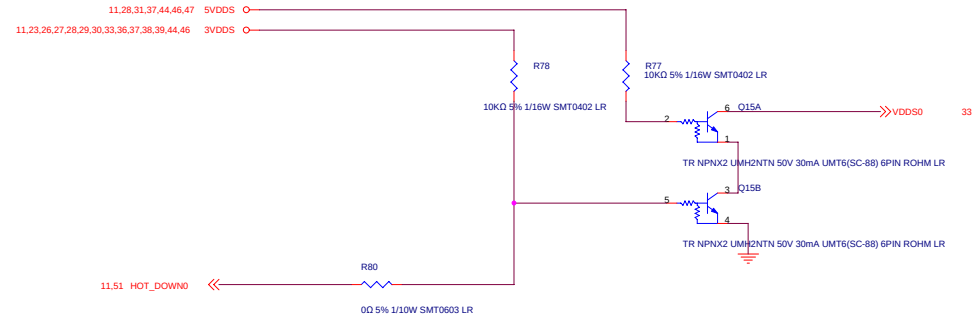
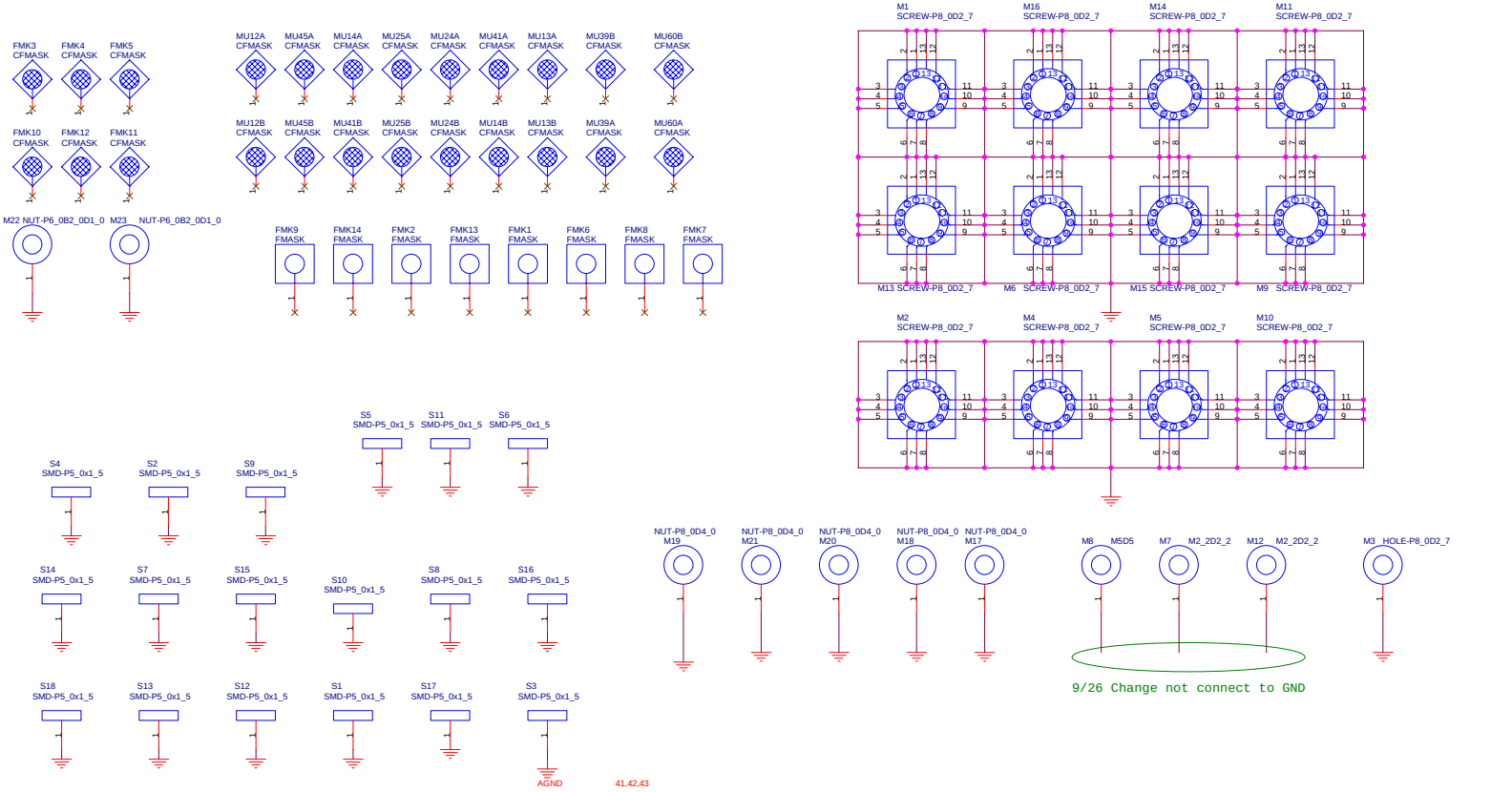
Title: LM7W < VIA VN800 + VT8237R >

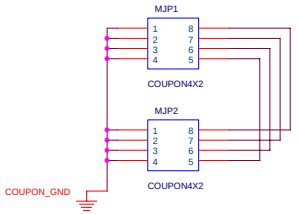
Size: C | Document Number: <Reset Circuit> | Rev: 0.2

Date: Monday, November 14, 2005 | Sheet 39 of 55




# COUPON4X2





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| Size | Document Number | Rev |
|---|---|---|
| C | <OVP CKT> | 0.2 |

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10mil A_GND_POWER
10mil AC97_PCBEEP
10mil A_GND_POWER

9/8 Change

10/25 Change to 0 ohm SMT0805(11-14211-00)

10/12 Add HP out to G1410

U56
ASIC CODEC ALC655 LQFP 48PIN REALTEK LR

PC_BEEP PHONE AUX_L AUX_R JD2 JD1/GPIO1 CD_L CD_R CD_GND MIC1 MIC2 LINE_IN_L LINE_IN_R JD0/GPIO0 XTLSEL EAPD/SPDIFI SPDIFO XTL_IN XTL_OUT SDATA_OUT BIT_CLK SYNC RESET# DVDD1 DVDD2 AVDD1 AVDD2

FRONT_OUT_L FRONT_OUT_R MONO_OUT SURR_OUT_L SURR_OUT_R VREF VREFOUT AFILT1 AFILT2 VRAD VRDA NC Front-MIC CENTER-OUT SDATA_IN NC DVSS1 DVSS2 AVSS1 AVSS2 LFE-OUT

C824 2.2uF 16V 80-20% SMT0805 Y5V C2012Y5V1C225Z TDK LR
C324 1uF 10V 10% SMT0603 X5R C1608X5R1A105K TDK LR
C349 18pF 50V 5% SMT0402 NPO LR
C341 18pF 50V 5% SMT0402 NPO LR
C335 22pF 5% 50V 0603 NPO(NU)
R391 0 5% 1/16W 0402(NU)
R390 0Ω 5% 1/16W SMT0402 LR(NU)
R389 10K 5% 1/16W 0402(NU)
R381 22Ω 5% 1/10W SMT0603 LR
24.576MHz SMD 12pF ±30ppm 40Ω X8A024576FC1H-H HARMONY LR
Y6
C838 10uF 10V ±10% SMT0805 X5R T=1.25mm C2012X5R1A106KT TDK LR
C840 10uF 10V ±10% SMT0805 X5R T=1.25mm C2012X5R1A106KT TDK LR
C351 680pF 50V 10% 0603 X7R(NU)
C346 680pF 50V 10% 0603 X7R(NU)
R386 10K 5% 1/16W 0603(NU)
R394 10K 5% 1/16W 0603(NU)
TP1
C350 0.1uF 16V 80%-20% 0402 Y5V(NU)
R784 4.7KΩ 5% 1/16W SMT0402 LR
C355 0.01uF 16V 10% SMT0603 X7R(NU)
C340 0.047uF 16V 10% SMT0603 X7R LR
C339 1uF 6.3V 10% SMT0402 X5R LR
C344 1uF 10V 10% SMT0402 X7R(NU)
C338 1000pF 50V 10% SMT0402 X7R LR
C334 1000pF 50V 10% SMT0402 X7R LR
C342 100uF 10V ±20% SMT3216 ESR=4.0Ω T491A106M010AT KEMET LR
C332 0.1uF 16V 80-20% SMT0402 Y5V LR
R373 22Ω 5% 1/16W SMT0402 LR Sn
R393 0 5% 1/16W 0402(NU)
R392 0 5% 1/16W 0402(NU)

NU FOR AUDIO QUALITY

3VDDM 3VDDM_AUDIO
Please close to CODEC CHIP
L44 600Ω±25% 100MHz 1000mA SMT0603 MLB-160808-0600P-N2 MAG.LAYERS LR
C327 100uF 10V ±20% SMT3216 ESR=4.0Ω T491A106M010AT KEMET LR
C326 0.1uF 16V 80-20% SMT0402 Y5V LR
C343 0.1uF 16V 80-20% SMT0402 Y5V LR
C337 0.1uF 16V 80-20% SMT0402 Y5V LR
R382 0Ω 5% 1/10W SMT0603 Lead-Free

L45 600Ω±25% 100MHz 2000mA SMT0805 MLB-201209-0600P-N2 MAG.LAYERS LR
C336 100uF 10V ±20% SMT3216 ESR=4.0Ω T491A106M010AT KEMET LR
C353 0.1uF 16V 80-20% SMT0402 Y5V LR
C333 0.1uF 16V 80-20% SMT0402 Y5V LR
C354 0.1uF 16V 80-20% SMT0402 Y5V LR

R396 0 5% 1/10W 0805(NU)
R395 0 5% 1/10W 0805(NU)

9/14 Change G924
9/14 Add

U28
LNR-IC LDO G924-475T1Uf 4.75V SOT23-5 5PIN GMT LR
VIN BYP SHDN GND VOUT

C358 1000pF 50V 10% SMT0402 X7R LR
C356 0.1uF 16V 80-20% SMT0402 Y5V LR
C348 0.1uF 16V 80-20% SMT0402 Y5V LR
C841 10uF 10V ±10% SMT0805 X5R AVXTV21X5R106K10AT AVX LR
R397 0Ω 5% 1/8W SMT0805 LR

AGND to GND res

## AC97 CODEC Layout Guide:

1.The digital and analog gnd should be separated 2-3mm gap
2.All the analog trace routing should be over the analog plane
3.The analog and digital planes should electrically shorted at one place
4.All supply high frequency decoulping ,reference high freguency decoulp and filter caps miust be routed on the same layer as the codec
5.Analog I/O routing should be kept a short as possible
6.Analog I/O routing should be shielding with analog ground traces
7.Use of ground plane fill and the copper fill should be shorted to the analog ground plane
8.The AC-link signal should be as short as possible
9.AC-link clock signal should have a series resistor close to the codec
10.The AC-link signal should be shielding with ground
11.Split analog and digital ground planes and 2-3mm
12.Analog signals only over analog ground plane
13.Digital signals only over digital ground plane
14.Locate analog section away from high speed digital circuits
15.Place smallest bypass capacitor closest to IC pin
16.Use metal film resistors and NPO capacitors in analog path
17.The Audio signals trace width is 12mil or more

**AC97 CODEC Power Consumption:**
Power Dissipation: TYP 330mW
Icc: TYP 40mA (Digital)
Icc(stdby): TYP 0mA (Digital)
Icc: TYP 40mA (Analog)
Icc(stdby): TYP 0.13mA (Analog)

A_GND 10mil
A_LINE_OUT_L 10mil
A_GND 10mil
A_LINE_OUT_R 10mil
A_GND 10mil

A_CD_GND 10mil
A_CD_L 10mil
A_CD_GND 10mil
A_CD_R 10mil
A_CD_GND 10mil

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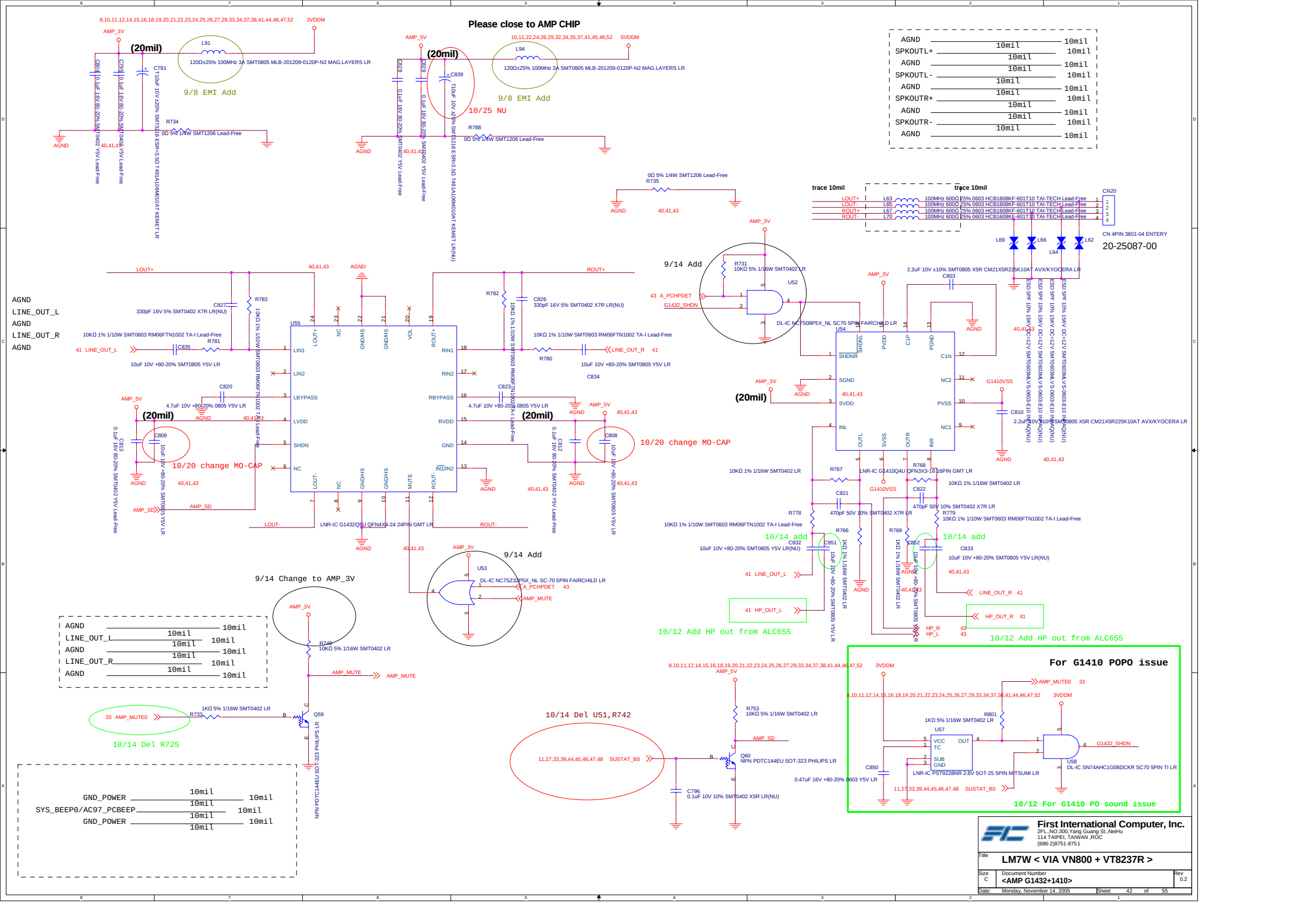
(886-2)8751-8751

Title: LM7W < VIA VN800 + VT8237R >
Size: C | Document Number: <ALC655 codec> | Rev: 0.2
Date: Monday, November 14, 2005 | Sheet 41 of 55


Please close to AMP CHIP
(20mil)
9/8 EMI Add
10/25 NU
9/14 Add
9/14 Change to AMP_3V
10/20 change MO-CAP
10/14 add
10/12 Add HP out from ALC655
10/14 Del R725
10/14 Del U51,R742
For G1410 POPO issue
10/12 For G1410 PO sound issue
trace 10mil
CN 4PIN 3801-04 ENTERY
20-25087-00
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114 TAIPEI, TAIWAN ,ROC
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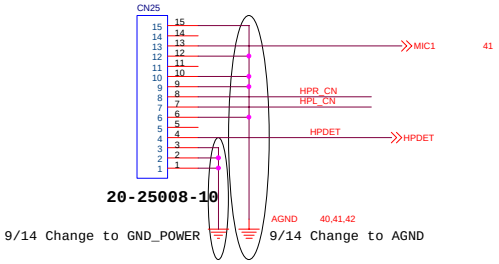
LM7W < VIA VN800 + VT8237R >
<AMP G1432+1410>
Monday, November 14, 2005

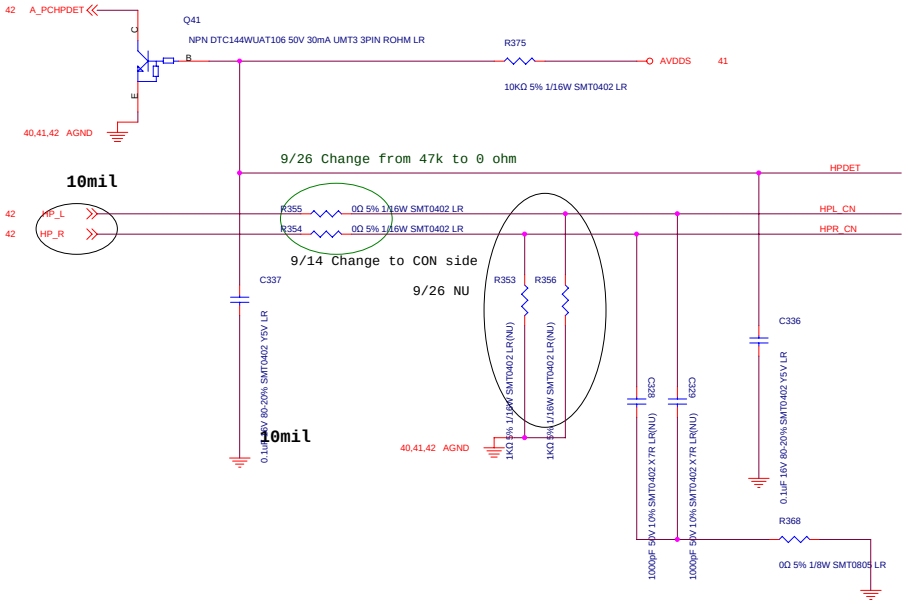
9/16 Cancel USB CON




9/14 Change to GND_POWER

9/14 Change to AGND

Normal=LOW
Headphone insert=High




10,11,22,24,26,29,32,34,35,37,41,42,45,46,52 5VDDM

5VDDM

| | | |
|---|---|---|
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| Title: LM7W < VIA VN800 + VT8237R > | | |
| Size: C | Document Number: <SPDIF / HP OUT / Audio CN> | Rev: 0.2 |
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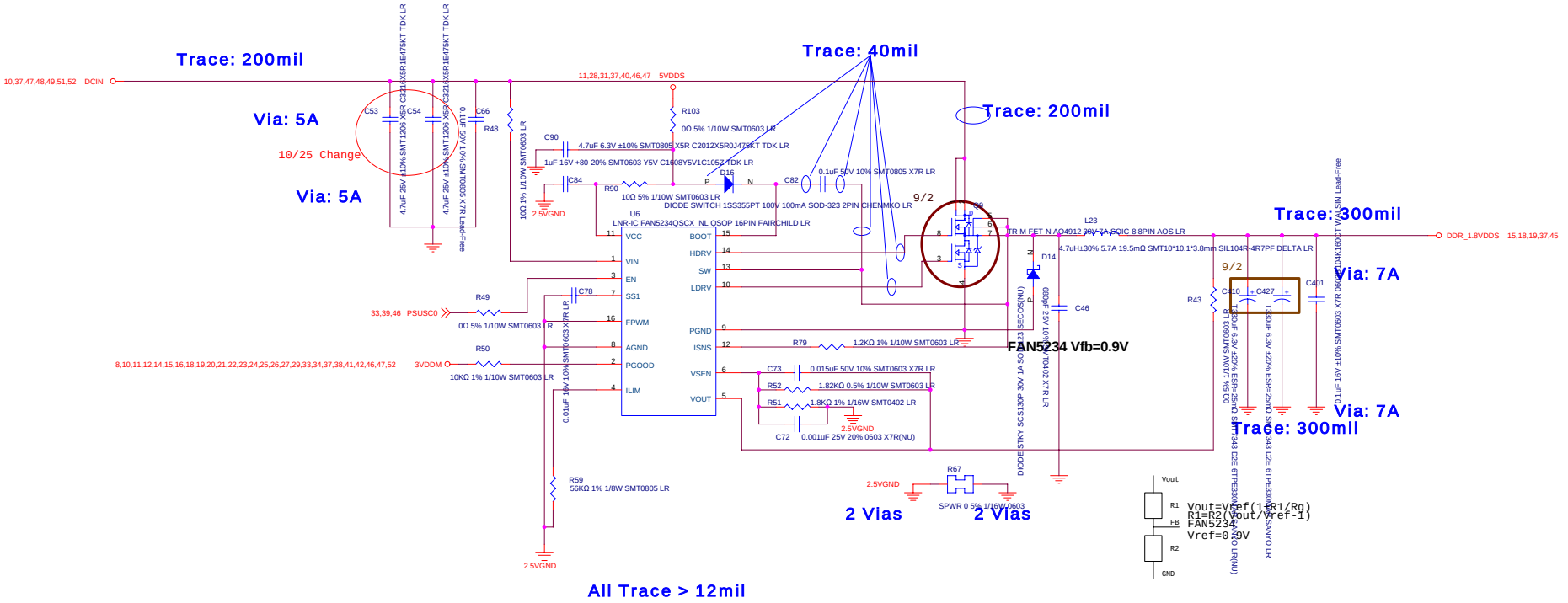
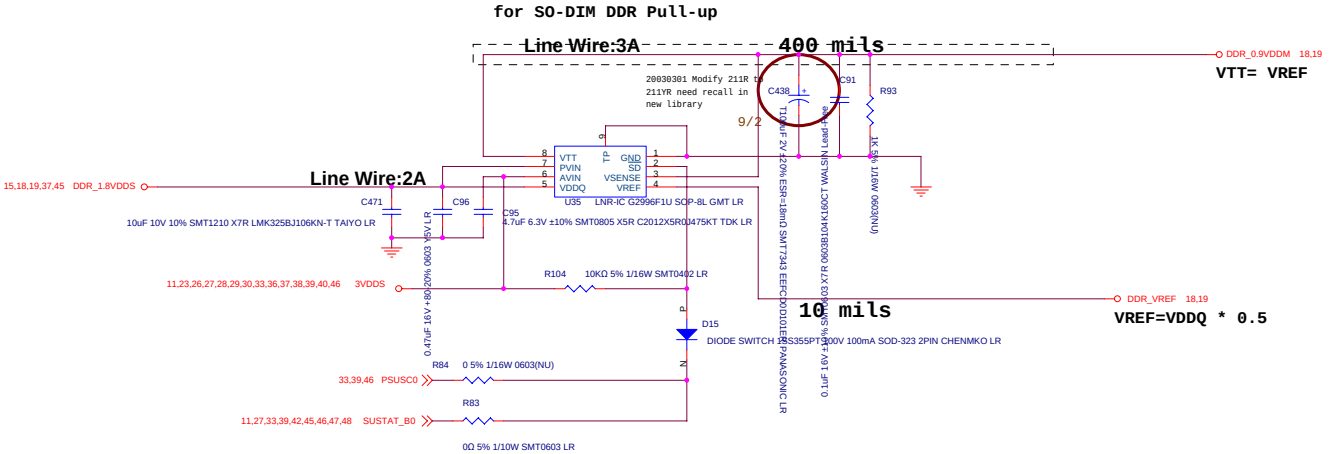
# DDR POWER




| | | |
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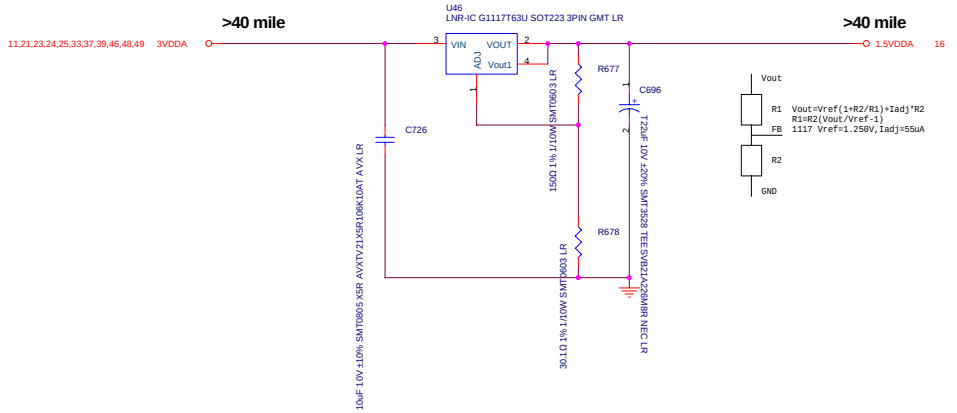
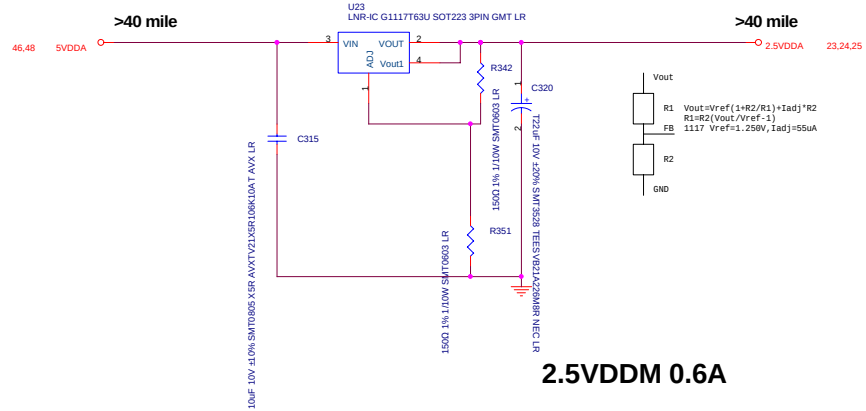
| Size C | Document Number <DDR2 POWER> | Rev 0.2 |
| Date: Monday, November 14, 2005 | Sheet 44 of 55 | |

9/12 Cancel

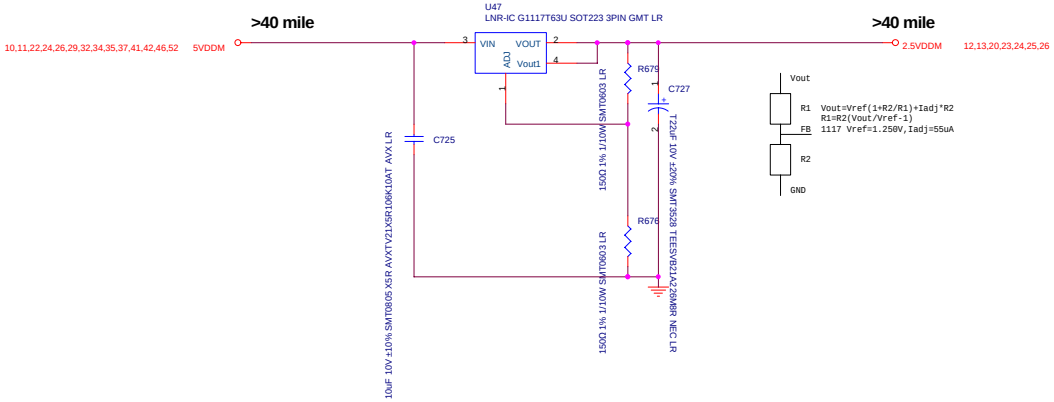
## 1.5VDDA 0.7A



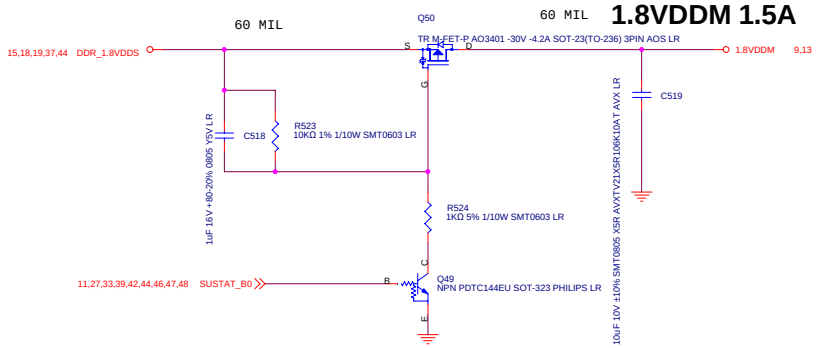

## 2.5VDDA 0.6A




## 2.5VDDM 0.6A




## 1.8VDDM 1.5A





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Size: C | Document Number: <1.5V / 2.5V /1.8V> | Rev: 0.2

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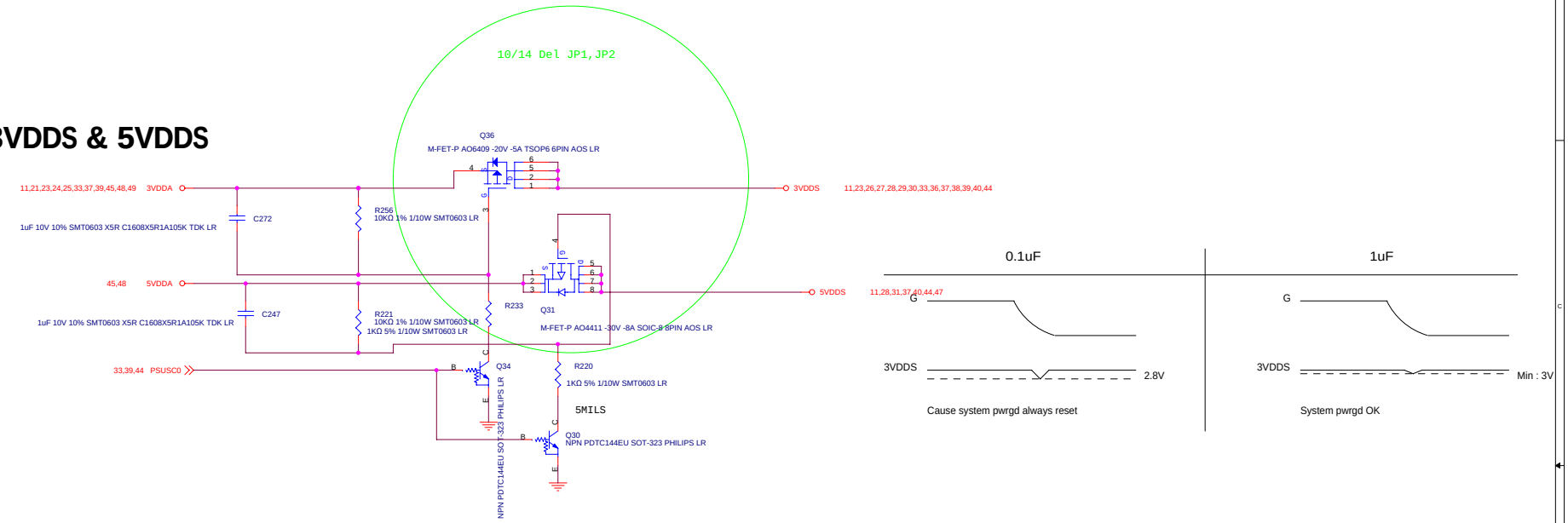
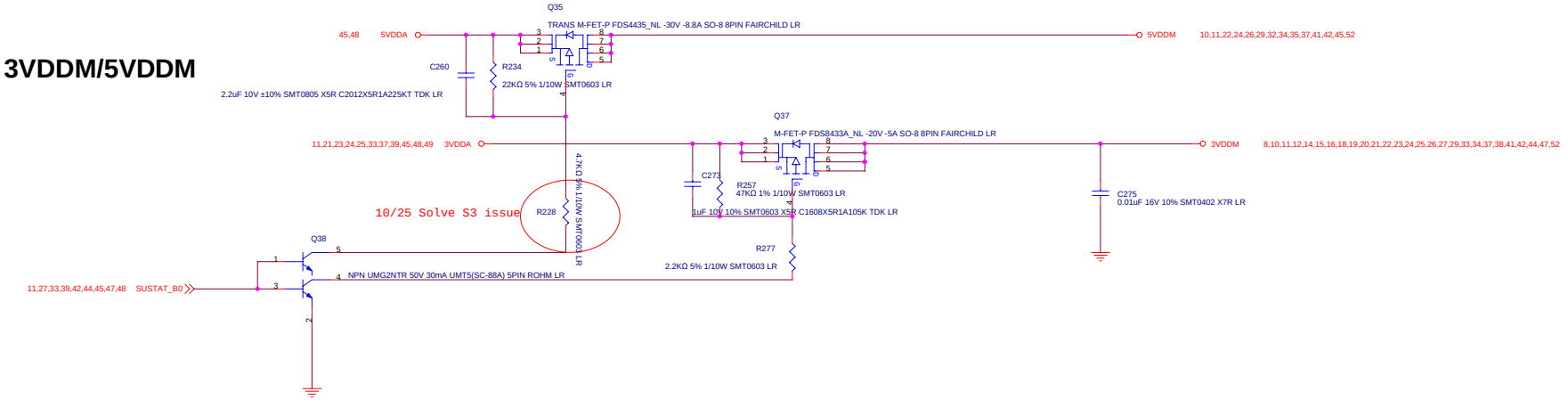
# 3VDDS & 5VDDS




# 3VDDM/5VDDM





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Size: C | Document Number: <POWER 3/5 VDDS/VDDM> | Rev: 0.2

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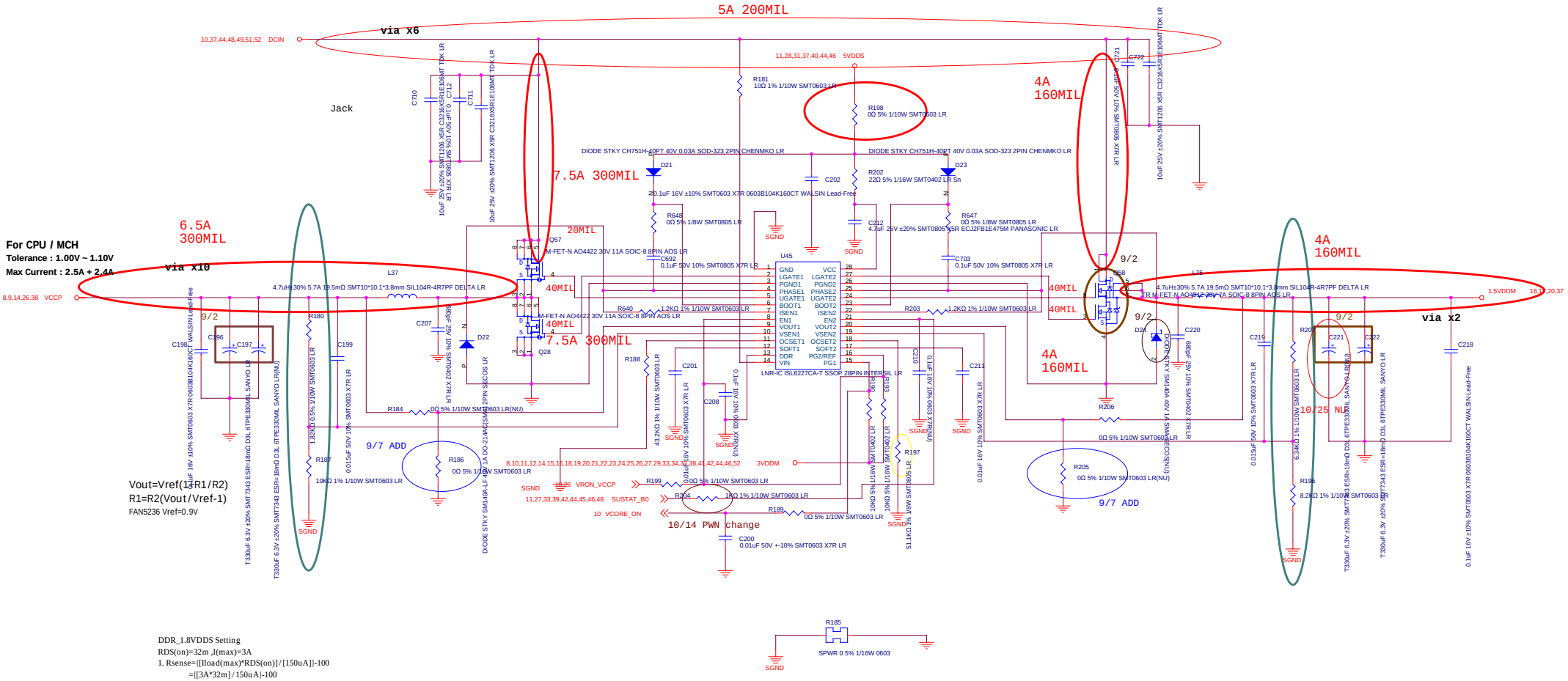
# VCCP ,VORE_GMCH




Vout=Vref(1+R1/R2)
R1=R2(Vout/Vref-1)
FAN5236 Vref=0.9V

DDR_1.8VDDS Setting
RDS(on)=32m ,I(max)=3A
1. Rsense=[[Iload(max)*RDS(on)]/[150uA]]-100
=[[3A*32m]/150uA]-100
=640
2. Ilimit=1.2*1.25*1.6*3A=7.2A
3. Rlimit=[11.2*(100+Rsense)]/[Ilimit*RDS(on)]
=[11.2*(100+640)]/[7.2*32m]
=35.9K

| | | | |
|---|---|---|---|
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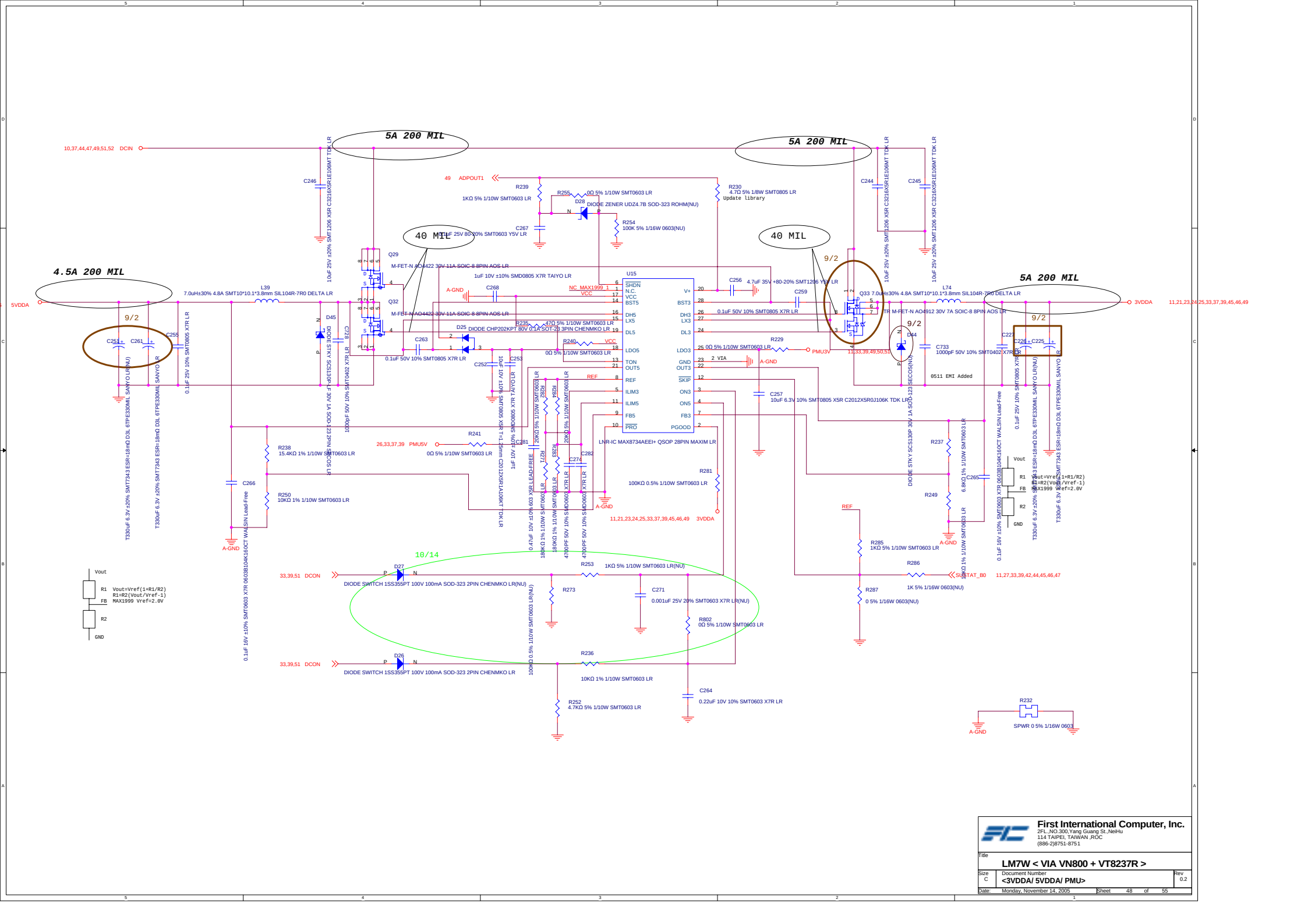
| Size: Custom | Document Number: <VCCP & 1.5VDDM> | | Rev: 0.2 |
| Date: Monday, November 14, 2005 | Sheet 47 of 55 | | |




| | | |
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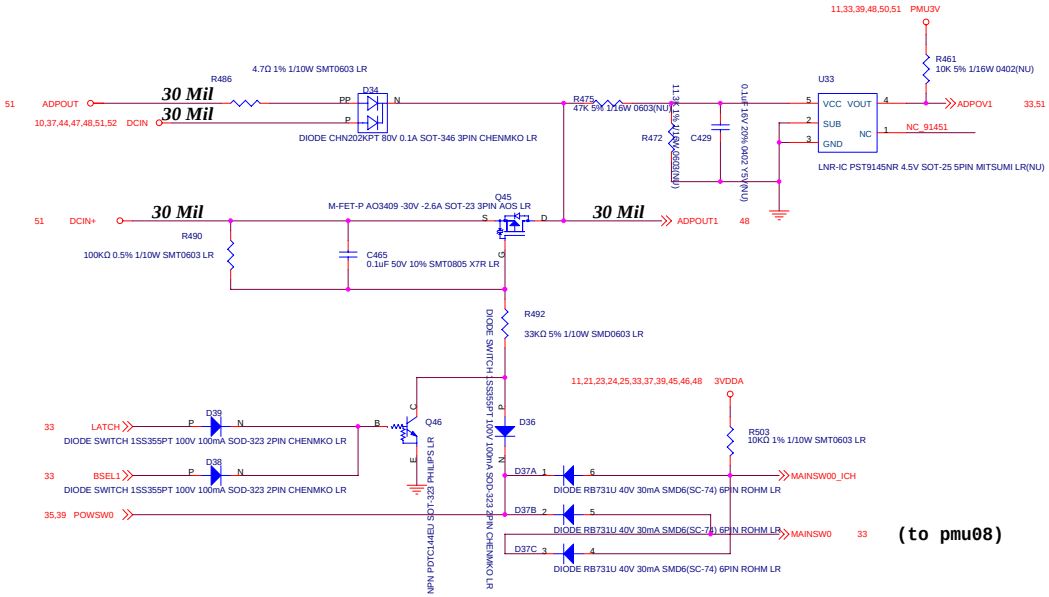
| Title | LM7W < VIA VN800 + VT8237R > | |
| Size: C | Document Number: <3VDDA/ 5VDDA/ PMU> | Rev: 0.2 |
| Date: Monday, November 14, 2005 | Sheet 48 of 55 | |





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|---|---|---|
| Custom | <power-on switch control> | 0.2 |

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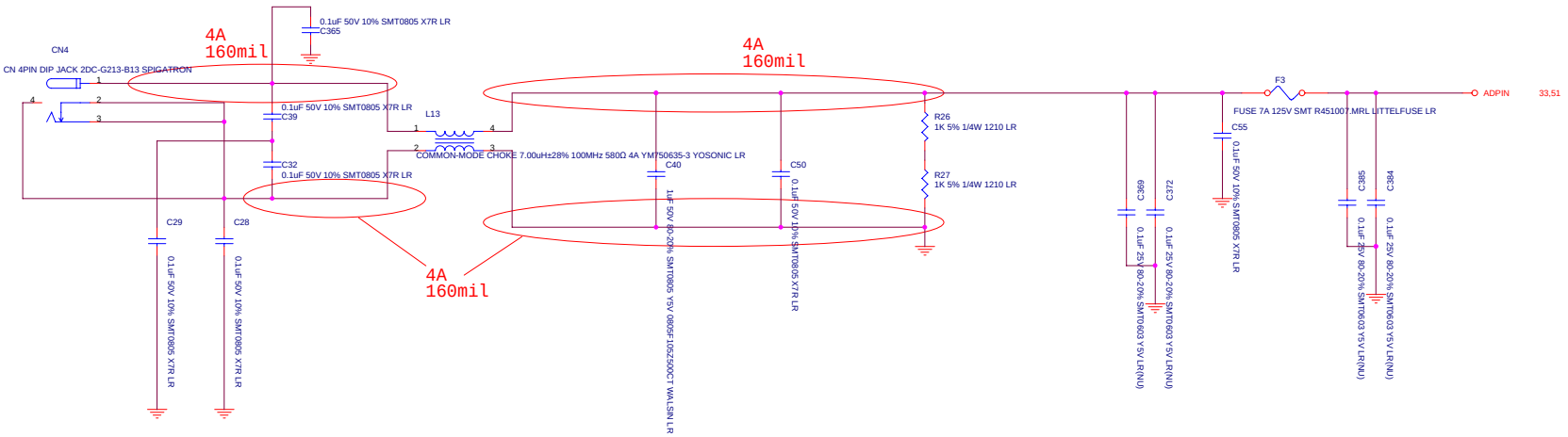
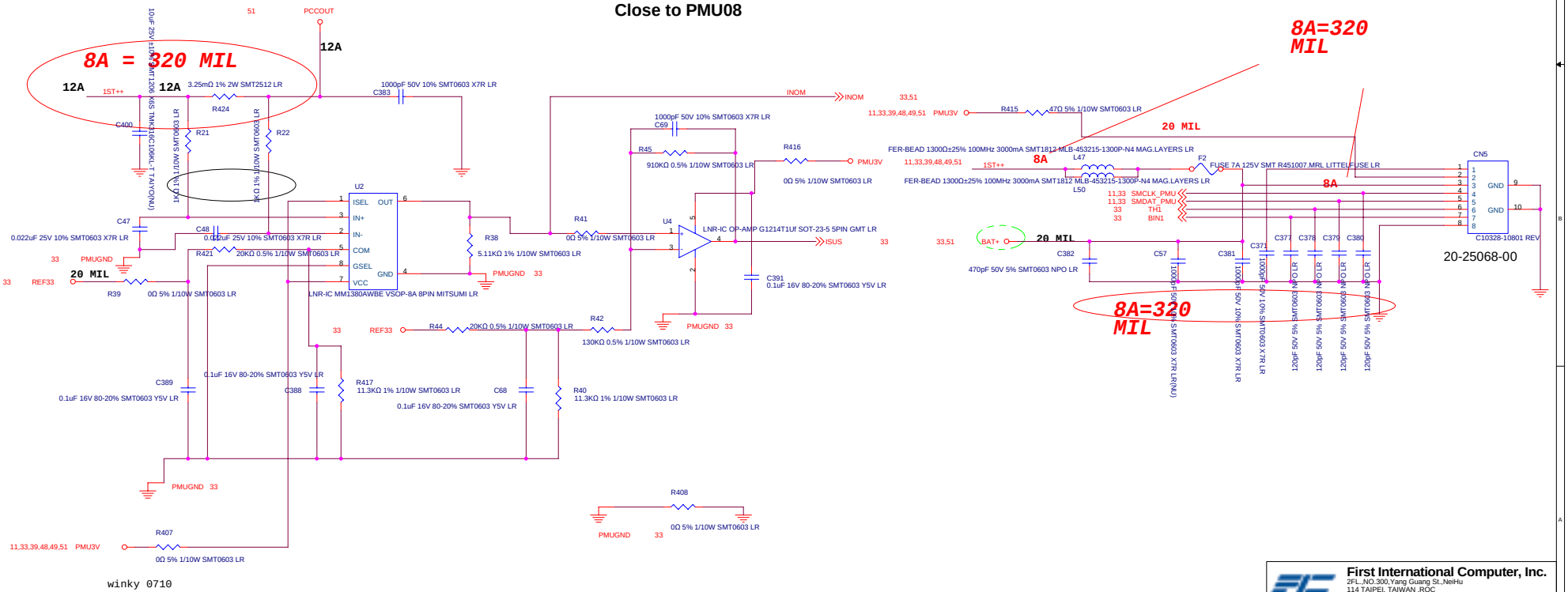



# CHR BATTERY IN

**Close to PMU08**





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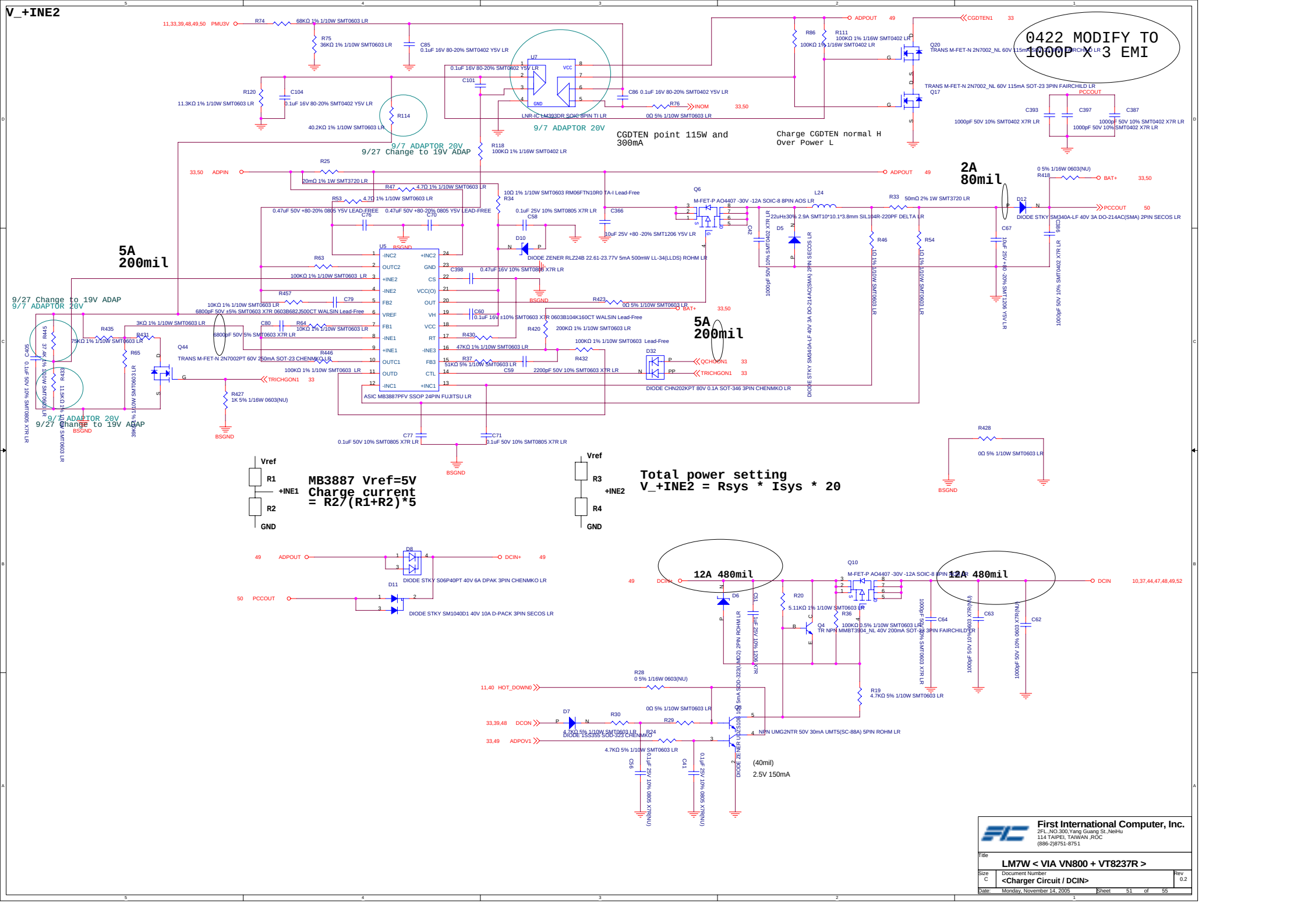
| | | |
|---|---|---|
| Title | LM7W < VIA VN800 + VT8237R > | |
| Size: C | Document Number: <AC-IN / Battery CNN> | Rev: 0.2 |
| Date: Monday, November 14, 2005 | Sheet 50 of 55 | |


V_+INE2
0422 MODIFY TO 1000P X 3 EMI
9/7 ADAPTOR 20V
9/27 Change to 19V ADAP
CGDTEN point 115W and 300mA
Charge CGDTEN normal H Over Power L
2A 80mil
5A 200mil
5A 200mil
MB3887 Vref=5V
Charge current = R27(R1+R2)*5
Total power setting
V_+INE2 = Rsys * Isys * 20
12A 480mil
12A 480mil
(40mil)
2.5V 150mA
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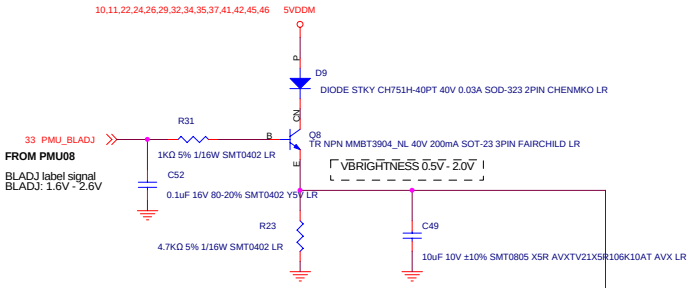
LM7W < VIA VN800 + VT8237R >
<Charger Circuit / DCIN>
Monday, November 14, 2005

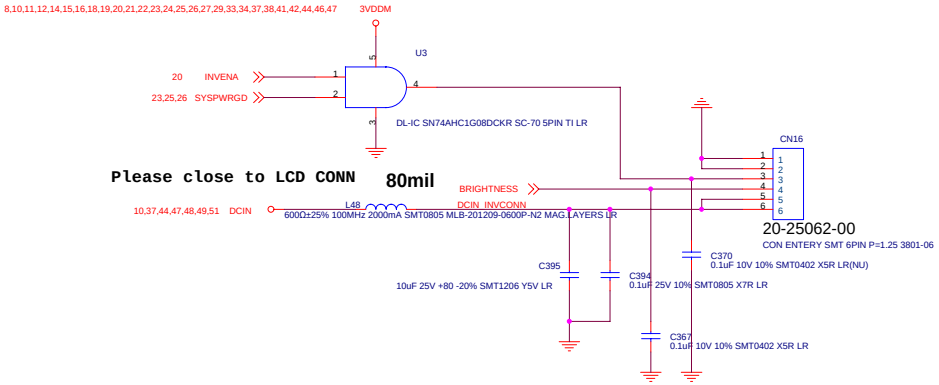
# Inverter Control

## LCD brightness control




**PWM OUTPUT 200Hz**

BRIGHTNESS





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Title: LM7W < VIA VN800 + VT8237R >

Size: C | Document Number: <Inverter> | Rev: 0.2

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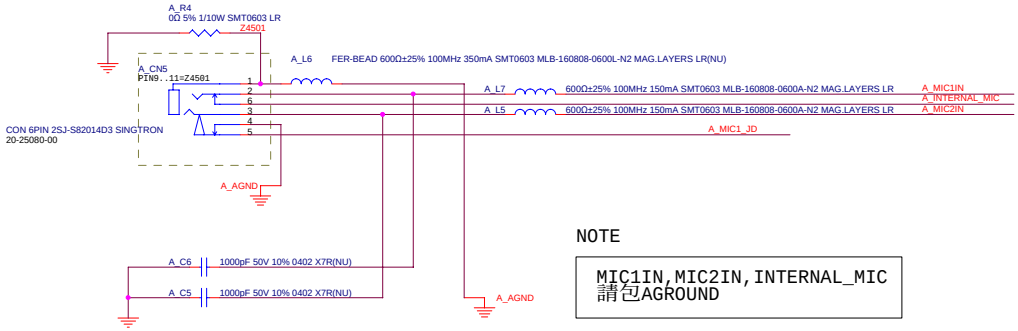
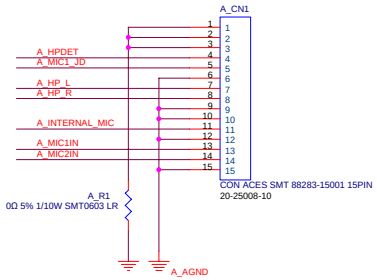


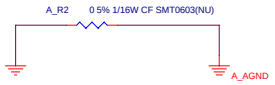

NOTE

MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND

9/16 Cancel USB CON

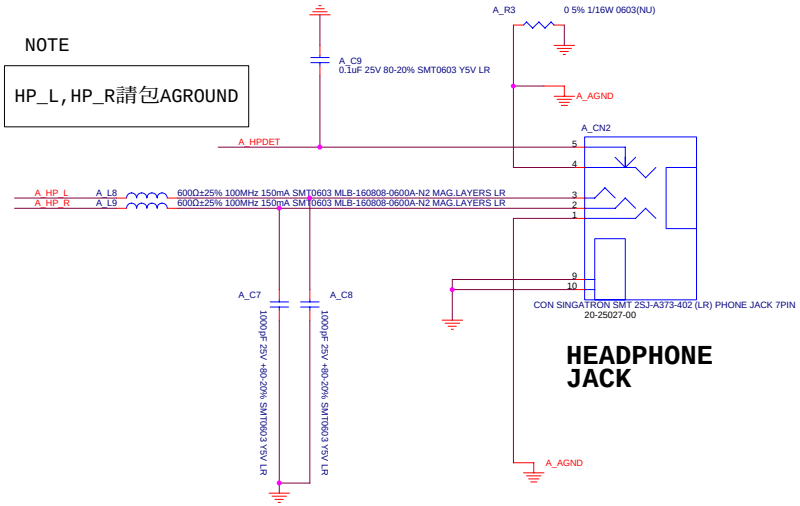
9/16 Cancel USB CON



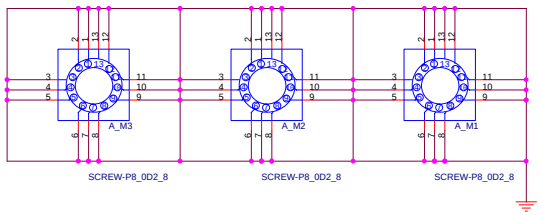



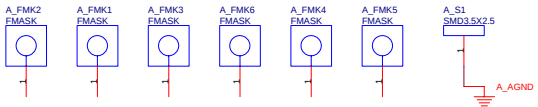

NOTE

HP_L,HP_R請包AGROUND




**HEADPHONE JACK**

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Title: **LM7W < VIA VN800 + VT8237R >**

| Size | Document Number | Rev |
|---|---|---|
| C | <Audio Board> | 0.2 |

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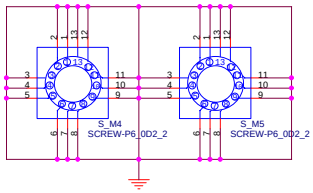
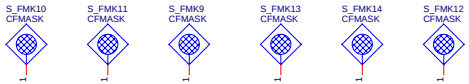
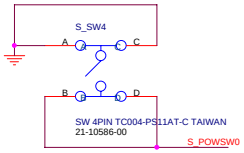
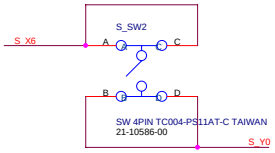


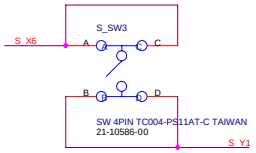

## POWER SW



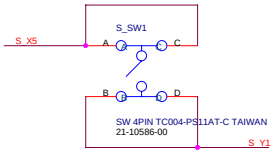

## INTERNET SW

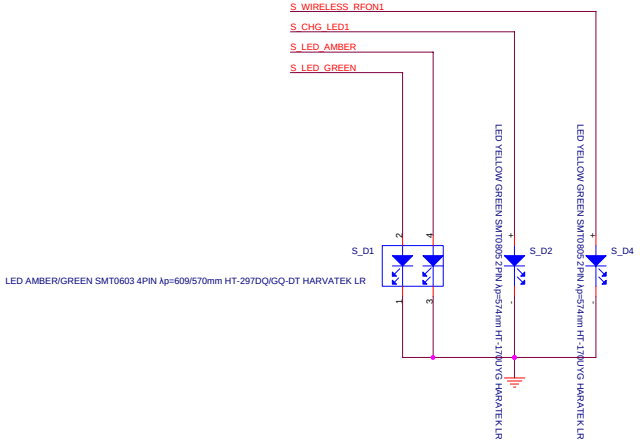



## RF SW

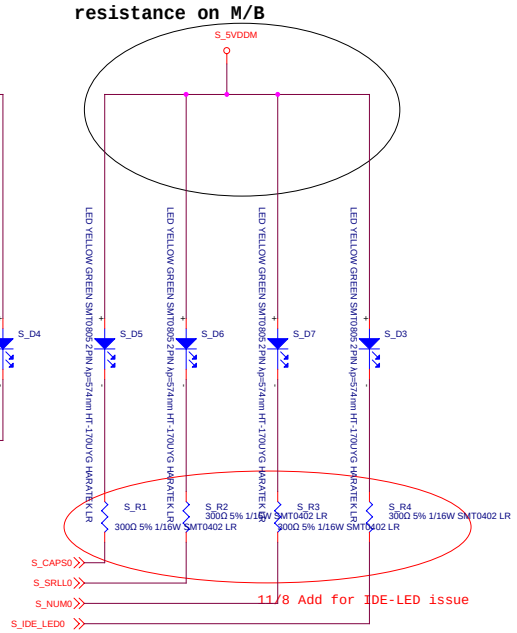



## SILEN SW

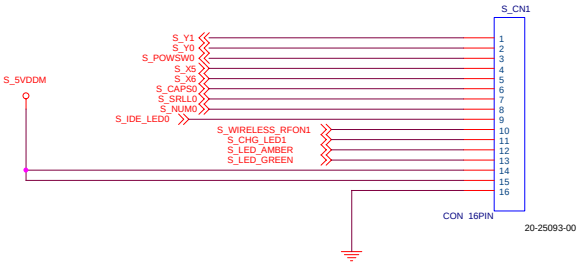



## resistance on M/B




## switch board con




| | | |
|---|---|---|
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| Title | LM7R VIA VN800+ VT8237W | |
| Size: C | Document Number: <Switch transfer board> | Rev: 0.2 |
| Date: Monday, November 14, 2005 | Sheet 54 of 55 | |

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Title

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| Size | Document Number | Rev |
|---|---|---|
| C | **<updata list>** | 0.2 |

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